Power Electronic Systems
Laboratory

Proceedings of the 37th Annual Conference of the IEEE Industrial Electronics Society (IECON 2011), Melbourne, Australia, November 7-10, 2011.

Novel 3-Level Hybrid Neutral-Point-Clamped Converter

T. Soeiro
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Novel 3-level Hybrid Neutral-Point-Clamped Converter

Thiago B. Soeiro and Johann W. Kolar
Power Electronic Systems Laboratory, ETH Zürich, Physikstrasse 3, CH-8092 Zürich, Switzerland.
E-mail: soeiro@lem.ee.ethz.ch

***Abstract*-- This paper introduces a novel 3-level Voltage Source Converter (VSC) as an alternative to known 3-level topologies, including the conventional Neutral-Point-Clamped Converter (NPCC), many T-type VSCs, and Active NPCC. It is shown that operating in the low converter DC-link voltage range, this new solution can achieve not only higher efficiency than many typical 3-level structures, but can also overcome their drawback of unsymmetrical semiconductor loss distribution. The switching states and commutations of the new converter, named here as Hybrid NPCC, are analyzed and a loss balancing scheme is introduced. New 5- and 7-level VSC topologies with loss balancing features are also presented.**

I. INTRODUCTION

3-level Voltage Source Converters (VSCs), particularly the 3-level Neutral-Point-Clamped Converter (NPCC) [1] [2], are widely used in industrial medium voltage range applications (e.g. rolling mills, fans, pumps, marine appliances, mining, tractions, and renewable energy) [3] [4]. Recent investigations have shown that the NPCC is also a promising alternative for low-voltage applications [5] [6].

Compared to the 2-level VSC shown in Fig. 1(a), the 3-level NPCC (c.f. Fig. 1(b)) features two additional active switches, two extra isolated gate drivers, and four diodes per phase leg. The 3-phase 3-level NPCC allows 27 switch states in the space-vector diagram, whereas the 2-level VSC allows eight switch states only [4]. Hence, the clearly superior controllability of the phase currents and DC-link voltage, U_{DC}, are the most distinct advantages over the 2-level converter [4]. Additionally, in applications, such as photovoltaic grid inverters, rectifiers, motor drives and active filters, 3-level NPCC and/or T-type VSC, i.e. (cf. Fig. 1(c)) systems can achieve lower losses than 2-level converters, if the switching frequency is high enough [6].

The main disadvantages of the 3-level NPCC and/or T-type VSCs are the necessary partial DC-link voltage balancing control and the commonly uneven loss distribution across the bridge-leg semiconductors [3].

The semiconductor chips assembled in a 3-level NPCC bridge leg module are mostly dimensioned, neglecting the loss distribution to the specific elements. This often results in an oversized design with an expensive and weakly utilized semiconductor area [6]. In addition, the typical uneven loss distribution and the resulting different junction temperature operation of the individual chip devices, could lead to unacceptable high thermal stresses on some power devices and thermo-mechanical damage could arise, thus reducing the system reliability [7] [8].

A 3-level Active NPCC (A-NPCC), which features loss balancing capability between the power devices, is shown in Fig. 1(d). The two extra active switches per phase-leg added to the 3-level NPCC, T_{Ax1} and T_{Ax2}, allow a substantial improvement in semiconductor loss distribution (cf. [9]).

In this paper, a novel 3-level VSC is introduced as an alternative to many 3-level topologies, i.e. the conventional NPCC, T-type VSCs, and A-NPCC. This new converter shown in Fig. 1(e) is named Hybrid NPCC (H-NPCC). It combines operation of different VSC topologies, having the freedom to control the system in a 2- or 3-level manner. It is shown that operating in the low converter DC-link voltage range this new solution can achieve not only higher efficiency than many typical 3-level structures, but can also overcome their drawback of extremely asymmetrical loss distribution for some operating conditions. Therefore, a remarkable increase of the converter output power capability and/or system reliability can be accomplished.

The article is organized as follows. Section II presents a survey on 3-level VSC topologies, including the conventional NPCC, the A-NPCC and various T-type VSC systems. The loss distribution problem of the 3-level converters is investigated. Subsequently, the novel 3-level VSC is introduced in Section III, where the switching states and commutations of the converter are analyzed. A loss-balancing scheme suitable for enhancing the temperature distribution over the employed semiconductor devices is presented. Finally, in Section IV an efficiency comparison between the studied topologies for 10 kVA 50 Hz inverter operation in the switching frequency range of 5 kHz to 48 kHz and low DC-link voltage level is presented to demonstrate the performance and feasibility of the novel 3-level Hybrid NPCC.

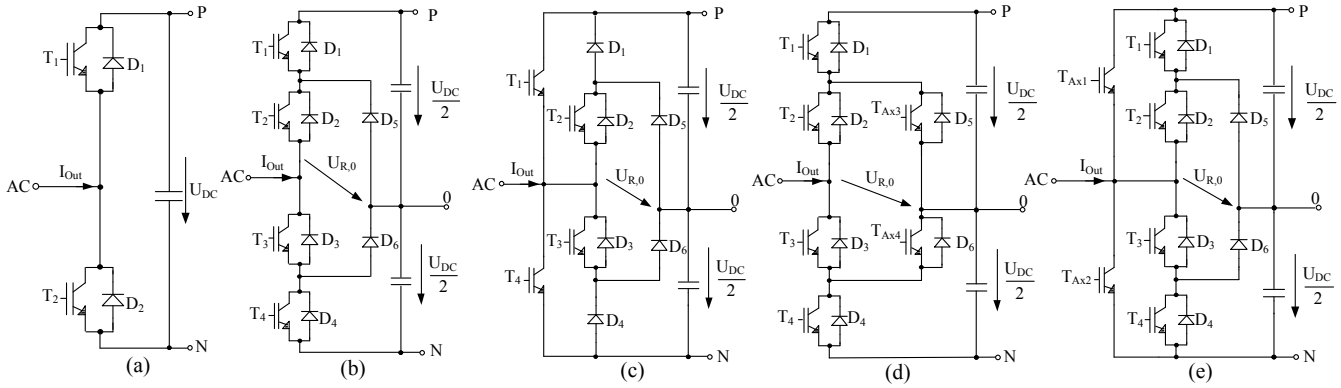

Fig. 1. Voltage Source Converters: (a) 2-level VSC; (b) Conventional NPCC; (c) 3-level T-type NPCC; (d) 3-level A-NPCC; and (e) 3-level H-NPCC.

II. SURVEY ON 3-LEVEL VSC TOPOLOGIES

Fig. 1 shows bridge-leg structures of 3-phase voltage source converters in 2- and 3-level configurations, including the conventional NPCC, the T-type NPCC, the A-NPCC and the proposed Hybrid NPCC.

A typical 3-level T-type converter constitutes a standard 2-level VSC with an active bidirectional switch connecting the AC terminal with the DC-link mid-point "0". Fig. 1(c) and Fig. 2 show several arrangements of T-type VSCs. For low rated DC-link voltage level in the range of 700V to 1000V, as for the 2-level VSC, any of the presented T-type topologies would require 1200V IGBTs for the top and bottom switches, T_1 and T_4. The systems depicted in Fig. 2(a) and 2(b) also need 1200V anti-parallel diodes for the top and bottom switches, D_1 and D_4. Since the bidirectional mid-point switches have to block only half of the DC-link voltage, 600V IGBT and diodes can be used.

The 3-level NPCC topology is most often used for medium voltage range applications [3]. The factors preventing the NPCC from being successful in the low voltage market are increased costs and complexity. For low DC-link voltage level, 6 diodes and 4 IGBTs per phase-leg rated at 600V are required. However, the number of IGBTs and isolated gate drives is twice that of the 2-level VSC. Compared to the T-type NPCC (cf. Fig. 1(c)), the NPCC needs 2 more diodes and 1 isolated gate drive per phase-leg.

Adding two extra active switches to each phase leg of the conventional NPCC allows a substantial improvement in loss distribution, with utilizing the additional switching states and new commutation possibilities (cf. Fig. 1(d)) [9]. This configuration, known as active NPCC, permits a specific utilization of the upper and lower path of the neutral tap and, thus, affects the distribution of conduction and switching losses among the semiconductor devices [9] [10]. When compared to the conventional NPCC, the A-NPCC requires 2 extra active switches and 1 isolated gate drivers per phase-leg (T_{Ax3} and T_{Ax4}).

In order to verify the problem of the unequal loss distribution of the typical 3-level systems, loss calculations are performed for three 3-phase inverters based on the conventional NPCC, the T-type NPCC, and the A-NPCC. These systems, rated to 10 kVA, are considered to operate at 48 kHz and specifications: $\hat{U}_{Out}$ =325V, $\hat{I}_{Out}$ =20.5A/50Hz, ϕ=0°, and 700V DC-link. A Space Vector Modulation (SVM) scheme incorporating an optimal clamping of each phase, as described in [11], is selected for analysis. When compared to a simple carrier-based sine-triangle modulation (SPWM), the SVM strategy can accomplish better efficiency and loss distribution features. For the A-NPCC, in addition to the SVM, the loss balancing scheme proposed by [4] is used. The Infineon IGBTs IKW30N60T and IGW25T120 are selected for the assessment and their loss characteristics are determined with a test set-up specially designed to enable operation of any of the single phase topologies depicted in Fig. 1 (cf. Fig. 3). An optimized heat sink with thermal resistance of R_{th}=0.1K/W has been designed and considered in the thermal analysis. The thermal models of the devices are obtained directly from the datasheet, including the thermally conductive insulating material.

For each inverter, the resulting averaged power loss distribution and the operating junction temperature, T_J, of the individual elements in a phase-leg are shown in Fig. 4 and Fig. 5, respectively. In Fig. 5 a constant ambient temperature, T_A, of 50°C is assumed in the analysis. The temperature distribution across the heat sink, T_{HS}, is regard as uniform. It can be seen that during high switching frequency operation the loss distribution across the switches of the T-type inverter is very different. Additionally, this system exhibits the lowest efficiency, η_T. The 3-level A-NPCC achieves an outstanding loss distribution performance, enabling the main semiconductor chips for IGBTs or diodes to operate with similar junction temperatures. The A-NPCC and the conventional NPCC systems display very similar total semiconductor loss, P_T. This occurs, because in both systems during each commutation one diode and one active switch always experience switching and conduction losses [4].

It is important to point out that for the inverter operation considered in this analysis, the T-type structures shown in Fig. 1(c), 2(a) and 2(d) would display very similar efficiency and loss distribution across the components. This is particularly true because the commutations during switching transitions and the number of components conducting in the current path, including device technologies, is always the same for all these topologies.

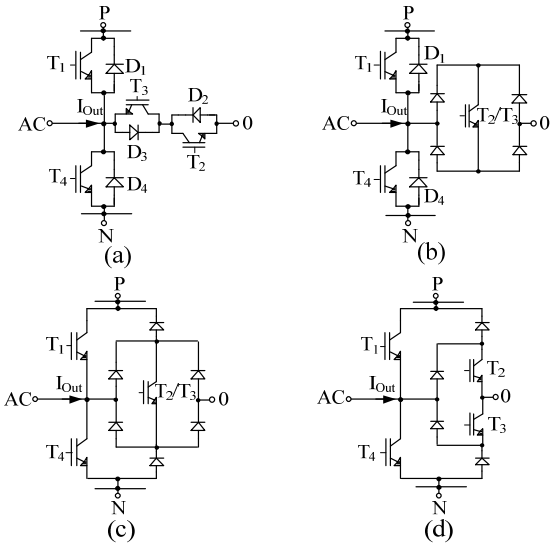

Fig. 2. (a-d) T-type topologies using bidirectional switch configurations.

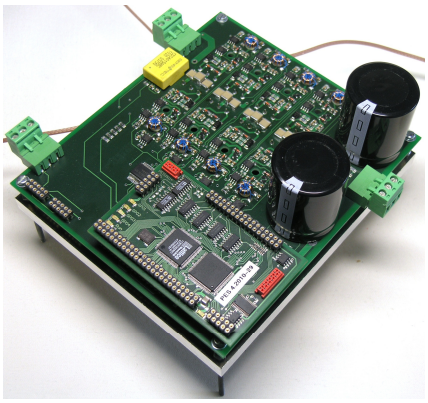

Fig. 3- Switching loss test set-up.

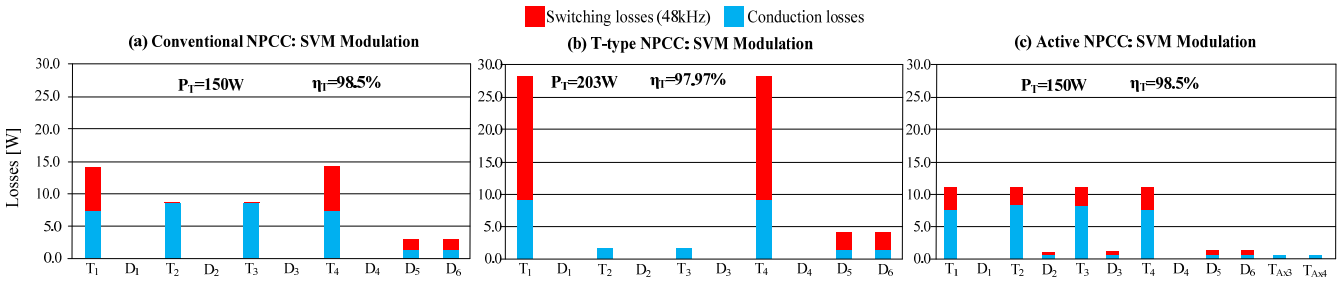

Fig. 4. Phase-leg components loss distribution for 3-phase 3-level inverters: (a) conventional NPCC, (b) T-type NPCC, and (c) Active-NPCC.

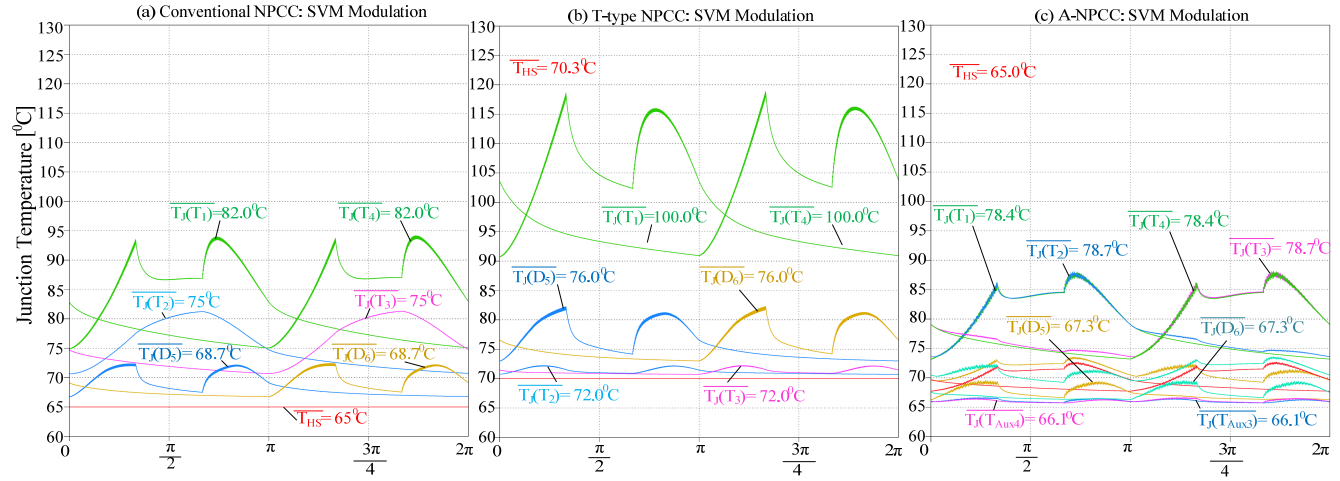

Fig. 5. Phase-leg components operating/averaged junction temperature for 3-phase inverters: (a) conventional NPCC; (b) T-type NPCC; and (c) A-NPCC.

III. HYBRID NEUTRAL-POINT-CLAMPED CONVERTER

As for the A-NPCC, the proposed H-NPCC requires two extra switches when compared to the conventional NPCC (per phase-leg). The power supplies of the isolated gate drives for T_2 and T_4 can be advantageously used for T_{Ax1} and T_{Ax2}, respectively. For operation in the low DC-link voltage converter range, in contrast to the A-NPCC, 1200V devices are employed as auxiliary switches (see T_{Ax1} and T_{Ax2} in Fig. 1(e)). The A-NPCC would require two extra 600V rated active switches per phase leg.

The strategically placed auxiliary switches, T_{Ax1} and T_{Ax2}, allow the system to operate like the conventional NPCC (cf. Fig. 1(b)), the T-type NPCC (cf. Fig. 1(c)), and/or the 2-level VSC. In contrast to the A-NPCC, which offers extra redundant zero states to the conventional NPCC (central tap "0"), the new switches create redundant switch states to the "P" and "N" potentials. Therefore, the losses across the devices within the phase-leg can be strategically distributed.

Note that during T-type NPCC operation, conduction losses can be drastically reduced, as fewer devices exist in the current path. This characteristic allows a higher efficiency operation when compared to the NPCC and/or A-NPCC, which always contains two conducting devices.

In inverter operation, by proper selection of the positive and negative switching states, it is possible to improve the efficiency of the new 3-level VSC. The losses of the system can be distributed such that the auxiliary switches, T_{Ax1} and T_{Ax2}, mainly display conduction losses while the outer switches, T_1 and T_4, are mostly stressed with switching losses. Hence, transistors with excellent on-state features could be selected for the auxiliary switches, while high speed devices would be more suitable for the outer switches.

A. *Switching States and Commutations*

Consider a single phase leg of the H-NPCC shown in Fig. 1(e). The switching states of the proposed system are given in Table I. As can be noted, the redundant switch states "P1" and "N1" define the conventional NPCC operation, while the states "P2" and "N2" match to the T-type NPCC operation. The states "P3" and "N3" characterize a hybrid operation of the system, where T-type and NPCC operations are blended in order to improve the system efficiency. Note that the direct commutation to or from the terminals "P" and "N" (P↔N), using "P1", "P2", "P3", "N1", "N2" or "N3", describes the 2-level VSC operation.

Table. I- Switch States of the 3-level Hybrid NPCC.

Device	T_1	T_2	T_3	T_4	T_{Ax1}	T_{Ax2}	Operating mode
State P1	1	1	0	0	0	0	NPCC
State P2	0	1	0	0	1	0	T-type NPCC
State P3	1	1	0	0	1	0	NPCC/T-type
State 0	0	1	1	0	0	0	NPCC/T-type
State N1	0	0	1	1	0	0	NPCC
State N2	0	0	1	0	0	1	T-type NPCC
State N3	0	0	1	1	0	1	NPCC/T-type

The commutations to or from the new states, incorporated in the conventional NPCC, determine the distribution of power losses across the semiconductor devices of the system. As for the conventional and active NPCC, all commutations take place between one active switch and one diode, even if more than two devices turn-on or -off, only one active switch and one diode experience essential switching losses [4]. Assuming the operating conditions where the AC terminal has impressed positive or negative

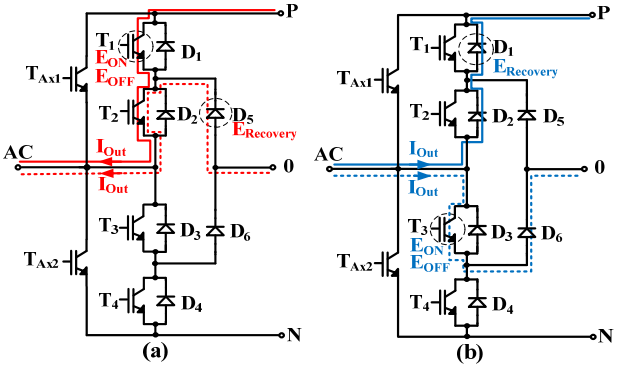

Fig. 6. Commutation (P1↔0) in the proposed 3-level VSC for conventional NPCC operation mode: (a) I_{Out}>0 and (b) I_{Out}<0.

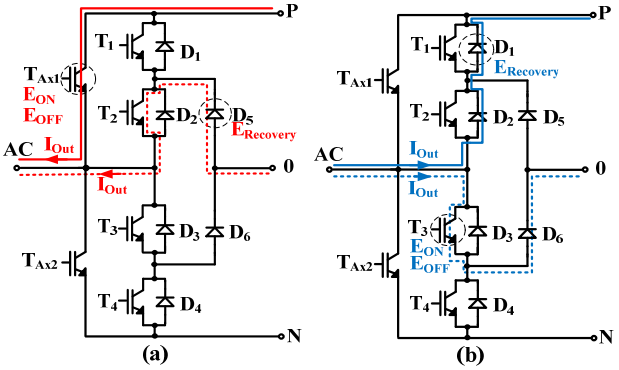

Fig.7. Commutation (P2↔0) in the proposed 3-level VSC for T-type NPCC operation mode: (a) I_{Out}>0 and (b) I_{Out}<0.

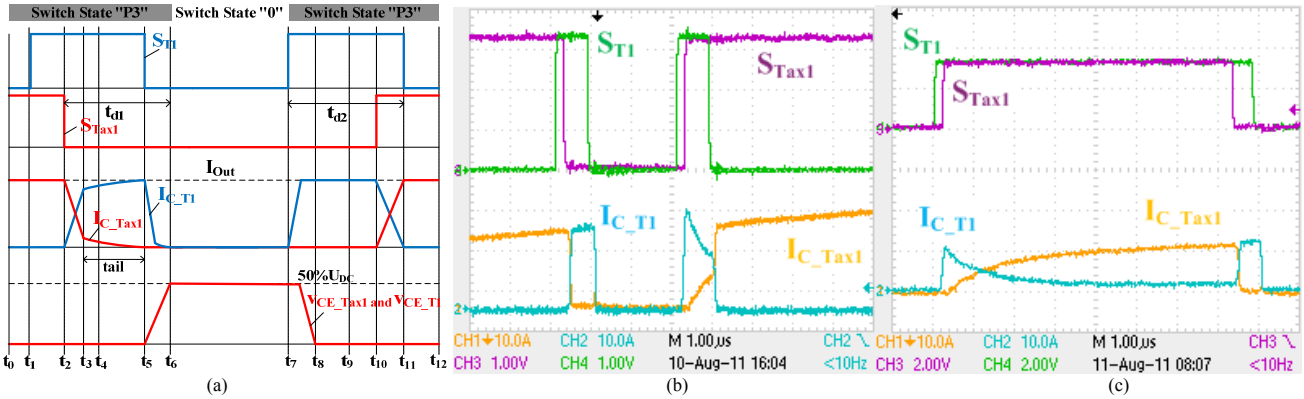

Fig. 8. Commutations (P3↔0). (a) Ideal; (b) and (c) experimental waveforms for (P3↔0). S_{T1} and S_{Tax1} are the switch commands for T_1 and T_{Ax1}, respectively. I_{C_T1} and I_{C_Tax1} are the collector currents of T_1 and T_{Ax1}, respectively. V_{CE_Tax1} is the collector-emitter voltage across T_{Ax1}.

current (I_{Out}>0 or I_{Out}<0) and positive output voltage, U_{Out}, the commutation to or from "P1", "P2" and "0" are given in the following:

a) Commutation "P1" to "0" (P1→0): this commutation starts when T_1 is turned off, and it finishes after a dead time, when T_3 is turned on. If I_{Out}>0, as shown in Fig. 6(a), the current I_{Out} commutates from T_1 to D_5 after T_1 is turned off, and essential turn-off losses occur at T_1. If I_{Out}<0, as shown in Fig. 6(b), the current I_{Out} commutates from D_1/D_2 to T_3 and D_6 after T_3 is turned on. Hence, T_3 face turn-on losses, while D_1 suffers recovery losses.

b) Commutation "0" to "P1" (0→P1): this commutation starts when T_3 is turned off, and it finishes after a dead time, when T_1 is turned on. If I_{Out} >0, as shown in Fig. 6(a), the current I_{Out} commutates from D_5 to T_1 during the turn-on of T_1. In this case, T_1 and D_5 experience turn-on and recovery losses, respectively. If I_{Out} <0, as shown in Fig. 6(b), the current I_{Out} commutates from D_6/T_3 to D_1/D_2 during the turn-off of T_3. Therefore, essential turn off losses occur at T_3.

c) Commutation "P2" to "0" (P2→0): this commutation starts when T_{Ax1} is turned off, and it finishes after a dead time, when T_3 is turned on. If I_{Out} >0, as shown in Fig. 7(a), during the turn-off of T_{Ax1} the current I_{Out} commutates from T_{Ax1} to T_2 and D_5, and essential turn off losses occur at T_{Ax1}. If I_{Out} <0, as shown in Fig. 7(b), the current I_{Out} commutates from D_1/D_2 to T_3 and D_6 after T_3 is turned on. Therefore, T_3 and D_1 experience turn-on and recovery losses, respectively.

d) Commutation "0" to "P2" (0→P2): this commutation starts when T_3 is turned off, and it finishes after a dead time, when T_{Ax1} is turned on. If I_{Out}>0, as shown in Fig. 7(a), the current I_{Out} commutates from T_2 and D_5 to T_{Ax1} after T_{Ax1} is turned on. In this case, T_{Ax1} and D_5 experience turn-on and recovery losses, respectively. If I_{Out} <0, as shown in Fig. 7(b), the current I_{Out} commutates from D_6/T_3 to D_1/D_2 after T_3 is turned off. Therefore, essential turn off losses occur at T_3.

For the switch states "P3" and "N3", particular attention has to be paid to the current distribution between the two redundant paths. For instance, in case T_1 and T_{Ax1} are turned on at once, the on-state characteristics of these devices, the prior switching state, and parasitic inductances would strongly influence the current distribution between these devices and their losses would not be precisely defined.

In order to take advantage of the commonly good switching performance of the path T_1/T_4 and the usually superior on-state characteristic of the path T_{Ax1}/T_{Ax2}, the switching commutation to or from "P3" and "0" (P3↔0), shown in Fig. 8(a), is recommended. Therein, the optimum current transitions between T_1 and T_{Ax1} are shown, where T_1 displays mainly switching losses (turn-off: $t_5 \rightarrow t_6$, and turn on: $t_7 \rightarrow t_8$). T_1 suffers conduction losses only during the times t_{d1} and t_{d2}. These time intervals must be selected considering the current "tail" of the slow switch in order to preserve the soft-switching feature in T_{Ax1}. Note that the interval $t_0 \rightarrow t_2$, with $t_1 \rightarrow t_2$ being very short, must be much bigger than $t_3 \rightarrow t_5$ in order to ensure that the conduction losses during "P3" are mainly dissipated across T_{Ax1}. This commutation was implemented in the prototype depicted in Fig. 3 and the experimental result is shown in Fig. 8(b).

Another commutation possibility for (P3↔0) is shown in Fig. 8(c), where the on-time interval during the "P" state for T_1 overlaps the one for T_{Ax1} in order to ensure that the

switching transitions is performed only by T_1 and the current conduction is executed mainly by T_{Ax1}.

An alternative to the desired commutations, (P3↔0) or (N3↔0), is achieved if during the optimal clamping interval of the SVM modulation (cf. [11]) the system operates only as T-type NPCC, and during all other intervals the system operates solely as the conventional NPCC. Therefore, T_{Ax1}/T_{Ax2} only displays conduction losses, while T_1/T_4 is mainly stressed with switching losses.

B. Loss Balancing Control

As for the A-NPCC, the general approach used to optimize the distribution of the losses over the power semiconductors and/or to equalize their junction temperatures is to always keep the hottest devices as cool as possible [4]. For real-time optimization, the junction temperatures of the main semiconductors need to be estimated, or measured every sampling time. Based on the temperatures and phase current information, a simple algorithm then could select the appropriate commutations in order to alleviate losses from the hottest device for the coming switching period. Therefore, a substantial improvement in the loss distribution can be achieved that enhances the reliability and/or power capability of the system. This feedback-controlled loss balancing method was previously proposed for the A-NPCC in [4], and can be simply adapted to the proposed 3-level H-NPCC by the use of a decision chart for the commutations shown in Table II.

C. New H-NPCC with Five and Seven Levels

Multilevel VSCs, with loss-balancing control characteristics, can be derived from the proposed 3-level H-NPCC version shown in Fig. 1(e). As examples, Fig. 9(a) and 9(b) show the 5- and 7-level VSC, respectively.

IV. Inverter Systems Comparative Evaluation

In order to quantify the feasibility of the proposed 3-level VSC, operating with the loss minimized space vector modulation, an efficiency comparison between this system and other 10kVA rated 3-phase inverters derived from the 2-level VSC, conventional NPCC, T-type NPCC and Active NPCC, is presented. Suitable commercial semiconductors are considered in the analysis (IGBTs IGW25T120 and IKW30N60T), where the loss data is obtained with the test setup shown in Fig. 3. Note that for an accurate analysis of the switching losses the information from the datasheets only would not be enough to enable a fair comparison of the studied systems. Due to the mismatch of voltage rated devices, *e.g.* during the T-type NPCC operation, the turn-on energy of the 1200V IGBTs will be lower if the commutating diode is only 600V rated because of the considerably lower reverse recovery charge. Similarly, the 600V diodes turn-off loss energy will be higher due to the commutating 1200V IGBT.

For the new 3-level H-NPCC two operation modes are considered in the analysis:

a) High efficiency operation (mode 1): the losses of the system are distributed in such a way that the auxiliary switches, T_{Ax1} and T_{Ax2}, only display conduction losses while T_1 and T_4 are mainly stressed with switching losses.

b) Loss balanced operation (mode 2): the operation mode, T-type NPCC or Conventional NPCC, is defined by the real-time calculation of the junction temperatures of the switches following the algorithm presented in Table II.

Table. II- Decision chart for the new 3-level H-NPCC.

Commutation	Phase current	Junction temperatures		Operation
(P ↔ 0)	$I_{out}>0$	$\Delta T_{j\_T1}>\Delta T_{j\_T2}$	$\Delta T_{j\_T1}>\Delta T_{j\_Tax1}$	Ttype NPCC
			$\Delta T_{j\_T1}<\Delta T_{j\_Tax1}$	Conv. NPCC
		$\Delta T_{j\_T2}>\Delta T_{j\_T1}$	$\Delta T_{j\_T2}>\Delta T_{j\_Tax1}$	Ttype NPCC
			$\Delta T_{j\_T2}<\Delta T_{j\_Tax1}$	Conv. NPCC
	$I_{out}<0$	$\Delta T_{j\_T1}>\Delta T_{j\_T2}$		Type or NPCC
		$\Delta T_{j\_T2}>\Delta T_{j\_T1}$		Type or NPCC
(N ↔ 0)	$I_{out}>0$	$\Delta T_{j\_T4}>\Delta T_{j\_T3}$		Type or NPCC
		$\Delta T_{j\_T3}>\Delta T_{j\_T4}$		Type or NPCC
	$I_{out}<0$	$\Delta T_{j\_T4}>\Delta T_{j\_T3}$	$\Delta T_{j\_T4}>\Delta T_{j\_Tax2}$	Ttype NPCC
			$\Delta T_{j\_T4}<\Delta T_{j\_Tax2}$	Conv. NPCC
		$\Delta T_{j\_T3}>\Delta T_{j\_T4}$	$\Delta T_{j\_T3}>\Delta T_{j\_Tax2}$	Ttype NPCC
			$\Delta T_{j\_T3}<\Delta T_{j\_Tax2}$	Conv. NPCC

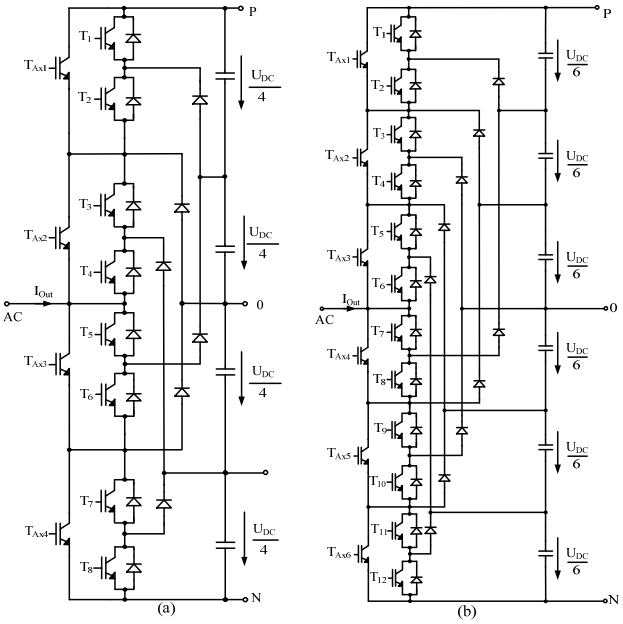

Fig. 9- Novel multilevel H-NPCC: (a) 5-level; and (b) 7-level versions.

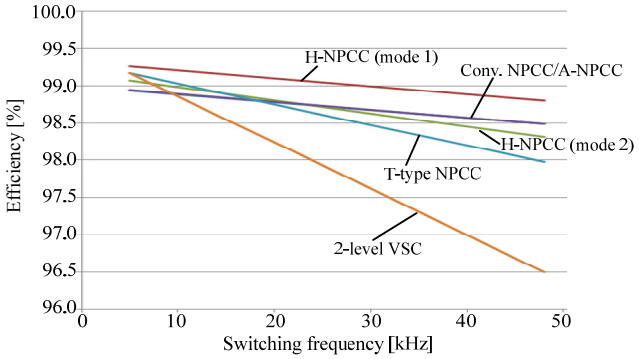

Fig. 10- Efficiency comparison between the different topologies of 10kVA inverters employing commercial semiconductors (operation: unity power factor; output voltage peak $\hat{U}_{Out}$=325V; and $\hat{I}_{Out}$=20.5A).

In Fig. 10 the pure semiconductor efficiency of the studied inverters is presented for operation in the switching frequency range of 5 kHz to 48 kHz and low DC-link voltage level (U_{DC}=700V). For each system, the resulting averaged power loss distribution of the individual elements in a phase-leg for 48 kHz switching frequency operation is

shown in Fig. 4 and 11. The simulated junction temperatures for the new 3-level H-NPCC in mode 2 operating at 48 kHz with SVM modulation are presented in Fig. 12.

As can be seen in Fig. 10, the H-NPCC, operating in mode 1, can always achieve the highest efficiency. This happen because this system suffers the lowest conduction and switching losses among all analyzed topologies. However, in contrast to the A-NPCC, the power losses across the transistors T_1, T_2, T_3 and T_4 are not equalized.

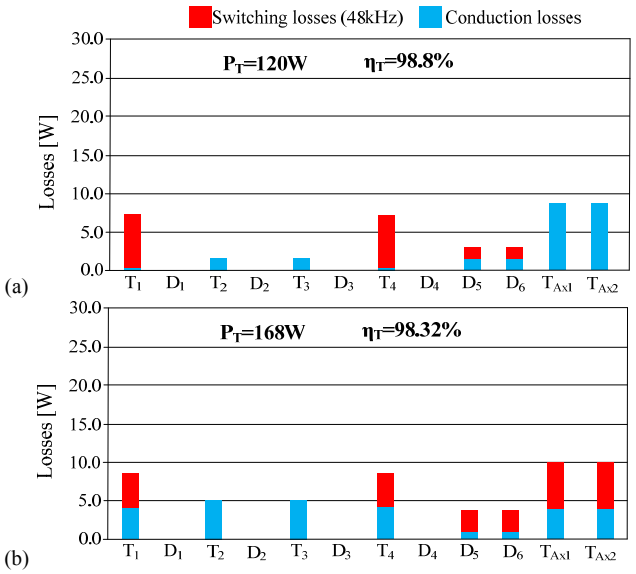

Fig. 11- New 3-level H-NPCC phase-leg components loss distribution: (a) mode 1; and (b) mode 2.

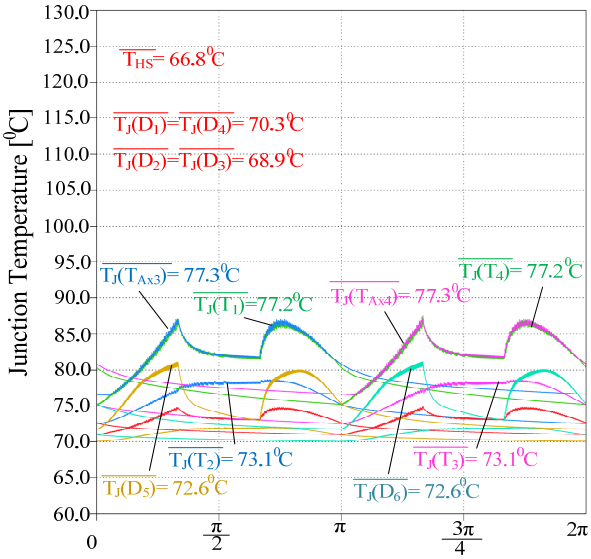

Fig. 12. New 3-level H-NPCC phase-leg components operating/averaged junction temperatures.

As for the A-NPCC, a substantial improvement in the loss and junction temperature distribution across the devices of the phase-leg can be achieved with the new 3-level H-NPCC. As can be seen in Fig. 10, the new 3-level inverter in mode 2, only displays better efficiency than the A-NPCC for switching frequencies below 25 kHz. Due to the fact that the A-NPCC cannot balance the losses across the auxiliary switches, a better thermal distribution among all the devices could be achieved with the new system. Note that the loss balancing algorithm of Table II aims to distribute the losses between T_1 and T_2 (T_3 and T_4), but it does not permit the auxiliary switches to be more thermally stressed than these devices. This is the reason that the junction temperature across the NPCC switches are not even for the 48 kHz operation (cf. Fig 12). In fact, without the loss limitation of the auxiliary switches, the thermal profile of the NPCC switches would be indeed equalized; however the auxiliary switches would face very high losses during high operating switching frequency.

V. CONCLUSIONS

This paper has studied several 3-level VSC topologies, including the conventional NPCC, the A-NPCC and various T-type systems. The problem of loss and junction temperature distribution across the semiconductors in the 3-level NPCC and T-type VSCs has been investigated.

A novel 3-level H-NPCC is introduced, where the switch states and commutations of the converter have been thoroughly analyzed. It was shown that this new solution can achieve not only higher efficiency than many typical 3-level structures, but it can also overcome their drawback of unsymmetrical semiconductor loss distribution. Therefore, a remarkable increase of the converter output power capability and/or system reliability can be accomplished.

An efficiency comparison between the studied topologies for 10 kVA inverter operation in the switching frequency range of 5kHz to 48 kHz and low DC-link voltage level was presented to demonstrate the performance and feasibility of the novel 3-level solution.

REFERENCES

[1] R. H. Baker, "Bridge converter circuit," U.S. Patent 4 270 163, May 26. 1981.

[2] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 17, no. 5, pp. 518-523, Sept./Oct. 1981.

[3] T. Soeiro, M. Schweizer, J. Linner, P. Ranstad, and J. W. Kolar, "Comparison of 2- and 3-level active filters with enhanced bridge-leg loss distribution," in *Proc. 8th International Conf. on Power Electronics (ECCE Asia)*, 2011.

[4] T. Brückner, S. Bernet, and H. Güldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 855-868, June 2005.

[5] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low voltage drives, traction, and utility applications," *IEEE Trans. Ind. Appl.*, vol. 41, May 2005.

[6] M. Schweizer, I. Lizama, T. Friedli, and J. W. Kolar, "Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies," in *Proc. 36th Annual Conf. of IEEE Industrial Electronics (IECON)*, 2010.

[7] A. Stupar, D. Bortis, U. Drofenik, and J. W. Kolar, "Advanced setup for thermal cycling of power modules following definable junction temperature profiles," IPEC, Sapporo, Japan, 2010.

[8] T. Anzawa, Q. Yu, M. Yamagiwa, T. Shibutani, and M. Shiratori, "Power cycle fatigue reliability evaluation for power device using coupled electrical-thermal-mechanical analysis," *ITHERM 2008*, pp.815-821, May 2008.

[9] T. Brückner and S. Bernet, "Loss balancing in three-level voltage source inverters applying active NPC switches," in *Proc. IEEE Power Electron. Spec. Conf.*, Vancouver, BC, Canada, 2001, pp. 1135-1140.

[10] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219-2230, July 2010.

[11] B. Kaku, I. Miyashita, and S. Sone, "Switching loss minimized space vector PWM method for IGBT three-level inverter," *IEE Proceedings. Electric Power Applications*, Vol. 144, pp. 182-190, May 1997.