Volume Minimization of the Main DM/CM EMI Filter Stage of a Bidirectional Three-Phase Three-Level PWM Rectifier System

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Abstract—Three-phase voltage source AC–DC converters disclose a differential mode (DM) and a considerable common mode (CM) bridge-leg output voltage at the switching frequency, which need to be filtered by an EMI input filter to comply with conducted EMI standards (e.g. CISPR 11) at the mains terminal. Additionally, the EMI filter (which in this paper includes the boost inductor) should usually limit the maximum peak-to-peak bridge-leg output current ripple, to which a DM and CM component contribute, to 20%–40% of the nominal peak current. Typically, the DM current ripple is defined by the boost inductance $L_{dm,1}$ and the CM current ripple by the CM inductance $L_{cm,1}$. Therefore, a degree of freedom in the filter design exists: different combinations of $L_{dm,1}$ and $L_{cm,1}$ lead to the same peak-to-peak bridge-leg output current ripple. Accordingly, this paper investigates the optimal ratio $k_{L,opt} = L_{cm,1}/L_{dm,1}$, which minimizes the volume of the main LC stage of the DM/CM EMI input filter. To achieve a compact filter, it is demonstrated for a 10 kW PWM rectifier system that for $k_L \geq 3$ the boxed filter volume is almost constant. Additionally, $k_{L,opt} = 14$ minimizes the stray field of the CM choke $L_{cm,1}$ and leads to a minimal boxed filter volume of 0.43 ltr. for a filter cooled by natural convection.

Keywords: *EMI Filter, PWM Rectifier System, Common Mode, Differential Mode, Volume Minimization, Protective Earth, Leakage Inductance*.

I. INTRODUCTION

Three-phase voltage source AC–DC converters with sinusoidal input current, also denominated as Power Factor Correction (PFC) rectifiers, are widely used, e.g. as mains interfaces of photovoltaic systems [1], input stages of telecommunication power supply modules [2] or controllable AC sources [3]. The bidirectional Pulse Width Modulation (PWM) rectifier system considered in this paper is depicted in **Fig. 1** and is employed as the input stage of a high bandwidth AC source [4]. The system is based on a 3-level Neutral Point Clamped (NPC) Voltage Source Converter (VSC) topology with the electrical specifications summarized in **Table I**.

Mains connected converter systems need to comply with international standards limiting the amplitudes of the low-frequency and the high-frequency current and voltage harmonic components. The standards limiting the amplitudes of the low-frequency harmonics usually consider only harmonics

TABLE I. ELECTRICAL PARAMETERS OF THE BIDIRECTIONAL THREE-PHASE PWM RECTIFIER SYSTEM SHOWN IN **FIG. 1**.

Nominal power P_{nom}	10 kW
Mains voltage U_{mains}	400 $V_{ll,rms}$ ($+10\%, -15\%$)
Nominal current I_{nom}	14.5 A_{rms}
Nominal DC-link voltage $U_{dc,nom}$	700 V
Mains frequency f_{mains}	50 Hz
Switching (carrier) frequency f_s	50 kHz

with ordinal numbers $\leq$ 40, i.e. $f_h \leq$ 2 kHz for 50 Hz systems (e.g. IEC 61000-3-2 / IEC 61000-3-12). Thus, for the selected switching frequency of the system of $f_s =$ 50 kHz (cf. **Table I**), these regulations can be fulfilled with a proper adjustment of the phase current and DC-link voltage controllers.

The standards limiting the amplitudes of the high-frequency spectral components specify the threshold in terms of conducted noise emission (measured in dBμV), e.g. in the frequency range of [150 kHz, 30 MHz] for CISPR 11, class A and B. Hence, the Electro-Magnetic Interference (EMI) input filter, consisting of a Differential Mode (DM) and a Common Mode (CM) filter, of the PWM rectifier system (cf. **Fig. 1**), needs to be designed such that the levels of the conducted emissions are below the specified limits. Additionally, the maximum peak-to-peak current ripple of the bridge-leg output currents, e.g. i_a (cf. **Fig. 1**), is typically limited to 20%–40% of the nominal peak current $\hat{i}_{nom} = \sqrt{2} \cdot I_{nom}$. The reasons are the following: first, to avoid a drastic control performance degradation of the input currents i_a, i_b, i_c due to a small time deviation from the ideal sampling instants; second, to possibly obviate a large difference of the switching losses in all power semiconductors within one bridge-leg depending on the loss distribution among the semiconductors and the dependency of the losses on the switched current; and third, the high-frequency winding and core losses of the inductive components (mainly $L_{dm,1}$ and $L_{cm,1}$) should be kept at reasonable values.

Furthermore, in order to be able to utilize the full (linear) modulation range, e.g. to maintain converter operation at
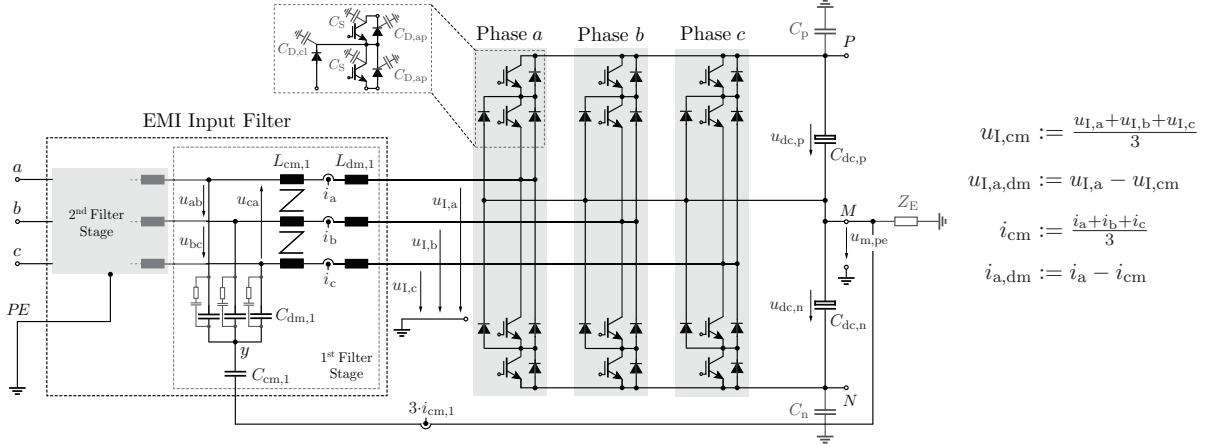
Figure 1. Bidirectional three-phase PWM rectifier system with an EMI input filter which builds the input stage of a high bandwidth AC source.

$$u_{I,cm} := \frac{u_{I,a} + u_{I,b} + u_{I,c}}{3}$$

$$u_{I,a,dm} := u_{I,a} - u_{I,cm}$$

$$i_{cm} := \frac{i_a + i_b + i_c}{3}$$

$$i_{a,dm} := i_a - i_{cm}$$

an increase of the mains voltage by 10% (cf. **Table I**), and to reduce the converter AC side current ripple in i_a at the switching frequency, a Space Vector Modulation (SVM) or a carrier based sinusoidal modulation with a superimposed third harmonic can be employed as modulation scheme. In this paper, the latter modulation scheme is considered. Since the converter AC side voltages $u_{I,a}$, $u_{I,b}$, $u_{I,c}$ contain discrete voltage levels, e.g. three voltage levels for the considered three-level NPC VSC, the sum of all converter voltages $u_{I,a} + u_{I,b} + u_{I,c}$ is not zero for all instants resulting in a CM voltage component. The definitions of CM and DM voltages and currents are given in **Fig. 1**.

Thus, considering the selected modulation scheme, the bridge-leg and the DC-link in **Fig. 1** can be replaced for each phase, e.g. phase a, by a low-frequency DM voltage source $u_{I,a,dm,lf}$ (at f_{mains}), a high-frequency DM voltage source $u_{I,a,dm,hf}$ (at f_s), a low-frequency CM voltage source $u_{I,cm,lf}$ (at $3 \cdot f_{mains}$) and a high-frequency CM voltage source $u_{I,cm,hf}$ (at f_s) as shown in **Fig. 2**. Besides the investigated first filter stage, a second filter stage is required in order to comply with e.g. CISPR 11. This stage can be realized as a LCL stage as shown in **Fig. 2**.

The difficulty of filtering the switched CM converter output voltage $u_{I,cm,hf}$ is the limited capacitance of the Y-capacitors (a few tens of nanofarads) connected to ground in order not to exceed the maximum allowed protective conductor current of $3.5\,mA_{rms}$ (e.g. IEC 60335-1 for household and similar electrical appliances; IEC 60950-1 for information technology equipment). Thus, it is preferred to achieve the filtering with an internal CM filter capacitor, i.e. with the capacitor $C_{cm,1}$ that is connected between the star-point y of the DM capacitors $C_{dm,1}$ and the midpoint of the DC-link capacitors M (cf. **Fig. 1**) [5]. $C_{cm,1}$ together with an additional CM inductor $L_{cm,1}$ in series to the DM boost inductor $L_{dm,1}$ build then a CM LC filter stage. For $C_{cm,1}$ higher capacitance values can be employed and therefore the achieved CM attenuation, especially at the

switching frequency (cf. **Section II**), can be increased (for the same CM inductance $L_{cm,1}$) as the low-frequency as well as the high-frequency CM currents $i_{cm,lf}$, $i_{cm,hf}$ are confined to the converter system. Typically, the emissions are measured with a Line Impedance Stabilization Network (LISN) connected to the converter system.

However, the higher the value of the capacitance $C_{cm,1}$ the lower the impedance of the return path from y to M for the high-frequency as well as the low-frequency CM currents. Meanwhile, a lower impedance of $C_{cm,1}$ has the advantage to reduce the high-frequency CM emissions, it has the disadvantage to increase the low-frequency CM current: Because the impedance of the CM choke $L_{cm,1}$ is typically negligible compared to the impedance of $C_{cm,1,eff} = C_{cm,1} \cdot 3 \cdot C_{dm,1} / (C_{cm,1} + 3 \cdot C_{dm,1}) \approx C_{cm,1}$ (assuming $C_{dm,1}$ to be at least one order of magnitude larger than $C_{cm,1}$) at $3 \cdot f_{mains}$, the third harmonic converter output voltage generated by the selected modulation scheme is directly applied to $C_{cm,1}$ [cf. **Fig. 3(b)**]. Thus, a lower impedance value of $C_{cm,1}$ at $3 \cdot f_{mains}$, due to the increased capacitance of $C_{cm,1}$, increases the low-frequency CM current $i_{cm,lf}$. Accordingly, to limit the amplitude of $i_{cm,lf}$ to reasonable values, the capacitance of $C_{cm,1}$ cannot exceed a certain maximum value.

Moreover, the higher capacitance values of $C_{cm,1}$ compared to the ones of the aforementioned Y-capacitors lead to a non negligible CM current ripple superimposed on the DM current ripple. Hence, considering **Fig. 2** and phase a, both, the DM current $i_{a,dm}$ as well as the CM current i_{cm} contribute to the maximum peak-to-peak bridge-leg output current ripple, i.e.

$$\Delta i_{a,pp,max} = \max\{i_{a,dm,hf}(t) + i_{cm,hf}(t)\} - \min\{i_{a,dm,hf}(t) + i_{cm,hf}(t)\}. \quad (1)$$

$i_{a,dm,hf}$ is generated by $u_{I,a,dm,hf}$ and $i_{cm,hf}$ by $u_{I,cm,hf}$. Therefore,
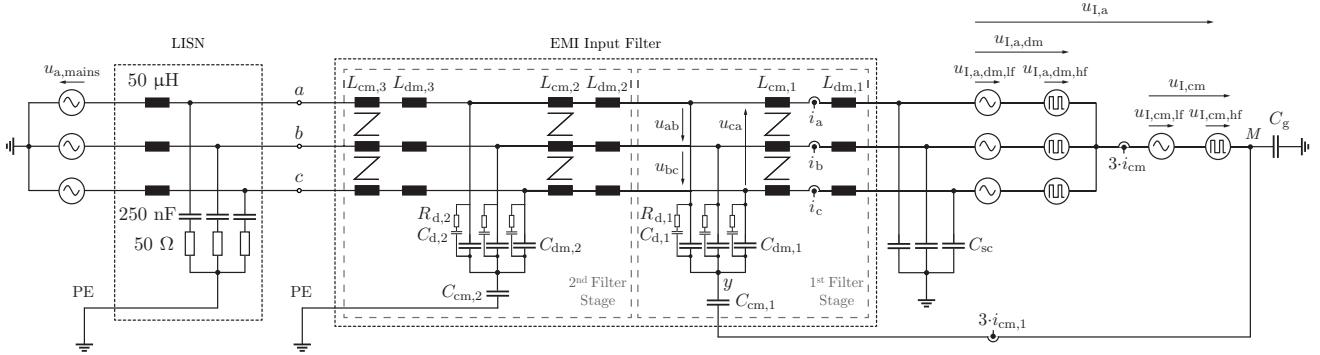
Figure 2. Equivalent circuit of the bidirectional three-phase PWM rectifier system depicted in **Fig. 1**, where the bridge-legs and the DC-link are replaced by low- and high-frequency DM voltage sources $u_{\mathrm{I,a,dm,lf}}$, $u_{\mathrm{I,a,dm,hf}}$ and CM voltage sources $u_{\mathrm{I,cm,lf}}$, $u_{\mathrm{I,cm,hf}}$. A possible realization of the 2nd filter stage as a DM and CM LCL stage is shown. It is assumed that the midpoint of the DC-link M is connected to ground by a parasitic capacitance C_{g} and that the entire low-frequency CM current is flowing through the return path from y to M built by $C_{\mathrm{cm,1}}$ - i.e. the magnitude of the impedance of $C_{\mathrm{cm,1,eff}} = C_{\mathrm{cm,1}} \cdot 3 \cdot C_{\mathrm{dm,1}} / (C_{\mathrm{cm,1}} + 3 \cdot C_{\mathrm{dm,1}})$ [damping elements neglected] is much lower than the one of C_{g} at $3 \cdot f_{\mathrm{mains}}$ [cf. **Fig. 3(b)**], leading to $i_{\mathrm{cm,1,lf}} = i_{\mathrm{cm,lf}}$.

if $\Delta i_{\mathrm{a,pp,max}}$ is kept constant, i.e.

$$\Delta i_{\mathrm{a,pp,max}} = \mathrm{const.}, \tag{2}$$

a weaker limitation of the peak value of $i_{\mathrm{a,dm,hf}}$ (smaller inductance of $L_{\mathrm{dm,1}}$) requires a stronger limitation of the peak value of $i_{\mathrm{cm,hf}}$ (higher inductance of $L_{\mathrm{cm,1}}$) and vice versa. Accordingly, the ratio between $L_{\mathrm{dm,1}}$ and $L_{\mathrm{cm,1}}$ represents a degree of freedom in the filter design. On the one hand, for the theoretical case of $L_{\mathrm{dm,1}} \to \infty$, the DM as well as the CM current ripple would be zero. On the other hand, for $L_{\mathrm{cm,1}} \to \infty$ only the CM current ripple would vanish (neglecting the straying of the CM choke). Hence, this paper analyzes if an optimal ratio

$$k_{\mathrm{L,opt}} = \frac{L_{\mathrm{cm,1}}}{L_{\mathrm{dm,1}}} \tag{3}$$

exists which minimizes the total filter volume $V_{\mathrm{1,tot}} = 3 \cdot V_{\mathrm{L,dm,1}} + V_{\mathrm{L,cm,1}} + 3 \cdot V_{\mathrm{C,dm,1}} + V_{\mathrm{C,cm,1}}$ of the 1st stage of the EMI input filter depicted in **Fig. 1**. Additionally, other aspects as e.g. the maximum peak-to-peak DM and CM voltage ripple across $C_{\mathrm{dm,1}}$ and $C_{\mathrm{cm,1,eff}} = C_{\mathrm{cm,1}} \cdot 3 \cdot C_{\mathrm{dm,1}} / (C_{\mathrm{cm,1}} + 3 \cdot C_{\mathrm{dm,1}})$ [cf. **Fig. 2**] respectively, are taken into considerations (as further explained in **Section III**).

As mentioned above, the focus of the paper is on the optimal selection of $L_{\mathrm{dm,1}}$, $L_{\mathrm{cm,1}}$ to obtain the minimal total filter volume $V_{\mathrm{1,tot}}$ and not on the design of the second filter stage. Accordingly, this paper is structured as follows: **Section II** motivates the structure of the first DM/CM LC stage of the EMI input filter shown in **Fig. 1** and **Section III** explains the electrical side conditions to have a well-defined interface of this first filter stage to the second stage as well as to the converter. The proposed approach to design the first DM/CM LC filter stage with minimal volume and, thus, to determine $k_{\mathrm{L,opt}}$ is detailed in **Section IV**. Because the DM and CM inductor modeling is crucial for the optimization, **Section V** describes in detail the modeling of the two inductive filter components. Finally, the optimization results are presented in

Section VI and the conclusions are given in **Section VII**.

II. STRUCTURE OF THE FIRST DM/CM LC STAGE OF THE EMI INPUT FILTER

To compare the proposed filter structure with a capacitor $C_{\mathrm{cm,1}}$ connected between y and M to a conventional EMI filter where a Y-capacitor $C_{\mathrm{cm,1,pe}}$ is connected between y and ground, the parasitic capacitances from the converter to ground need to be considered. In accordance to [5], the parasitic capacitors considered in this paper are depicted in **Fig. 1** and are

- C_{S}, $C_{\mathrm{D,ap}}$, $C_{\mathrm{D,cl}}$: parasitic capacitances of the IGBTs, antiparallel and clamping diodes to the grounded heat sink. Typically, to avoid floating potentials, the heat sink is connected to <u>P</u>rotective <u>E</u>arth (PE).
- C_{p}, C_{n}: parasitic capacitances of the positive and negative DC-link rails to ground.
- Z_{E}: parasitic impedance of the DC-link midpoint M to ground. Typically, this impedance is assessed by a capacitor, i.e. $Z_{\mathrm{E}} = \frac{1}{s \cdot C_{\mathrm{E}}}$ in the complex frequency domain, which is assumed in this paper.

The switches with the antiparallel diodes are embedded in a DuoPack (IKW50N60T - PG-TO-247-3-21) and the clamping diodes are fast recovery diodes (IDW50E60 - PG-TO-247-3) from Infineon Technologies Inc. Considering the electrical insulation pad (Hi-Flow™ 625 manufactured by The Bergquist Company) between the power semiconductors and the grounded heat sink, the parasitic capacitance of the PG-TO-247-3 packages to ground is assessed to

$$C_{\mathrm{S}} + C_{\mathrm{D,ap}} = C_{\mathrm{D,cl}} \approx 50 \text{ pF}, \tag{4}$$

and, accordingly, the maximum parasitic capacitance of one bridge-leg to ground (cf. **Fig. 2**) is obtained when e.g. phase a is connected to the positive DC-link rail and amounts to

$$C_{\mathrm{sc}} = 3 \cdot (C_{\mathrm{S}} + C_{\mathrm{D,ap}}) + C_{\mathrm{D,cl}} \approx 200 \text{ pF}. \tag{5}$$

The equivalent circuit shown in **Fig. 2** can be separated in single-phase DM and CM equivalent circuits as depicted in
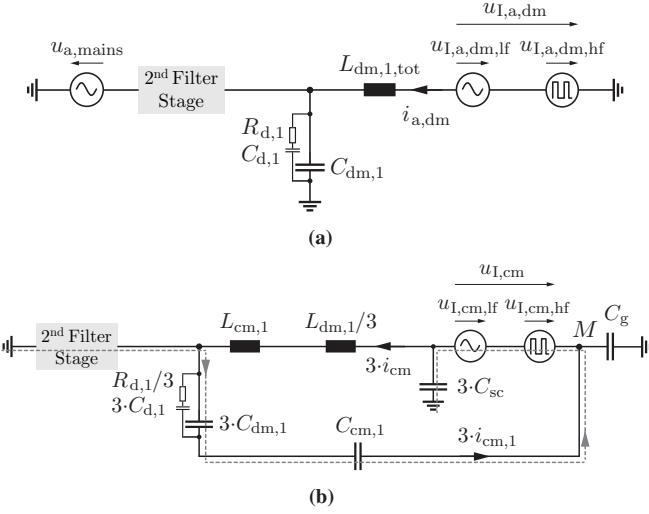
(a)

(b)

Figure 3. DM equivalent circuit **(a)** and CM equivalent circuit **(b)** of the bidirectional PWM rectifier system (cf. **Fig. 1** and **Fig. 2**). The damping elements $C_{d,1}$ and $R_{d,1}$ are however neglected in the optimization.

Fig. 3. $L_{dm,1,tot}$ and $L_{cm,1,tot}$ are the total inductances which limit the DM and CM currents, respectively, and are defined as

$$
\begin{aligned}
L_{dm,1,tot} &:= L_{dm,1} + L_{\sigma,1}, \\
L_{cm,1,tot} &:= L_{cm,1} + \frac{L_{dm,1}}{3},
\end{aligned}
\tag{6}
$$

where $L_{dm,1}$ denotes the DM inductance realized by the DM inductor, $L_{cm,1}$ is the CM inductance and $L_{\sigma,1}$ is the leakage inductance of the CM choke as further explained in **Section V**. The parasitic capacitances from the positive and negative DC-link rails to ground as well as the capacitance from the DC-link midpoint to earth are all in parallel (in the CM equivalent circuit) and can, thus, be summarized to one capacitance

$$
C_g = C_p + C_n + C_E,
\tag{7}
$$

which is typically in the range of nanofarads and, hence, much larger than C_{sc}, i.e. $C_g \gg C_{sc}$.

In order to assess the benefit of connecting the capacitor $C_{cm,1}$ between the star-point y of the first DM filter stage and the DC-link midpoint M compared to the conventional approach where a Y-capacitor $C_{cm,1,pe}$ is connected between y and ground, the obtained CM attenuations of the first filter stage for both filter configurations are compared in **Fig. 4**. $u_{LISN,yM}$ and $u_{LISN,yPE}$ are the CM voltages across the 50 Ω/50 µH LISN resistance when $C_{cm,1}$ is connected between y and M and when $C_{cm,1,pe}$ is connected between y and ground, respectively. The LISN (cf. **Fig. 2**) is directly connected to the first filter stage (not considering the second filter stage). For the comparison a total CM inductance of $L_{cm,1,tot} = 1$ mH is assumed and the value of $C_{cm,1,pe}$ is selected based on the following considerations. For safety reasons, the regulation IEC 60990 specifies the measurement setup and (normal as well as fault) conditions for which the protective conductor current is measured. The
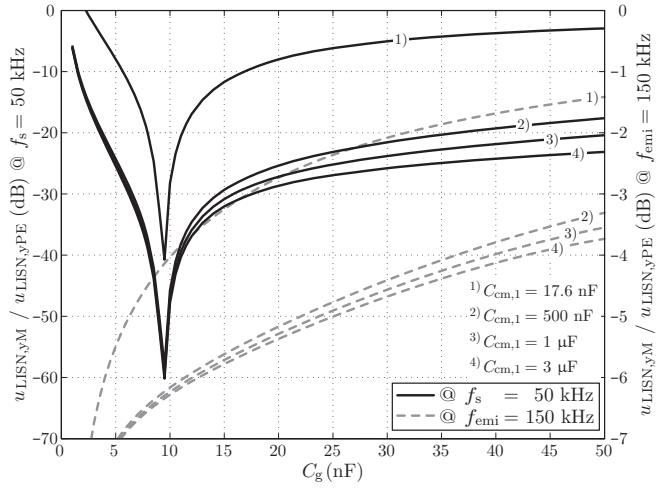

Figure 4. Comparison of the CM voltage drops $u_{LISN,yM}$, $u_{LISN,yPE}$ at the 50 Ω/50 µH LISN's resistance (LISN connected to the first filter stage) for different values of $C_{cm,1}$ for the proposed filter structure of the first stage where $C_{cm,1}$ is connected between y and M (cf. **Fig. 2**) and the conventional filter structure where a Y-capacitor $C_{cm,1,pe}$ is connected between y and ground: obtained CM attenuation at the switching frequency $f_s = 50$ kHz (black curves) and at the first harmonic frequency within [150 kHz, 30 MHz] (range which is relevant for the EMI emissions, e.g. defined by CISPR 11), i.e. $f_{emi} = 150$ kHz (dashed gray curves).
Circuit parameters: $L_{dm,1,tot} = 165$ µH, $C_{dm,1} = 3$ µF, $C_{d,1} = 0.6$ µF, $R_{d,1} = 42.6$ Ω, $L_{cm,1,tot} = 1$ mH, $C_{cm,1,pe} = 17.6$ nF, $C_{sc} = 200$ pF [cf. **Fig. 3(b)**].

applicable fault conditions change depending on the power system (e.g. star TN-S, star 3-line IT or unearthed delta power system) the three-phase PWM rectifier system is connected to. The worst case protective conductor current is obtained in case one of the phases is short-circuited to ground (e.g. for the star 3-line IT and the unearthed delta power system). In this case and for the filter structure as given (cf. **Fig. 2**), the contribution of the current through $C_{cm,1,pe}$ to the protective conductor current can be assessed by $2 \cdot \pi \cdot f_{mains} \cdot C_{cm,1,pe} \cdot 1.1 \cdot U_{mains}/\sqrt{3}$. The factor 1.1 takes the increase by 10% of the mains voltage into account (cf. **Table I**). Because one filter stage is typically insufficient to achieve enough CM attenuation to fulfill e.g. CISPR 11, the contribution of the current through $C_{cm,2}$ to the protective conductor current under fault conditions needs to be accounted as well. If the same current through $C_{cm,1,pe}$ and $C_{cm,2}$ is allowed, the maximum capacitance value of $C_{cm,1,pe}$ is given by

$$
C_{cm,1,pe,max} = \frac{0.8 \cdot \frac{3.5 \text{ mA}_{rms}}{2}}{2 \cdot \pi \cdot f_{mains} \cdot \frac{U_{mains}}{\sqrt{3}}} = 17.6 \text{ nF},
\tag{8}
$$

considering a margin of 20% to account for the high-frequency protective conductor currents. Thus, the maximum protective conductor current limits directly the maximum value of the CM Y-capacitors and accordingly the effectiveness of their filtering.

Considering **Fig. 4**, the advantages of connecting $C_{cm,1}$ between y and M (and not to ground) are the following:

- Reduction of the required CM attenuation which needs to be provided by the second filter stage in order to

comply with CISPR 11. Thus, the 2nd filter stage can be realized with smaller filter elements, resulting potentially in a reduced volume, losses and parasitic elements of the components.

- Reduction of the CM voltage ripple across the capacitor $C_{cm,1}$ at the switching frequency and hence reducing the CM volt-seconds for the CM chokes (less core cross-section needed) of the second filter stage.
- Increasing the capacitance of $C_{cm,2}$ is possible, because $C_{cm,1}$ does not potentially contribute to the protective conductor current. Therefore, the CM inductance of the CM chokes (in the 2nd filter stage) can be reduced.

It is noted by considering **Fig. 3(b)**, that the connection of y and M with the capacitor $C_{cm,1}$ evokes an additional path for the high-frequency CM emissions which bypasses the CM inductor $L_{cm,1}$ [5]. The indicated path can be dominant for the CM noise emissions, depending on the impedances of the filter components and, especially, depending on the value of the parasitic capacitance C_{sc} of the power semiconductors to earth. For the case at hand, the higher the value of the parasitic capacitance C_{sc} the lower the obtained CM attenuation of the first filter stage. This means, that for higher C_{sc}'s than the considered 200 pF, the proposed structure of the first filter stage [cf. **Fig. 3(b)**] possibly has a lower attenuation than a conventional filter structure with $C_{cm,1,pe}$ connected between y and ground. Therefore, for each case at hand it needs to be investigated which filter structure gives the better CM noise suppression.

III. ELECTRICAL SIDE CONDITIONS FOR THE MINIMIZATION OF THE FILTER VOLUME

Before presenting the approach to find the minimal volume of the first DM/CM LC filter stage, the electrical side conditions, i.e. the voltages and currents at the interface of the 1st filter stage to the 2nd and at the interface of the filter to the converter, are defined and motivated in this section. The side conditions are needed to guarantee, firstly, an electrically meaningful optimization result, and, secondly, to avoid that the 1st filter stage is optimized at the cost of the 2nd stage. It is the goal that with the subsequently derived side conditions, the 2nd

TABLE II. ELECTRICAL SPECIFICATIONS FOR THE VOLUME MINIMIZATION OF THE FIRST DM/CM LC STAGE OF THE EMI INPUT FILTER.

Max. peak-to-peak converter output current ripple $\Delta i_{a,pp,max} = 0.25 \cdot \sqrt{2} \cdot I_{nom}$	5.1 A
Max. peak-to-peak DM voltage ripple across $C_{dm,1}$ $\Delta u_{C,dm,1,pp,max} = 0.025 \cdot \sqrt{\frac{2}{3}} \cdot U_{ll,nom}$	8.1 V
Max. peak-to-peak CM voltage ripple across $C_{cm,1,eff}$ $\Delta u_{C,cm,1,pp,max} = 0.025 \cdot \sqrt{\frac{2}{3}} \cdot U_{ll,nom}$	8.1 V
Max. capacitive reactive peak current $\hat{i}_{C,dm,1,lf,max}$	0.51 A
Max. low-frequency CM peak current $\hat{i}_{cm,1,lf,max}$	0.51 A

filter stage and the converter can be designed without knowing the exact values of the 1st filter stage.

As explained in **Section I**, on the one hand the maximum peak-to-peak bridge-leg output current ripple $\Delta i_{a,pp,max}$ is usually limited to 20%–40% of the nominal peak current $\hat{i}_{nom}$. In this paper, the limit is set to 25% (cf. **Table II**). Moreover, the current ripple $\Delta i_{a,pp,max}$ depends on both, the DM inductance $L_{dm,1,tot}$ and CM inductance $L_{cm,1,tot}$ (cf. **Fig. 3**). However, the maximum peak-to-peak DM and CM current ripples $\Delta i_{a,dm}$ and Δi_{cm} do not occur at the same instants. On the other hand, the values of the inductances $L_{dm,1,tot}$ and $L_{cm,1,tot}$ (for constant capacitance values of $C_{dm,1}$ and $C_{cm,1}$) affect the current ripples of $\Delta i_{a,dm}$ and Δi_{cm}, and hence also the voltage ripples $\Delta u_{C,dm,1}$ across $C_{dm,1}$ and $\Delta u_{C,cm,1}$ across $C_{cm,1,eff} = C_{cm,1} \cdot 3 \cdot C_{dm,1} / (C_{cm,1} + 3 \cdot C_{dm,1})$, respectively.

The DM and CM attenuations which are achieved with the first filter stage are plotted in **Fig. 5** for different DM and CM maximum peak-to-peak voltage ripples $\Delta u_{C,dm,1,pp,max}$, $\Delta u_{C,cm,1,pp,max}$. The figure highlights that the achieved CM attenuation is almost independent of $\Delta u_{C,cm,1,pp,max}$ due to the aforementioned path for the current through C_{sc} which bypasses the CM inductor [cf. **Fig. 3(b)**]; meanwhile the DM attenuation depends strongly on $\Delta u_{C,dm,1,pp,max}$.

The total EMI input filter (1st + 2nd filter stage) typically needs to provide roughly 80 dB–86 dB of DM as well as CM attenuations in order to comply with e.g. CISPR 11. Furthermore, it is preferred to distribute the entire attenuation equally to both filter stages. Thus, considering **Fig. 5**, the maximum peak-to-peak DM voltage ripple $\Delta u_{C,dm,1,pp,max}$ is
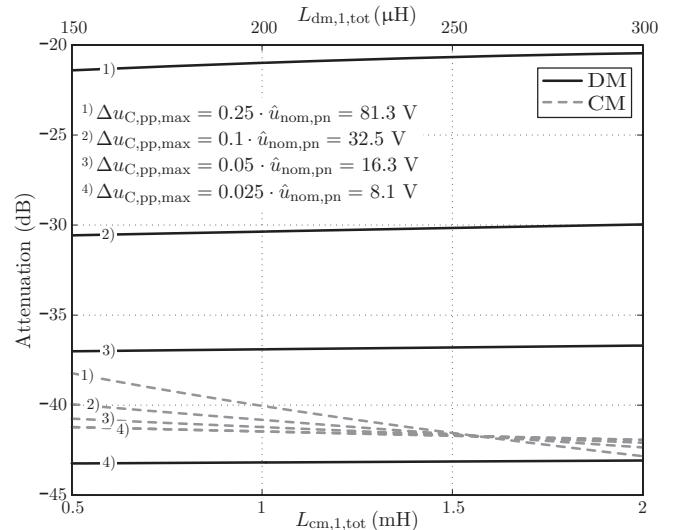

Figure 5. Achieved DM and CM attenuations of the first filter stage over $L_{dm,1,tot}$ and $L_{cm,1,tot}$, respectively (cf. **Fig. 3**), for different DM as well as CM maximum peak-to-peak voltage ripples $\Delta u_{C,dm,1,pp,max}$ and $\Delta u_{C,cm,1,pp,max}$. In the figure, $\Delta u_{C,pp,max} = \Delta u_{C,dm,1,pp,max} = \Delta u_{C,cm,1,pp,max}$ is set.

limited to 2.5% of the nominal peak voltage (phase to neutral) $\hat{u}_{\mathrm{nom,pn}} = \sqrt{2} \cdot U_{\mathrm{ll,nom}}/\sqrt{3}$.

Even though the CM attenuation of the first filter stage is almost unaffected by the value of $\Delta u_{\mathrm{C,cm,1,pp,max}}$, it is reasonable to limit the maximum peak-to-peak voltage ripple. In this way, the CM volt-seconds for the CM chokes of the 2$^{\mathrm{nd}}$ filter stage (cf. **Fig 2**) are restricted. Therefore, in this paper $\Delta u_{\mathrm{C,cm,1,pp,max}}$ is limited as well to 2.5% of the nominal peak voltage $\hat{u}_{\mathrm{nom,pn}}$ (phase to neutral).

To benefit from a full utilization of the (linear) modulation range and to reduce the current ripple of the converter output current i_{a} at the switching frequency, a carrier based sinusoidal modulation with a superimposed third harmonic is employed for the PWM rectifier system (cf. **Fig. 1**). The amplitude of the superimposed third harmonic voltage is selected as $\frac{m}{6} \cdot \frac{U_{\mathrm{dc}}}{2}$, where m is the modulation index given by $m = 2 \cdot \hat{u}_{\mathrm{ll,nom}}/(\sqrt{3} \cdot U_{\mathrm{dc}}) = 2 \cdot \sqrt{2} \cdot U_{\mathrm{ll,nom}}/(\sqrt{3} \cdot U_{\mathrm{dc}})$. This modulation scheme is similar to a SVM and it leads to a low-frequency CM voltage $u_{\mathrm{I,cm,lf}}$ which drives a low-frequency CM current $i_{\mathrm{cm,lf}}$.

Another issue to be considered is that, if the DM capacitance $C_{\mathrm{dm,1}}$ is increased, the capacitive reactive current amplitude is increased as well, resulting in higher ohmic losses of the filter, conduction and switching losses in the power semiconductors. Thus, the maximum reactive peak current $\hat{i}_{\mathrm{C,dm,1,lf,max}}$ is limited to 2.5% of the nominal peak current $\hat{i}_{\mathrm{nom}}$ (cf. **Table II**) and, therefore, it can be assumed that the ohmic losses due to the capacitive reactive current are negligible compared to the ohmic losses generated by the current at the mains fundamental frequency f_{mains}. In the same way, also the peak value of the low-frequency CM current $\hat{i}_{\mathrm{cm,1,lf,max}}$ is limited to 2.5% of the nominal peak current $\hat{i}_{\mathrm{nom}}$ (cf. **Table II**).

Typically, damping elements, e.g. a parallel R_{d}–C_{d} damping branch (cf. **Fig. 2**), are added to the EMI input filter to avoid adverse effects of a possible excitement of the filter's resonances. However, for the analysis presented below, these damping elements are neglected. The electrical side conditions for which the minimal volume of the 1$^{\mathrm{st}}$ DM/CM LC filter stage is computed are summarized in **Table II**.

IV. Volume Minimization Approach

As explained in the previous section, five electrical side conditions are to be considered when designing the 1$^{\mathrm{st}}$ filter stage (cf. **Table II**). However, only four elements $L_{\mathrm{dm,1}}$, $L_{\mathrm{cm,1}}$, $C_{\mathrm{dm,1}}$, $C_{\mathrm{cm,1}}$ need to be laid out. Accordingly, the problem is overdetermined. Thus, one side condition can be relaxed to get a unique solution (assuming a good conditioning of the problem); two side conditions can be relaxed resulting in a degree of freedom which can be employed to find the design with the smallest filter volume for example; and so forth.

For a given DM inductance and specified maximum peak-to-peak bridge-leg output current ripple which should exactly be achieved, the CM inductance is uniquely determined. Hence, limiting the max. peak-to-peak DM voltage ripple and the max. capacitive reactive peak current results in two conditions to design just one component, i.e. $C_{\mathrm{dm,1}}$. Analogously, there are two conditions, the max. peak-to-peak CM voltage ripple and the max. low-frequency CM peak current, to obtain $C_{\mathrm{cm,1}}$. Thus, to minimize the filter volume, the two side conditions regarding the max. capacitive reactive peak current and the max. low-frequency CM peak current are relaxed and set as an upper limit. Filter designs which exceed $\hat{i}_{\mathrm{C,dm,1,lf,max}}$ and/or $\hat{i}_{\mathrm{cm,1,lf,max}}$ are excluded from the optimization.

The algorithm to find the filter design which results in the smallest volume $V_{\mathrm{1,tot,min}}$ of the 1$^{\mathrm{st}}$ filter stage is as follows:

1) Assumption of a certain total DM inductance $L_{\mathrm{dm,1,tot},i}$.
2) Computation of $L_{\mathrm{cm,1,tot},i}$ in order that the max. peak-to-peak phase current ripple $\Delta i_{\mathrm{a,pp,max}}$ is met (cf. **Table II**).
3) Calculation of the DM capacitance $C_{\mathrm{dm,1},i,\mathrm{ref}}$ first and then of the CM capacitance $C_{\mathrm{cm,1},i,\mathrm{ref}}$ to not exceed the max. peak-to-peak voltage ripples given in **Table II**. Because of the capacitors' availability of discrete capacitance values, $C_{\mathrm{dm,1},i}$ and $C_{\mathrm{cm,1},i}$ are selected to fit $C_{\mathrm{dm,1},i,\mathrm{ref}}$ and $C_{\mathrm{cm,1},i,\mathrm{ref}}$ within a margin of $\pm 10\%$.
4) Computation of the required CM inductance value $L_{\mathrm{cm,1},i,\mathrm{ref}} = L_{\mathrm{cm,1,tot},i} - L_{\mathrm{dm,1,tot},i}/3$ and design of the CM choke (based on available cores) to obtain an inductance value $L_{\mathrm{cm,1},i}$ at the switching frequency which matches $L_{\mathrm{cm,1},i,\mathrm{ref}}$ with a deviation of $\pm 10\%$ (cf. **Section V**).
5) Calculation of the required DM inductance $L_{\mathrm{dm,1},i,\mathrm{ref}} = L_{\mathrm{dm,1,tot},i} - L_{\sigma,1,i}$ where $L_{\sigma,1,i}$ is the leakage inductance of the CM choke. $L_{\mathrm{dm,1},i}$ at the switching frequency presents an accuracy of $\pm 10\%$ with respect to $L_{\mathrm{dm,1},i,\mathrm{ref}}$, since available cores are employed for the DM inductor (cf. **Section V**).
6) Iteration over all $L_{\mathrm{dm,1,tot},i}$ in one microhenry steps, which allow to fulfill the electrical side conditions given in **Table II**.

To realize $C_{\mathrm{dm,1}}$ and $C_{\mathrm{cm,1}}$, MKP X2 (305 V$_{\mathrm{AC}}$)[1] capacitors from TDK EPCOS are employed. Among all different combinations of paralleling capacitors of the same type to achieve the desired value $C_{\mathrm{dm,1},i,\mathrm{ref}}$ and $C_{\mathrm{cm,1},i,\mathrm{ref}}$, the one leading to the smallest volume is selected. The modeling of the DM and CM inductors are explained in more detail in the next section.

V. CM and DM Inductor Modeling

A. CM Inductor Modeling

For the design of the CM choke [cf. **Fig. 6(a)**], the available toroidal cores with plastic casing from Vacuumschmelze GmbH (VAC) are considered [6]. A plastic casing is preferred

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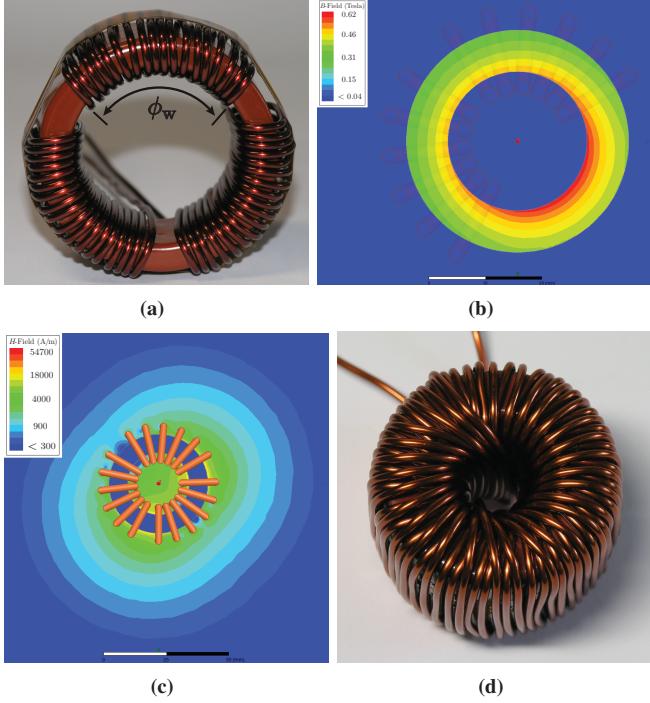[1]Capacitance tolerance: M = $\pm 20\%$, K = $\pm 10\%$.

(a)   **(b)**

(c)   **(d)**

Figure 6. Representative 3-phase CM choke **(a)**; flux density distribution in **(b)** and magnetic field distribution around **(c)** the CM choke's core as given in **Table III** for $i_a = 30.0\,\text{A} + 135\,\text{mA}$ and $i_b = i_c = -15.0\,\text{A} + 135\,\text{mA}$; and DM inductor realized with a toroidal core **(d)**.
Remark: The maximum contribution of the low-frequency DM currents to the maximum total flux density of $B_{\text{choke,1,max}} = 0.62\,\text{T}$ in the core of the CM choke is 58 mT and thus 9.4% of $B_{\text{choke,1,max}}$.

since, compared to an epoxy coating, no additional isolation between core and windings is required. The core material can either be VITROPERM 250F or 500F[2] and they are selected for their high relative permeability ($5'000 \leq \mu_r \leq 100'000$), high saturation flux density ($B_{\text{sat}} \approx 1.2\,\text{T}$) and their reasonable losses [6]. Nanocrystalline cores made of NANOPERM from Magnetec GmbH would be an alternative, which is, however, not further considered, since the core material specifications are very similar to the ones of VITROPERM.

Generally, a valid CM inductor design needs to fulfill three conditions: first, it should provide the required inductance value $L_{\text{cm,1},i,\text{ref}}$; second, the core should not saturate; and third, the inductor should not overheat. A CM choke design with Core_i from the list of the selected cores is valid if the three points are fulfilled. For the design of the CM choke with Core_i up to three stacked cores are considered. For a higher number of stacked cores the realization of the CM choke becomes more difficult, thus the limit is set to three.

The required CM inductance $L_{\text{cm,1}}$ is computed at the switching frequency and, thus, the frequency dependency of the core material's relative permeability is taken into account. From

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[2]A_L-value tolerance: +45% / -25%.

the VAC data sheet [6], the A_L-values are given at 10 kHz and 100 kHz. To obtain the value at the switching frequency a linear interpolation (in a $\log_{10}$-$\log_{10}$ representation) between the given A_L-values is made. The dependency of the relative permeability from the DC magnetic field strength is, according to the data sheet, small and thus neglected.

The CM inductance $L_{\text{cm,1}}$ of a symmetrical 3-phase CM choke is given by [7]

$$L_{\text{cm,1}} = L_{\text{choke,1}} \cdot \frac{1 + 2 \cdot k_{\text{cm,1}}}{3}, \qquad (9)$$

where $k_{\text{cm,1}}$ denotes the coupling factor given by

$$k_{\text{cm,1}} = \frac{L_{\text{choke,1}} - L_{\sigma,1}}{L_{\text{choke,1}}}; \qquad (10)$$

$L_{\text{choke,1}}$ is the self-inductance of one phase wound on the CM choke's core and $L_{\sigma,1} = L_{\text{choke,1}} - M_{\text{choke,1}}$ is the leakage inductance of the CM inductor for one phase[3]. $M_{\text{choke,1}}$ is the mutual inductance between the windings on the CM choke core.

Reference [7] derives an equation for $L_{\sigma,1}$ for a 3-phase CM choke based on the work carried out in [8] for a single-phase CM choke. However, 3D <u>F</u>inite <u>E</u>lement <u>M</u>ethod (FEM) simulations and measurements showed that the accuracy of the mentioned equation is not satisfactory for the considered CM choke cores. Thus, the leakage inductance is computed with the help of Ansys Maxwell 3D simulations.

In order to achieve a high first self-resonance frequency of the CM choke, only single-layer windings are considered. It is assumed that each winding spreads out equally over an angle of $\phi_w = 110°$ [cf. **Fig. 6(a)**] in order to improve the heat evacuation and to allow more flexibility in the selection of the wire diameters for the CM choke designs. However, a smaller angle ϕ_w is increasing the leakage inductance which is effective for the DM currents and which would help to reduce the DM inductance value $L_{\text{dm,1}}$. For the CM choke as given in **Table III**, the leakage inductance would increase from 2.6 µH for $\phi_w = 110°$ to 3.1 µH for $\phi_w = 90°$. The associated DM inductance is 163 µH and, thus, the benefit of the increased leakage inductance is only marginally. In contrast, the commercially available CM choke from VAC have a maximum angle of $\phi_{w,\text{max}} \approx 90°$–$95°$. However, due to the two mentioned reasons, $\phi_w = 110°$ is selected. It is however noted that, depending on the core geometry, an additional mechanical construction possibly be needed to comply with the minimum clearance and creepage distances given in international standards (e.g. EN 60950-1).

The flux density in the core part covered by the windings [e.g. the winding of phase a – cf. **Fig. 6(a)** and **Fig. 6(b)**] can be

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[3]In this paper, the term "leakage inductance" is employed for $L_{\sigma,1}$ to be consistent with the nomenclature in literature. However, "effective DM inductance of the CM choke" would be in the authors' opinion a more convenient naming.

assessed by

$$B_{\text{choke},1}(t) = \frac{1}{N \cdot A_{\text{e}}} \cdot [L_{\text{cm},1,\text{lf}} \cdot 3 \cdot i_{\text{cm},\text{lf}}(t) + 3 \cdot \text{VS}_{\text{cm},1}(t) + L_{\sigma,1} \cdot (i_{\text{a,dm,lf}}(t) + i_{\text{a,dm,hf}}(t))].$$

$$(11)$$

In the equation above, N is the number of turns of one phase, A_{e} denotes the magnetic effective core cross-section, $\text{VS}_{\text{cm},1}(t)$ are the high-frequency CM volt-seconds over one switching period and $L_{\text{cm},1,\text{lf}}$ is the low-frequency CM inductance which differs from $L_{\text{cm},1,i}$ (designed at the switching frequency). A factor three is considered in front of $i_{\text{cm,lf}}(t)$ and $\text{VS}_{\text{cm},1}(t)$ since the quantities are defined for one phase only.

The peak of the low- as well as high-frequency DM and CM currents and current ripples do not occur at the same instant and therefore the maximum of the flux density has to be assessed by considering the time behavior of the different parts. To avoid saturation of the core the maximum flux density $B_{\text{choke},1,\text{max}} = \max_{T_{\text{mains}}}[B_{\text{choke},1}(t)]$ should be below $0.7 \cdot 1.2\ \text{T} = 0.84\ \text{T}$ (where $1.2\ \text{T}$ is B_{sat} of the material and with 0.7 a margin of 30% is included).

To compute the core losses P_{cl}, the flux waveform is separated into a major loop (containing the frequency components at f_{mains} and $3 \cdot f_{\text{mains}}$) and a minor loop (at f_{s}) [9]. For both loops the improved Generalized Steinmetz Equation (iGSE) [10] is employed to compute the loop's associated core losses. To obtain the total core losses, the contributions of both loops are added; this is possible because f_{s} is by orders of magnitude higher than f_{mains}. The Steinmetz parameters, resulting in typical losses, obtained from VAC are employed and, according to the recommendation of VAC, the same Steinmetz parameters are used for the 250F and the 500F core material.

The winding losses P_{wl} are computed as presented in [9]. Round Enameled Wire (EW) or Litz Wire (LW) are two common options to realize the windings. On the one hand, the high-frequency losses are more pronounced for EW than for LW. 2D FEM simulations (with Femm 4.2 [11]) showed that, for the given specifications and EWs, the high-frequency losses (predominantly proximity effect related losses) can be as high as 20%-25% of the total winding losses (especially for small core and large wire diameters). On the other hand, litz wires, e.g. from Pack Feindrähte, can have a fill factor down to 50% which would, for the same outer diameter of the LW and the EW, increase the low-frequency copper losses by a factor of 2. Because the low-frequency copper losses are, for the considered specifications, typically higher than the high-frequency copper losses, it is preferred to employ round enameled wire to realize the windings of the CM choke.

The total losses P_{tl} of the CM choke are the sum of the core losses P_{cl} and the winding losses P_{wl}. For the purpose of simplification and because the windings enclose the toroidal core, it is assumed that the total losses are equally distributed in the choke leading to a uniform temperature distribution.

Therefore, the temperature in the windings and the core as well as the temperature on the windings' and the core's surfaces are equal and denoted by T_{choke}. Furthermore, it is assumed that the cooling is achieved by thermal natural convection. Thus, the heat flow P_i through a surface S_i of the CM choke can be determined by

$$P_i = h_{\text{S},i} \cdot A_{\text{S},i} \cdot (T_{\text{choke}} - T_{\text{ambient}}), \qquad (12)$$

where $h_{\text{S},i}$ is the heat transfer coefficient of the considered surface S_i and $A_{\text{S},i}$ is its surface area. For more details, it is referred to [12], [13]. For the top and bottom side as well as for the inside of the choke, a smooth surface is assumed. Because of the distance between two turns on the outside surface of the choke [cf. **Fig. 6(a)** and **Fig. 6(c)**], the bumpiness of this surface is considered in the thermal modeling.

In Eq. (12), T_{ambient} is the ambient temperature which is assumed to be $T_{\text{ambient}} = 40°\text{C}$ and T_{choke} is the choke's temperature. On the one hand, CM inductor designs which exceed $T_{\text{choke}} = 100°\text{C}$ are discarded. On the other hand, if T_{choke} is below $100°\text{C}$, to reduce the volume, the diameter of the enameled wire is reduced until approximately $T_{\text{choke}} \approx 100°\text{C}$ is reached.

B. DM Inductor Modeling

As it can be seen from point 5) of the algorithm presented in **Section IV**, the DM inductance $L_{\text{dm},1,i,\text{ref}}$ depends on the leakage inductance of the CM inductor. Thus, to find the global minimum of the boxed filter volume, a DM inductor is designed for each valid CM choke design with Core$_i$.

As can be seen from Eq. (6), for a constant $L_{\text{dm},1,\text{tot}}$, a higher leakage inductance $L_{\sigma,1}$ allows to reduce $L_{\text{dm},1}$ and thus the volume of the DM inductor. However, in case the CM choke core saturates, not only the CM inductance, but also the DM inductance provided by $L_{\sigma,1}$ drop to a few microhenries (or even lower values). Therefore, to limit the DM and CM current ripples under such circumstances, it is recommended to provide a minimum DM inductance, e.g. $L_{\text{dm},1,\text{min}} = 90\ \mu\text{H}$ in the case at hand, by the DM inductor. This consideration is reasonable for practical applications, where usually a certain robustness in addition to the electrical performance is required. Typically, the assessment of the maximum low-frequency DM peak current can be conducted with high accuracy (in normal operation), meanwhile the computation of the maximum low-frequency CM peak current is often related to much higher uncertainties. Hence, it is preferred to set a lower limit of the DM inductance.

Powder core materials are selected to realize the DM inductor [cf. **Fig. 6(d)**]. Iron powder toroidal cores and E-cores from Micrometals and powder E-cores from Magnetics®, listed in [14] and [15], are considered in the optimization. Toroidal cores and E-cores from Micrometals are considered to have a comparison between the inductor designs. However, since toroids are more difficult to wind than E-cores, only Magnetics® E-cores are additionally taken into account. Two manufacturer are considered because of the difference in the

magnetic performance between the cores from Micrometals and Magnetics®.

The Micrometals materials -2, -8, -14, -18, -19, -26, -30, -34, -35, -40, -45, -52 [14] and the material Kool Mµ from Magnetics® [15][4] are employed. Ferrite cores would have been an adequate choice as well, which is however in a first step not further investigated in this paper. A nanocrystalline material is not considered because the fringing field at the air-gap (which is necessary) would lead to high eddy-current losses in the lamination of the core [16].

The maximum allowed flux density in the DM inductor is set to $B_{\text{inductor,1,max}} = 1$ T, the impact of the DC magnetizing force on the relative permeability is accounted with the material type specific equations given in [14], [15]. In order to obtain a better magnetic material utilization, the DM inductor is designed such that $L_{\text{dm,1},i,\text{ref}}$ is obtained at zero current (zero DC magnetizing force). At the maximum mains current (rms) a minimum inductance of 40% of $L_{\text{dm,1},i,\text{ref}}$ is required.[5] Designs leading to a lower inductance value are not considered. For a three-phase system not all three phases carry simultaneously the same current and therefore the inductance reduction is not as severe in all phases at the same time. However, the nonlinear inductance results in a DM to CM noise conversion and vice versa. The impact will be studied in a next step.

Moreover, on the one hand, for the computation of the maximum flux density $B_{\text{inductor,1,max}}$ and the core losses of the DM inductor, the dependency of the DM inductance value on the DC magnetizing force is considered. On the other hand, as it will be shown in **Section VI**, a small boxed filter volume is obtained for $L_{\text{cm,1}}$ being at least three times higher than $L_{\text{dm,1}}$ and thus it can be roughly assumed that the CM current is almost negligible. Accordingly, the peak-to-peak bridge-leg output current ripple is predominantly composed of the DM part. Additionally, computations of the peak-to-peak bridge-leg output current ripple over the mains period for the given modulation scheme and modulation index range showed that the maximum of this current ripple occurs at the maximum of the low-frequency mains current ($\cos(\phi) = 1$) and, thus, at the instant when the DM inductance is the lowest. Hence, if the DM inductance drops by 60%, the maximum peak-to-peak bridge-leg output current ripple $\Delta i_{\text{a,pp,max}}$ increases by a factor of $1/(1-0.6) = 2.5$. However, for the optimal filter design as given in **Table III**, the inductance at the maximum current is though 64% of $L_{\text{dm,1}}$ which leads to a maximum peak-to-peak phase current ripple of 7.3 A (which is an increase of 42%). Furthermore, GeckoCIRCUITS [17] simulations revealed that the maximum total noise emissions of the converter system increased by approximately 4 dBµV due to the reduction of the DM inductance with the fundamental mains current.
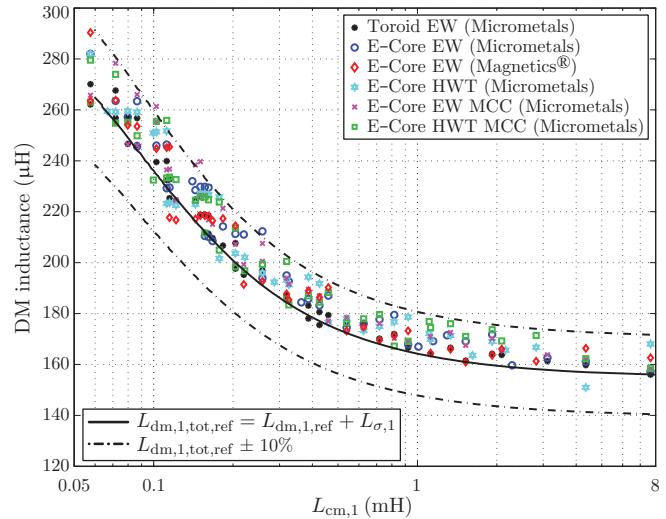
Figure 7. Total achieved DM inductance $L_{\text{dm,1,tot}} = L_{\text{dm,1}} + L_{\sigma,1}$ for different DM inductor cores and DM inductor cooling methods plotted over the achieved CM inductance $L_{\text{cm,1}}$ of the first filter stage (cf. **Fig. 1**) for $\Delta i_{\text{a,pp,max}} \simeq 5.1$ A. $L_{\text{dm,1}}$ is realized by the DM inductor, $L_{\sigma,1}$ by the leakage of the CM choke and $L_{\text{cm,1}}$ is the CM inductance of the CM choke. The solid black line shows the reference design value for the total DM inductance and the dashed black lines represent the design limits set to ±10% inductance variation. If not otherwise indicated, the DM inductor is cooled by natural convection (the CM choke is always cooled by natural convection).
Legend: EW = Enameled Wire; HWT = Helical Winding Technology [20]; MCC = Mixed-mode Convection Cooling (see text).

Moreover, the Steinmetz parameters are extracted from the core loss equations as given in [14], [15] and to compute the winding losses the proximity effect is accounted as proposed in [9], [18]. The minimum inductance (at the max. low-frequency current) is used to computed the current harmonics. Compared to the thermal model of the CM choke, the one for the toroidal cores assumes also a smooth surface on the outside of the core. In contrast to toroidal cores, E-cores require a certain isolation to the core (realized with a bobbin, e.g. polyamide - 6/6 Nylon for Micrometals and Rynite® FR530 for Magnetics®) and thus a distinction between the core and winding temperatures, T_{c} and T_{w}, is made based on the equivalent thermal model presented in [19]. It is assumed that the core has a uniform temperature distribution denoted by T_{c} and that the winding has a uniform temperature distribution denoted by T_{w}. Accordingly, the maximum of T_{c} and T_{w} should be below 100°C. Otherwise, the modeling of the DM inductor is done in the same way as for the CM choke.

VI. OPTIMIZATION RESULTS

The results of the optimization are summarized in **Fig. 7** and **Fig. 8**. In the first figure, the total DM inductance $L_{\text{dm,1,tot}} = L_{\text{dm,1}} + L_{\sigma,1}$ achieved for the different designs is plotted over the achieved CM inductance $L_{\text{cm,1}}$ in order to obtain $\Delta i_{\text{a,pp,max}} \simeq 5.1$ A (cf. **Table II** - zero DC magnetizing force for the DM inductors). The black solid line denotes the reference design value for the total DM inductance and the

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[4]Micrometals: A_{L}-value tolerance: ±10% (except for -2: ±5%). Magnetics®: A_{L}-value tolerance: ±8%.

[5]It is noted that for the computation of the phase current harmonics for the design of the CM choke the minimal DM inductance is used, i.e. 40% of $L_{\text{dm,1},i,\text{ref}}$.

dashed black lines represent the design limits set to $\pm 10\%$ inductance variation.

As a comparison to the optimization results obtained with toroidal (black asterisk) and E-cores (Micrometals: blue circles; Magnetics®: red diamond) for the DM inductor, three other results are plotted in **Fig. 7**: First, Schott Corporation describes a <u>H</u>elical <u>W</u>ound <u>T</u>echnology (HWT) in [20]. In this case, a flat copper band is wound around the middle leg of the E-core, where the short side of the band faces the middle leg. The main advantage of such a winding structure is, compared to a winding with a enameled wire, the increased winding filling factor [20], resulting in lower low-frequency copper losses. The isolation between the copper layers is in this case 0.1 mm (cyan star). Second, a combination of natural and forced convection with an average air flow speed of 2 m/s is assumed to additionally cool the E-core from Micrometals (magenta cross). This kind of cooling method, the combination of natural and forced convection cooling, is denominated <u>M</u>ixed-mode <u>C</u>onvection <u>C</u>ooling (MCC) in the following. And third, the HWT (E-core - Micrometals) is combined with a MCC as described for the second point (green square).

The total boxed filter volume of the first DM/CM LC filter stage is given in **Fig. 8** as a function of k_L, the ratio between CM and DM inductance, for the six different designs of the boost inductor $L_{dm,1}$. It can be seen from the figure that for $k_L \geq 3$ the curves are almost horizontal lines and therefore the optimum is flat. Hence, to achieve a compact filter design of the first filter stage, it is beneficial to make the CM inductance at least a factor three bigger than the DM inductance. E.g. the minimal boxed volume for a DM inductor with an E-core from Magnetics® (Kool Mµ core material), which is cooled by natural convection, is 0.43 ltr. and obtained for $k_{L,opt} \approx 14$. These optimal CM and DM inductor designs are summarized in **Table III**.

Furthermore, it can be seen from **Fig. 8** that the toroid and E-core inductor designs lead to a similar boxed volume. Moreover, the total filter volume can be reduced by circa 40% if the boost inductor (employing E-cores from Micrometals) is in addition to the natural convection actively cooled by an air flow of 2 m/s (MCC). Additionally, there is no major difference between inductors designed with round enameled wires than with HWT. Furthermore, it is shown in **Fig. 8** that by employing Kool Mµ as the DM inductor core material, a reduction of nearly 40% in the total boxed volume of the first filter stage compared to a Micrometals E-core design can be achieved. Summarizing, according to the results of the optimization, the cores made of Kool Mµ are the most suitable for the given application, due to the lower core losses. Therefore, the focus is in the following on the E-core designs with Kool Mµ and natural convection cooling.

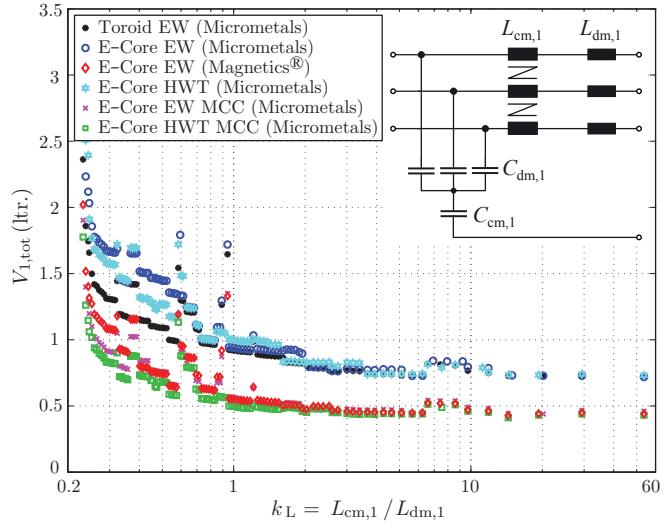The CM choke for the design of the first filter stage, summarized in **Table III**, is not only optimal in the sense

Figure 8. Total boxed volume $V_{1,tot} = 3 \cdot V_{L,dm,1} + V_{L,cm,1} + 3 \cdot V_{C,dm,1} + V_{C,cm,1}$ of the first DM/CM LC filter stage (cf. **Fig. 1**) over the ratio k_L of CM inductance $L_{cm,1}$ to DM inductance $L_{dm,1}$ for different DM inductor designs and cooling methods. The curves are almost horizontal lines for $k_L \geq 3$ and, thus, the optimum is flat. The minimal volume for a boost inductor with an E-core from Magnetics®, cooled by natural convection, is 0.43 ltr. and is obtained for $k_{L,opt} \approx 14$ (cf. **Table III**). If not otherwise indicated, the DM inductor is cooled by natural convection (the CM choke is always cooled by natural convection). *Legend: See **Fig. 7**.*

of volume reduction, but also in terms of the CM choke's leakage inductance. It has the smallest leakage inductance of all optimization results with $k_L \geq 3$. This is advantageous because the magnetic stray field closes over the air and hence there are two additional points to consider as explained in the following:

1) the impact of the CM choke's magnetic stray field on the surrounding environment; and
2) the impact of the case around the filter on the magnetic stray field of the CM choke for a compact design (especially at frequencies equal or high than f_s). Because of the shielding effect of the case at the mentioned frequencies, the CM choke's stray field is reduced which leads to a smaller leakage inductance. A smaller leakage inductance results also in a smaller total DM inductance $L_{dm,1,tot}$ and accordingly in a higher peak-to-peak bridge-leg output current ripple.

Depending on the application, the magnetic stray field of the CM choke outside the case of the filter may not exceed the values specified by the <u>I</u>nternational <u>C</u>ommission for <u>N</u>on-<u>I</u>onizing <u>R</u>adiation <u>P</u>rotection (ICNIRP). For occupational exposure[6] the limit is set to 1 mT$_{rms}$ for the mains frequency of 50 Hz [21]. To give an example about the value of the stray field for the CM choke as summarized in **Table III**, the maximum flux density at the mains frequency in 13 mm distance from the choke (outer diameter of the choke is 49.2 mm) is assessed by a 2D FEM simulation (with Femm

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[6]All exposure to electric and magnetic fields experienced by individuals as a result of performing their regular or assigned job activities [21].

TABLE III. With the optimization algorithm designed first DM/CM LC stage of the EMI input filter (cf. **Fig. 1**) as well as CM choke and DM inductor data to obtain the smallest total filter volume $V_{1,\text{TOT,MIN}}$ of this stage (cf. **Fig. 8**). To realize the DM inductor an E-core from Magnetics® is selected and only natural convection is assumed for the cooling of the components. The design considerations are as given in the text.

Circuit Parameters	
$L_{\text{dm,1,tot}}$ ($L_{\text{dm,1,tot,ref}}$)	166 µH (159 µH)
$L_{\text{dm,1}}$	163 µH
$L_{\text{cm,1}}$	2.1 mH
$C_{\text{dm,1}}$ (B32922C3684M***, EPCOS)	3×680 nF = 2.04 µF
$C_{\text{cm,1}}$ (B32922C3224+***, EPCOS)	220 nF
CM Choke – T60006-L2040-W453	
(Toroid, VITROPERM 500F – VAC)	
Number of turns / stacked cores	$N = 6$ / $n = 3$
Enameled wire (Pack Feindrähte)	$\varnothing_{\text{cu}}$ 2.9 mm
Leakage inductance	$L_{\sigma,1} = 2.6$ µH
Max. peak flux density	$B_{\text{choke,1,max}} = 0.65$ T
Core losses	$P_{\text{cl}} = 5.8$ W
Winding losses	$P_{\text{wl}} = 3.8$ W
Max. choke temperature	$T_{\text{choke,max}} = 99.7°C$
DM Inductor – 00K4017E090	
(E-core, Kool Mµ 90 µ – Magnetics®)	
Number of turns / stacked cores	$N = 19$ / $n = 3$
Enameled wire (Pack Feindrähte)	$\varnothing_{\text{cu}}$ 2.5 mm
Max. peak flux density	$B_{\text{inductor,1,max}} = 0.32$ T
Core losses	$P_{\text{cl}} = 3.0$ W
Winding losses	$P_{\text{wl}} = 3.4$ W
Max. coil temperature	$T_{\text{coil,max}} = 99.4°C$
Boxed Volumina	
$V_{\text{L,dm,1}}$	81 cm³
$V_{\text{L,cm,1}}$	150 cm³
$V_{\text{C,dm,1}}$	11.0 cm³
$V_{\text{C,cm,1}}$	1.6 cm³

4.2 [11]) to 0.99 mT$_\text{rms}$. At such low frequencies, the case of the filter has almost no shielding impact.

At the switching frequency of 50 kHz, due to the lower amplitudes of the current harmonics compared to the fundamental current and due to shielding effect of the case, the ICNIRP limits can be fulfilled. However, the magnetic stray field of the CM choke possibly couple to other filter components possibly leading to a reduction of the EMI filter attenuation. For a CM choke the dominant coupling mechanism is between the leakage inductance and the equivalent series inductance (ESL) of the DM capacitors of the first filter stage [22]. For the capacitor type mentioned in **Table III**, the measured ESL is roughly 8.3 nH (self-resonance at 2.2 MHz). Because three capacitors are connected in parallel, the effective ESL is $L_{\text{ESL}} = 8.3$ nH/3 = 2.8 nH.

To assess the impact of the coupling between $L_{\sigma,1}$ and L_{ESL} on the DM attenuation, a worst case mutual coupling of $M_{\text{ESL,w}} = \pm\sqrt{L_{\sigma,1} \cdot L_{\text{ESL}}}$ (assuming a worst case coupling factor of $k_{\text{ESL}} = 1$) is considered. Computations of the achieved attenuation from the converter DM noise source to the LISN (cf. **Fig. 2**) showed that just the introduction of the ESL without being coupled with $L_{\sigma,1}$, i.e. $k_{\text{ESL}} = 0$

and $M_{\text{ESL}} = 0$, has no impact on the attenuation achieved at 150 kHz, at the first harmonic in the range [150 kHz, 30 MHz] which is considered to comply with CISPR 11. However, a negative coupling $M_{\text{ESL}} = -\sqrt{L_{\sigma,1} \cdot L_{\text{ESL}}}$ leads to a maximum reduction in the attenuation of slightly less than 1.2 dB, which is within the typically considered attenuation margin of 9 dB–12 dB in the EMI filter designs.

Additionally, for a compact filter design, the CM choke is closely surrounded by the case and, thus, the shielding effect of the magnetic stray fields at the switching and higher frequencies can be considerably pronounced. This leaves a reduced space for the stray field to close over the air and thus the stray factor is reduced leading to a lower leakage inductance. To give an example, the CM choke of **Table III** would be surrounded by a stainless steel case with a thickness of 1.5 mm. The distance from the CM choke to the case would be uniformly 5 mm. Performing a 3D Maxwell Eddy-Current simulation revealed that the leakage inductance is reduced at $f_{\text{s}} = 50$ kHz from 2.6 µH to 1.5 µH and that the associated ohmic losses in the steel case are approximately 0.3 W. This is a reduction of the leakage inductance by 42% (!) and means that at the switching frequency only 58% of the leakage inductance computed in **Table III** would contribute to the filtering of the converter DM output voltage.

It is noted that for the case at hand, the total DM inductance at the switching frequency would drop from $L_{\text{dm,1,tot}} = 166$ µH to 165 µH which is a reduction of 0.6%. This percentage reduction is far lower than the material's tolerance of the A_{L} specified by Magnetics® ($\pm 8\%$).[7]

In conclusion, to keep the described adverse issues associated to the magnetic stray field of the CM choke at the strict minimum, a small leakage inductance in addition to a small volume is preferred. Both is achieved with the design summarized in **Table III**.

VII. Conclusion

In conventional EMI input filters of three-phase voltage source AC–DC converters with sinusoidal input current, the CM capacitance of the Y-capacitors is strongly limited (to a few tens of nanofarads) by the maximum allowed protective conductor current of 3.5 mA$_\text{rms}$ (e.g. IEC 60335-1, IEC 60950-1). To overcome this restriction, it is preferred to achieve the filtering with an internal CM filter capacitor, i.e. a capacitor $C_{\text{cm,1}}$ that is connected between the star-point of the DM capacitors and the midpoint of the DC-link capacitors. A CM LC filter stage is then realized in combination with a CM inductance $L_{\text{cm,1}}$ connected in series with the boost inductors. For $C_{\text{cm,1}}$, higher capacitance values can be employed and, therefore, the achieved CM attenuation, especially at the switching frequency, can be increased. However, it should

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[7]Especial care has to be addressed to the design of the CM choke, if a larger part ($> 20\%$–30%) of the total DM filter inductance is realized with the leakage of the CM choke.

be kept in mind that this benefit of the proposed filter stage depends strongly on the parasitic capacitance of the power semiconductors to ground and, thus, it has to be investigated for each case separately.

The electrical side conditions to treat the first DM/CM LC filter stage of the EMI input filter, which includes a CM choke and the boost inductor of the converter, separately from the rest of the circuit are discussed in detail in the paper. These side conditions allow to find the ratio $k_{\mathrm{L,opt}} = L_{\mathrm{cm,1}}/L_{\mathrm{dm,1}}$ of CM inductance to DM inductance which minimizes the volume $V_{\mathrm{1,tot}}$ of the first filter stage. Moreover, a detailed modeling of the CM choke as well as DM inductor is presented and optimization results for different DM inductor designs as well as cooling methods are evaluated.

It is demonstrated, that to achieve a compact first DM/CM LC stage of the EMI input filter for a $10\,\mathrm{kW}$ PWM rectifier system, the boxed volume is almost constant for $k_{\mathrm{L}} \geq 3$, i.e. it is optimal to select the CM inductance at least a factor three larger than the DM inductance. The optimal ratio between CM inductance and DM inductance is $k_{\mathrm{L,opt}} = 14$, which leads to a minimum boxed filter volume of $V_{\mathrm{1,tot,min}} = 0.43\,\mathrm{ltr}$. for a filter cooled by natural convection.

The impact of the CM choke's stray field on the other filter components and the filter's steel case is addressed and it is shown that a small leakage inductance of the CM choke is desirable for a compact filter realization. Moreover, it is highlighted that the optimization result with the smallest total filter volume has a leakage inductance of $2.6\,\mu\mathrm{H}$, which is much smaller than the associated DM inductance of $163\,\mu\mathrm{H}$ and, thus, the unwanted issues associated to the CM choke's stray field,

- reduction of the total DM filter inductance in case the CM choke core saturates;
- magnetic coupling of the CM choke's stray field to other filter components, which possibly lowers the achieved filter attenuation;
- reduction of the leakage inductance of the CM choke due to the shielding effect of the filter's case,

are minimized.

VIII. ACKNOWLEDGEMENT

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