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Comparative Evaluation of Bidirectional Buck-Type PFC Converter Systems for Interfacing Residential DC Distribution Systems to the Smart Grid

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***Abstract*—This paper discusses three-phase bidirectional high-power factor mains interfaces for application in smart-houses featuring a local DC distribution grid. The DC grid demanded power can be supplied by local DC generators, such as renewable power sources, and/or by the public three-phase AC mains, which gives the option of feeding back power into the mains in case of a low local power consumption. In order to generate a local 400 V DC bus, bidirectionally connected to the European three-phase low voltage AC mains rated at 400 V line-to-line, buck-type converter topologies are required. Several possible converter concepts are initially presented and further comparatively evaluated based on the following performance indices: total required semiconductor chip area, overall efficiency, overall passive components volume, and required EMI filter damping. As result of the comprehensive evaluation, the Bidirectional 3rd Harmonic Injection Active Filter Type Rectifier with DC/DC Output Stage is identified as most advantageous topology for the realization of a bidirectional buck-type PFC rectifier in the considered power range of 5 to 10 kW.**

I. Introduction

The development of smart-houses featuring a local DC distribution grid leads to higher efficiencies and lower costs due to the reduced requirements of power conversion [1]. Many decentralised generators such as the photovoltaic (PV) systems can be connected via a DC/DC converter interface of low complexity to the DC system, i.e. a more complicated DC/AC conversion can be omitted. A possible smart-house model introduced in [2] is presented in Fig. 1. It consists of a photovoltaic system and a heat pump, which feed power into the DC bus via unidirectional DC/DC converters, and a battery acting as a buffer to balance short-term power variations. The latter is able to both supply and store power, thus requiring a bidirectional DC/DC converter. The installation of renewable energy systems causes power fluctuation because their output power is dependent on the weather condition. An alternative to providing a large battery buffer is a bidirectional connection of the local DC grid to the public three-phase AC mains, using a bidirectional AC/DC converter. This converter drains energy from the AC mains when the locally generated power is low, or supplies it into the mains in case of a decreased local load.

An appropriate voltage level for the local DC grid, requiring the least amount of power conversions in order to connect multiple sources (PV systems, Heat Pumps, etc.), as well as loads (like Switch Mode Power Supplies) would be 400 V [3]. Ideally, to minimize stress on the AC mains, the bidirectional AC/DC interface converter should feature a Power Factor Correction (PFC). In the European low voltage mains (with a line-to-line voltage of 400 Vrms, i.e. a voltage amplitude of 565 V), the converter furthermore should be capable of decreasing the input voltage to achieve the desired 400 V, e.g. a buck-type PFC converter topology is required. Boost-type topologies would generate an output voltage level which would be too high to directly feed the DC-bus (typ. 700 V to 900 V). Accordingly, a second step-down DC-DC converter would be required at the output, decreasing the overall system efficiency.

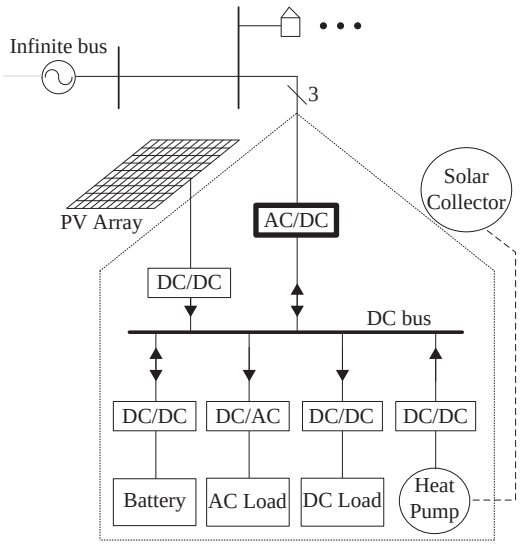

Fig. 1. DC smart-house model; arrows symbolize possible power flows to and from the DC bus.

In order to achieve the desired bidirectional power flow capability, conventional unidirectional AC/DC buck-type rectifier topologies have to be modified. An overview of several options is presented in **Section II**. First, a simple way to convert a conventional unidirectional buck-type topology into a bidirectional system by using an inverting link-circuit is presented. For comparison purposes this concept is applied to the Unidirectional Six-Switch Buck-Type PFC System (cf. Fig. 2(a)). Additionally, a second option is suggested, the Antiparallel Six-Switch Converter Combination (cf. Fig. 2(b)), where the reverse power flow is guaranteed for unipolar output by allowing a current flow back into the mains. Furthermore by bidirectional extension of unidirectional topologies based on the 3rd harmonic injection concept presented in [4], [5], i.e. the bidirectional Swiss Rectifier (cf. Fig. 2(c)), and bidirectional 3rd Harmonic Injection Active Filter Type Rectifier with DC/DC Output Stage (cf. Fig. 2(d)) are introduced. **Section II** also presents simulations and characteristic waveforms, which allow an easy estimation of the semiconductor and passive component losses for a bidirectional 7.5 kW, 3 × 400 V/50 Hz

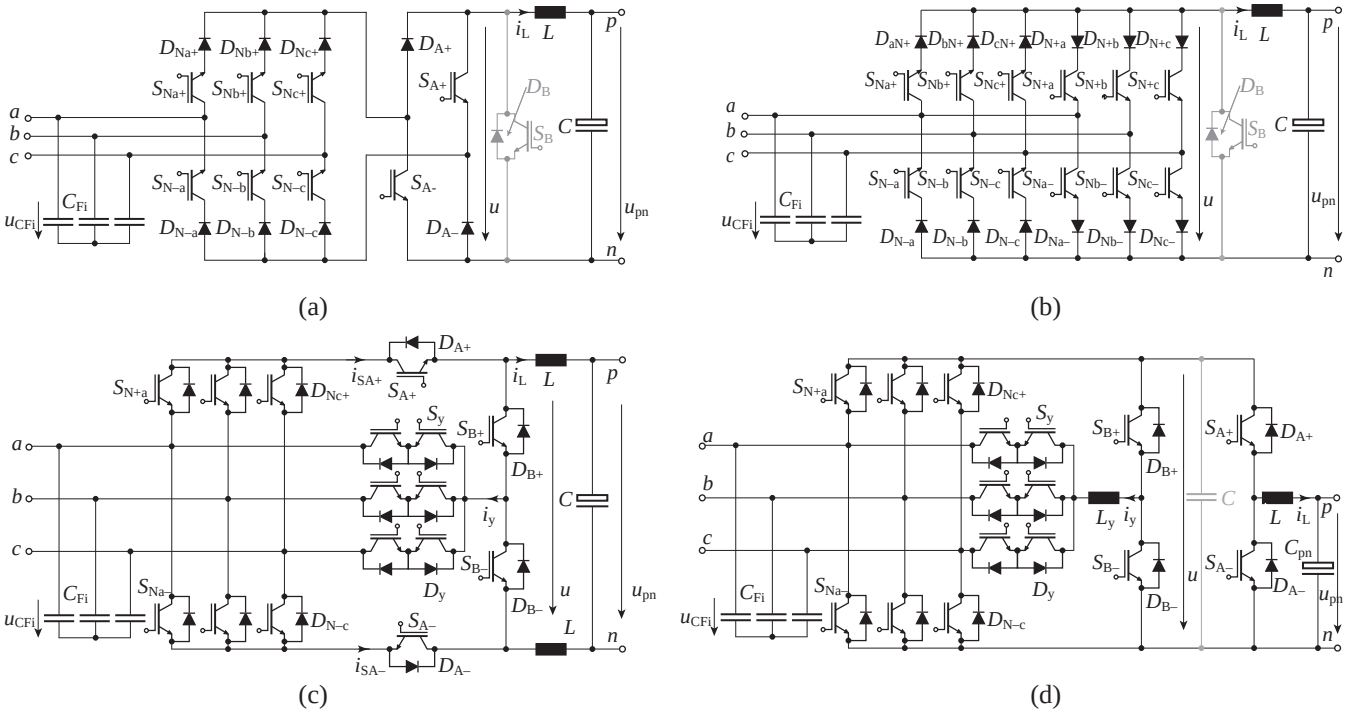

Fig. 2. Overview of all considered topologies: (a) Six-Switch Rectifier with Switchable Output Polarity, (b) Antiparallel Six-Switch Converter Combination, (c) Bidirectional SWISS Rectifier, (d) Bidirectional 3rd Harmonic Injection Active Filter Type Rectifier with DC/DC Output Stage.

TABLE I
OVERALL BIDIRECTIONAL PFC RECTIFIER SPECIFICATIONS AND COMPONENTS USED IN THE EFFICIENCY CALCULATION.

Characteristics	Specifications
Input phase voltage $u_{a,b,c}$	$3 \times 400\,\mathrm{V}$
Mains frequency f_n	$50\,\mathrm{Hz}$
DC Output Voltage U_{pn}	$400\,\mathrm{V}$
Switching frequency f_{sw}	$36\,\mathrm{kHz}$
Rated power P_{dc}	$\pm 7.5\,\mathrm{kW}$
Output capacitor C	$10 \times 47\,\mu\mathrm{F}/450\mathrm{V}$, EPCOS
DC inductor L	$2 \times 305\,\mu\mathrm{H}$, $2 \times$ E64-50-10, 3C91
	$N = 16$ turns, $A_{Cu} = 8.5\mathrm{mm}^2$
Inductor L_y	$2\,\mathrm{mH}$, Metglas AMCC-32, $N = 60$ turns
S_y / D_y	Si T&FS IGBTs, 1200 V/25 A
	IKW25N120
$S_{A+/-}$ / $S_{B+/-}$	Si HighSpeed T&FS IGBTs
	IGW40N120H3
$D_{A+/-}$ / $D_{B+/-}$	SiC Schottky diodes, 1200 V/20 A
	C2D20120A
S_N	Si T&FS IGBTs, 1200 V/25 A
	IKW25N120
D_N	Si fast recovery diode, DSEP060-12AR

system.

In **Section III**, to facilitate the selection of one topology in favor of another, efficiency comparisons, as well as a comprehensive evaluation are performed. This also considers the total required semiconductor chip area in order to ensure a fair comparison of the PFC circuits, as introduced in [6].

Finally in **Section IV**, the most advantageous system concept is identified and topics of further research are discussed.

II. TOPOLOGY PRESENTATION

In the following, four bidirectional buck-type PFC rectifier topologies will be presented, based on the extension of unidirectional topologies, which were shown in [7], starting with the Six-Switch Rectifier with Switchable Output Polarity (cf. Fig. 2(a)). It is based closely on the unidirectional six-switch buck-type PFC topology, but for energy feedback into the mains, the DC-side voltage polarity can be inverted by turning on the switches $S_{A+/-}$. An alternative is the Antiparallel Six-Switch Converter Combination (cf. Fig. 2(b)). Here, the polarity of the output voltage of the input side bridge circuit is kept unchanged, but a power feedback into the mains is allowed with an additional antiparallel six-switch converter stage. Two further bidirectional converter topologies considered are based on unidirectional buck-type 3rd harmonic injection concepts [4], [5], i.e. the bidirectional SWISS Rectifier (cf. Fig. 2(c)), and the bidirectional 3rd Harmonic Injection Active Filter Type Rectifier with DC/DC Output Stage (cf. Fig. 2(d)). The specifications as well as the components used for the loss calculation of the four considered topologies are kept the same, to allow for a better comparison and are compiled in Table I. They were chosen based on existing prototypes of the unidirectional SWISS Rectifier introduced in [8] and of the 3rd harmonic injection active filter type rectifier with DC/DC output stage presented in [9].

A. Six-Switch Rectifier with Switchable Output Polarity

Fig. 2(a) presents a bidirectional rectifier topology, which is based on the front-end circuit of an inverting link-matrix converter [10]. This system combines the standard unidirectional six-switch buck-type PFC rectifier topology with a circuit that reverses the polarity of the input side bridge circuit output voltage for energy feedback into the mains.

In case of a power flow from the AC to the DC side, the switches $S_{A+/-}$ are turned off and the current i_L is positive, flowing through

TABLE II
APPLIED DUTY CYCLE FOR THE SIX-SWITCH RECTIFIER WITH SWITCHABLE OUTPUT POLARITY IN CASE OF A POWER FLOW AC TO DC.

Sector	$\delta_{\text{eff,a}}$	$\delta_{\text{eff,b}}$	$\delta_{\text{eff,c}}$
0°– 30°	δ_a	$1\text{-}\delta_c\text{+}t_d$	δ_c
30°– 60°	δ_a	$1\text{-}\delta_a\text{+}t_d$	δ_c
60°– 90°	$1\text{-}\delta_b\text{+}t_d$	δ_b	δ_c
90°– 120°	$1\text{-}\delta_c\text{+}t_d$	δ_b	δ_c
120°– 150°	δ_a	δ_b	$1\text{-}\delta_a\text{+}t_d$
150°– 180°	δ_a	δ_b	$1\text{-}\delta_b\text{+}t_d$
180°– 210°	δ_a	$1\text{-}\delta_c\text{+}t_d$	δ_c
210°– 240°	δ_a	$1\text{-}\delta_a\text{+}t_d$	δ_c
240°– 270°	$1\text{-}\delta_b\text{+}t_d$	δ_b	δ_c
270°– 300°	$1\text{-}\delta_c\text{+}t_d$	δ_b	δ_c
300°– 330°	δ_a	δ_b	$1\text{-}\delta_a\text{+}t_d$
330°– 360°	δ_a	δ_b	$1\text{-}\delta_b\text{+}t_d$

TABLE III
APPLIED DUTY CYCLE FOR THE SIX-SWITCH RECTIFIER WITH SWITCHABLE OUTPUT POLARITY IN CASE OF A POWER FLOW DC TO AC.

Sector	$\delta_{\text{eff,N+a}}$	$\delta_{\text{eff,Na-}}$	$\delta_{\text{eff,N+b}}$	$\delta_{\text{eff,Nb-}}$	$\delta_{\text{eff,N+c}}$	$\delta_{\text{eff,Nc-}}$
0°– 30°	1	$1\text{-}\delta_a$	0	$1\text{-}\delta_c\text{+}t_d$	0	δ_c
30°– 60°	δ_a	0	$1\text{-}\delta_a\text{+}t_d$	0	$1\text{-}\delta_c$	1
60°– 90°	$1\text{-}\delta_b\text{+}t_d$	0	δ_b	0	$1\text{-}\delta_c$	1
90°– 120°	0	$1\text{-}\delta_c\text{+}t_d$	1	$1\text{-}\delta_a$	0	δ_c
120°– 150°	0	δ_a	1	$1\text{-}\delta_b$	0	$1\text{-}\delta_a\text{+}t_d$
150°– 180°	$1\text{-}\delta_a$	1	δ_b	0	$1\text{-}\delta_b\text{+}t_d$	0
180°– 210°	$1\text{-}\delta_a$	1	$1\text{-}\delta_c\text{+}t_d$	0	δ_c	0
210°– 240°	0	δ_a	0	$1\text{-}\delta_a\text{+}t_d$	1	$1\text{-}\delta_c$
240°– 270°	0	$1\text{-}\delta_b\text{+}t_d$	0	δ_b	1	$1\text{-}\delta_c$
270°– 300°	$1\text{-}\delta_c\text{+}t_d$	0	$1\text{-}\delta_b$	1	δ_c	0
300°– 330°	δ_a	0	$1\text{-}\delta_b$	1	$1\text{-}\delta_a\text{+}t_d$	0
330°– 360°	1	$1\text{-}\delta_a$	0	δ_b	0	$1\text{-}\delta_b\text{+}t_d$

the diodes $D_{\text{A+/-}}$. In this work, the modulation scheme for the unidirectional topology presented in [11], which guarantees minimum switching losses as well as minimum input filter capacitor voltage ripple and minimum DC current ripple, is adapted to the proposed bidirectional system (cf. Fig. 2(a)). As a consequence, the duty ratios for the three bridge legs are set according to

$$\delta_i = \frac{U_{\text{pn,ref}}}{\sum_{j=a,b,c} u_{\text{CF},j}^2} \left| u_{\text{CF},i} \right| , \qquad (1)$$

where $U_{\text{pn,ref}}$ is the rectifier output voltage reference value, $u_{\text{CF},j}$ is the input phase voltage (as defined in Fig. 2) and $i = \{\text{a,b,c}\}$ corresponds to the considered input phase.

In case of a power flow from the AC side to the DC side, the switches $S_{\text{N}k+}$, $S_{\text{N-}k}$, $k = \{\text{a,b,c}\}$, the freewheeling diode D_{B} and the inductor L form a buck converter. Diode D_{B} allows to reduce the freewheeling state conduction losses compared to an alternative shoot-through switching state of the input side bridge circuit. Both IGBTs of each bridge leg are switched at the same time, with duty cycles corresponding to the values shown in Table II. This also guarantees the required freewheeling state of the inductor L, while the overlap-time t_{d} ensures a smooth current transition between the phases.

In case of the reverse power flow, the switches $S_{\text{N-}k}$ and $S_{\text{N}k+}$, $k = \{\text{a,b,c}\}$, the switch S_{B} (used mostly for efficiency considerations, as the switching states corresponding to the turn-on and turn-off of S_{B} can also be guaranteed by proper modulation of the switches $S_{\text{N-}k}$ and $S_{\text{N}k+}$, $k = \{\text{a,b,c}\}$) and the inductor L form a boost converter topology, injecting a sinusoidal current into the AC mains. Unlike the buck converter, where the freewheeling state was guaranteed not only by the switching strategy, but also passively by the diode D_{B}, in boost operation the uninterrupted current flow through the inductor L needs to be actively imposed by a proper gating of the switches. Because of this, the modulation presented in Table III is used, which includes again a certain overlap-time t_{d}.

Fig. 3 presents simulated characteristic waveforms of the Six-Switch Rectifier with Switchable Output Polarity, operated under rated conditions of $\pm 7.5\,\text{kW}$ power on the DC side. The results demonstrate that the line currents $i_{\text{a,b,c}}$ can effectively follow the sinusoidal input phase voltages $v_{\text{a,b,c}}$ for both directions of the power flow. The rms and average current values of the IGBTs obtained from the simulation, which are used later in the calculation of the switching and conduction losses, are compiled in Table IV.

B. Antiparallel Six-Switch Converter Combination

Another three-phase PFC rectifier solution that allows bidirectional power flow and controlled output voltage, while drawing a sinusoidal mains current, is shown in Fig. 2(b). The origin of this topology is associated with the conventional unidirectional 6-switch buck-type rectifier, which was thoroughly studied in [12]. In this converter topology, the bidirectional power flow capability is achieved with six four-quadrant switches, each consisting of 2 switches and 2 diodes $S_{\text{N}k+}$, $S_{\text{N-}k}$ and $D_{\text{N}k+}$, $D_{\text{N-}k}$, $k = \{\text{a,b,c}\}$,

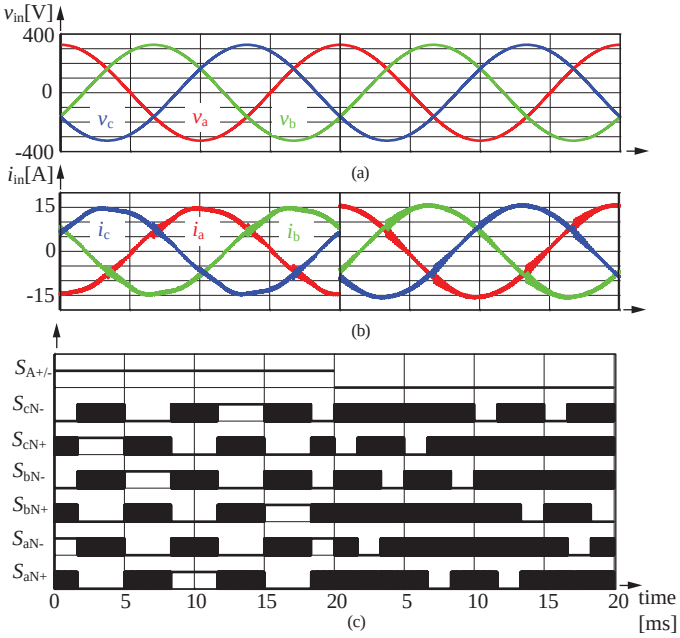

Fig. 3. Simulated characteristic waveforms of the Bidirectional Six-Switch Rectifier with Switchable Output Polarity, with power flow from DC to AC (left) and AC to DC (right). (a) input voltage, (b) input current, (c) IGBT gating signals.

TABLE IV
SIMULATED CURRENT STRESSES FOR THE 7.5KW THREE-PHASE BIDIRECTIONAL SIX-SWITCH RECTIFIER WITH SWITCHABLE OUTPUT POLARITY.

Component	$P_{\text{dc}} = 7.5\text{kW}$		$P_{\text{dc}} = -7.5\text{kW}$	
	I_{RMS}[A]	I_{AVG}[A]	I_{RMS}[A]	I_{AVG}[A]
S_{N} / D_{N}	10.85	6.25	9.65	4.93
$D_{\text{A+/-}}$	16.68	14.8	0	0
$S_{\text{A+/-}}$	0	0	18.8	18.75
S_{B} / D_{B}	8.6	3.94	5.35	2.11
C	0.75	0	∼0	∼0
L	18.8	18.75	18.8	18.75

TABLE V
SIMULATED CURRENT STRESSES FOR THE 7.5KW THREE-PHASE BIDIRECTIONAL ANTIPARALLEL SIX-SWITCH CONVERTER COMBINATION.

Component	$P_{dc} = 7.5$kW		$P_{dc} = -7.5$kW	
	I_{RMS}[A]	I_{AVG}[A]	I_{RMS}[A]	I_{AVG}[A]
S_{N+k} / S_{Nk-}	0	0	9.62	4.92
D_{N+k} / D_{Nk-}	0	0	9.62	4.92
S_{Nk+} / S_{N-k}	10.84	6.24	0	0
D_{Nk+} / D_{N-k}	10.84	6.24	0	0
S_B / D_B	8.65	3.98	5.3	2.18
C	0.74	0	∼0	∼0
L	18.8	18.7	18.8	18.7

which share the same DC inductance and capacitance, both for AC to DC and DC to AC power flow. Due to the 400 V line-to-line voltage of the AC mains the circuit requires semiconductor devices with a blocking capability of 565 V (for rated mains voltage, not considering switching overvoltages). Accordingly, 1200 V devices have to be employed in the practical realisation.

In this system, the output voltage U_{pn} is formed by low pas filtering (L and C) of the bridge circuit output voltage u, which is generated from segments of the AC line-to-line voltages. In order to maximize the achievable voltage level, while supplying each mains phase with sinusoidally PWM modulated currents, always the two largest line-to-line voltages available within a mains sector are selected in each pulse period for the formation of the output voltage. As a result, ideally the output voltage U_{pn} can be adjusted in the range

$$0 < U_{pn} < \sqrt{\frac{3}{2}} \cdot U_{N,l-l,rms}. \tag{2}$$

An alternative to the three-phase Antiparallel Six-Switch Converter Combination (having twelve active switches) would be the front-end circuit of a sparse matrix converter (not shown here, but introduced in [10]), which advantageously requires a lower number of active switches (nine in total). A higher utilization of each switch is achieved, but at the cost of doubling the number of diodes. For this topology the higher number of components in the current conduction path (two switches and four diodes), generates higher conduction losses than the aforementioned six-four-quadrant-switch topology. For this reason, it is not examined further.

Unlike the Six-Switch Rectifier with Switchable Output Polarity presented in **Section II-A**, not all the IGBTs of the input side bridge circuit are used at all time in case of the Antiparallel Six-Switch Converter Combination (for each power flow direction, only one half of the switches and diodes is used). The same modulation schemes are employed as presented in Table II and Table III respectively, but applied just to the switches which are conducting current for a given power flow direction.

The main simulated waveforms of the Antiparallel Six-Switch Converter Combination are presented in Fig. 4, together with the gating signals of the switches. Table V presents the rms and average current stresses on the semiconductor devices.

C. *Bidirectional* SWISS *Rectifier*

Fig. 2(c) shows a novel bidirectional three-phase PFC rectifier solution combining two buck-type DC-DC converters ($S_{A+/-}$, $S_{B+/-}$, L and C), an active 3rd harmonic current injection network (S_y and D_y), and a bidirectional fundamental frequency rectifier bridge. This topology is denominated here as bidirectional SWISS Rectifier and allows to achieve a controlled DC output voltage and a high power factor with a control strategy of low complexity. The topology is based on the unidirectional SWISS Rectifier, presented in detail in [8].

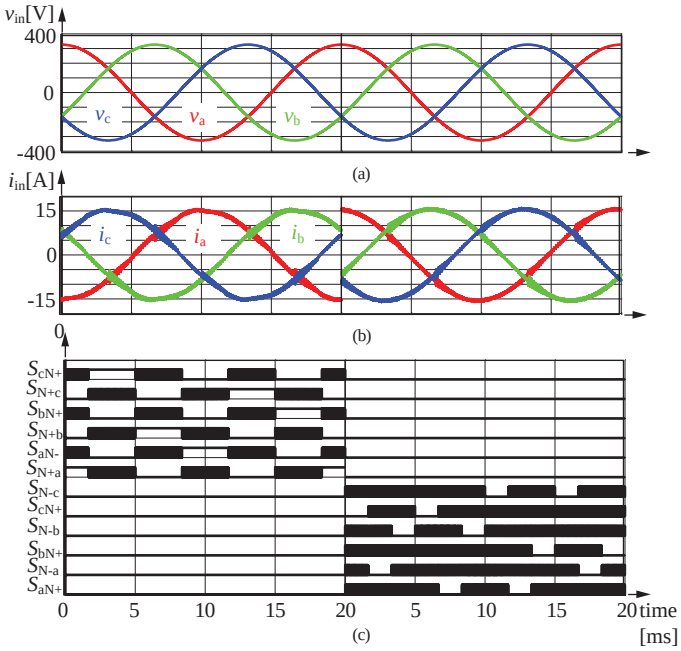

Fig. 4. Simulated characteristic waveforms of the Bidirectional Antiparallel Six-Switch Converter Combination, with power flow DC to AC (left) and AC to DC (right). (a) input voltage, (b) input current, (c) low-frequency IGBT gating signals.

The new rectifier system allows to shape the local average values of currents in the positive and negative active switches, i_{SA+} and i_{SA-} proportional to the input phase voltages which define the positive and negative output voltage of the input side rectifier bridge. The current i_y is fed back into the third mains phase with the currently smallest absolute voltage value. The selection of the proper phase is done via a current injection network, formed by three four-quadrant switches. The switchover of the switches S_y (cf. Fig. 2(c)) follows a four-step commutation scheme which considers dead-times t_d (cf. Fig. 5 to prevent short circuits amongst the phases, and depends on the direction of the power flow. The input current amplitude is set depending on the output load. Note that the DC side voltage range is limited by the maximal value of the six-pulse diode bridge output voltage as given by (2).

In order to form a sinusoidal current at the AC side, the duty cycles of $S_{A+/-}$ (or $S_{B+/-}$ in case of the DC to AC power flow) can be defined as

$$\alpha_+ = \frac{2}{3}\frac{U_{pn}}{\hat{U}_N^2}\max(u_a, u_b, u_c) \tag{3}$$

and

$$\alpha_- = \frac{2}{3}\frac{U_{pn}}{\hat{U}_N^2}\,|\min(u_a, u_b, u_c)| \tag{4}$$

as presented in detail in [8]. By setting the PWM modulator for the generation of the gating signals of $S_{A+/-}$ and $S_{B+/-}$ to operate either with in-phase carriers or carriers with a phase difference of 180° (interleaving), as proposed in [8], the system is able to minimize the current ripple of i_y while the DC current ripple i_L is maximized or vice versa.

The switchover of the current injection network is performed for both power flow directions at twice the mains frequency (100 Hz), and follows the rectifier input voltages $u_{a,b,c}$ in such a way that the active current injection always occurs only the mains phase

TABLE VI
MODULATION OF THE ACTIVE RECTIFIER SWITCHES (S_N IN FIG. 2(C) AND (D)) FOR DC TO AC POWER FLOW.

Sector	S_{N+a}	S_{Na-}	S_{N+b}	S_{Nb-}	S_{N+c}	S_{Nc-}
0°– 60°	1	0	0	0	0	1
60°– 120°	0	0	1	0	0	1
120°– 180°	0	1	1	0	0	0
180°– 240°	0	1	0	0	1	0
240°– 300°	0	0	0	1	1	0
300°– 360°	1	0	0	1	0	0

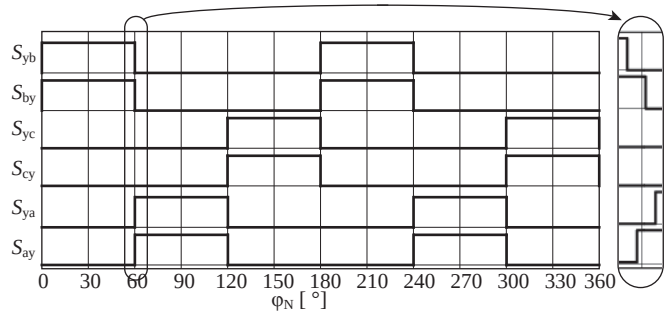

Fig. 5. Gating signals of the 3rd harmonic current injection switches $S_{y,k}$, k = a,b,c, when considering a four-step, current direction dependent commutation scheme for AC-DC power flow (and zoom in of the commutation interval to improve visibility).

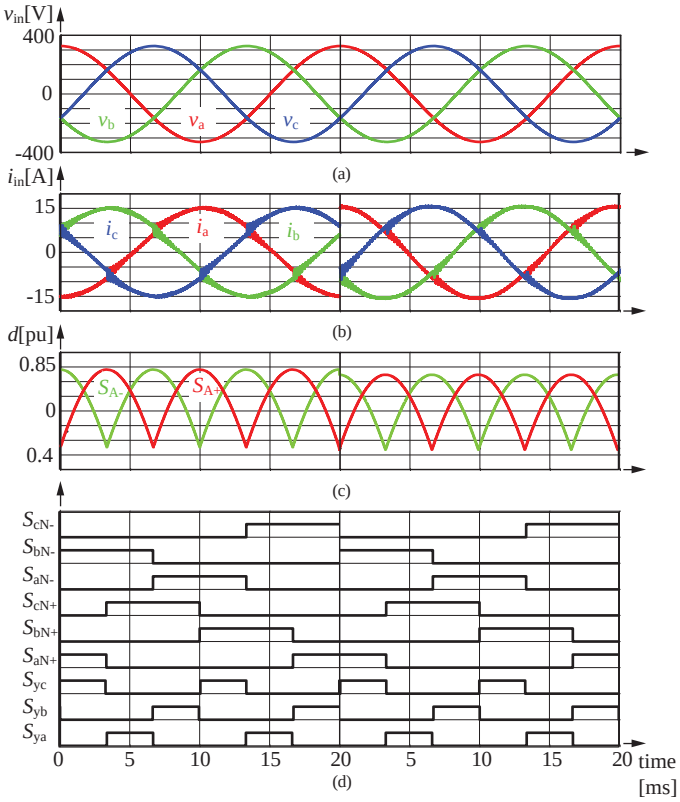

Fig. 6. Simulated characteristic waveforms of the bidirectional SWISS Rectifier, with power flow DC to AC (left) and AC to DC (right). (a) input voltage, (b) input current, (c) duty cycle of the high-frequency IGBT gating signals, (d) low-frequency IGBT gating signals.

with the minimum instantaneous absolute voltage value. Table VI presents the modulation of the 3rd harmonic injection switches S_y, corresponding to a power flow from the AC to the DC side. In case of reverse power flow, the four-step commutation is adapted to the reverse direction of the current flow.

In extension of the unidirectional version, the bidirectional SWISS Rectifier employs IGBTs S_{N+k} and S_{Nk-}, k={a,b,c} connected in antiparallel to the diodes of the input rectifier bridge, in order to allow bidirectional power flow. These switches are commutated with mains frequency (50 Hz) (cf. Table VI), i.e. always the switches antiparallel to conducting diodes are in the turn-on state. Correspondingly, no fast switching behaviour is required and the conduction losses can be reduced by employing devices (IGBTs and diodes) with a low on-state voltage drop. In the same way, the four-quadrant injection switches (S_y and D_y) could be implemented with an anti-parallel connection of RB-IGBTs in order to lower the conduction losses.

The simulation results, depicting the principle of operation of the bidirectional SWISS Rectifier, are shown in Fig. 6, for converter specifications according to Table I, and in-phase PWM carriers for both power flow directions (+7.5 kW and −7.5 kW on the DC side) . The results demonstrate that the line currents $i_{a,b,c}$ can effectively follow the sinusoidal input phase voltages $u_{a,b,c}$ for both directions of the power flow, attesting the feasibility of the proposed rectifier topology. The switches S_y and the corresponding diodes D_y have to block a maximum voltage which corresponds to the 60° sinusoidal progression of the amplitude of the line-to-line input voltage $U_{N,l\text{-}l,max}$,

$$U_{Sy,max} = \frac{\sqrt{3}}{2} U_{N,l-l,max} = 537\,\mathrm{V}. \quad (5)$$

All the remaining semiconductors (D_N, S_N, $D_{A+/-}$, $S_{A+/-}$) have to block the voltage $U_{N,l\text{-}l,max}$,

$$U_{N,l-l,max} = \sqrt{6}\, U_{a,rms}. \quad (6)$$

TABLE VII
SIMULATED CURRENT STRESSES FOR THE THREE-PHASE BIDIRECTIONAL SWISS RECTIFIER.

Component	$P_{dc} = 7.5$kW		$P_{dc} = -7.5$kW	
	I_{RMS}[A]	I_{AVG}[A]	I_{RMS}[A]	I_{AVG}[A]
S_N	0	0	8.97	4.2
D_N	8.94	4.2	0	0
S_y	3.75	~0	3.35	~0
D_y	3.75	~0	3.35	~0
$S_{B+/-}$	0	0	10.85	6.28
$D_{B+/-}$	10.63	5.95	0	0
$S_{A+/-}$	15.50	12.80	0	0
$D_{A+/-}$	0	0	15.53	12.63
C	1.21	0	~0	~0
L	18.8	18.76	18.96	18.91

The simulated current stresses for all semiconductors are compiled in Table VII.

D. Bidirectional 3rd Harmonic Injection Active Filter Type Rectifier with DC/DC Output Stage

The basic configuration of the Bidirectional 3rd Harmonic Injection Active Filter Type Rectifier with DC/DC Output Stage is shown in Fig. 2(d). The presented topology allows bidirectional power flow and is an extension of the unidirectional active 3rd harmonic current injection mains interface presented in [9]. In order to achieve bidirectional power flow capability, active switches S_N are connected antiparallel to the diodes of the three-phase input rectifier bridge, allowing negative current flow. These switches are commutated according to Table VI.

The line-commuted bidirectional rectifier is combined with an active 3rd harmonic current injection network, which is formed by a single fast-commuted bridge-leg ($S_{B+/-}$), an inductor (L_y), and three low frequency four-quadrant switches (S_y and D_y). Accordingly, the circuit shows a relatively low implementation effort, however, at the expense of missing output voltage control. The output voltage is determined directly by the diode bridge rectifier and hence exhibits a six-pulse shape. Additionally, the front-end circuit requires a constant power load/source for sinusoidal input current generation. The bidirectional DC/DC converter output stage (switches $S_{A+/-}$, diodes $D_{A+/-}$ and inductor L) implementing the constant power behaviour is also used for output voltage regulation and eliminates the six-pulse voltage variation at the output of the rectifier input stage.

Similar to the SWISS Rectifier, the modulation of the current injection circuit is performed at low frequency (twice the mains frequency, with two 60° conduction intervals within a mains period). The active current injection always is only into the mains phase with the lowest absolute instantaneous voltage value, as presented in Fig. 5. Due to the requirement of uninterrupted current flow through the inductor L_y, a four-step switching policy as presented in [13] is mandatory for this topology. Alternatively, freewheeling diodes connected from the star point of the four quadrant switches to the positive and negative output voltage rail could be employed [9]. Similar to the modulation of the injection circuit of the SWISS Rectifier, Fig. 5 presents the modulation of the 3rd harmonic injection switches S_y, for a power flow from the AC to the DC side. In case of reverse power flow, the modulation is adapted to the inverse current flow direction. Due to the relatively high voltage at the output of the front-end converter, a relatively large value for L_y has to be used, in order to lessen the injected current ripple and consequently reduce the size of the EMI filter.

Fig. 7 presents the simulated characteristic waveforms of the Bidirectional 3rd Harmonic Injection Active Filter Type Rectifier with DC/DC Output Stage, operated under rated conditions (±7.5 kW power). As can be observed, the results demonstrate that the line currents $i_{a,b,c}$ can effectively follow the sinusoidal input phase voltages $u_{a,b,c}$ for both directions of the power flow. The rms and average current values of the IGBTs obtained from the simulation, and to be used in the calculation of the switching and conduction losses further, are displayed in Table VIII.

Due to the circuit similarities with the bidirectional SWISS Rectifier, the blocking voltage stress on the semiconductors of the bidirectional switches, S_y and D_y, is equal to (5) while that of the remaining semiconductors (D_N, S_N, $D_{A+/-}$, $S_{A+/-}$, $D_{B+/-}$, $S_{B+/-}$) is equivalent to (6).

III. Comparative Evaluation

In order to achieve the highest possible efficiency, losses of all components must be calculated as accurately as possible and minimized during the design stage. The circuit losses can be divided broadly into two categories: semiconductor losses and losses of passive components. In order to evaluate and compare the different converter concepts discussed in **Section III** several performance indices are defined: transistor losses (conduction losses $P_{C,S}$ and switching losses $P_{S,S}$), diode losses (conduction losses $P_{C,D}$ and switching losses $P_{S,D}$), losses of the passive components (capacitor losses P_{cap} and inductor losses P_{ind}), and the required total semiconductor chip area A_{chip}, as well as the total passive components volume, related to the output power (relative capacitor volume ρ_{cap}^{-1} and inductor volume ρ_{ind}^{-1}). Additional performance indices considered are the generated common mode and differential mode noise levels, u_{CM} and u_{DM}, which give an insight regarding the damping requirements of the EMI filter. The EMI comparison was performed according to the method introduced in [7].

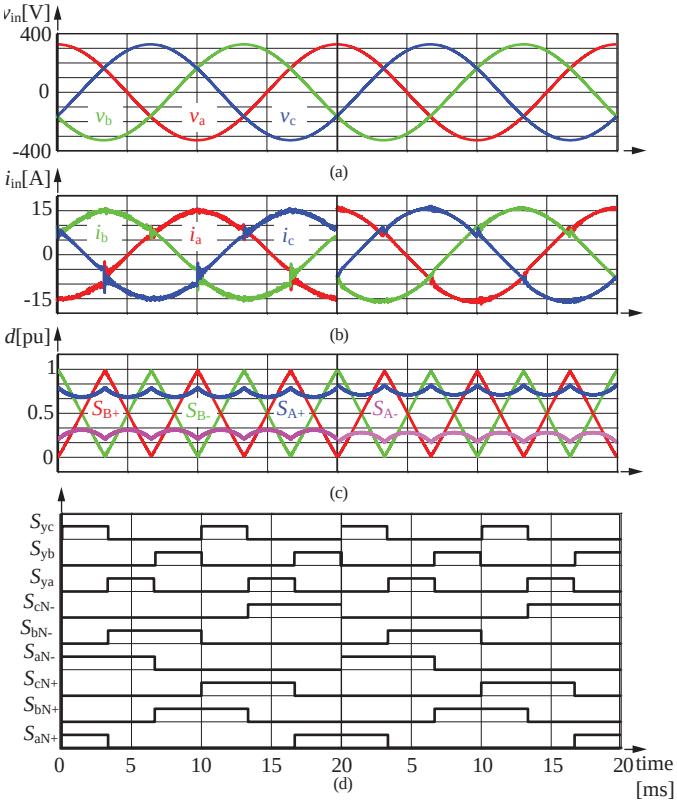

Fig. 7. Simulated characteristic waveforms of the Bidirectional 3rd Harmonic Injection Active Filter Type Rectifier with DC/DC Output Stage, with power flow from DC to AC (left) and from AC to DC (right). (a) input voltage, (b) input current, (c) duty cycle of the high-frequency IGBT gating signals, (d) low-frequency IGBT gating signals.

TABLE VIII
SIMULATED CURRENT STRESSES FOR THE BIDIRECTIONAL 3RD HARMONIC INJECTION ACTIVE FILTER TYPE RECTIFIER WITH DC/DC OUTPUT STAGE.

Component	$P_{dc} = 7.5$kW		$P_{dc} = -7.5$kW	
	I_{RMS}[A]	I_{AVG}[A]	I_{RMS}[A]	I_{AVG}[A]
S_N	0	0	8.57	4.26
D_N	8.73	4.3	0	0
S_y	2.18	∼0	1.88	∼0
D_y	2.18	∼0	1.88	∼0
$S_{B+/-}$	1.10	0.31	2.35	1.26
$D_{B+/-}$	3.46	1.90	1.27	0.40
S_{A+}	16.41	14.26	0	0
D_{A+}	0	0	15.88	13.54
S_{A-}	0	0	9.97	5.20
D_{A-}	4.55	2.52	0	0
C	0.4	0	∼0	∼0
L	18.77	18.75	18.75	18.74
L_y	4.5	∼0	4.5	∼0

In the following, first the efficiencies of all topologies are calculated considering the employed components listed in Table I. The rms and average values of the series diode currents I_D and IGBT currents I_S, obtained from the simulations, can be used to calculate the conduction losses of the switches,

$$P_{C,S} = I_{S,avg} \cdot U_{CE,sat}, \tag{7}$$

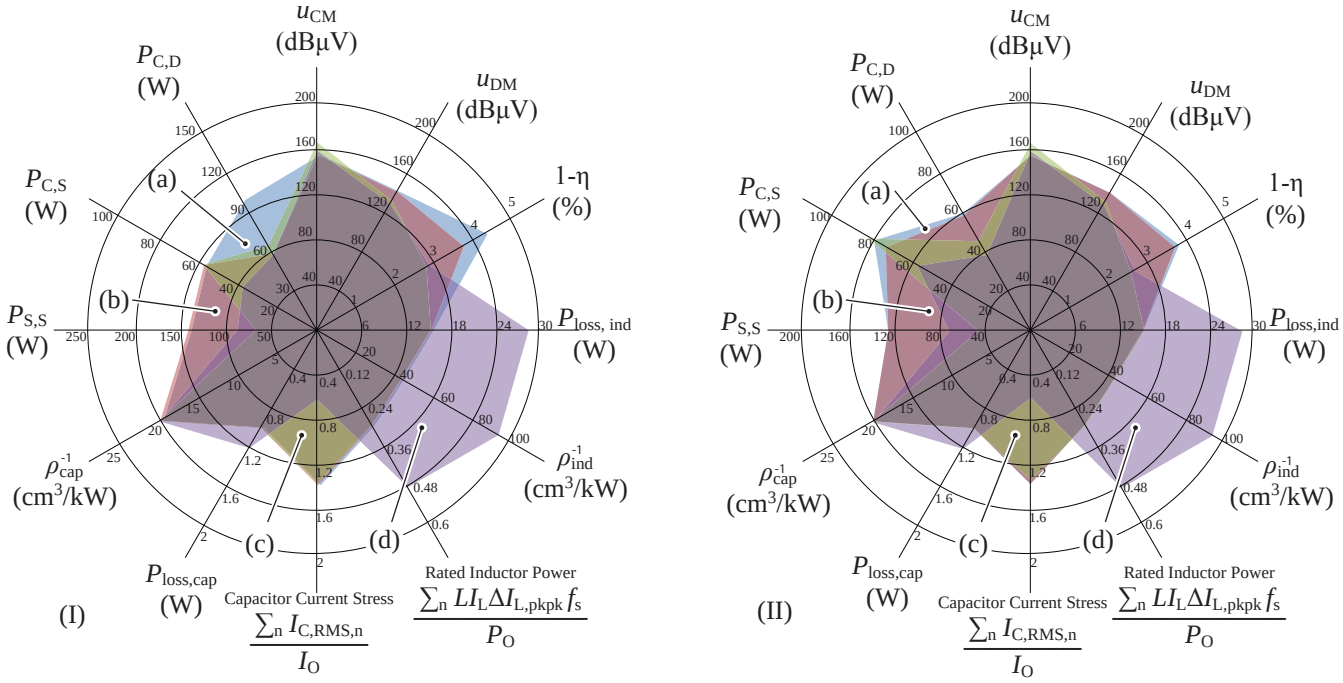

Fig. 8. Direct comparison of the performance indices ((I) Rectifier operation and (II) Inverter operation). (a) Six-Switch Rectifier with Switchable Output Polarity, (b) Antiparallel Six-Switch Converter Combination, (c) Bidirectional SWISS Rectifier, (d) Bidirectional 3rd Harmonic Injection Active Filter Type Rectifier with DC/DC Output Stage.

and of the diodes,

$$P_{C,D} = I_{CE,awg} \cdot U_D + I^2_{CE,RMS} \cdot R_D, \tag{8}$$

where $U_{CE,sat}$ is the IGBT collector emitter saturation voltage, R_D is the differential diode on-resistance, and U_D is the diode forward voltage. All parameters are extracted from the datasheets. It is possible to calculate similarly the average switching losses (turn-on and turn-off) of the IGBTs

$$P_{S,S} = k_S \cdot I_{S,avg} \cdot f_{sw}, \tag{9}$$

where k_S relates the switching loss energy to the switched current, $I_{S,avg}$ is the average value of the current of the corresponding switch, and f_{sw} is the switching frequency of the converter. The losses of the output capacitor P_{cap} can also be estimated, based on characteristic values obtained from the datasheet, as

$$P_C = I^2_{C,rms} \frac{\tan\delta}{2\pi f_{sw} C} + I_{leak} \cdot U_{pn}. \tag{10}$$

Using the loss factor $\tan\delta$, where C is the capacitance of the output capacitor, the leakage current I_{leak} (determined using characteristic equations given in the capacitor datasheet), $I_{C,rms}$ is the rms current through the capacitor and U_{pn} is the average capacitor voltage.

The inductor losses P_{ind} can be divided into two major parts: core losses and low frequency and high frequency losses in the winding (e.g. skin effect and proximity effect). For the sake of simplicity, no HF copper losses have been taken into consideration here. The low frequency copper losses can be derived as

$$P_{Cu} = I^2_{L,rms} \frac{\rho N l_T}{A_w}, \tag{11}$$

where $I_{L,rms}$ is the rms current through the inductor, N is the number of turns, l_T the average length of a turn, A_w the wire cross-sectional area and ρ the resistivity.

The core losses can be calculated using the modified Steinmetz equation [14]. For triangular switching frequency current present in the inductors we have

$$P_{core} = k \cdot f_{sw} \cdot \left(\frac{8 f_{sw}}{\pi^2}\right)^{\alpha-1} \cdot V_{core} \cdot \left(\frac{L \cdot (1/2 \cdot \Delta I_L)}{N \cdot A_e}\right)^{\beta}, \tag{12}$$

where k, α, and β are Steinmetz parameters, given or extracted from core material datasheets; V_{core} is the total core volume, I_L is the average inductor current, ΔI_L is the peak-to-peak inductor current ripple amplitude and A_e the inductor core cross-sectional area. It is neglected that core losses vary with DC magnetic bias [15]; since the output inductor DC bias is equal for all topologies (and equal to the output current), this does not take significant influence on the comparison. Fig. 8 shows the distribution of the losses amongst the components.

The Bidirectional 3rd Harmonic Injection Active-Filter-Type Rectifier with DC/DC Output Stage exhibits equal or lower EMI noise levels when compared to the other topologies, which can be explained by the large inductance located in the 3rd harmonic injection path.

The comparison could be further improved, as the selected IGBTs and diodes are not optimized for each specific topology. Hence, some semiconductors in some converter topologies might be over dimensioned, while others are at their thermal limit. Nevertheless, the comparison gives a first overview of the performances of the topologies.

For a more detailed comparison, an approach proposed in [6] could be applied, which allows the determination of optimal chip areas of the individual semiconductors, while guaranteeing certain thermal boundary conditions. The chip sizes of each topology are then adapted such that the junction temperature of each element reaches a mean value of T_j = 125°C. Accordingly, the chip area for elements with low losses is decreased; elements with high losses are assigned a larger chip area. In order to perform this chip size optimization, the analytical models for conduction and switching

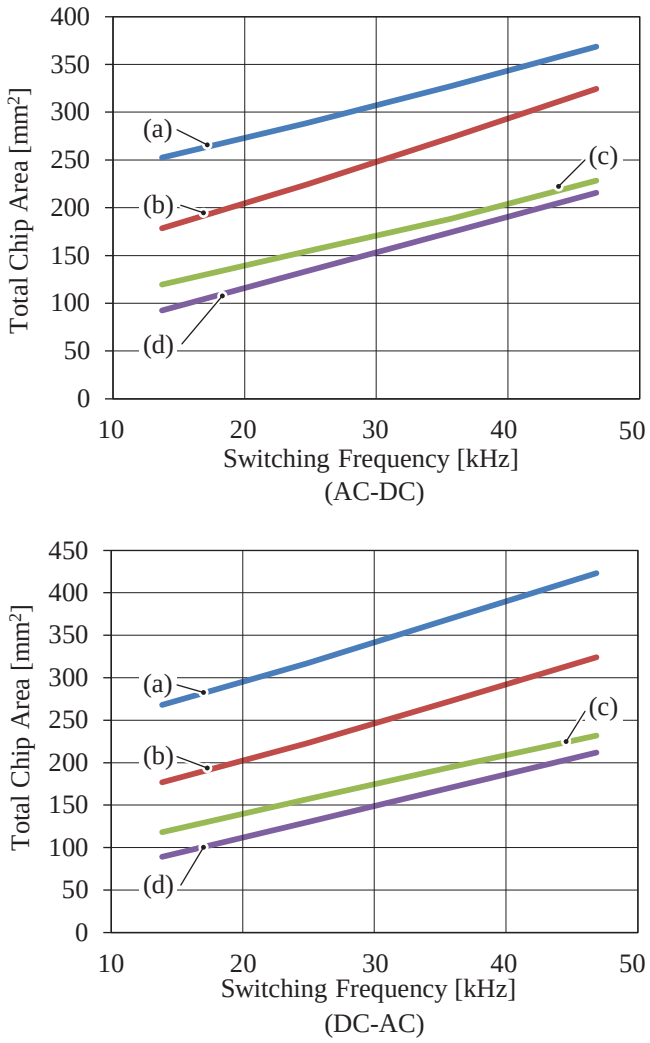

Fig. 9. Comparison of the required total semiconductor area depending on the switching frequency (Rectifier operation/Inverter operation) (a) Six-Switch Rectifier with Switchable Output Polarity (b) Antiparallel Six-Switch Converter Combination (c) Bidirectional SWISS Rectifier (d) Bidirectional 3rd Harmonic Injection Active Filter Type Rectifier with DC/DC Output Stage.

losses, as well as the thermal equivalent circuit have to be adapted to incorporate the semiconductor chip area [16]. The results of the chip area optimization for the the different topologies are given in Fig. 9 and confirm the initial efficiency calculations, showing the topologies with lower efficiency to require a larger semiconductor chip area.

IV. Conclusion and Future Work

This paper proposes three-phase high power factor bidirectional mains interfaces, appropriate for smart-house applications, where a local DC grid is available, supplied from several local sources and connected to the three-phase AC grid.

The characteristics of the presented bidirectional three-phase buck-type PFC systems, including the principles of operation and modulation strategies are summarized in this paper. Finally, the comparison of the studied converters rated for an output power of 7.5kW, 400Vrms line-to-line AC input, 400V DC output and 36kHz switching frequency is shown. This identifies the Bidirectional 3rd Harmonic Injection Active-Filter-Type Rectifier with DC/DC Output Stage as the most advantageous solution when considering the overall efficiency of the system as well as the required total semiconductor chip area. Additional indices included in the comparison are the passive components volume and the expected requirements of the EMI filter based on simulated noise levels of the converters.

Future work will include a detailed experimental analysis of each system and a verification of the theoretical analysis.

Furthermore, an optimization of the systems for cases where the rated DC to AC power flow, i.e. the power injection from the local DC grid into the AC grid, is lower than the AC to DC power rating will be performed.

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