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J. Huber,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

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Jonas E. Huber and Johann W. Kolar
Power Electronic Systems Laboratory
ETH Zurich
8092 Zurich, Switzerland
huber@lem.ee.ethz.ch

***Abstract*—When power electronic systems are connected to the medium-voltage grid, often multilevel topologies consisting of a number of cascaded converter cells are considered. For a given grid voltage level, either few cells featuring semiconductors with high blocking voltage capability or many cells using low-voltage semiconductors can be employed. This paper proposes efficiency/power density (η-ρ) Pareto analysis to comprehensively identify the optimum number of cascaded cells. Recent advances in silicon carbide (SiC) semiconductor technology point towards devices with blocking voltages exceeding 15 kV. The switching characteristics that hypothetical SiC devices would have to provide in order to realize a simple single-stage full-bridge converter competitive to a multilevel solution are derived and found to be impracticably fast. Furthermore, it is shown that reliability concerns arising with increasing number of cascaded cells can be mitigated by means of redundancy.**

I. Introduction

Utility scale transformers operated at the grid frequency of 50 Hz or 60 Hz are bulky and costly but very important components of the power system, since they provide voltage scaling and isolation between different system sections. While the first patent of an "electronic transformer" describing a converter with a high-frequency AC link for isolation has been issued already in 1970 [1], only more recent advances in power semiconductor technology have laid the basis for power electronic systems to play a major role in the transmission and distribution grid; nevertheless, applications such as HVDC, FACTS and STATCOMs have become well established technologies in the meantime [2].

The "electronic transformer" has been revived around the turn of the millennium, now with grid-scale ratings and termed Solid State Transformer (SST) or Power Electronic Transformer (PET), aiming at replacing 50 Hz transformers [3]–[7]. Besides the reduction in size and weight owed to the high-frequency potential separation, which makes SSTs also an interesting option for traction applications [8]–[11], there are additional degrees of freedom that allow for features such as power flow control, active filtering of harmonics, connection of energy storage to the DC link [12] and many more. These make SSTs an enabling technology for the smart grid [2].

Advances in wide band-gap semiconductor technology, i. e. silicon carbide (SiC), will contribute to improved efficiency and power density because of superior material performance compared with silicon (Si) [13]–[17]. Recent examples include proposals for an SST on the basis of 10 kV SiC devices [18], a transformerless substation employing 15 kV SiC IGBTs [19], microgrid applications [20] and a SiC JFET based small-scale prototype of a modular multilevel converter for HVDC applications [21]. SiC technology needs to mature further and costs have to decrease until it can be considered for industrial solutions, though.

Therefore, conventional silicon (Si) based systems will prevail in real-world applications for the foreseeable future. However, the blocking voltage ratings of readily available Si power semiconductors are limited to 6.5 kV. In order to interface a 10 kV medium voltage (MV) grid, either series connections of semiconductors or multilevel converters have to be employed [6]. The latter can exploit the additional switches to obtain multilevel output voltages, which improves the harmonic performance [22]. Paralleling [23] or series connecting [24] of converter modules instead of the power semiconductors themselves is a well-known concept already proposed in the early 1990ies.

While three-level diode-clamped [25] and capacitor-clamped topologies [26] have found widespread application for example in the MV drives industry, they are not feasible for grid-scale applications because of the limited voltage capability. More levels are possible but lead to increased system complexity without providing modularity. Therefore, cascading of converter cells is usually considered instead. Cascading of H-bridge cells (CHB) has been patented for the first time in the 1970ies [27], [28]. It has been used in a wide range of high power applications such as railway drive systems [8]–[11] or smart-grid applications [15], [29]. Instead of cascading H-bridges, cells featuring two NPC legs could be employed, creating a cascaded NPC-bridge converter (CNB) [30].

Fig. 1 illustrates three typical application examples of cascaded cell converters, where only one of the three phase legs is shown, respectively. While reactive power compensating systems (Fig. 1(a)) do not require isolated DC supplies, most power processing systems such as SSTs (Fig. 1(b)) or drive systems (Fig. 1(c)) do. The modular multilevel converter (MMC) [31], [32] or battery storage applications [29] should be named as exceptions here, though. In case of SSTs, the DC supply for the individual cells is usually implemented by means of isolated DC/DC converters operating in the medium-frequency range, whereas for drives also solutions employing multi-winding transformers and passive rectification are considered.

In the following, only the grid-connected CHB (or CNB) part of the example systems shown in Fig. 1 and mentioned in the

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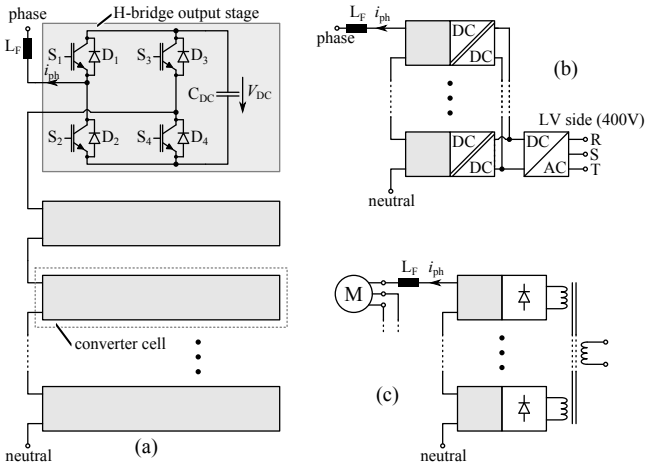

Fig. 1. Different application examples of cascaded converter structures, where one out of three phase legs is shown, respectively. (a) STATCOM, (b) solid state transformer (SST), (c) drive system. The grey boxes symbolize H-bridges (CHB) or NPC-bridges (CNB).

TABLE I
TRADE-OFFS AFFECTED BY THE NUMBER OF CASCADED CELLS.

Fewer cascaded cells	More cascaded cells
lower conduction losses	higher conduction losses
few output levels (higher f_S and/or larger L_F)	many output levels
worse switching loss behavior of semiconductors	better switching loss behavior
less components	more components (reliability!)

text is considered for reasons of generality and clarity. However, the approach shown could be extended to more specific cases by including e. g. the DC/DC converters in the case of an SST system; however, the design of a DC/DC converter is a η-ρ-Pareto optimization problem on its own [33] and therefore the computational requirements would be increased significantly.

This paper therefore comprehensively approaches the question of the optimum number of cascaded H-bridge or NPC-bridge cells in such high-power multilevel converter systems by means of employing efficiency/power density (η-ρ) Pareto analysis, which is discussed in the next section. Section III introduces a way of comparing multilevel designs based on different semiconductors similar to approaches known from power semiconductor technology. Then, the switching characteristics that a hypothetical SiC device would have to provide in order to realize a competitive solution based on only a single full-bridge converter are derived in Section IV. Because cascaded cells systems usually consist of a high number of devices, Section V finally addresses reliability and redundancy issues.

II. Optimum Number of Cascaded Converter Cells

For a given grid voltage, either few cascaded inverter cells with semiconductors featuring high blocking voltages or many cells with low-voltage semiconductors can be used. Semiconductors with higher blocking voltage generally show

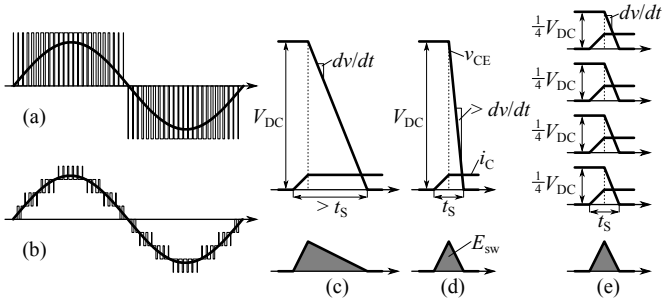

Fig. 2. Converter output voltage and its fundamental for a single-cell solution (a) and for a multilevel solution (b) featuring four cascaded H-bridges; switching process in a cascaded cell system (e) and in a single-cell solution for the same overall DC link voltage, where (d) the same switching energy as in the multilevel case is achieved by increased dv/dt or (c) the dv/dt is left unchanged with respect to the multilevel case.

worse switching behavior (higher switching losses), but on the other hand more series connected cells lead to potentially higher conduction losses. Fig. 2(c)-(e) illustrates this by comparing the switching processes of a system featuring four cascaded cells with those of a single-cell solution for the same overall DC link voltage. If the switching energies of the latter should be comparable, much higher dv/dt values would be required (d), else the loss energies would increase (c) due to speed limitations [34]. The power density is mainly influenced by the size of the heat sinks, which depends on semiconductor losses, and the grid filter inductor, L_F. Any equipment connected to the MV grid must comply with harmonic standards such as IEEE 519 [35]. A system with many output voltage levels and high switching frequency requires a smaller L_F than a system with only a few output voltage steps and low switching frequency (cf. Fig. 2(a),(b)). Note that these trade-offs would be similar also for the DC/DC stages of the SST example, where instead of the filter inductor the medium frequency transformers would have to be considered.

While the basic trade-offs between conduction and switching losses have been briefly addressed in [8] and [29], and while [36] analyzed power density benefits of multilevel approaches for low power applications, in the approach that is presented here, both, efficiency and power density are considered together. η-ρ Pareto analysis [37] is a feasible way of quantifying the trade-offs outlined above, and summarized in Table I, in a comprehensive way.

A. Basic Considerations

To first illustrate the basic dependencies of converter losses on the number of cascaded cells with an extremely simplified model, conduction and switching losses need to be expressed as a function of the number of series connected converter cells, n. Assuming constant forward voltage drops across the semiconductors to be independent of the voltage rating, i. e. $V_{CE,on} = const.$, the overall conduction losses of a system with n cascaded cells are given by

$$P_c(n) = I_0 V_{CE,on} \cdot n, \quad (1)$$

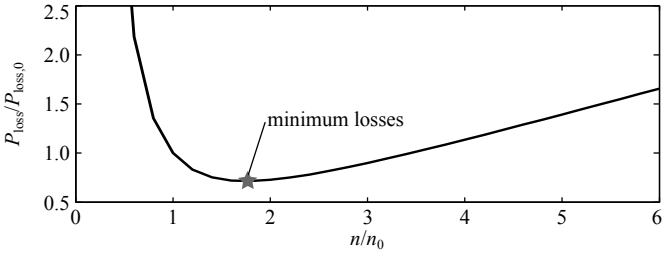

Fig. 3. Basic dependence of the system losses on the number of series cells for $I_0 = 80\,\text{A}$, $V_{CE,on} = 1.5\,\text{V}$, $n_0 = 5$, $V_0 = 2\,\text{kV}$, $t_S = 1\,\mu\text{s}$ and $f_{S,0} = 1\,\text{kHz}$.

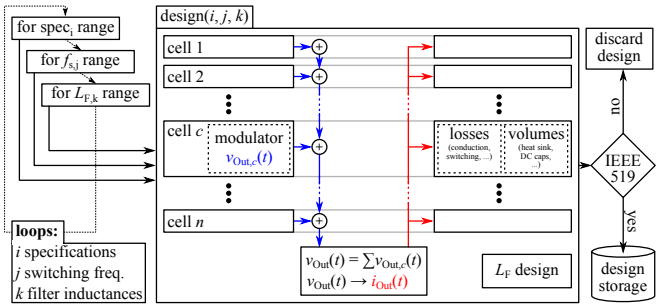

Fig. 4. Flowchart illustrating the optimization procedure that is used to generate a large number of design points.

where I_0 can be regarded as an equivalent phase current, which depends on the system power but not on n. Switching losses are modeled assuming equal slopes of current and voltage such that the overall duration of the switching transition, $t_{S,0}$, the collector current, I_0, and the blocking voltage, $V(n)$, define the switching energy (cf. also Fig. 2) as $E_{sw} = I_0 V(n) t_{S,0}/2$. Both, the blocking voltage and the switching frequency per cell depend on n (cf. Table I), which is modeled as

$$V(n) = V_0 \cdot \frac{n_0}{n} \quad \text{and} \quad f_S(n) = f_{S,0} \cdot \frac{n_0^2}{n^2}, \tag{2}$$

where the switching frequency is scaled such as to result in equal current ripple considering the same filter inductance as described in [38]. The overall switching losses can thus be described as

$$P_{sw}(n) = 2 f_{S,0} V_0 I_0 t_{S,0} \cdot \frac{n_0^3}{n^2}, \tag{3}$$

where n_0 is the number of series cells for which $f_{S,0}$ and the cells' DC voltage V_0 are given. The overall losses, i. e. the sum of conduction and switching losses, are shown in Fig. 3 as a function of n/n_0. It can clearly be seen that there is a certain n for which the overall losses are lowest, i. e. that there is an optimum number of series connected converter cells. In the following, a much more detailed model based on device data sheet characteristics and including also losses in passive filtering components as well as considering the system volume as a second dimension is presented.

B. Optimization Procedure Overview

Fig. 4 gives an overview on the implemented optimization procedure. For a number of design *specifications* (comprising the number of cascaded cells, CNB or CHB type, the cells' DC voltage and the semiconductor model), the switching frequency, f_S, and the filter inductance, L_F, are varied over specific ranges (cf. Table II).

TABLE II
SST SPECIFICATIONS FOR OPTIMIZATION.

MV voltage	10 kV (line-line)
power	1 MW
phase power	333 kW
f_S range	50 Hz – 15 kHz
L_F range	1 mH – 250 mH

A combination of a specification, a switching frequency and a filter inductance is referred to as a *design*. For each of these designs, the main converter waveforms during one steady-state period with pure active power transfer from MV to LV side are calculated, whereby PWM modulation with phase-shifted carriers is considered [39], [40]. The superposition of the modulated output voltages of all series connected cells gives together with the grid voltage and the filter inductor the output phase current. If a design's output current spectrum does not comply with IEEE 519, the design is discarded. Else, the overall conduction and switching losses are estimated using datasheet curve fitting [41] and procedures to classify switching transitions [42], [43], which allows for calculating switching losses for all affected devices based on datasheet information. Forced air cooling is assumed and the heat sink volume is estimated using the Cooling System Performance Index [44] with $CSPI = 10\,\text{W/(KL)}$, 50 °C ambient and 125 °C junction temperature. The DC link capacitance is chosen for a voltage ripple specification of 5 % and the capacitor volume is estimated using a constant energy density of $6.33\,\text{cm}^3/\text{J}$ for film capacitors, which has been found by averaging datasheet values of capacitors with various capacitance and voltage ratings. A loss-optimizing design procedure with core dimensions as free parameters is used to obtain volume and losses of the design's filter inductance L_F. Of course, the inductor design, as any other magnetics design, is an η-ρ-Pareto problem on its own as for example discussed in [45] for transformers; while this is not considered here, it could, e. g. together with the Pareto optimization of the DC/DC stage, be included in a comprehensive optimization of a complete SST system, which may be subject to future work.

C. Results

The optimization procedure calculates a high number of designs for each specification. Each of these designs features a specific efficiency, η, and power density, ρ. The power density is obtained by dividing the nominal phase power by the sum of all component volumes. A scaling factor of $C_p = 0.7$ is then applied to account for spacing between components, etc. as suggested in [37]. Color-coded by specifications, these designs can be plotted as points in the $\eta\rho$-plane. The corresponding Pareto fronts are shown in Fig. 5.

It is directly visible that solutions based on semiconductors with a blocking voltage of 3.3 kV and higher are not competi-

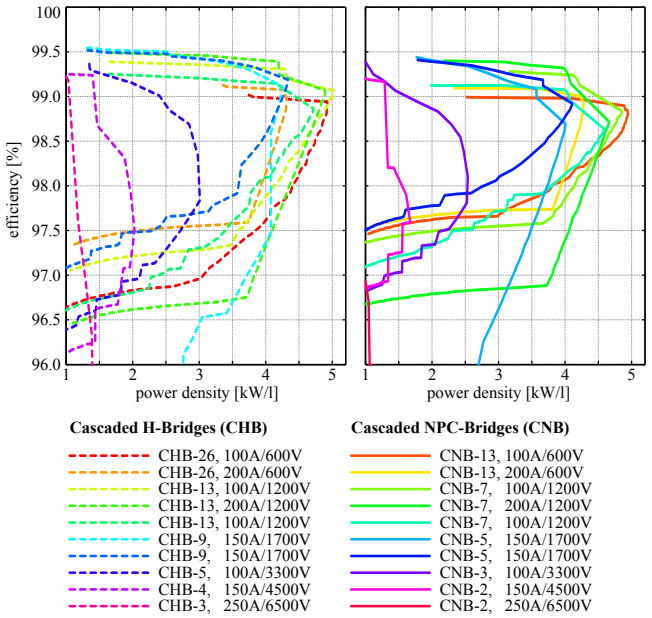

Fig. 5. η-ρ Pareto fronts for designs based on a range of commericallyavailable IGBT modules with blocking voltages between 600 V and 6.5 kV. "CHB-9" denotes a design with 9 cascaded H-bridge cells, etc.

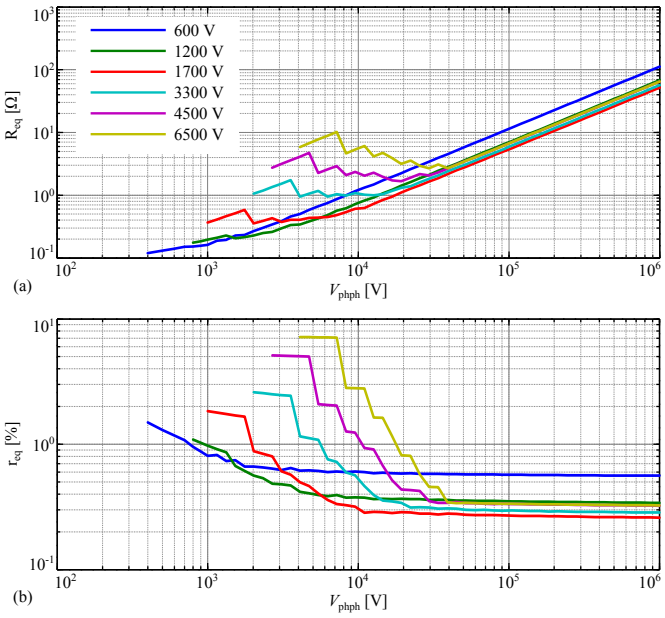

Fig. 6. Equivalent loss resistance of cascaded cell converters based on IGBTs of different blocking voltage classes as a function of the phase-to-phase voltage. (a) Absolute values and (b) per unit values. Note that plots of the absolute losses and of relative losses versus the grid voltage look qualitatively the same.

tive. Highest power density for an efficiency requirement of 99 % can be achieved with a solution based on 13 cascaded H-bridge cells (CHB-13) using 100 A/1200 V IGBTs. In general, solutions based on 1200 V and 1700 V class IGBTs offer the best trade-off between system efficiency and volume.

III. The Si Multilevel Limit

In power semiconductor technology, diagrams showing the device's on-state resistance as a function of the blocking voltage on a double log scale are commonly used to characterize the limits of certain semiconductor categories such as Si or SiC. The same can be done to compare the different Si-based cell types considered in this paper.

The question to be addressed is how the losses, which can be expressed by an equivalent loss resistance, R_{eq}, scale with the grid voltage level. To do so and starting from the specifications used throughout this paper (cf. Table II), the peak phase current is fixed at 80 A whereas the phase-to-phase voltage is varied from 400 V to 1 MV. The filter inductor is set to 5 % (pu), corresponding to a constant relative passive filtering effort.

For each grid voltage level and cell specification (blocking voltage rating), the required number of series connected converter cells is obtained from considering a nominal modulation index of $M = 0.8$ and a minimum utilization of the devices' blocking voltages of 40 %. The lowest possible switching frequency required to meet IEEE 519 [35] is used, however, a lower bound of 100 Hz is imposed, since for lower frequencies special modulation techniques such as optimized pulse patterns would have to be employed. System losses are calculated using the same methods as described in Section II.

Since the phase current is always the same, an equivalent loss resistor, R_{eq}, can be defined as

$$R_{\mathrm{eq}} = \frac{P_{\mathrm{loss}}}{I^2_{\mathrm{ph,rms}}}, \tag{4}$$

which allows to obtain a R_{eq} versus system phase-to-phase voltage plot as shown in Fig. 6.

Solutions based on 600 V devices offer lowest R_{eq} values up to a grid voltage level of about 1 kV. From there to about 5 kV, designs employing 1200 V devices are more suitable. Finally, systems using 1700 V-based cells offer best performance for higher voltages. A clear convergence can be observed for very high voltages, which is due to the fact that there the switching losses are very low because of the high number of levels and consequently very low switching frequencies. Therefore, conduction losses dominate R_{eq}, which are similar for the different technologies in overall, although 600 V solutions clearly seem to suffer from the much higher number of series voltage drops.

IV. Equivalent Two-Level SiC Converter

Recent advances in SiC technology have resulted in 4H-SiC IGBTs with blocking voltages of 15 kV and beyond [46], [47]. In theory, this would allow for a single H-bridge inverter with a DC voltage of e. g. 10 kV to interface the 10 kV MV grid (cf. Fig. 7(a)), which would reduce system complexity. It is thus an interesting question what switching characteristics such a SiC device would require in order for this solution to be competitive with cascaded systems based on readily available Si devices.

A single two-level converter solution classifies as a FB-1 design using the terminology from above. The DC link voltage is set to 10 kV and the conduction characteristics of a 15 kV SiC

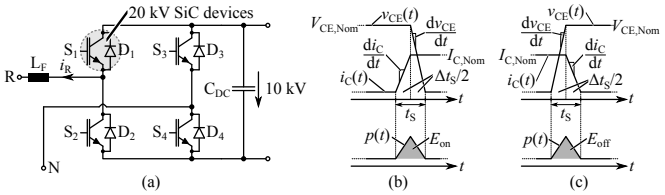

Fig. 7. Equivalent SiC two-level converter. (a) output stage of phase R; (b) simplified E_{on} modeling and (c) simplified E_{off} modeling.

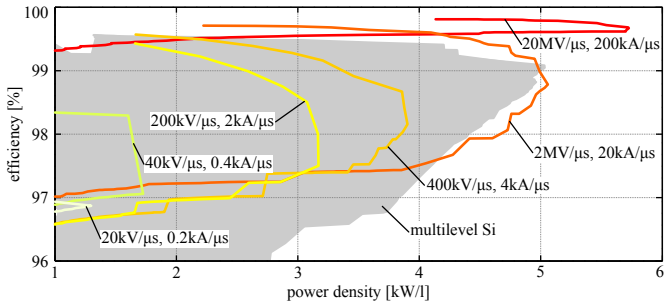

Fig. 8. Pareto fronts of an equivalent SiC two-level converter for different switching characteristics. The range covered by the Si multilevel designs from Fig. 5 is shown in the background for reference.

IGBT described in [47] are considered. Since no commercial devices with appropriate packaging are available, the thermal resistance and the package volume are assumed to be equal to those of the 6.5 kV IGBT considered above, while a higher junction temperature of 200 °C is allowed. While it is clear that these might be coarse approximations, since for example the higher blocking voltage would require a special package design including extremely low inductive conduction paths and thicker DCBs for isolation purposes, the qualitative validity of the results obtained below should hardly be affected.

Switching losses are modeled as indicated by Fig. 7(b) and (c). Considering the turn-off process, it is assumed that the first half of the total duration, t_{S}, of the switching transition is used for the voltage across the switch to rise to the DC voltage and that the current decays to zero from the initial value during the second half. The switching energy thus results as

$$E_{\mathrm{off}} = \frac{1}{2} V_{\mathrm{CE}} I_{\mathrm{C}} \cdot t_{\mathrm{S}}, \tag{5}$$

and the involved switching characteristics are given by

$$\frac{di_{\mathrm{C}}}{dt} = \frac{I_{\mathrm{C}}}{t_{\mathrm{S}}/2} \quad \text{and} \quad \frac{dv_{\mathrm{CE}}}{dt} = \frac{V_{\mathrm{CE}}}{t_{\mathrm{S}}/2}. \tag{6}$$

The turn-on process can be described accordingly.

By specifying several switching durations, t_{S}, different virtual SiC devices are modeled. The resulting specifications are processed using the same optimization procedure as in Section II. This results in η-ρ Pareto fronts for different switching characteristics, which are shown in Fig. 8.

It can clearly be seen that a SiC two-level solution could only outperform a Si multilevel solution if the SiC device provided di/dt and dv/dt values in extreme order of magnitudes such as 20 kA/µs and 2 MV/µs, respectively. Considering a commutation stray inductance of only 100 nH, this results in a 2 kV voltage overshoot; a common mode capacitance of 10 pF would result in peak common mode currents of 20 A.

These considerations clearly indicate that SiC technology, at least in the near future, will not supersede the need for cascading converter cells in MV and of course also high voltage applications. On the other hand, significant improvements can be expected from replacing low-voltage Si devices by their SiC counterparts in multilevel systems.

V. Reliability Considerations

The Pareto optimization from Section II indicates that designs featuring a comparatively high number of cascaded cells deliver the best performance. However, high component counts generally lead to reduced reliability. Assuming a constant FIT rate of $\lambda_{\mathrm{Semi}} = 100\,\mathrm{FIT}$ for power semiconductors ($1\,\mathrm{FIT} = 1/10^9\mathrm{h}$), the FIT rate of one converter cell is given by $\lambda_{\mathrm{Cell}} = n_{\mathrm{device}} \lambda_{\mathrm{Semi}}$ [48], where n_{device} denotes the number of power semiconductors per converter cell. Thus, the cumulative reliability function, i. e. the probability of a system with n cascaded cells being operational after t hours, is given by [48]

$$R_{\mathrm{S}}(t) = R_{\mathrm{S,Cell}}(t)^n = \mathrm{e}^{-\lambda_{\mathrm{Cell}} n t}, \tag{7}$$

and the mean time to failure of the system, $MTTF_{\mathrm{S}}$, can for the case of constant FIT rates be described as

$$MTTF_{\mathrm{S}} = \frac{1}{n \lambda_{\mathrm{Cell}}}, \tag{8}$$

which, as expected, illustrates that designs with more cells are less reliable.

However, because of the modular nature of multilevel converter systems, redundancy can easily be implemented. After a brief discussion of the junction temperature's influence on system reliability in the next section, different redundancy concepts and their effect on overall system reliability will be discussed. It is shown that the reliability of modular systems does not suffer from the higher component count, which has already been discussed in the 1990ies [49] for the case of paralleled converter cells and in [50] to some extent for series/parallel structures, since modularity implies the possibility of redundancy and on-line repairability.

A. Reliability vs. Power Density Trade-Off

It is well known and considered by relevant standards [51], [52] that the reliability of power semiconductors strongly depends on the blocking voltage utilization and the junction temperature, T_{J}. The latter offers the possibility to improve reliability by increasing the capability of the cooling system, e. g. the size of the heat sinks.

This is illustrated using the example of a CNB-5 design. According to [52], the base FIT rate at $T_{\mathrm{J}} = 100\,°\mathrm{C}$ has to be scaled by a factor, π_{T}, to account for different junction temperatures:

$$\pi_{\mathrm{T}} = \mathrm{e}^{3480 \cdot \left(\frac{1}{373} - \frac{1}{T_{\mathrm{J}} + 273}\right)} \tag{9}$$

A number of design points for different combinations of f_{S}, L_{F} and T_{J} are generated in the same way as described in

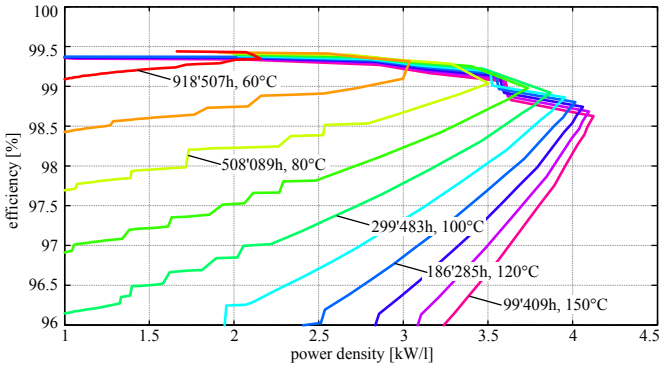

Fig. 9. Reliability vs. power density at different junction temperatures for a CNB-5 design using 1700 V IGBTs and no redundancy. Note that the absolute $MTTF_{\mathrm{S}}$ values depend on the quality of the FIT rate data.

Section II. For lower T_{j} values, the resulting heat sink volumes become larger, resulting in lower power densities. Fig. 9 shows the Pareto fronts for different reliability levels associated with different junction temperatures, illustrating the power density vs. reliability trade-off.

Reliability as a function of junction temperature and in a similar way also of the blocking voltage utilization [51], [52] can thus be regarded as a third dimension in a comprehensive Pareto analysis of the number of cascaded cells.

B. Redundancy

As indicated above, the modular design of CHB and CNB systems allows for easy implementation of cell-level redundancy by adding spare cascaded cells. The system then features k-out-of-n redundancy, which means that the system is up as long as at least k cells are operational. Basically, there are two different concepts for implementing this type of redundancy: standby redundancy, where the reserve cells are not active during normal operation, and active redundancy with load sharing, where all healthy cells are sharing the total system load. These are discussed in the following on the basis of results given in a reliability textbook [48], to which the interested reader is referred for full derivations.

1) Standby redundancy: In this case, the reserve modules are not active but simply in a ready state, which would allow them to immediately start taking over the power share of a broken module. Since in the reserve state the cell's stress level is significantly lower compared to that of cells in operation, the FIT rate in the reserve state is assumed to be zero. The mean time to failure of the complete system under these conditions is given by

$$MTTF_{\mathrm{S}} = \frac{n-k+1}{k\lambda_{\mathrm{Cell}}}. \tag{10}$$

2) Active redundancy with load sharing: Instead of keeping the reserve cells in a waiting state, they could also participate in the system operation, which would reduce the power processed per cell. While this, in turn, reduces the losses and lowers the junction temperature, increasing the reliability of the cells as discussed above, on the other hand the system efficiency might be degraded since a sub-optimal number of cells is used. In any case, the reserve cells' failure rate is not zero anymore but equal to that of all other cells. In addition, the failure rate depends on the number of healthy cells, since as soon as one cell is lost, its share of the total power needs to be taken over by the remaining cells.

Let i be the number of failed cells, i. e. $0 \leq i \leq n-k$ as long as the system is operational. The temperature-dependency of the FIT rate can then be expressed as

$$\lambda_{\mathrm{i}} = \lambda_{\mathrm{Cell}} \pi_{\mathrm{T,i}}, \tag{11}$$

where

$$\pi_{\mathrm{T,i}} = \mathrm{e}^{3480\left(\frac{1}{373}-\frac{1}{T_{\mathrm{j,i}}+273}\right)}, \tag{12}$$

and

$$T_{\mathrm{j,i}} = T_{\mathrm{j,max}} + (T_{\mathrm{j,max}} - T_{\mathrm{A}})\left(\frac{1}{n-i} - \frac{1}{k}\right), \tag{13}$$

with $T_{\mathrm{j,max}}$ being the maximum allowable junction temperature that appears for $i = n-k$, and T_{A} denoting the ambient temperature. The system-level mean time to failure becomes

$$MTTF_{\mathrm{S}} = \sum_{\mathrm{i}=0}^{n-k} \frac{1}{(n-i)\lambda_{\mathrm{Cell}}\pi_{\mathrm{T,i}}}. \tag{14}$$

3) Repairable systems: In reality, a faulty cell in a system would be repaired as soon as possible. Depending on the implementation, this could even be possible as a hot-swap operation without service interruption on system level. Again, based on derivations from [48], the $MTTF_{\mathrm{S}}$ value for a repairable system can be calculated from the following relations, which hold for the assumptions of there being only a single repair crew and no further failures at system down:

$$MTTF_{\mathrm{S,0}} = \frac{1}{v_0} + MTTF_{\mathrm{S,1}} \tag{15}$$

$$MTTF_{\mathrm{S,i}} = \frac{1}{v_{\mathrm{i}}+\mu}\left(1 + v_{\mathrm{i}} MTTF_{\mathrm{S,i-1}} + \mu MTTF_{\mathrm{S,i+1}}\right), \tag{16}$$

$$i = 1, \ldots, n-k-1$$

$$MTTF_{\mathrm{S,n-k}} = \frac{1}{v_{\mathrm{n-k}}+\mu}\left(1 + \mu MTTF_{\mathrm{S,n-k-1}}\right) \tag{17}$$

where

$$v_{\mathrm{i}} = k\lambda_{\mathrm{Cell}} + (n-k-i)\lambda_{\mathrm{Cell,reserve}}. \tag{18}$$

$\lambda_{\mathrm{Cell,reserve}}$ is the failure rate for cells in the reserve state and set to $\lambda_{\mathrm{Cell,reserve}} = 0$ (standby redundancy) here.

4) Discussion: Fig. 10(a) shows $MTTF_{\mathrm{S}}$ values for standby redundancy and several design variants with varying degree of redundancy versus the cost of this redundancy in terms of additionally installed power capability. Fig. 10(b) shows the same but for active redundancy with load sharing, where $T_{\mathrm{j,max}} = 125\,^{\circ}\mathrm{C}$ and $T_{\mathrm{A}} = 50\,^{\circ}\mathrm{C}$ have been assumed. In both cases, $\lambda_{\mathrm{Cell}} = 12 \cdot 100\,\mathrm{FIT}$ is considered, since twelve power semiconductors are present in a NPC cell. This means that the dependence of the FIT rate on the semiconductor type,

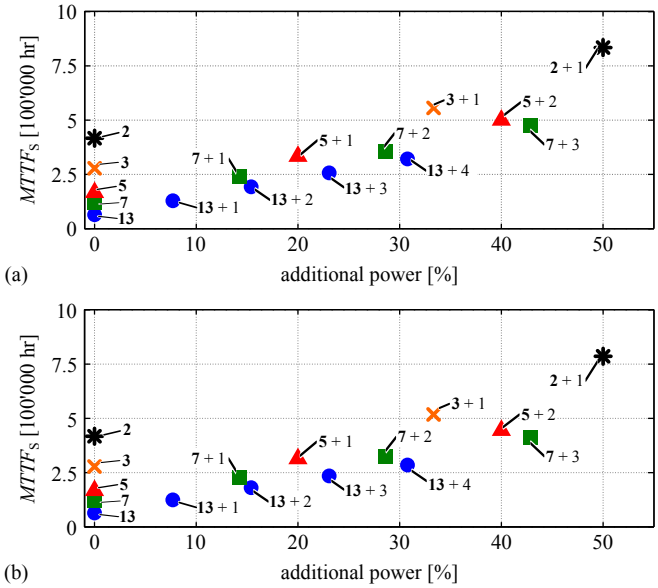

Fig. 10. $MTTF_S$ versus additionally installed power capability for CNB designs with required number of cascaded cells (k, bold) and additional redundant modules for (a) standby redundancy and (b) active redundancy with load sharing.

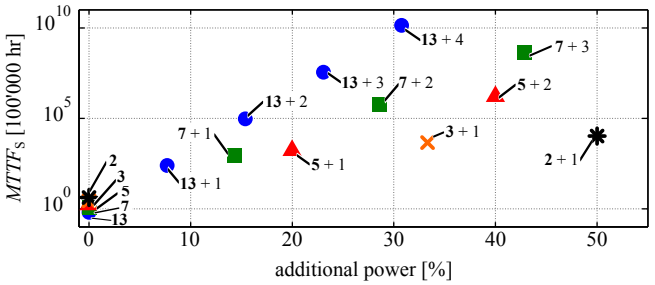

Fig. 11. $MTTF_S$ versus spare power capability for CNB designs with required number of cascaded cells (k, bold) and additional redundant modules of a repairable system with standby redundancy. Note the logarithmic scale of the y-axis.

etc. is not considered here. Note that the absolute $MTTF_S$ values depend on this base FIT rate; the relative differences between designs, however, do not as can directly be seen from the inverse proportionality between $MTTF_S$ and λ_{Cell} in both, (10) and (14).

The most important conclusion to be drawn from the data presented in Fig. 10 is that redundancy can be used to mitigate a decrease in reliability associated with increasing number of cascaded cells: consider for example a CNB-7 design with one additional spare module $(7+1)$ and a CNB-13 design with two spare modules $(13+2)$. For both types of redundancy, the $MTTF_S$ of the CNB-13 solution is almost as high as that of the CNB-7 solution, while the costs to achieve this redundancy levels are also comparable. Of course, the highest reliability in this example is achieved with a CNB-2 design with one spare module—but also at by far the highest costs, since 50 % of the nominal system power have to be added as reserve.

Comparing the two concepts, standby redundancy and active redundancy with load sharing, slightly higher $MTTF_S$ values are achieved with standby redundancy. However, since these differences are only minor, other factors such as for example the feasibility of simultaneously bypassing a faulty cell and turning on a reserve cell and, most prominently, the effect of the non-optimal number of series cells on the efficiency should be carefully taken into consideration for decisions regarding the redundancy concept.

Fig. 11 shows the $MTTF_S$ versus additional power for the case of a *repairable* system with standby redundancy and repair rate $\mu = 1/(7 \cdot 24\,\mathrm{h})$, corresponding to a mean time to repair (MTTR) of one week, which is a rather conservative assumption. Obviously, the reliability is massively improved compared with the non-repairable case discussed above. It is particularly interesting to observe that here the CNB-13 design with two spare cells turns out to be significantly more reliable than the CNB-7 design with one spare cell, again roughly at the same costs. In the first case, after a first cell has failed, two more would have to fail before the repair of the first one is completed in order for the complete system to fail whereas in the second case a single additional failure before completion of repair leads to system down. Under the assumption of independent elements, the latter is much more likely, which corresponds to lower $MTTF_S$ values.

All in all, the above discussion indicates that reliability considerations are not preventing the decision for designs with higher number of cascaded cells, especially as such designs can be superior regarding efficiency and power density as has been shown in Section II.

VI. Conclusion

This paper proposes efficiency versus power density (η-ρ) Pareto analysis to comprehensively asses the question of the optimum number of cascaded converter cells in power electronic systems connected to the MV grid. In addition, a diagram type known from power semiconductor technology has been introduced to compare different multilevel solutions. Since recent advances in SiC technology point towards devices with very high blocking voltages, it has been analyzed what switching characteristics such devices would have to provide in order for a single two-level SiC inverter to be competitive with Si multilevel solutions. The results suggest that SiC technology will not eliminate the need for cascading converter cells in the near future. Furthermore, reliability concerns arising from the high number of components in multilevel systems have been addressed. It has been shown how cell-level redundancy, which is easily implemented due to the modular structure, and repairability drastically reduce the dependency of the system reliability on the number of cascaded converter cells for practical applications.

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