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New Current Control Scheme for the Vienna Rectifier in Discontinuous Conduction Mode

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***Abstract*—The Vienna rectifier (VR) is used in applications that require unidirectional, non-isolated, three-phase AC to DC conversion with constant output voltage and sinusoidal input currents. However, because of the unidirectional topology, the input currents become discontinuous at small output power values. As a consequence, the relationship between rectifier input voltage and duty cycle changes compared to continuous conduction mode. Therefore, if no additional measures are taken, the rectifier input currents will be distorted. This work describes a new control scheme that allows operation of the VR with sinusoidal input currents in discontinuous conduction mode (DCM). The limits of operation are described, concerning maximum mains voltage, maximum midpoint current and minimum resistance to the mains in DCM. Further, the noise emission in DCM is compared to continuous conduction mode (CCM) operation. Finally, the proposed scheme is experimentally verified on a hardware prototype.**

I. Introduction

Three-phase, three-level rectifiers are widely used if constant output voltage and sinusoidal input currents are required. The Vienna Rectifier (VR), originally described in [1], allows the use of 600 V power transistors when operated in 400 V or 480 V three-phase grids. Therefore, a reduction in switching losses is possible, which makes the VR an attractive solution if no input-output isolation and only unidirectional power flow is required. Furthermore, because of the three-level topology of the VR, the volume of the boost inductor is smaller than that of a two-level rectifier with the same amount of current ripple. Usually voltage source rectifiers are controlled using two cascaded control loops. The inner loop controls the boost inductor phase currents and the outer one the output voltage. In continuous conduction mode (CCM) the local average value of the phase voltage at the rectifier input, referred to the output voltage midpoint M is $\langle u_{\bar{k}\mathrm{m}} \rangle = \mathrm{sign}(i_k)(1-d_k)\frac{U_{\mathrm{pn}}}{2}$ with $k = \mathrm{a}, \mathrm{b}, \mathrm{c}$ (see Fig. 1). The rectifier input voltage is therefore proportional to $1-d_k$, where d_k denotes the relative on-time of the switch $\mathrm{S}_{\bar{k}\mathrm{m}\bar{k}}$ of phase k, and each current controller acts on a plant which behaves linearly in good approximation. However, CCM can only be assumed as long as the ripple of the current in a boost inductor is small compared to the phase current fundamental. As soon as the phase current fundamental is less than half of the peak-peak ripple, discontinuous current mode (DCM) occurs. In DCM the relationship between duty-cycle and rectifier input voltage changes and therefore also the plant of the current controller. If this is not taken into account when designing the current controller, distortions in the input currents occur. The problem is illustrated in Fig. 2a and 2b. In a circuit simulation with a switching frequency $f_{\mathrm{s}} = 28\,\mathrm{kHz}$, a boost inductance $L = 50\,\mu\mathrm{H}$, a DC-link voltage $U_{\mathrm{pn}} = 800\,\mathrm{V}$, and a phase-to-phase RMS voltage $U_{\mathrm{n}} = 400\,\mathrm{V}$, the rectifier achieves a THD of 0.22 % at full load (65 kW), disregarding the switching frequency harmonics. In this case, all low frequency current harmonics are below 0.1 % of the fundamental. If the load is reduced to 6.5 kW, DCM is observed, the THD increases to 5.8 % and the 7th current harmonic is 18 % of the fundamental. There are now basically two ways of avoiding distorted input currents. One would be to avoid the occurrence of DCM at all by reducing the ripple at small input current. This could be done actively by increasing the switching frequency or passively by using a non-linear inductance of the boost inductor. The other approach is to find a control scheme that allows operation in DCM, while still ensuring a sinusoidal local average value of the phase currents. In this work the latter approach is taken. First a review of conventional DCM control schemes is given in Sec. II. In Sec. III the proposed control scheme and its operational limits are derived, the scheme is verified using a circuit simulation and the noise emission is compared to that in CCM. Finally, in Sec. IV the control scheme is experimentally verified on a hardware prototype.

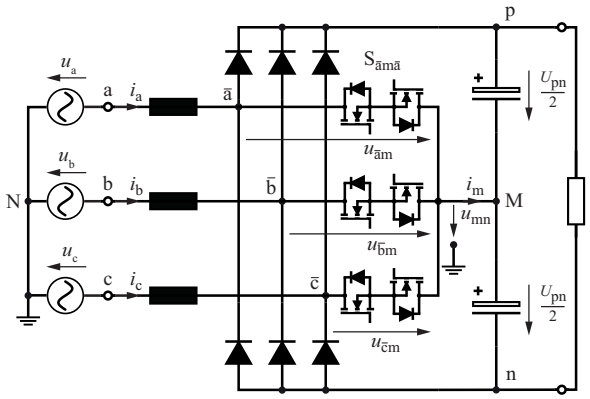


Fig. 1. Simplified circuit schematic of the Vienna Rectifier used for the analysis in this paper (EMI input filter is not shown and not considered in the calculations of this paper).

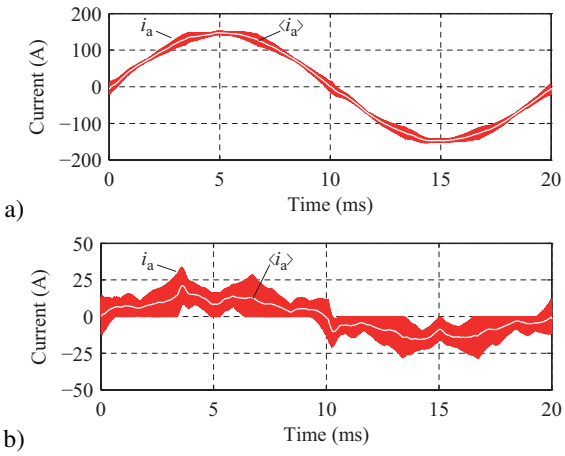


Fig. 2. Current in the boost inductor of phase a, at 65 kW (a) and at 6.5 kW (b). The local average value of the current is indicated as white line. At full load (cf. a) the local average is sinusoidal, if the load is reduced (cf. b), the current becomes partially discontinuous and its average is distorted.

II. Conventional DCM Control Schemes

Two control schemes to operate the VR in DCM are already known. In the first control scheme [2] all switches are turned on and off at the same time (single-switch rectifier control scheme, [3]). The currents have triangular shape but their local average value is not varying sinusoidally. The reason for that is, that the currents rise at a rate proportional to the phase voltages, but drop at different rates, therefore the local average values of the currents are not always proportional to the corresponding phase voltages. This is shown in Fig. 3. However the control is simple because the duty cycle is directly set by the output voltage controller and no current sensors are required. Furthermore, the switch that carries the highest current can be turned off a little sooner or later than the other two switches. This allows to actively balance the DC link voltages.

The second solution, proposed in [4], extends the DCM control loop by an adaptive compensator. The currents in the boost inductors are modeled using an observer and compared to the measured values. The error of the local average of each current is then fed into a PI-controller, whose integral part is inverted at each zero crossing of the current. This way the error voltage of each phase, which is the difference between the voltage set according to the duty cycle and the actually applied voltage because of current discontinuity, can be compensated. However, after a load step the controller takes considerable time, approximately 10 ms, to adapt to the new error voltages. Furthermore, the control scheme relies on current measurements during DCM control. This measurements are not as easy to obtain as in CCM, since the time when the instantaneous value of the current equals its local average is not known in advance. However, it offers the advantage that no change between different control schemes occurs throughout the whole power range.

In the following a new DCM control scheme is introduced that requires no current measurement or control loop, achieves sinusoidal local phase current average values and output voltage balancing.

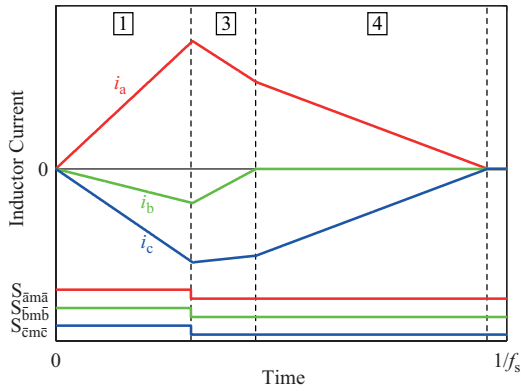


Fig. 3. Currents i_a,i_b,i_c in the boost inductors and control signals of the four quadrant switches during a single switching period T_s at $\varphi = 15\,^\circ$ mains voltage angle with all switches turned on and off at the same time. During state 1 all currents rise at a rate proportional to the according phase voltage. During switching state 3 three diodes are conducting and the current of the phase with minimum phase voltage absolute value drops at the highest rate. As soon as it reaches zero, state 4 begins. Only two diodes remain conducting and the currents are dropping at the same rate until they reach zero.

III. New Sinusoidal Current DCM Control

For the following considerations of the currents in the boost inductors during a single switching cycle T_s it is assumed that the values of the phase voltages show a relation $u_a > 0 > u_b > u_c$ and that all inductor currents are zero at the beginning of the cycle. Since the VR exhibits phase symmetry and bridge symmetry [5] the same considerations can be applied to any other 30 ° section of the mains period.

A. Switching States

State 1: At the start of each switching cycle all switches are turned on and the currents are rising at a rate proportional to the corresponding phase voltage; the duration of the state is defined by the duty cycle D_1. State 2a: If all switches were turned off at the same time, the current with the smallest absolute peak value, in this case i_b, would drop too fast and its local average would therefore be too low. In order to avoid this, the absolute value of i_b has to be increased. This can be achieved by turning-off the switch conducting the current with middle absolute peak value (in this case i_c) first, before turning off the switches conducting the currents with minimum and maximum absolute peak value, i.e. i_b and i_a (see Fig. 4a). The duration of this state 2a is given by the duty cycle D_{2a}, which has to be set such that the local average values of all currents are proportional to the corresponding phase voltages. State 2b: Alternatively, the absolute value of i_b could also be increased by leaving only the switch conducting the current with the smallest absolute value ($S_{\bar{b}m\bar{b}}$) turned on after state 1 (see Fig. 4b). This state 2b can therefore also be used to achieve resistive mains behaviour, concerning the relation of the boost inductor currents local average values and the mains phase voltages. In both states 2a and 2b, a current i_m is flowing into the midpoint M of the DC-link capacitors (Fig. 1). In state 2b the direction of that current equals the direction of the current with the lowest absolute value, in state 2a it is the opposite. Therefore, the choice between states 2a and 2b offers a degree of freedom which can be used to balance the voltage

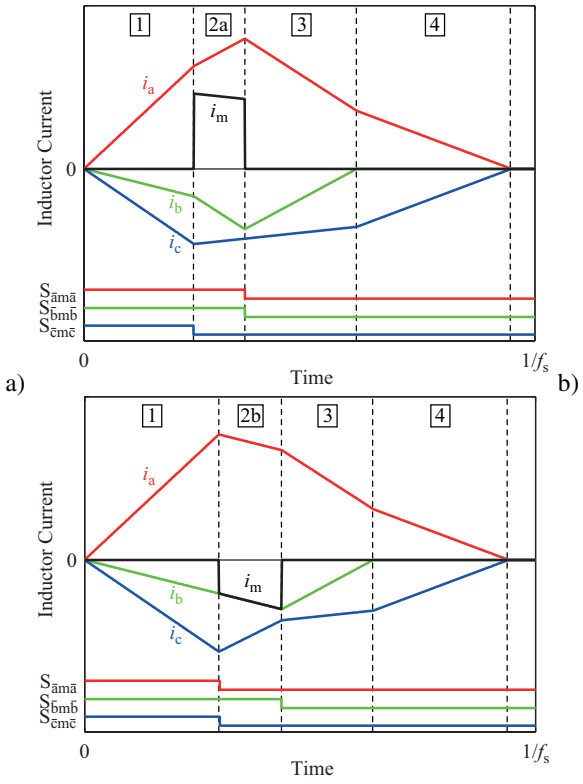


Fig. 4. Currents i_a, i_b, i_c in the boost inductors, current into the DC-link midpoint i_m, and control signals of the four quadrant switches during a single switching cycle T_s using state 2a (a) and 2b (b) to achieve resistive behaviour.

sharing between the upper and lower DC-link capacitor. The duration of state 2b is given by the duty cycle D_{2b} which has to be selected such that the local average values of the boost inductor currents are proportional to the corresponding phase voltage. State 3: After state 2a or 2b is finished all currents are flowing through the free-wheeling diodes. The duration of state 3 is defined by the time the current i_b takes to reach zero. State 4: During state 4 only two diodes remain conducting, the duration of the state is given by the time it takes until the currents reach zero. After state 4 the currents remain zero until the next switching period begins again with state 1. The switching cycles are repeated at a constant frequency f_s as in CCM.

B. Calculation of the Duty-Cycles

The described five switching states, their equivalent circuits, the current changes Δi_{kn} in each phase k in each state n and the duration T_n of each state are given in Tab. I. Using these equations the local average values of the currents in the boost inductors are calculated as

$$\langle i_k \rangle = \frac{1}{2}\left(\Delta i_{k1}T_1 + (\Delta i_{k1} + \Delta i_{k2x})T_{2x} + (\Delta i_{k1} + \Delta i_{k2x} + \Delta i_{k3})T_3 + (\Delta i_{k1} + \Delta i_{k2x} + \Delta i_{k3} + \Delta i_{k4})T_4\right) f_s \quad (1)$$

with x being either a or b. In order to obtain sinusoidal input currents the rectifier has to act like a symmetric three-phase resistive load concerning the local current average values $\langle i_k \rangle$. Therefore, it is required that for each phase k the resistance $r_k = \frac{u_k}{\langle i_k \rangle}$ is the same, i.e. $r_k = r$. Assuming $\sum_k u_k = 0$ and $\sum_k i_k = 0$, this condition is guaranteed if the resistance of two phases is the same. Therefore, solving the equation

$$\frac{u_a}{\langle i_a \rangle} = \frac{u_b}{\langle i_b \rangle} \quad (2)$$

with the local average values of the currents inserted from (1), yields the value of D_{2a} or D_{2b} that is necessary for resistive behaviour, i.e. sinusoidal input currents after filtering switching frequency components. The value of D_1 follows by inserting the values D_{2a} or D_{2b} obtained from (2) into any of the equations $r = \frac{u_k}{\langle i_k \rangle}$ for a required resistance r at the mains side. Analytic expressions for the duty cycles have been obtained for both switching patterns a and b. Using the expressions

$$D_0 = \sqrt{\frac{f_s L}{r}}, \quad (3)$$

$$m_{max} = \frac{2 \cdot \max(|u_a|, |u_b|, |u_c|)}{U_{pn}}, \quad (4)$$

$$m_{min} = \frac{2 \cdot \min(|u_a|, |u_b|, |u_c|)}{U_{pn}} \quad (5)$$

the duty cycles for a switching cycle of either pattern a or b can be calculated using the equations in Tab. II. Using these analytical expressions is possible in a circuit simulation, but because of the complexity of the expressions for pattern a, a realization in hardware is only possible using look-up tables. For ideal mains voltages

$$\begin{aligned} u_a &= \hat{U}\cos(\varphi) \\ u_b &= \hat{U}\cos(\varphi + 120°) \\ u_c &= \hat{U}\cos(\varphi + 240°) \end{aligned}$$

with the mains angle φ and $\hat{U} = M \cdot \frac{U_{pn}}{2}$ with the modulation index M, the values of the duty cycles are shown for the first 30 ° section of the mains period in Fig. 5. The pattern is mirrored and repeated throughout all other 30 ° sections of the mains period. It is observed that the duty cycle functions are continuous and that they are therefore well suited for an implementation if one uses look-up tables.

C. Limits of Operation

It has been shown that the proposed control scheme allows the operation of the VR in DCM, maintaining sinusoidal currents and output voltage balancing. In this section the limiting values are investigated that define the application range of the control scheme.

1) Maximum input voltage: If the rectifier is operated in CCM, the maximum input voltage depends on the third harmonic modulation function which is used to maximize the linear modulation range [6]. Ideally a maximum modulation index of $M_{max} = \frac{2}{\sqrt{3}} \approx 1.15$ can be achieved. It is observed that for high values of the modulation index, the duty cycle functions of Tab. II result in negative values. Numerical investigations show that all duty cycle values are valid for modulation indices up to $M_{max} \approx 1.12$.

TABLE I. SWITCHING STATES OF THE PROPOSED SINUSOIDAL CURRENT DCM CONTROL SCHEME, ASSUMING $u_\mathrm{a} > 0 > u_\mathrm{b} > u_\mathrm{c}$.

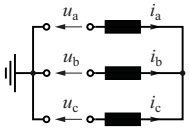
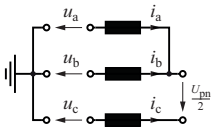
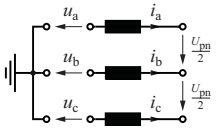
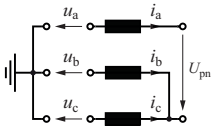
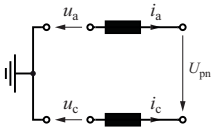
Switching State	$S_{\bar{a}m\bar{a}}$,$S_{\bar{b}m\bar{b}}$,$S_{\bar{c}m\bar{c}}$	Equivalent Circuit	Changes of inductor currents	Duration of state
1	1 - 1 - 1		$\Delta i_{\mathrm{a}1} = \frac{T_1}{L} \cdot u_\mathrm{a}$ $\Delta i_{\mathrm{b}1} = \frac{T_1}{L} \cdot u_\mathrm{b}$ $\Delta i_{\mathrm{c}1} = \frac{T_1}{L} \cdot u_\mathrm{c}$	$T_1 = \frac{D_1}{f_\mathrm{s}}$
2a	1 - 1 - 0		$\Delta i_{\mathrm{a}2\mathrm{a}} = \frac{T_{2\mathrm{a}}}{L} \cdot (u_\mathrm{a} - \frac{U_\mathrm{pn}}{6})$ $\Delta i_{\mathrm{b}2\mathrm{a}} = \frac{T_{2\mathrm{a}}}{L} \cdot (u_\mathrm{b} - \frac{U_\mathrm{pn}}{6})$ $\Delta i_{\mathrm{c}2\mathrm{a}} = \frac{T_{2\mathrm{a}}}{L} \cdot (u_\mathrm{c} + \frac{U_\mathrm{pn}}{3})$	$T_{2\mathrm{a}} = \frac{D_{2\mathrm{a}}}{f_\mathrm{s}}$
2b	0 - 1 - 0		$\Delta i_{\mathrm{a}2\mathrm{b}} = \frac{T_{2\mathrm{b}}}{L} \cdot (u_\mathrm{a} - \frac{U_\mathrm{pn}}{2})$ $\Delta i_{\mathrm{b}2\mathrm{b}} = \frac{T_{2\mathrm{b}}}{L} \cdot u_\mathrm{b}$ $\Delta i_{\mathrm{c}2\mathrm{b}} = \frac{T_{2\mathrm{b}}}{L} \cdot (u_\mathrm{c} + \frac{U_\mathrm{pn}}{2})$	$T_{2\mathrm{b}} = \frac{D_{2\mathrm{b}}}{f_\mathrm{s}}$
3	0 - 0 - 0		$\Delta i_{\mathrm{a}3} = \frac{T_3}{L} \cdot (u_\mathrm{a} - \frac{2U_\mathrm{pn}}{3})$ $\Delta i_{\mathrm{b}3} = \frac{T_3}{L} \cdot (u_\mathrm{b} + \frac{U_\mathrm{pn}}{3})$ $\Delta i_{\mathrm{c}3} = \frac{T_3}{L} \cdot (u_\mathrm{c} + \frac{U_\mathrm{pn}}{3})$	$T_3 = -\frac{L \cdot (\Delta i_{\mathrm{b}1} + \Delta i_{\mathrm{b}2\mathrm{x}})}{u_\mathrm{b} + \frac{U_\mathrm{pn}}{3}}$
4	0 - 0 - 0		$\Delta i_{\mathrm{a}4} = \frac{T_4}{2L} \cdot (u_\mathrm{a} - u_\mathrm{c} - U_\mathrm{pn})$ $\Delta i_{\mathrm{b}4} = 0$ $\Delta i_{\mathrm{c}4} = \frac{T_3}{2L} \cdot (u_\mathrm{c} - u_\mathrm{a} + U_\mathrm{pn})$	$T_4 = -\frac{2L \cdot (\Delta i_{\mathrm{a}1} + \Delta i_{\mathrm{a}2\mathrm{x}} + \Delta i_{\mathrm{a}3})}{u_\mathrm{a} - u_\mathrm{c} - U_\mathrm{pn}}$

TABLE II. DUTY-CYCLES FOR RESISTIVE BEHAVIOUR OF THE RECTIFIER IN DCM.

Pattern a	$D_{1\mathrm{a}}$	$=$	$\frac{D_0 \cdot \left((9m_\mathrm{min}^2 + 6m_\mathrm{min} + 2)m_\mathrm{max} - (6m_\mathrm{min} + 2)m_\mathrm{max}^2 - 3m_\mathrm{min}^3 - 4m_\mathrm{min}^2\right)}{\sqrt{y}}$
	$D_{2\mathrm{a}}$	$=$	$\frac{D_{1\mathrm{a}} \cdot (9m_\mathrm{min}^2 m_\mathrm{max} - 2m_\mathrm{min}^2 - 6m_\mathrm{min} m_\mathrm{max}^2 + 4m_\mathrm{max} m_\mathrm{min} - 3m_\mathrm{min}^3 - \sqrt{x})}{(3m_\mathrm{min}^3 - 9m_\mathrm{min}^2 m_\mathrm{max} + 4m_\mathrm{min}^2 + 6m_\mathrm{min} m_\mathrm{max}^2 - 6m_\mathrm{max} m_\mathrm{min} + 2m_\mathrm{max}^2 - 2m_\mathrm{max})}$
	x	$=$	$(2m_\mathrm{max} - 2 - m_\mathrm{min})m_\mathrm{min}(3m_\mathrm{min} - 2)(2m_\mathrm{max} - m_\mathrm{min})(m_\mathrm{max}^2 - m_\mathrm{min}^2)$
	y	$=$	$3m_\mathrm{min}^5 + (24m_\mathrm{max}^2 - 23m_\mathrm{max} + 2)m_\mathrm{min}^3 + (20m_\mathrm{max}^2 - 8m_\mathrm{max} - 12m_\mathrm{max}^3)m_\mathrm{min}^2 +$
			$(\sqrt{x} - 4m_\mathrm{max}^3 + 6m_\mathrm{max}^2)m_\mathrm{min} + m_\mathrm{max}(\sqrt{x} + 2m_\mathrm{max} - 2m_\mathrm{max}^2) + (7 - 15m_\mathrm{max})m_\mathrm{min}^4$
Pattern b	$D_{1\mathrm{b}}$	$=$	$D_0\sqrt{2 - 2m_\mathrm{max} + m_\mathrm{min}}$
	$D_{2\mathrm{b}}$	$=$	$D_0\sqrt{2 - 3m_\mathrm{min}} - D_{1\mathrm{b}}$

2) Minimum resistance R_min: Since the rectifier is operating at constant switching frequency, the total time T for all states is limited to

$$T = T_1 + T_{2x} + T_3 + T_4 < \frac{1}{f_\mathrm{s}}. \tag{6}$$

Since the slopes of the currents are defined by the voltages (and the inductance of the boost inductors), the peak value of the current and therefore the minimum resistance which can be emulated for the mains considering local phase current average values is limited. The lowest resistance r_min is normalized as $r_\mathrm{min} = r_\mathrm{min,p.u.} \cdot R_0$ using a base resistor $R_0 = f_\mathrm{s}L$, determined by the switching frequency and the boost inductance. The dimensionless value $r_\mathrm{min,p.u.}$ is only depending on the relative values of the phase voltages with maximum and minimum absolute value. It can be calculated by solving (6). For a switching cycle the minimum relative resistance is

$$r_\mathrm{min,p.u.,b} = \frac{4}{2 + m_\mathrm{min} - 2m_\mathrm{max}} \tag{7}$$

with m_max, m_min as defined in (5) and (4). It is possible to find an analytic expression for $r_\mathrm{min,p.u.,a}$ for pattern a using symbolic math software, however, the result is too complicated to be shown here. Instead it shall be mentioned that numerical investigations reveal

$$r_\mathrm{min,p.u.,a} < 1.1 r_\mathrm{min,p.u.,b}. \tag{8}$$

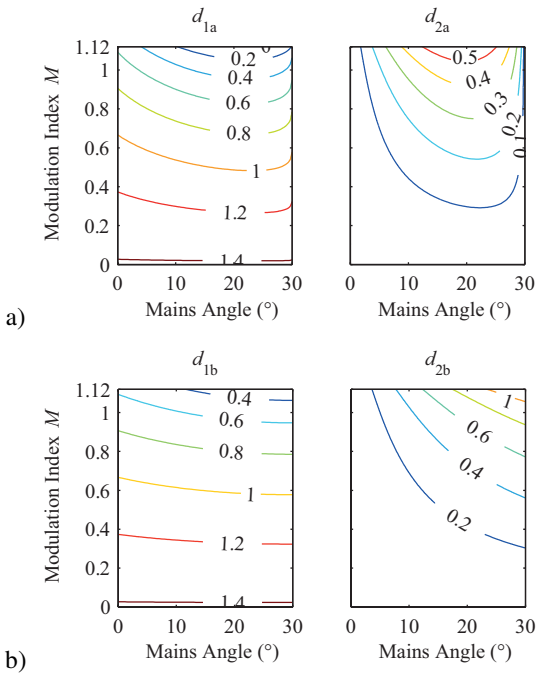


Fig. 5. Relative duty cycles $d_k = \frac{D_k}{D_0}$ for resistive behaviour for a switching cycle using switching state 2a (a) and for a switching cycle using switching state 2b (b).

Therefore the local minimum resistance which allows DCM with both patterns a and b can be approximated as

$$r_{\mathrm{min,p.u.}} \approx \frac{4.4}{2 + m_{\mathrm{min}} - 2m_{\mathrm{max}}}. \tag{9}$$

However, one is usually only interested in the minimum resistance which is achievable with both patterns a and b throughout the whole mains period at a certain modulation index M. This value,

$$R_{\mathrm{min,p.u.}}(M) = \max_{\varphi \in [0°, 30°]} (r_{\mathrm{min,p.u.,a}}(M, \varphi), r_{\mathrm{min,p.u.,b}}(M, \varphi)), \tag{10}$$

is shown in Fig. 6. The minimum resistance which is achievable in DCM marks the border for the phase current controllers to switch to DCM. To avoid that the controller constantly switches between CCM and DCM a hysteresis has to be implemented, so that DCM is only entered if the voltage controller requires a resistance of, e.g. $2R_{\mathrm{min,p.u.}}$, and CCM is only re-entered if the required resistance drops below $R_{\mathrm{min,p.u.}}$. Using such a hysteresis for the selection of the current control mode requires that the operating ranges for DCM and CCM are overlapping. That is actually the case since at the value $R_{\mathrm{p.u.}} = R_{\mathrm{min,p.u.}}$ the current ripple in DCM is approximately twice as high than it is in CCM. Therefore operation in CCM with satisfactory input current quality is possible for emulated mains resistance values up to $2R_{\mathrm{min,p.u.}}$.

3) Maximum global midpoint current $I_{\mathrm{m,max}}$: Throughout the mains period (globally), the VR is able to supply an average current I_m into the midpoint of the output voltage. In CCM the amount of current that can be supplied is proportional to the phase current amplitude and reduces with increasing modulation index [7]. At a modulation index $M = 1$ approximately

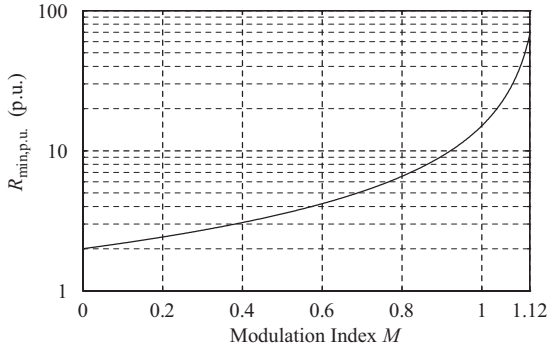


Fig. 6. Minimum relative resistance that can be emulated for the mains throughout the whole mains period using the DCM patterns a or b.

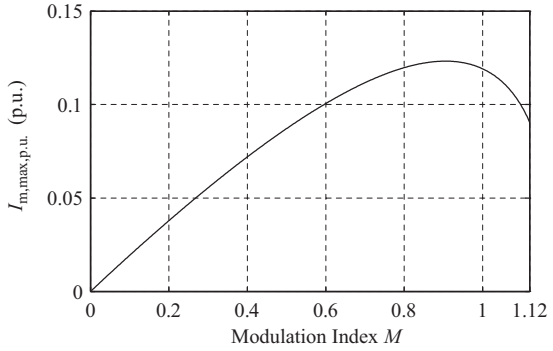


Fig. 7. Relative maximum midpoint current global average value $I_{\mathrm{m,max,p.u.}}$, which is the maximum midpoint current global average value that can be supplied into the midpoint of the DC-link relative to the phase current fundamental RMS value.

45 % of the phase rms current amplitude can be supplied into the midpoint. In DCM there is also current supplied to the midpoint during states 2a and 2b. The maximum positive midpoint current is generated if state 2a is always used while the phase voltage with the smallest absolute value is negative and state 2b is always used while the phase voltage with the smallest absolute value is positive. The global (mains period related) average current $I_{\mathrm{m,max}}$ which is then fed into the midpoint during one mains period is normalized with the RMS value I_{p} of the phase current fundamental as base. The resulting maximum relative midpoint current $I_{\mathrm{m,max,p.u.}} = \frac{I_{\mathrm{m,max}}}{I_{\mathrm{p}}}$ is shown in Fig. 7 as a function of the modulation index M. It is observed that the maximum midpoint current for modulation indices in the range of $M \in [0.6, 1.1]$ amounts to at least 10 % of the phase current rms value. This is substantially less than the value which is possible in CCM (cf. [7]), but more than enough to cover asymmetric leakage currents and to recover from transient unbalances.

D. Simulated Waveforms

The proposed control scheme is demonstrated using an idealized circuit simulation of the VR for a phase-to-phase RMS voltage of $U_{\mathrm{n}} = 400\,\mathrm{V}$, a DC-link voltage of $U_{\mathrm{pn}} = 800\,\mathrm{V}$, a switching frequency of $f_{\mathrm{s}} = 28\,\mathrm{kHz}$, a boost inductance of $L = 50\,\mu\mathrm{H}$ and a resistance emulated for the mains of $R = 40\,\Omega$, corresponding to an input power of $P_{\mathrm{n}} = 4\,\mathrm{kW}$. The differential mode (DM) voltage of the rectifier phase a,

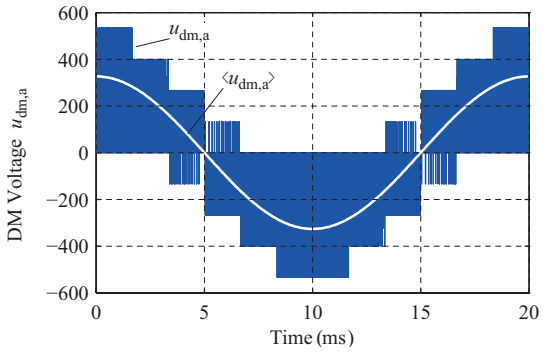


Fig. 8. Simulated DM phase voltage $u_{\mathrm{dm,a}}$ of a VR operating in DCM and its local average $\langle u_{\mathrm{dm,a}} \rangle$.

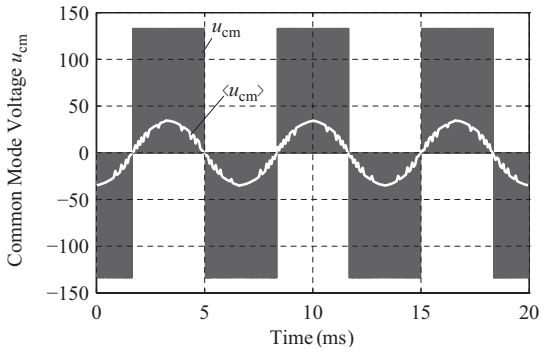


Fig. 9. Simulated CM voltage $u_{\mathrm{cm}} = \frac{u_{\bar{a}\mathrm{m}}+u_{\bar{b}\mathrm{m}}+u_{\bar{c}\mathrm{m}}}{3} = -u_{\mathrm{mn}}$ of a VR operating in DCM and its local average value $\langle u_{\mathrm{cm}} \rangle$ over two switching cycles.

$u_{\mathrm{dm,a}} = u_{\bar{a}\mathrm{m}} - u_{\mathrm{cm}}$ with $u_{\mathrm{cm}} = \frac{u_{\bar{a}\mathrm{m}}+u_{\bar{b}\mathrm{m}}+u_{\bar{c}\mathrm{m}}}{3} = -u_{\mathrm{mn}}$ is shown in Fig. 8. It is observed that other than in CCM the DM voltage always becomes zero during a switching period which causes higher DM noise (compare to CCM DM voltage waveform as shown in [8]). However, the common mode (CM) voltage u_{cm} (Fig. 9 is substantially reduced compared to CCM (compare [8]), and its local average is almost sinusoidal, with three times the mains frequency. The total power of the switching frequency harmonics is therefore partitioned differently into CM and DM parts than in CCM operation. The simulated current waveform in the boost inductor of phase a is shown in Fig. 10, indicating clearly a sinusoidal local average value. In the simulation the output voltages are balanced using bang-bang control, i.e. the control always selects either pattern a or b depending on which one results in a midpoint current that compensates the voltage unbalance between the two output capacitors. If no midpoint current has to be supplied to the output, the average of the midpoint current over two switching cycles is almost zero as can be seen in Fig. 11. The simulation shows that the calculated duty cycles in fact allow sinusoidal currents in DCM, after filtering switching frequency components. However, the proposed scheme results in an increased DM component of the rectifier input voltages, but reduces the CM component. Using the two states 2a and 2b alternatively depending on the sign of the voltage difference between the two output voltages, allows to reduce the low frequency component of the midpoint current virtually to zero. Since the values of the midpoint current of state 2a and state 2b are not the same, the switching patterns a and b will be used with a ratio other than 1:1. However one could also use both states in one cycle (1-2a-2b-3-4); this way the average of the midpoint current during one switching period could be set to zero or to a defined value. An analytic solution for the required duty cycles in this case was not successful. Solving for the duty-cycles numerically would be possible, but would result in a look-up table for each duty cycle with the desired value of midpoint current as third dimension. However, since the DCM control is only used for low power values, the magnitude of the midpoint current in DCM is not directly relevant for the dimensioning of the output capacitor.

E. Noise Emission

Contrary to the operation in CCM, all switches are turned on at the same time if the proposed DCM control scheme is

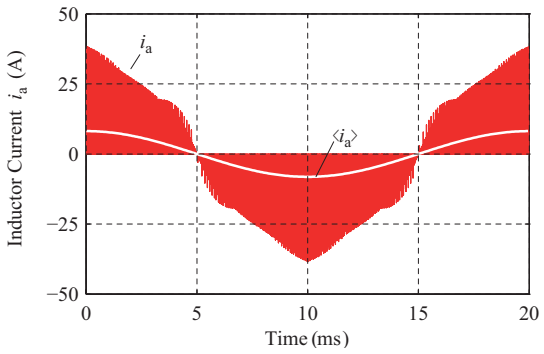


Fig. 10. Simulated current i_{a} in the boost inductor of phase a of a VR operating in DCM and its local average $\langle i_{\mathrm{a}} \rangle$.

used. Therefore higher differential mode (DM) noise emission is expected. On the other hand lower common mode (CM) noise should be observed since the high frequency CM voltage amplitude in DCM is lower by approximately a factor of 3 compared to CCM. For the design of the input filter the noise as measured with an EMI test receiver is relevant. Therefore, for the comparision of the noise levels in CCM and DCM, the DM and CM noise parts of the simulated rectifier input voltages are separately fed into a simulated [9] peak detection test receiver according to CISPR11 [10]. The

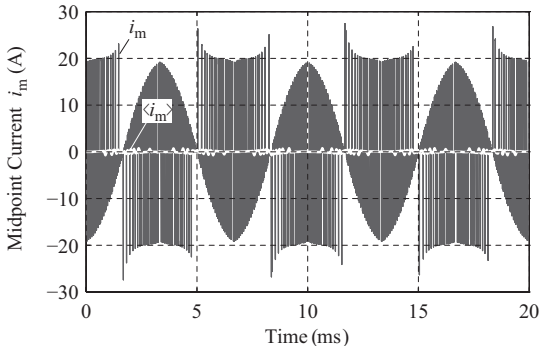


Fig. 11. Simulated midpoint current i_{m} of a VR operating in DCM and its local average value $\langle i_{\mathrm{m}} \rangle$ over two switching cycles.

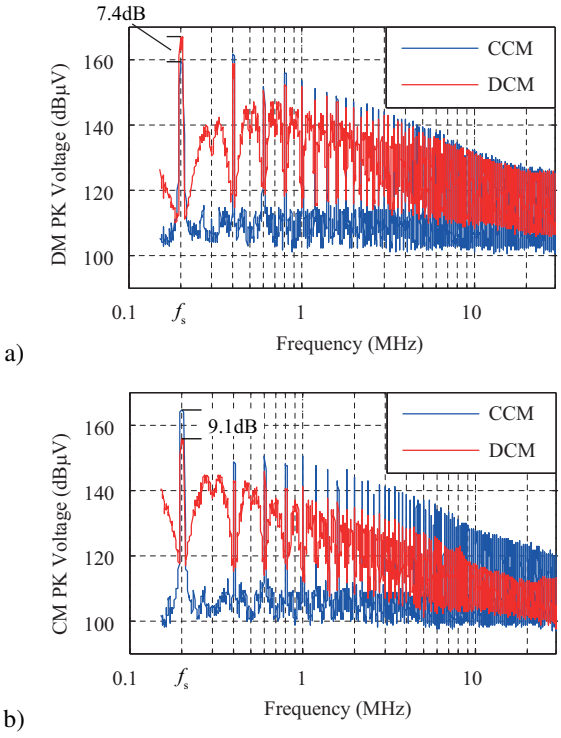


Fig. 12. Simulated noise emission detected with a CISPR11 peak receiver for the VR operating in CCM (blue) and in DCM (red). The DM noise with peak (PK) detection is shown in (a). It is observed that the DM noise in DCM at switching frequency is higher than in CCM. However, the noise levels at higher frequencies in DCM are the same or a little lower than in CCM. The CM noise with PK detection is shown in (b). It is shown that the CM noise level in DCM is lower than in CCM at all frequencies.

switching frequency of the simulated circuit is set to 200 kHz, so that the full PWM spectrum is shown by the CISPR detector. The resistance that the rectifier applies to the mains is set to the lowest value ($R_{\min}$) which represents the case of highest noise emission. Both switching patterns a and b are used to balance the output voltage using bang-bang control. The resulting noise spectra are shown in Fig. 12. It is confirmed that in DCM the DM noise is 7.4 dB higher at switching frequency than in CCM. At higher frequencies the DM noise levels in DCM and CCM are comparable. On the other hand, the CM noise level in DCM is lower by 9.1 dB at all frequencies compared to CCM. Therefore, if the switching frequency is less than 150 kHz, which is the lowest frequency for which CISPR defines noise emission limits, one can operate the rectifier in DCM using the same EMI filter as designed for CCM. If this is not the case, one has to increase the DM attenuation of the filter by $\approx$ 7.4 dB or increase the switching frequency in DCM to obtain higher filter attenuation.

IV. Experimental Verification

The simulated waveforms presented in Sec. III-D are generated using a simplified circuit of the VR without EMI input filter, employing idealized switching devices and inductors. Furthermore, the duty cycles in the simulation are calculated using the exact expressions given in Tab. II. In order to show that the proposed control scheme also works on real converter systems the DCM control scheme has been implemented on a

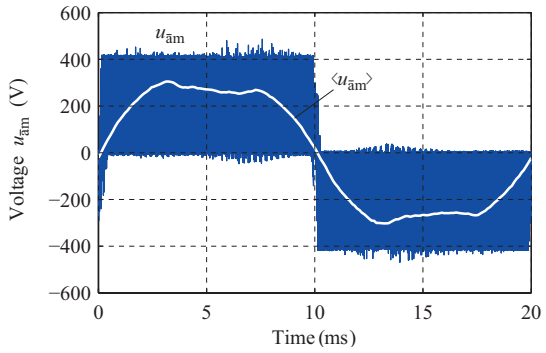


Fig. 13. Measured bridge-leg voltage $u_{\bar{a}m}$ of the VR and its local average value $\langle u_{\bar{a}m} \rangle$.

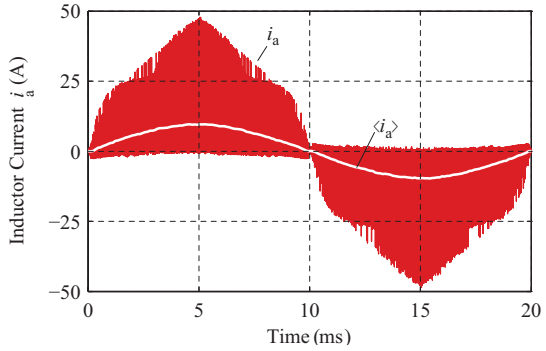


Fig. 14. Measured current i_a in the VR boost inductor of phase a and its local average value $\langle i_a \rangle$. Small negative current values are caused by the reverse recovery of the free-wheeling diodes.

65 kW VR prototype operating at 28 kHz switching frequency. The system is shown in Fig. 16. The boost inductors of the prototype use amorphous cut-cores with air gaps, therefore good linearity of the inductance is expected. The measurements are performed with 800 V DC-link voltage at a three-phase mains voltage of 400 V phase-to-phase RMS with a load of 4300 W at the DC-link. The voltage from rectifier input to the output midpoint M $u_{\bar{a}m}$ is shown in Fig. 13. Its local average reveals the third harmonic component of the midpoint voltage. The measured current in the boost inductor of phase a is shown in Fig. 14. If current components above 9 kHz are removed, the THD of the current in the boost inductor is 0.8 %. The THD of the rectifier input current, shown in Fig. 15, is improved by the EMI filter to 0.3 %. The control is implemented on a TI TMS320F28335 floating point DSP using look-up tables. Four tables are used that contain the values of the relative duty-cycles $d_{1a} = \frac{D_{1a}}{D_0}$, $d_{2a} = \frac{D_{2a}}{D_0}$, $d_{1b} = \frac{D_{1b}}{D_0}$, and $d_{2b} = \frac{D_{2b}}{D_0}$. The tables have 7 rows for $m_{\min} = 0..0.1..0.6$ and 12 columns for $m_{\max} = 0..0.1..1.1$. The relative duty cycles are stored with a precision of 8 bits. In total the look-up tables therefore add up to only 337 Bytes. However, in order to be able to reach the stated values of THD, bilinear interpolation has to be applied. The normalization base $D_0 = \sqrt{\frac{f_s L}{r}}$ is calculated directly on the DSP, although another 1D look-up table for applicable values of $\sqrt{r}$ could also be used.

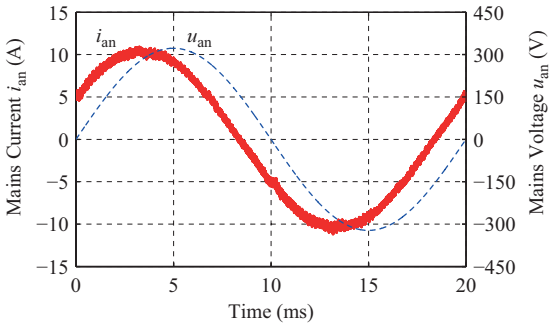


Fig. 15. Measured current i_{an} of the VR (at the mains side of the EMI input filter) and the mains phase voltage u_{an}. Because of the low power level, the EMI input filter causes a relatively high capacitive phase shift between current and mains phase voltage. (A total of 50 μ F filter capacity per phase causes a capacitive RMS phase current of 3.6 A. At full load the phase-shift between phase voltage and current is therefore less than $\approx 2\,^{\circ}$, at low power levels the phase shift increases.)

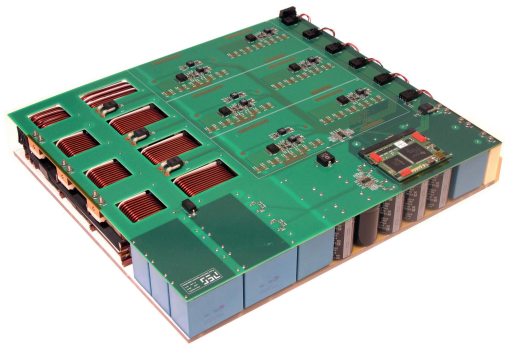


Fig. 16. 65 kW/28 kHz VR prototype used for the measurements to verify the proposed DCM control scheme. width × length × height = 33.6 cm × 37.4 cm × 5.4 cm (13.2 in × 14.7 in × 2.13 in), power density $\varrho = 9.56\,\mathrm{kW/dm^3}$ ($157\,\mathrm{W/in^3}$)

V. Conclusion

A new way to control the Vienna Rectifier with discontinuous phase currents has been proposed. The control requires no current sensing, offers output voltage balancing and - other than simpler DCM control concepts - sinusoidal currents, after filtering switching frequency components. If the noise level at switching frequency is not limited, which is usually the case for switching frequencies $f_s < 150\,\mathrm{kHz}$, the scheme can be used with an EMI input filter that was designed for CCM operation. Although the functions to calculate the duty-cycles can be expressed analytically, one would rather implement them in hardware using look-up tables. Measurements on a prototype have shown that a THD of the input current of 0.3 % is possible using 337 Bytes of look-up tables and bilinear interpolation.

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