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# The Triple Buck Converter – An Efficient Low-Distortion Switch-Mode Power Amplifier Topology

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# Triple buck converter – an efficient low-distortion switch-mode power amplifier topology

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**Abstract:** A switch-mode power amplifier topology that can achieve both a high conversion efficiency and low-output signal distortion is introduced. Such systems are desirable for ultra-high precision amplifiers that, for example, drive actuators in nanometre-accuracy mechatronic positioning applications in integrated semiconductor manufacturing. An efficient Class-D power stage, which is limited in output signal quality due to its inherent half-bridge interlock time, is combined through a magnetically coupled inductor with a dual buck conversion stage that does not require interlock time and, due to its circulating bias current that defines the half-bridge switching waveforms, achieves very low-harmonic output signal distortion. The control system can seamlessly adjust the current sharing of the two converter stages such that overall conversion efficiencies over 95% and output total harmonic distortion values below −100 dB are achievable at power levels up to several kilowatts. Detailed computer simulations demonstrate the feasibility of the concept.

## 1 Introduction

Low-distortion power converters/amplifiers are required in numerous industrial and medical applications such as nanometre-precision positioning or magnetic resonance imaging. The systems must reproduce control signals with highly linear transfer characteristics such that the output voltages or currents are provided with low total harmonic distortion (THD); values below −100 dB must be reached for the most demanding applications, as posed by positioning systems in the integrated semiconductor manufacturing industry [1, 2]. The amplifiers are regularly designed for output powers of several kilowatts and output voltages ranging from 48 V into the kilovolt range, as an actuator or gradient coil currents must often be controlled with high dynamics.

The Class-D power amplifier topology, essentially comprising one or several (paralleled, interleaved) half-bridge power stages, is commonly employed due to its low-power conversion losses. However, the half-bridge interlock/dead time, which is the time interval required between subsequent switching actions of the half-bridge transistors during which both devices are turned off to prevent a DC-link short circuit, significantly deteriorates the achievable output signal THD [3]. Even with interlock times below 50 ns, the THD of Class-D amplifiers is often limited to values higher than −90 dB [2].

The dual buck (DB) power stage alleviates this drawback of the Class-D topology [1, 2, 4]. Fig. 1 illustrates the DB converter power circuit. The key characteristics of the system are the two individual half-bridges and the fact that the half-bridge currents are controlled as exemplarily drawn in Fig. 1*b*. By introducing a circulating bias current $I_B$ between the two half-bridges, their current polarities are rendered unidirectional: $i_{1,2}(t) = i_o(t)2 \pm I_B$ and a diode instead of a second half-bridge transistor can be employed. This eliminates distortion components related to dead time and renders the half-bridge switching actions more uniform across varying output currents, as each half-bridge current is dominated by the (constant) bias current $I_B$ [1, 2]. Note that $I_B$ must be selected in consideration of the expected peak output current amplitudes $\hat{i}_o$ always to ensure current unidirectionality.

The two half-bridge currents $i_1$ and $i_2$ of the DB stage can be characterised by their common-mode (CM) and differential-mode (DM) components: $i = i_{CM} = i_1 + i_2$ and $i_{DM} = i_1 - i_2$. Note that $i_{DM}$ characterises the circulating bias current between the two DB half-bridges and $i_{CM}$ is the effective output current (compare Fig. 1*a*).

The bridge-leg diodes can also be replaced by synchronously rectifying transistors. This improves the achievable THD further due to the equal on-state voltage drops of each half-bridge side. The DB topology can reach THD values below −100 dB [2]. However, the half-bridge root-mean-square current amplitudes are given the modulation method shown in Fig. 1*b*, at least by a factor of $\sqrt{3}$ higher than with a conventional, two-phase parallel interleaved Class-D topology that provides an identical output current. This significantly reduces the achievable power conversion efficiency, which, even with modern wide-bandgap semiconductors, is limited to values below 90% (in a 400 V system) [5].

Hence, this work proposes the combination of a Class-D power stage with a DB converter to benefit from the unique characteristics of both systems. The circuit arrangement, denominated as triple buck (TB) converter, is described as follows. Additionally, the feedback control system structure is outlined and computer circuit simulations verify the functionality of the design.

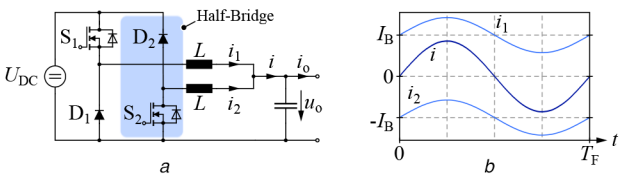


**Fig. 1** *DB converter power circuit and key operating waveforms*

***(a)*** Regular DB power amplifier topology, comprising two interleaved half-bridges, ***(b)*** Typical current waveforms for sinusoidal output. Neglecting any reactive currents caused by the output filter capacitor $i_o = i$. The half-bridge currents $i_{1,2}$ are unidirectional; accordingly, a diode can be employed instead of a second half-bridge transistor and dead-time-related distortion can be avoided

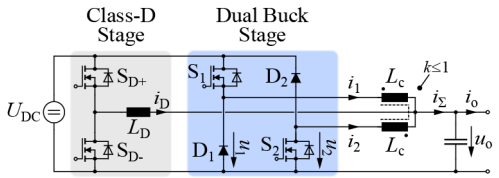


**Fig. 2** *Proposed new TB Topology. The Class-D power stage provides a high conversion efficiency, while the DB stage can generate low-distortion output signals. As for the DB topology, synchronously rectified transistors could be employed instead of the freewheeling diodes $D_1$, $D_2$*

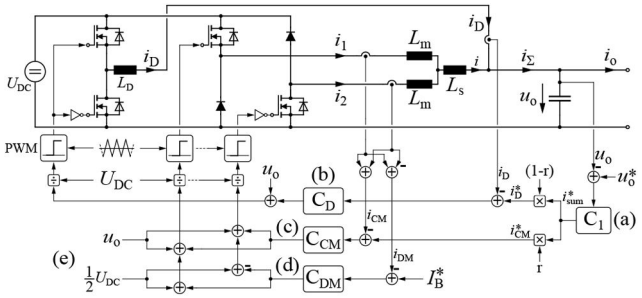


**Fig. 3** *Possible TB feedback control topology, employing cascaded controllers ($C_x$)*

***(a)*** Output voltage control, ***(b)*** Class-D output current ($i_D$) control, ***(c)*** CM current control of the DB stage, ***(d)*** DM bias current control of the DB stage, ***(e)*** Feed-forward compensation

## 2 TB topology

The circuit of the proposed power conversion topology is shown in Fig. 2. Its name arises from the fact that it employs three half-bridges. It combines a regular Class-D with a DB power stage, which are connected through a coupled inductor as shown. Note that in Fig. 2, a single half-bridge is illustrated for both the Class-D and the DB stage, whereas it is possible to interleave several paralleled half-bridges for the individual conversion stages to increase the output power capability and/or to increase the effective switching frequency, hereby mitigating output electromagnetic interference (EMI) filtering efforts.

The key concept behind the TB topology is that significant output power levels, up to several kilowatts, can be provided by the efficient Class-D stage. As this topology introduces considerable distortion components due to its half-bridge interlock time intervals, a DB stage, which can provide the desired output signals (voltage) with low error, is also employed as illustrated.

The magnetically coupled inductors are characterised by their turns ratio $N_1N_2 = 1$, the self-inductances $L_{c1} = L_{c2} = L_c$, the coupling factor $k \in [0, 1]$ and the resulting mutual inductance $M = kL_c$. This transformer fulfils two purposes: first, it provides an impedance for the circulating DM current of the DB stage, which is required for its control and to limit the DM ripple current amplitude. Second, it dynamically decouples the DB stage from the Class-D stage, which facilitates the design of the feedback control system that is commonly employed to further improve the output signal quality. Note that the magnetic coupling of the DB inductors can also reduce their overall volume [1].

It should be noted that the proposed converter does not utilise the Class-D stage to provide the circulating bias current of the DB stage, which is another concept to augment the DB converter as shown in [6].

In the following, a feedback control topology of the TB converter is outlined and its functionality demonstrated with computer simulations.

## 3 Control and functional verification

The TB converter provides a controlled output voltage $u_o(t)$ (or, by employing an additional feedback loop, a controlled output current $i_o(t)$ [5]). Fig. 3 illustrates the proposed control topology. Note that, for the sake of the argument, the coupled inductors, as shown in Fig. 2 with $k \leq 1$, are replaced by an equivalent circuit that provides the DM inductance ($L_m$) for the circulating current, and a series inductance $L_s$ that decouples the DB stage from the Class-D stage.

The compensator $C_1$, which is often a proportional–integral (PI) or PI–derivative (PID) type, provides feedback for the output voltage $u_o$, as Fig. 3*a* depicts. Its output is the reference for the combined current $i_\Sigma$ of the two converter stages. Note that an asterisk (*) indicates a controller reference signal.

The current $i_\Sigma$ is formed as $i_\Sigma = i_D + i$, and thus by introducing a (arbitrarily selectable) weighting factor $r \in [0, 1]$, the current references of the Class-D and DB stage can be given as $i_D^* = (1 - r)i_\Sigma^*$ and $i^* = ri_\Sigma^*$, respectively. Thus, if $r = 0$, the entire output current is provided solely by the Class-D stage, and if $r = 1$, the DB converter provides the entire load current. This allows an optimisation of the typical trade-off between power conversion losses and output THD in real time during converter operation.

The Class-D output current $i_D$ is controlled by $C_D$, which can also be a P, PI or PID compensator (compare Fig. 3*b*). Similarly, the output current $i$ of the DB stage is controlled by $C_{CM}$. The circulating bias current of the DB stage is, as outlined above, the difference of the two DB half-bridge currents $i_{1,2}$. It can be controlled independently of the current $i$ as illustrated in Fig. 3*d*. The outputs of the CM and DM current controllers of the DB stage are combined as illustrated to obtain the desired reference output voltages of the two DB half-bridges $u_1^*$ and $u_2^*$.

To improve the transient response of the control system and to decouple the cascaded control loops, the measured output voltage $u_o$ can be used as a feed-forward compensation term, as Fig. 3*e* shows. Finally, the required duty cycles of the three half-bridges are formed by pulse-width modulators, which can also be enhanced by delta–sigma modulators (noise shapers) to reduce quantisation noise and to increase the output signal-to-noise ratio, which is another key amplifier characteristic for certain precision applications [5].

The operation of the TB converter is demonstrated in Fig. 4 with a computer circuit simulation (*GeckoCIRCUITS*) that incorporates all important circuit elements and time-discrete control systems, corresponding to the diagram in Fig. 3. The output voltage reference $u_o^*$ is sinusoidal with an arbitrarily selected frequency of 600 Hz, which results in sinusoidal output current $i_o$, with a purely resistive load of 3 Ω.

As illustrated, the sharing of the output current by each converter stage can be arbitrarily selected during operation, and the currents are adjusted seamlessly according to the selection of $r$, which is changed during operation in Fig. 4*d* from 0.2 to 0.6, while at the same time, $I_B^*$ is also changed from 4 to 11 A to ensure the unidirectionality of the currents of the DB stage.

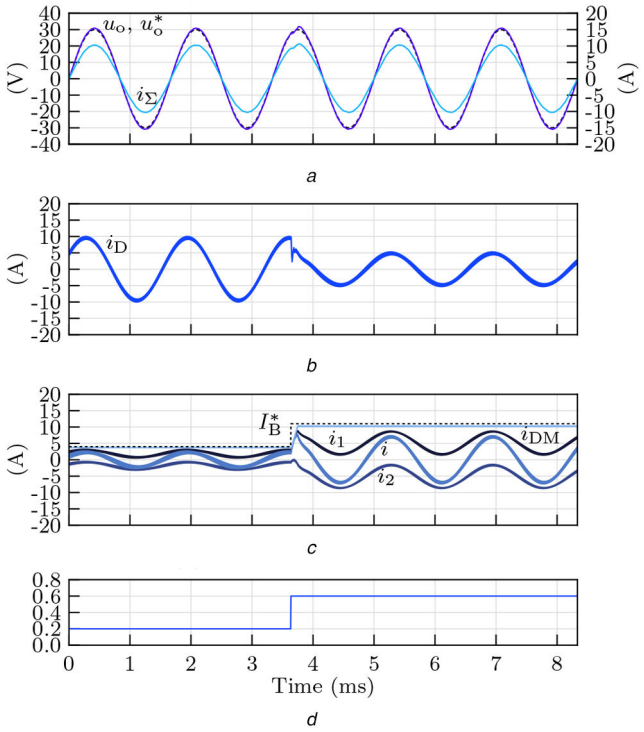


**Fig. 4** *Computer circuit simulation of the TB converter. The current sharing ratio and DB bias current are changed to demonstrate the topology's interoperability.* $L_D = L_s = L_m = 100\,\mu H$, $U_{DC} = 100\,V$, $f_{PWM} = 200\,kHz$. *$C_1$ is a PI controller and the other compensators are P-type*

***(a)*** Output voltage, current, ***(b)*** Class-D stage current, ***(c)*** DB stage currents, ***(d)*** Current weighting ratio *r*

This behaviour is especially useful for converters/amplifiers in nanometre-scale mechatronic positioning applications, where the power loss of nearby converters and motor drives must be limited to avoid a thermal distortion of the sensitive positioning stages. Thus, during high-speed positioning movements, which often do not require a high-output signal quality of the amplifiers, *r* can be selected close to 0 such that the efficient Class-D stage of the TB converter provides the desired high-power output. The achievable THD figures are then limited by the dead time of the Class-D stage, which are commonly above −90 dB, while the converter can achieve high-power conversion efficiencies of typically more than 96%, as exemplarily demonstrated in [5] with a 400 V, 4 kW system. Similarly, when the positioning stage must be moved with low THD of the driving signals (often at reduced power levels), *r* can be selected close to 1 such that only the low-distortion DB stage provides the desired output. THD values below −100 dB can be achieved [5], while the conversion efficiencies are limited to <90% [5]. If *r* is selected between 0 and 1, the inductive voltage divider formed by $L_D$ and $L_s$ (compare Fig. 3) determines the weighting of the contribution of the Class-D and DB stages to the overall TB converter output distortion and power conversion efficiency.

## 4 Conclusion

An improved power conversion topology, the TB converter, is presented. It is especially suited for applications that demand both high-output powers and low-distortion signals. The topology combines two well-established converters, namely a regular, efficient Class-D stage and a DB stage, which inherently provides low-distortion output signals. The output current of the converter can be arbitrarily shared between the two stages such that a high conversion efficiency or a low-output signal distortion, or a favourable combination of these two characteristics, is achieved.

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