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Component Cost Models for Multi-Objective Optimizations of Switched-Mode Power Converters

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***Abstract*—Besides product differentiation, cost is a key parameter for market success and sustainable competitive advantage of industrial companies. Academic research in the field of power electronics, however, is often confined to the search for technical innovations or optimizations with focus on pure physical performance indices while the cost dimension is neglected. An explanation for the lack of such cost considerations is the generally poor availability of cost data in academia. This paper discusses the necessity of an increased awareness and sensitivity towards costs and the related opportunities for academic research. Furthermore, cost models for the power semiconductors, the passive components, the cooling systems and the printed circuit boards of switched-mode power converters with an approximate rated power between 5 and 50 kW are derived. Based on manufacturer prices for large ordering quantities, numerical values for the cost model parameters are proposed. An example of a multi-objective comparison of different power converter topologies for photovoltaic applications regarding efficiency, volume and total semiconductor chip area is extended by the cost dimension to demonstrate the benefits of employing the developed cost models.**

I. Introduction

Today's fundamental trends and requirements in the development of new power electronics converter systems are diverse and highly challenging: besides shorter development cycle times, the trends also include the increase of the power density, efficiency and reliability while lowering the cost and weight [1], [2], [3] (**Fig. 1**). Whereas improvements regarding the physical performance indices (efficiency, volume and weight), either by means of novel technologies or by (multi-objective) optimization, has been a predominant topic of many papers in power electronics research, a deeper analysis and consideration of the converter cost has rarely been addressed so far.

Cost considerations for single components can be found in [4], [5], [6] for semiconductors, inductive components or heatsinks. The costs are indirectly estimated by considering representative physical quantities such as the total chip area or the stored energy and volume of the passive components. The significance of this approach is limited, however, when costs must be compared and evaluated in the context of more than one type of component, material or manufacturing process. Examples of direct and explicit cost models for litz wires, inductors or semiconductors can be found in [7], [8], [9], [10]. Partly for reasons of confidentiality, however, only normalized values or distributor prices for unknown ordering quantities are provided for the parameters of the cost models.

More detailed cost models enabling the description and comparison of several types of system components or processes are presented in [11], [12], [13] for the projection of levelized wind energy costs, the manufacturing costs of 3-D integrated circuits (IC) or for the optimization of photovoltaic (PV) power plant configurations at system level.

With respect to comprehensive cost analysis of modern switched-mode power converters including all relevant components (such as semiconductors, heatsinks and passives), some of the few examples which can be found in literature are [8], [14], [15], [16], where a mix of discrete cost data as well as continuous cost models are employed for multi-objective converter optimizations. Alas, all contributions miss to provide detailed information on the cost models and restrict to the presentation of the final, normalized converter cost.

Besides a general discussion of the possibilities and necessities of an increased awareness of cost in the field of academic power electronics research (**Sec. II**), the main contribution of this paper is the first step of a systematic approach towards integrated cost models for the power semiconductors, the passive components, the cooling systems and the printed circuit boards (PCB) of switched-mode power converters with approximate power ratings of 5-50 kW (**Sec. III**). Furthermore, the derived models are applied to an example from the field of PV power plants, where a multi-objective comparison of inverter topologies regarding efficiency, volume and total chip area is extended by cost evaluations (**Sec. IV**).

II. Necessity and Opportunities of Cost Considerations

From the viewpoint of academia, the availability of quantitative cost models and a better understanding of the cost structure of power electronics converters would enable several advantages and opportunities:

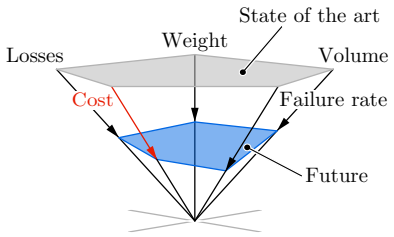

Fig. 1: Trends for performance improvements in the field of power electronics. Whereas the optimization of converter losses, weight and volume has been a major topic in research publications, cost and reliability issues have generally not yet been widely discussed. Considering this a motivation, this paper focuses on the analysis and modeling of the component costs of switched-mode power electronics converter systems.

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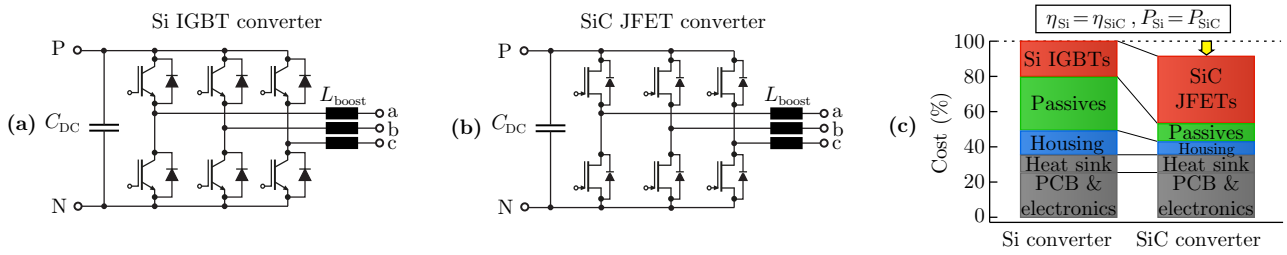

Fig. 2: Fictitious example for the utilization of cost models to assess the potential of the SiC technology. **(a)** Three-phase power converter employing standard Si IGBTs. **(b)** Same converter as in **(a)** employing SiC JFETs. **(c)** Cost models allow to analyze the potential of SiC, i.e. to determine the trade-off between increased power density (due to higher applicable switching frequencies for the same efficiency η) and the higher cost of SiC. In this example, both increased power density and reduced overall converter cost can be achieved as the high SiC JFET cost is compensated by the smaller and less expensive passives and housing. In a case where higher overall costs result, the same analysis would allow to define a cost target for SiC in order to become a viable option in cost-critical applications.

(i) Assessment of the potential of novel technologies and concepts from the cost point of view;
(ii) Multi-objective optimizations and comparisons not only regarding physical performance indices but also costs;
(iii) Identification of potentials for innovation and optimization based on a preceding cost analysis of an existing application.

Case (i) is particularly relevant to academic research in the field of power electronics since one of its main tasks is the search for novel topologies, control methods and the application of novel technologies and materials (exemplarily [17], [18], [19]). Here, cost can serve as an additional, highly industry-relevant criterion when assessing the potential of the innovation and comparing it to the state of the art [1]. A highly topical example, which is illustrated in **Fig. 2**, is the assessment of the potential and the search for appropriate applications of SiC semiconductors.

A practical example for case (ii) is presented in **Sec. IV**, where a multi-objective comparison of different power converter topologies for a PV application is extended by the cost criterion.

III. Derivation of Component Cost Models

In this section, models for the component costs from the viewpoint of converter manufacturers are developed. The models apply to typical components of a broad variety of switched-mode power converters with an approximate power rating of 5-50 kW.

Developing cost models for power electronics components poses several challenges:

- Complexity of the cost structure of components with a broad mix of different materials and manufacturing processes
- Influence of non-physical cost factors such as minimum ordering quantity (MOQ), location and negotiation
- Time-dependence of costs due to varying raw material prices and economy-of-scale effects
- Confidentiality of cost data and pricing strategies

The presented models in the following subsections largely use variables related to physical component properties. This approach is especially useful for engineers as the models can be incorporated into the converter dimensioning process in a straightforward manner. Due to the generic nature of the models, they are moreover expected to be insightful independently from the above mentioned non-physical cost factors. Nevertheless, numerical values for the model parameters are supposed to additionally provide an idea of the absolute cost impact of different components and materials. The parameters are derived based on empirical research and represent a snapshot of the market in spring 2013. Generally, MOQs larger than 10 000 units were considered to give more realistic figures for the industrial mass production of converters. For the remainder of this section, *cost* designates the component manufacturing cost, whereas *price* refers to the final component selling price which corresponds to the buying cost of the power converter manufacturers.

A. Power Semiconductors

Generally, the cost structure of semiconductors derives from a complex mix of sophisticated manufacturing processing steps and high R&D efforts, whereas the (unprocessed) raw materials take only a negligible share of the total cost [20]. From an engineering point of view, the two most important features of a semiconductor are its chip size and the package. Together they largely define the electrical and thermal behaviour of the device [21]. Therefore, the following cost model is proposed,

$$\Sigma_{SC} = \Sigma_{chip} + \Sigma_{pack,x} = \left(\sum_n \sigma_{chip,x(n)} A_{chip,n} \right) + \Sigma_{pack,x}, \tag{1}$$

where, $\sigma_{chip,x}$ is the specific price per chip area A_{chip} depending on the chip technology and $\Sigma_{pack,x}$ is the package price (including chip integration and bonding). Eq. (1) is motivated by [10], [21] where it is observed that the chip prices approximately scale linearly with the size. The parameter $\sigma_{chip,x}$ can hence be interpreted as the sum of all processing and R&D costs for a given chip technology. The validity of the model is further underpinned by an acquired database of over 60 discretes and power modules with associated prices and chip areas from two major semiconductor manufacturers (modules: MOQ = 10 000; discretes: MOQ = 50 000). The illustration of this data in **Fig. 3** shows relatively constant specific chip prices for each technology. **Tab. I** presents numerical values for $\sigma_{chip,x}$ which have been identified based on a multi-parametric least square fitting (mean error 4.7 %; standard deviation 3.9 %) of the database samples.

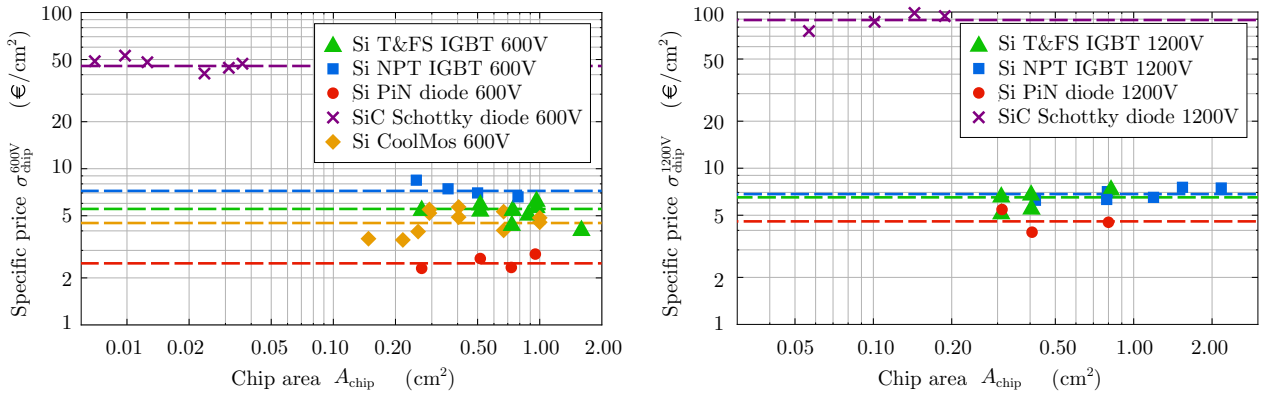

Fig. 3: Specific prices for common semiconductor chip technologies based on data from two major semiconductor manufacturers. The dashed lines represent the numerical values of the identified cost model parameters $\sigma_{\text{chip},x}$ according to **Tab. I**.

Tab. I: Proposed numerical values for the specific semiconductor chip prices $\sigma_{\text{chip},x}$ and package prices $\Sigma_{\text{pack},x}$ for the semiconductor cost model (1), based on data provided by two major semiconductor manufacturers (modules: MOQ = 10 000; discretes: MOQ = 50 000). The considered modules feature a copper base plate and a temperature sensor.

Chip technology:	**Si T&FS IGBT**	**Si NPT IGBT**	**Si PiN diode**	**SiC Schottky diode**	**Si CoolMos**
$\sigma_{\text{chip},x}^{600\text{ V}}$ (€/cm²)	5.52	7.22	2.46	46.24	4.48
$\sigma_{\text{chip},x}^{1200\text{ V}}$ (€/cm²)	6.57	6.65	4.46	86.47	
Package type:	**TO-247-3**	**SOT-227**	**Module (23.2 cm²)**	**Module (29.9 cm²)**	**Module (37.6 cm²)**
$\Sigma_{\text{pack},x}$ (€/unit)	0.55	8.10	7.62	10.01	15.06

B. Inductors

In contrast to most other power electronics components, inductors for converters in the considered power range are often material and labour intense, i.e. a large fraction of the total price can be explained by the material and labour cost. This motivates the use of the following inductor cost model, of which a simplified version can also be found in [8],

$$\Sigma_L^{\text{dc}} = \Sigma_{\text{mat},L} + \Sigma_{\text{lab},L}, \tag{2}$$

where

$$\begin{aligned}\Sigma_{\text{mat},L} &= \Sigma_{\text{core},x} + \Sigma_{\text{wdg},x} + \Sigma_{\text{mat},x}^{\text{fc}} \\ &= \sigma_{\text{core},x} W_{\text{core}} + \sigma_{\text{wdg},x} W_{\text{wdg}} + \Sigma_{\text{mat},x}^{\text{fc}}, \qquad (3)\\ \Sigma_{\text{lab},L} &= \sigma_{\text{lab},x} W_{\text{wdg}} + \Sigma_{\text{lab},x}^{\text{fc}}. \qquad (4)\end{aligned}$$

$\sigma_{\text{core},x}$, $\sigma_{\text{wdg},x}$ and $\sigma_{\text{lab},x}$ are specific costs per weight W_{core}, W_{wdg} of the core and winding depending on the employed core and winding type. $\Sigma_{\text{mat},x}^{\text{fc}}$ and $\Sigma_{\text{lab},x}^{\text{fc}}$ are fixed material and labour costs (e.g. coil former, connectors). **Tab. II** gives numerical values for the parameters of the supposed inductor cost model. The data is obtained from several inductor manufacturers for large MOQ > 15 000. Such MOQs usually imply Asian manufacturing due to lower labour cost. Moreover, the cost for manufacturing tools for custom core sizes (typically around 5 000-15 000 €) can be neglected in a first approximation. Special attention must be paid to the ferrites and rare earth elements which predominantly come from China and thus do not follow a world market price. If not intended for the Chinese market (as assumed for the data in **Tab. II**), a cost premium of roughly 15 % must be accounted for these materials. Eventually, (2) models the direct cost (all costs which can directly be attributed to the product) of the inductor supplier and hence does not yet include any overhead costs and profit. The final component price can be approximated by means of the supplier's gross margin Ξ [22],

$$\Xi = \text{Gross margin} = \frac{\text{Gross profit}}{\text{Revenue}} = \frac{\text{Revenue-COGS}}{\text{Revenue}}, \tag{5}$$

where COGS is the cost of all goods sold excluding any overhead costs and profit, or equivalently the sum of direct costs of all sold products and services. Hence, assuming a similar gross margin for all individual products and services, the selling price Σ_L can be estimated by

$$\Sigma_L = \frac{1}{1-\Xi_L} \cdot \Sigma_L^{\text{dc}}. \tag{6}$$

Tab. II: Proposed numerical values for the inductor cost models (3),(4),(6) based on data from several inductor manufacturers. A_{strand} (in mm²) is the diameter of a single strand of the litz wire. The indicated cost for grain-oriented electrical steel (GOES) are valid with good accuracy for the grades M2 to M4 (0.18-0.27 mm sheet thickness). High Si steel refers to electrical steel with a high Si content (>6 %) and a sheet thickness of 0.1 mm for lower core losses. The given parameters apply to inductors from Asian manufacturing facilities with a non-Chinese target market and an approximate total weight of 0.5 to 10 kg.

Core type:	**High flux ferrite**	**Amorphous**	**Nanocrystalline**	**High Si steel**	**GOES**
$\sigma_{\text{core},x}$ (€/kg)	5.5	16.0	23.0	12.0	2.5
Winding type:	**Solid round**	**Flat**	**Foil**	**Litz**	
$\sigma_{\text{wdg},x}$ (€/kg)	10.0	10.0	20.0	$\frac{15.0}{\frac{A_{\text{strand}}}{\text{mm}^2}+0.45}$	
$\Sigma_{\text{mat},x}^{\text{fc}}$ (€/unit)	1.0	2.0	2.0	1.0	
$\sigma_{\text{lab},x}$ (€/kg)	7.0	21.0	14.0	7.0	
$\Sigma_{\text{lab},x}^{\text{fc}}$ (€/unit)	2.0	4.0	2.5	2.0	
Ξ_L (%)			25.0		

C. Capacitors

1) Power Capacitors: The predominant types of power capacitors in the field of power electronics are electrolytic and thin film capacitors. **Fig. 4** shows the unit prices of a selection

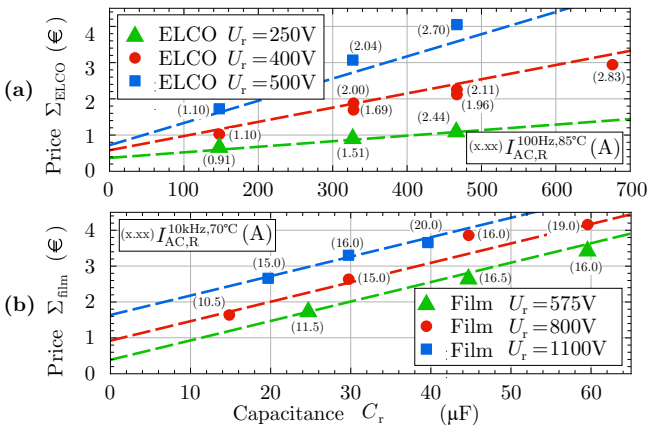

Fig. 4: Unit prices for **(a)** different standard type Al electrolytic (Al ELCO) and **(b)** metallized polypropylene thin film (MKP) power capacitors based on prices from a major capacitor manufacturer (MOQ = 10 000, PVC insulation). $I_{\mathrm{AC,R}}$ is the capacitor rated RMS current. The figures further depict the corresponding curves of the cost models (7), (8) based on the fitted parameters presented in **Tab. III**.

Tab. III: Proposed numerical values for the capacitor cost models (7),(8),(9),(10) for Al ELCO and MKP film capacitors based on data provided by a major capacitor manufacturer (MOQ = 10 000). $a_{\mathrm{X2}}/c_{\mathrm{X2}}$ are valid for $C_\mathrm{r} < 40\,\mu\mathrm{F}$ and $a_{\mathrm{Y2}}/c_{\mathrm{Y2}}$ for $C_\mathrm{r} < 0.35\,\mu\mathrm{F}$.

	a_x	b_x	c_x
ELCO		$1.437 \cdot 10^{-3}$ €/V	$24.757 \cdot 10^{-9}$ €/µF V²
Film	-1.022 €	$54.956 \cdot 10^{-3}$ €/V	$2.426 \cdot 10^{-3}$ €/µF
X2 305 V	-0.025 €		0.155 €/µF
Y2 300 V	0.073 €		2.604 €/µF

of standard aluminium electrolytic capacitors (Al ELCO) and metallized polypropylene thin film (MKP) capacitors from a major manufacturer (MOQ = 10 000). The data reveals the different price dependencies of the two considered capacitor types: whereas the price of Al ELCOs scales with the rated stored energy, i.e. $\Sigma_{\mathrm{ELCO}} \propto C_\mathrm{r} U_\mathrm{r}^2$, the MKP unit prices scale only linearly with the rated capacitance C_r and voltage U_r, i.e. $\Sigma_{\mathrm{film}} \propto C_\mathrm{r} + U_\mathrm{r}$. For the latter, this implies that the stored energy becomes cheaper for higher rated voltages. According to manufactureres, this characteristic is due to the lower manufacturing cost of thicker films which are used for higher rated voltages (holds true up to 2-3 kV).

Based on the subsequent observations, the following (unit) cost models are supposed for ELCOs and film capacitors,

$$\Sigma_{\mathrm{ELCO}} = b_{\mathrm{ELCO}} U_\mathrm{r} + c_{\mathrm{ELCO}} C_\mathrm{r} U_\mathrm{r}^2, \tag{7}$$

$$\Sigma_{\mathrm{film}} = a_{\mathrm{film}} + b_{\mathrm{film}} U_\mathrm{r} + c_{\mathrm{film}} C_\mathrm{r}. \tag{8}$$

Numerical values for Al ELCOs and MKP film capacitors were obtained by means of a multi-parametric least square fitting of the data shown in **Fig. 4** (mean error 7.7 %; standard deviation 3.9 %) and are listed in **Tab. III**.

2) EMI Capacitors: EMI suppression capacitors on the mains supply side of a power converter must comply with the applicable EMC directives and standards, such as IEC 60384-14 [23]. Depending on the safety class (X1-X3 for line-to-line and Y1-Y4 for line-to-ground capacitors), different degrees of safety requirements concerning overvoltages, (mains) transients and inflammability must be met [23]. Although this means higher capacitor cost and a potentially more complex cost structure, the simple (unit) cost models

$$\Sigma_{\mathrm{X2}} = a_{\mathrm{X2}} + c_{\mathrm{X2}} C_\mathrm{r}, \tag{9}$$

$$\Sigma_{\mathrm{Y2}} = a_{\mathrm{Y2}} + c_{\mathrm{Y2}} C_\mathrm{r}, \tag{10}$$

are proposed, which imply that the additional costs scale with the capacitance C_r. The models do not take into account varying safety classes or rated voltages since X2/Y2-ratings are usually sufficient for a wide range of applications and availability of different voltage ratings is often strongly limited. **Tab. III** suggests numerical values for the model parameters based on fitted manufacturer data (MOQ = 10 000, N = 10, mean error 7.1 %; standard deviation 4.6 %). The higher specific price per capacitance when compared to the power capacitors can be clearly seen.

D. Cooling Systems

1) Heatsinks: The cost of heatsinks generally depends on the base material, volume and weight as well as the manufacturing and engineering costs. **Fig. 5(a)** shows unit prices of different types of off-the-shelf aluminium heatsinks from two manufacturers (MOQ = 10 000). Comparing the weight of the heastsinks and taking into account the approximate world market price for aluminium (≈1.4 €/kg), it can be deduced that (for Al heatsinks) the cost only poorly scales with the weight (e.g. hollow-fin is light in weight but more expensive) and that the total cost must hence largely be a product of the manufacturing processes . However, the analysis of the data in **Fig. 5(a)** as well as additional distributor prices shows a strong linear dependence between price and volume for each type of heatsink.

Consequently, the following cost model is supposed,

$$\Sigma_{\mathrm{sink}} = \Sigma_{\mathrm{sink},x}^{\mathrm{fc}} + \sigma_{\mathrm{sink},x} V_{\mathrm{sink}}, \tag{11}$$

where $\sigma_{\mathrm{sink},x}$ is the specific cost per volume depending on the heatsink type. $\Sigma_{\mathrm{sink},x}^{\mathrm{fc}}$ are fix costs which can result from additional engineering work and processing steps which are independent from the heatsink volume (e.g. drilling holes, mounting of fans). For the considered heatsink data, no significant fix costs have been identified. The corresponding values for $\sigma_{\mathrm{sink},x}$ are listed in **Tab. IV** (mean error 0.4 %; standard deviation 0.2 %).

2) Fans: Empirical analyis of distributor prices for standard axial DC compact fans generally shows large price offsets and only weak dependencies from the fan power (maximum air flow) and size. This finding is also confirmed by the obtained manufacturer data (MOQ = 10 000) shown in **Fig. 5(b)**. According to manufacturers, the dominant cost factors of fans in the considered product segment are the bearings and their lubricants, whose cost, however, increases only slowly with growing fan size. Furthermore, the engineering and assembly costs (fully automated) are equal for all fans and thus additionally contribute to the high fix costs. Finally, also the cost for the motor electronics is relatively constant as often the same or very similar designs and components are used independent from the fan power. The price differences

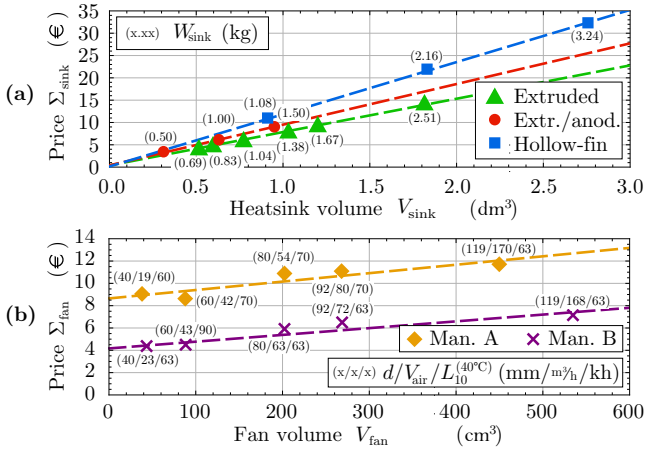

Fig. 5: **(a)** Unit prices of off-the-shelf extruded, extruded/anodized and hollow-fin aluminium heatsinks from two manufacturers (MOQ = 10 000). W_{sink} denotes the heatsink weight. **(b)** Unit prices for standard 12 V axial DC fans without additional features from two leading manufacturers (MOQ = 10 000). d is the fan diameter, V_{air} the maximum air flow and $L_{10}^{(40\,°\text{C})}$ denotes the life expectancy (90 % survival rate at continuous operation and 40 °C ambient). The figures further depict the corresponding curves of the cost models (11), (12) based on the fitted parameters in **Tab. IV**.

Tab. IV: Proposed numerical values for the heatsink and fan cost model (11),(12), based on data provided by two manufacturers (MOQ = 10 000).

Heatsink type:	**Extruded**	**Extruded/ anodized**	**Hollow-fin**
$\sigma_{\text{sink},x}$ (€/dm³)	7.69	9.30	11.94
$\Sigma^{\text{fc}}_{\text{sink},x}$ (€/unit)	0.23	0.25	0.17
Fan manufacturer:	**A**	**B**	
$\sigma_{\text{fan},x}$ (€/cm³)	$7.69 \cdot 10^{-3}$	$6.18 \cdot 10^{-3}$	
$\Sigma^{\text{fc}}_{\text{fan},x}$ (€/unit)	8.78	4.19	

between the two manufacturers depicted in **Fig. 5(b)** can partly be explained by the higher input voltage and temperature (more expensive lubricant) range of manufacturer B, while also different plant locations and price policies might have an impact.

Based on the above analysis, a simple linear cost model is supposed,

$$\Sigma_{\text{fan}} = \Sigma^{\text{fc}}_{\text{fan},x} + \sigma_{\text{fan},x} V_{\text{fan}}, \tag{12}$$

with $\Sigma^{\text{fc}}_{\text{fan},x}$ modelling the fix costs and $\sigma_{\text{fan},x}$ the volume dependency. Numerical values based on least square fits (mean error 4.9 %; standard deviation 3.0 %) can be found in **Tab. IV**.

E. PCBs and ICs

1) PCBs: The prices for PCBs generally depend on a multitude of physical variables. In order to reduce the model complexity and to focus on the most important criteria, which are the PCB area, the number of layers and the copper thickness, standard PCBs with fixed and typical values for the remainder of the variables are considered:

- FR4 TG 130 °C 1.55 mm base material;
- No blind/buried vias and controlled impedances;
- Drills > 0.3 mm, track width/spacing/annular ring > 0.15 mm;

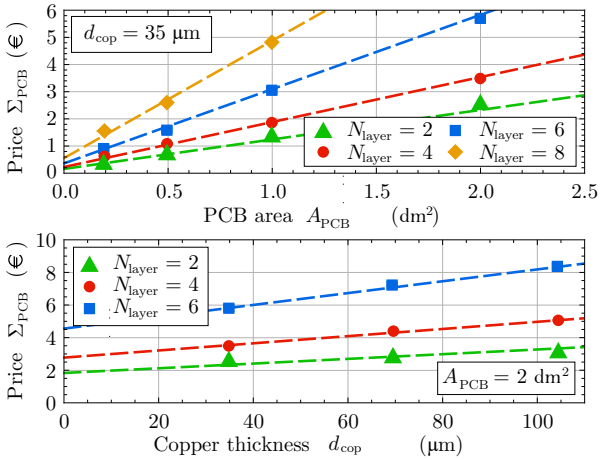

Fig. 6: Manufacturer price data (MOQ = 10 000) of standard PCBs (FR4 TG 130 °C 1.55 mm, drills > 0.3 mm, no blind/buried vias and controlled impedances, track width/spacing/annular ring > 0.15 mm, HAL leadfree surface finish, white marking print and green solder mask both sides, E-test, IPC-A-600G class 2). N_{layer} is the number of layers, d_{cop} the copper thickness (inner and outer layers) and A_{PCB} the PCB area. The figures further depict the corresponding curves of the cost model (13) based on the fitted parameters in **Tab. V**.

Tab. V: Identified numerical values for the PCB cost model (13) based on data provided by a manufacturer (MOQ = 10 000).

	a_x	b_x	c_x
A_{PCB}	0.407 €$^{1/3}$	3.240 €$^{1/3}$/dm²	
d_{cop}	8.489 €$^{1/3}$	$67.947 \cdot 10^{-3}$ €$^{1/3}$/µm	
N_{layer}	$29.409 \cdot 10^{-3}$ €$^{1/3}$	$-2.779 \cdot 10^{-3}$ €$^{1/3}$	$1.829 \cdot 10^{-3}$ €$^{1/3}$

- HAL leadfree surface finish, white marking print and green solder mask on both sides;
- E-test, IPC-A-600G class 2 quality standard.

Based on these assumptions, the price data depicted in **Fig. 6** was requested from a PCB manufacturer for MOQ = 10 000. The linear dependence of the unit price from the PCB area and the copper thickness is clearly visible, whereas the number of layers has a quadratic impact. The latter can be explained with additional required processing steps and the generally higher complexity of multilayer PCBs [24].

Based on the subsequent analysis, the following cost model for standard PCBs is supposed,

$$\Sigma_{\text{PCB}} = (a_{A_{\text{PCB}}} + b_{A_{\text{PCB}}} A_{\text{PCB}}) \cdot (a_{d_{\text{cop}}} + b_{d_{\text{cop}}} d_{\text{cop}}) \cdot (a_{N_{\text{layer}}} + b_{N_{\text{layer}}} N_{\text{layer}} + c_{N_{\text{layer}}} N^2_{\text{layer}}), \tag{13}$$

where A_{PCB} denotes the PCB area, d_{cop} the copper thickness (all layers) and N_{layer} the number of layers. The corresponding fitted numerical values are listed in **Tab. V** (mean error 4.1 %; standard deviation 3.9 %).

2) ICs and Electronics: Power converters usually rely on a multitude of different integrated circuits (ICs) and electronic components such as sensors, gate drivers and embedded microcontrollers, which enable the proper functioning of the device. Due to the vast variety of such ICs, developing detailed cost models would pose an elaborate and time-consuming task. It is hence suggested to estimate the approximate cost based on distributor data, which is for ICs often provided for high

MOQs. This is a pragmatic yet meaningful approach as for many investigations and optimization efforts the amounts and types of ICs and other electronic components do not change and thus represent fix costs.

IV. Example of Application

In this section, an application example will be presented in order to demonstrate the practical use and benefit of the derived cost models. The example is largely based on the work in [25], where the three-phase topologies shown in **Fig. 8** are employed in a PV application as depicted in **Fig. 7** and compared with respect to efficiency, volume and semiconductor chip area requirements. Motivated by the fact that the reduction of cost has become a main target of further improvements in the PV industry [26], [27], this example will be extended by a cost analysis.

A. Specifications and Dimensioning

The system specifications, the selection of components as well as the dimensioning criteria will be discussed in brief, while more detailed information can be found in [25]:

- Rated output power: $P_\mathrm{r} = 50\,\mathrm{kW}$;
- Secondary mains line-to-line RMS voltage: $u_\mathrm{LV} = (400 + 10\,\%)\,\mathrm{V}$;
- Input voltage range: high range $\bar{u}_\mathrm{PV,H} = [650\,\mathrm{V}, 1160\,\mathrm{V}]$ (2LVSI, single-stage), low range $\bar{u}_\mathrm{PV,L} = [450\,\mathrm{V}, 820\,\mathrm{V}]$ (others);
- Thermal conditions: ambient temperature $T_\mathrm{amb} = 40\,^\circ\mathrm{C}$, worst case average junction temperature of semiconductors $T_\mathrm{j,max} = 120\,^\circ\mathrm{C}$, worst case heatsink temperature $T_\mathrm{sink,max} = 80\,^\circ\mathrm{C}$, worst case inductor temperature $T_\mathrm{L,max} = 100\,^\circ\mathrm{C}$;
- Semiconductors: Si T&FS IGBTs and Si PiN diodes in $37.6\,\mathrm{cm}^2$ modules. Blocking voltages: 1700 V (2LVSI), 1200 V (2LVSI+BC,2LZSI) and 600/1200 V (3LI+BC,3LT+BC);
- Cooling system: $1.85\,\mathrm{dm}^3$ hollow-fin heatsink with 2 $90\,\mathrm{cm}^3$ DC axial fans from manufacturer A, the overall cooling system performance index ($CSPI$, [28]) is $7.3\,\mathrm{W/K\ dm}^3$;
- Inductors: C-shaped amorphous cores, foil windings;
- Capacitors (see **Fig. 7,8**): 1100 V/40 µF DC film MKP capacitors , (stacked) 500 V/220 µF/1.5 A Al ELCO capacitors , 10 µF X2 AC EMI capacitors.

The dimensioning methodology assumes continuous variables and thus allows for arbitrarily sized components or the employment of a non-integer amount:

- Semiconductors and cooling system: based on a thermal

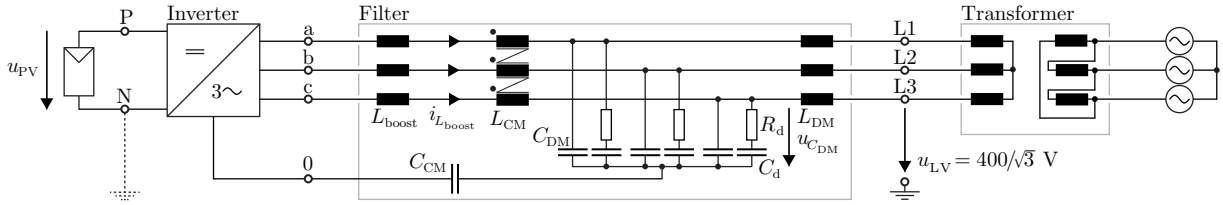

Fig. 7: Generic topology of the considered three-phase 50 kW PV inverter with output LCL filter. A Δ-Y transformer connects the 400 V industrial low voltage secondary grid side to a European 50 Hz medium voltage grid.

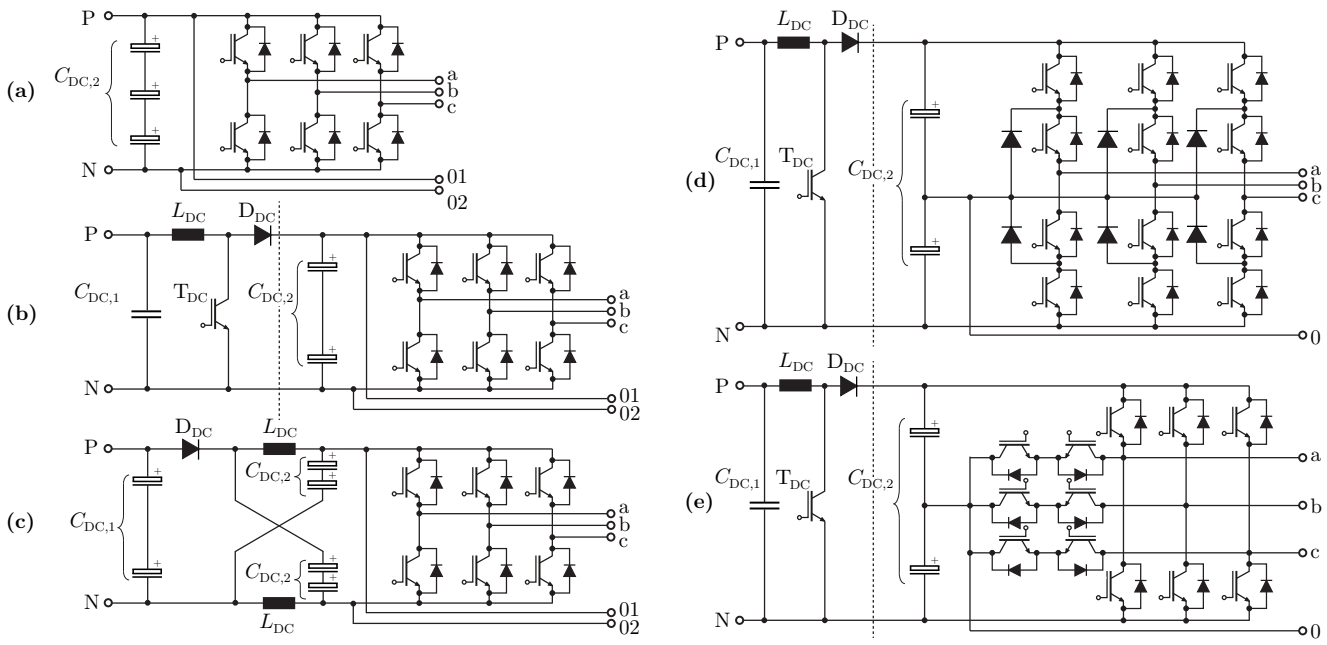

Fig. 8: Considered topologies. **(a)** 2-level voltage source inverter (2LVSI). **(b)** 2-level VSI with adjusting input side DC/DC boost converter (2LVSI+BC). **(c)** 2-Level Z-source inverter (2LZSI). **(d)** 3-level I-type topology with boost converter (3LI+BC). **(e)** 3-level T-type topology with boost converter (3LT+BC).

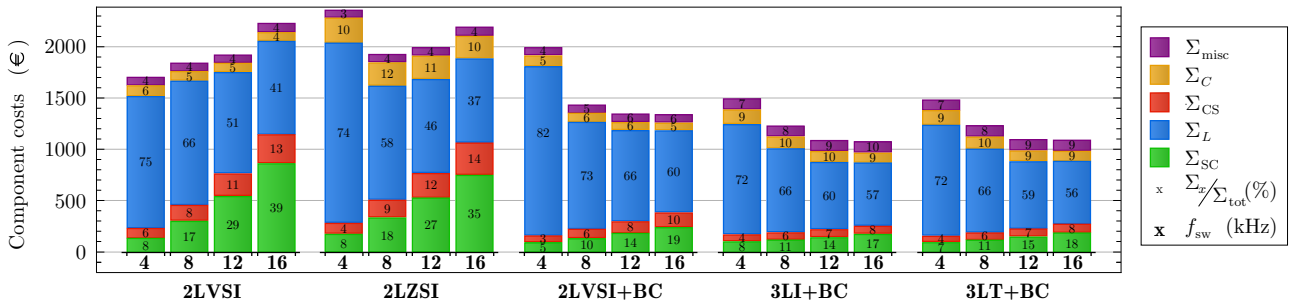

Fig. 9: Component cost structure per topology and switching frequency f_{sw}. $\Sigma_{\mathrm{misc}} = \Sigma_{\mathrm{PCB}} + \Sigma_{\mathrm{IC}}$ is the PCB and IC costs, $\Sigma_C = \Sigma_{\mathrm{ELCO}} + \Sigma_{\mathrm{film}}$ the total capacitor cost and $\Sigma_{\mathrm{CS}} = \Sigma_{\mathrm{sink}} + \Sigma_{\mathrm{fan}}$ the cooling system cost. The output LCL filter is included in this analysis.

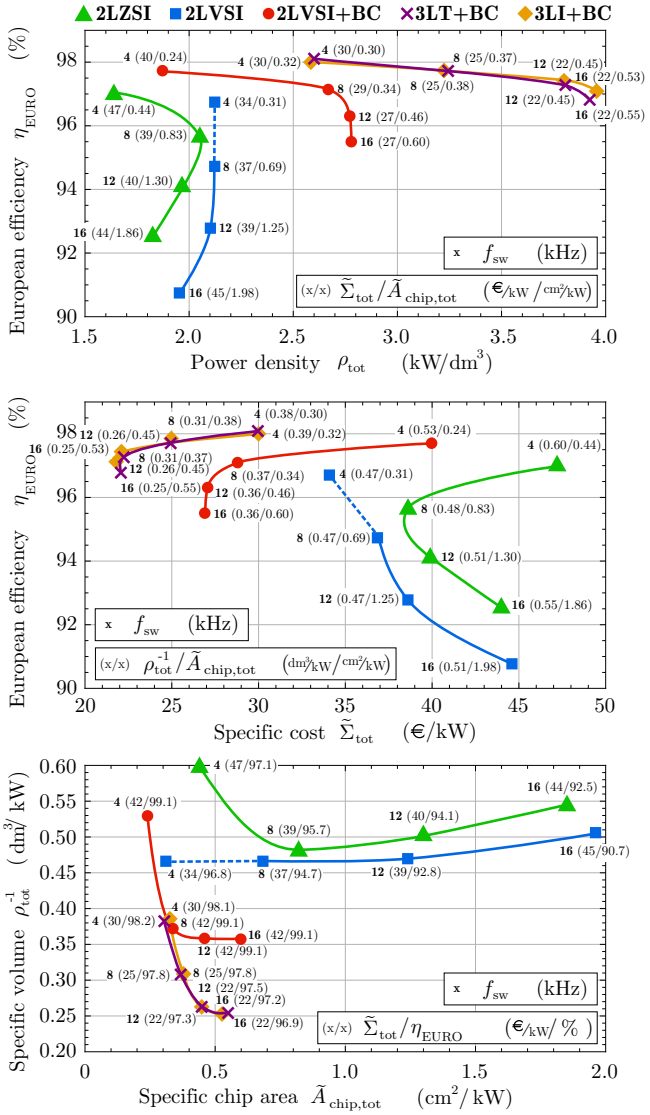

Fig. 10: Comparative evaluation of the topologies shown in **Fig. 8** and output LCL filter as depicted in **Fig. 7** according to the dimensioning criteria outlined in **Sec. IV-A** and as a function of the switching frequency f_{sw}. Normalized performance indices are used [25]: η_{EURO} is the (weighted) European efficiency, ρ_{tot} the power density, $\tilde{A}_{\mathrm{chip,tot}} = A_{\mathrm{chip,tot}}/P_{\mathrm{r}}$ the total specific semiconductor chip area and $\tilde{\Sigma}_{\mathrm{tot}} = \Sigma_{\mathrm{tot}}/P_{\mathrm{r}}$ the total specific component costs per rated power. The discontinuities in the performance curves of the 2LVSI between 4 and 8 kHz result from a change of the filter topology: an additional CM inductor $L_{\mathrm{CM}} \neq 0$ becomes necessary to maintain EMI compliance, which is not required for the remaining topologies due to more favourable modulation index ranges.

model, the individual semiconductor chip areas and the cooling system are dimensioned such that for the worst case of each component $T_{\mathrm{j}} = T_{\mathrm{j,max}}$ and $T_{\mathrm{sink}} = T_{\mathrm{sink,max}}$, given $T_{\mathrm{amb}} = 40\,^{\circ}\mathrm{C}$ [1], [29]. For the module cost calculation, a ratio of $k = 1/6$ between total chip area and required module area is assumed. 10 % higher specific chip area costs σ_{chip} are used for the 1700 V rated semiconductors when compared to the 1200 V rated ones. The cooling system and its cost are scaled so as to achieve the required thermal resistance.

- DC passives: the DC inductances are chosen such that the peak to peak ripple currents are limited to 30 % of the fundamental current. The cost is optimized under consideration of $T_{L,\mathrm{max}}$ and the flux density saturation. The film capacitors exhibit a worst case peak to peak voltage ripple of 1 % whereas the ELCO capacitors are designed so as to meet the required current handling capability. The DC-link allows to fulfil the fault-ride-through requirements according to [30].
- LCL filter: the filter elements are chosen so as to comply with the CISPR EMI Class A standards [31] and the grid harmonics requirements defined in [30]. The damping resistors R_{d} are not considered for the cost evaluations.
- PCB and ICs: A 1 dm²/2-layer/35 µm control board and a 4-layer/105 µm power board with variable size (sum of module and capacitor area) are considered. Based on distributor prices and existing converters, the IC cost is estimated to be 36 € for the control electronics and 4 € per gate driver unit.

B. Comparative Evaluation

Fig. 9 and **Fig. 10** depict the results of the comparative evaluation, parameterized by the switching frequency. It can be observed in both figures how the component mix and correspondingly the cost structure shifts from largely passive component dominated designs at low switching frequencies to more semiconductor and heatsink dominated designs at higher frequencies. However, the rate at which this shift occurs varies widely for the considered topologies: for the 2LVSI and 2LZSI the semiconductor and heatsink expenses grow quickly (mainly due to the high switching losses of the 1700 V semiconductors and unfavourable worst case conditions for the 2LZSI [25]) and outweigh the savings on the passive components already at low frequencies. In contrast, the two-stage topologies, which employ a boost converter, seem to reach a cost optimum only around 16 kHz, since the semi-

conductor cost increase much slower as a result of the higher efficiencies. It may thus generally be assumed that for efficient topologies the cost optimum is relatively flat with respect to the switching frequency and occurs near the minimum volume. This assumption holds particularly true in case of high relative inductor costs. In the example at hand, the high cost for inductors can be explained by the high degree of optimization for the semiconductors (see **Sec. IV-A**) and the expensive materials chosen for the inductive components. Alternative materials may be investigated and the calculated results should be verified with manufacturers.

Based on the multi-objective evaluation it can be concluded that the 3-level topologies feature superior efficiencies while achieving the lowest total component cost. Consequently, these topologies represent promising candidates for more detailed investigations and optimizations.

V. Conclusion and Outlook

Permanent cost reduction is a key strategy for industries to gain sustainable advantage in competitive markets. The intention of this paper is to broaden the sensitivity and awareness regarding cost in academic research and to take the first step of a systematic approach towards cost considerations by making the cost dimension available to multi-objective converter analysis and optimizations.

For this purpose, component cost models for power semiconductors, inductors, capacitors, cooling systems and PCBs for switched-mode power converters with an approximate rated power of 5-50 kW are suggested. Numerical reference values for the model parameters are presented based on manufacturing data for high ordering quantities. The application of the cost models is eventually demonstrated in a multi-objective comparison of different PV inverter topologies.

Future work could include the development of additional models for the remaining components such as the converter housings. Moreover, models for the PCB and converter assembly costs would complete the picture of the total cost. The major challenge for additional and more detailed cost models is imposed by the data availability acquisition. The publication of standardized cost parameters by an industry consortium, such as ECPE, would be of great assistance here.

Finally, the cost models developed in this work will be used to investigate the economic performance of the 10 kW SiC and Si PV inverter topologies shown [32]. There, the cost models can be utilized to estimate the initial component cost of the topologies employing different switching frequencies. Combining this with estimations of the corresponding total operating revenue, which also depends on the inverter efficiency, the economically optimal topology and switching frequency can be determined based on a net present value analysis.

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