



Power Electronic Systems
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Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE USA 2014), Pittsburgh, Pennsylvania, USA,
September 14-18, 2014

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Hyper-Efficient (98%) and Super-Compact (3.3kW/dm³) Isolated AC/DC Telecom Power Supply Module based on Multi-Cell Converter Approach

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Abstract—In this paper, a multi-cell converter approach for a telecom rectifier module breaking through the efficiency and power density barriers of traditional single-cell converter systems is shown. The potential of the multi-cell approach for high efficiency is derived from fundamental scaling laws of the system performances, such as the losses generated by the semiconductors and the harmonic spectrum, in dependence of the number of converter cells. Furthermore, a comprehensive optimization of the entire system with respect to efficiency and volume has been performed and the applied component loss models are described in detail. The achievable performance of the system is compared to a leading edge state-of-the-art single-cell converter system which currently sets the benchmark in terms of efficiency and power-density. In addition, the degrees of freedom of multi-cell converter systems in terms of converter operation are outlined and optimum control schemes are derived.

I. INTRODUCTION

Today's single-phase telecom power supply modules usually comprise a PFC rectifier stage and an isolated DC-DC converter output stage, typically generating a nominal output voltage of 48 V. The rectifier stage in conventional power electronic systems is a boost-type PFC rectifier which consists of a full-bridge diode rectifier in connection with a boost converter. Since the forward voltage drops of the diodes in the rectifier account for high conduction losses, alternative topologies have gained significant interest over the past years [1], [2]. E.g. in [3] a triple-parallel-interleaved TCM PFC rectifier system is described in combination with a double-parallel-interleaved phase-shift full-bridge isolated DC-DC converter for telecom applications (rated power $P_{\text{out}} = 3.3\text{ kW}$, output voltage $V_{\text{out}} = 48\text{ V}$) featuring a power density of $\rho = 3.3\text{ kW/dm}^3$ and an efficiency of $\eta = 97\%$ at half of the rated power. As shown in [4], this concept currently presents the leading edge technology for telecom power supplies and therefore serves as a benchmark system in this paper.

A new approach towards a hyper-efficient and super-compact telecom rectifier design beyond the barriers of traditional converter concepts is presented in this paper. The approach is based on a multi-cell converter concept that leverages the advantages obtained by employing multiple series-parallel connected converter cells instead of a single converter, such as lower conduction and switching losses and reduction of harmonics by interleaving [5]. The performance targets that can be achieved with this approach are an output power of $P_{\text{out}} = 3.3\text{ kW}$ with a conversion efficiency of 98% at part

load operation and a power density of $\rho = 3.3\text{ kW/dm}^3$.

A multi-cell telecom power supply with series connection of the cells at the input side and parallel connection at the output side can essentially be realized in three different ways, as shown in Fig. 1. Common to all three concepts is the application of multiple converter cells that equally share the input voltage and, by means of isolated DC-DC converters, are connected to the same output capacitor. This way of connecting converter cells is commonly termed input series output parallel (ISOP) concept. The three systems differ concerning the rectification of the sinusoidal mains voltage. In Fig. 1(a) a full-bridge diode rectifier is utilized, similar to a conventional boost PFC rectifier but with the difference that the boost stage is split up into multiple stages which are placed at the input of the converter cells. Since this diode full-bridge leads to significant conduction losses, this option will be discarded in this paper. In Fig. 1(b) and (c) the diode bridge is omitted and, instead, a full-bridge synchronous rectifier is integrated in each converter cell. The mains side inductor (L_g) can either be realized as a single inductor for the whole converter system (i.e. Fig. 1(b)) or by distributed inductors, each associated to one converter cell (i.e. Fig. 1(c)).

In the following, the optimization and the design of the multi-cell system of Fig. 1(b) are described. At first, in Sec. II fundamental scaling laws of power electronic systems which highlight the advantages of multi-cell converters are described. In Sec. III the available degrees of freedom in the design of a multi-cell converter system are analyzed, the modeling of the losses and volumes of the employed components is outlined and the optimization results are discussed. In Sec. IV an optimal control of the multi-cell converter is presented based on the degrees of freedom in the operation of the individual converter cells. Finally, conclusion are drawn in Sec. V.

II. FUNDAMENTAL SCALING LAWS

In this section the benefits offered by a multi-cell AC-DC rectifier system compared to its single-cell converter counterpart are presented. The discussion is based on the fundamental scaling laws of both parallel- and series-interleaved DC-DC converter systems which have been published in [5] and are now applied to the AC-DC multi-cell converter system at hand.

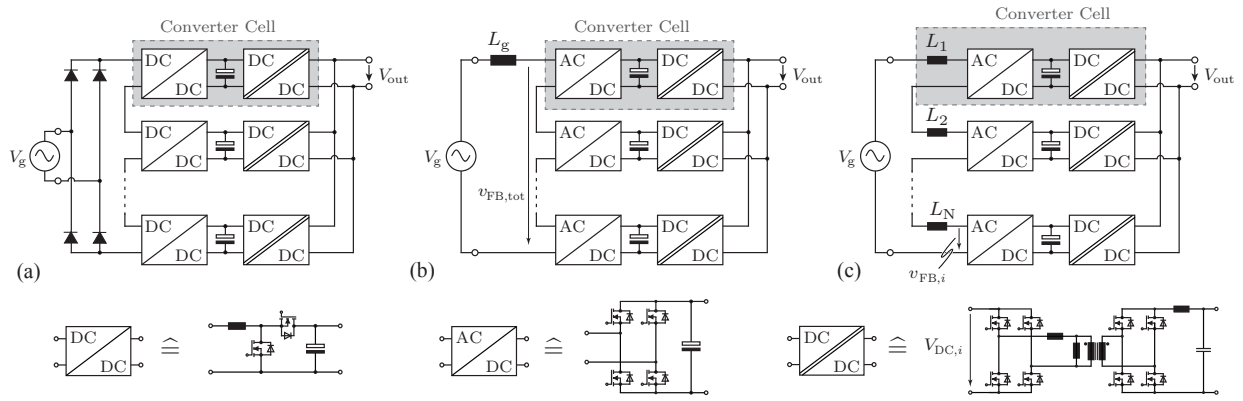


Fig. 1: Multi-cell telecom power supply module topologies: (a) input side diode rectifier with converter cells containing a DC/DC boost converter (processing a time-varying input voltage) and an isolated DC/DC converter connected in series; (b) and (c) topologies with AC-DC rectifier input stages in each converter cell with either a single line inductor (b) or distributed line inductance (c) and an isolated bidirectional DC-DC converter per cell.

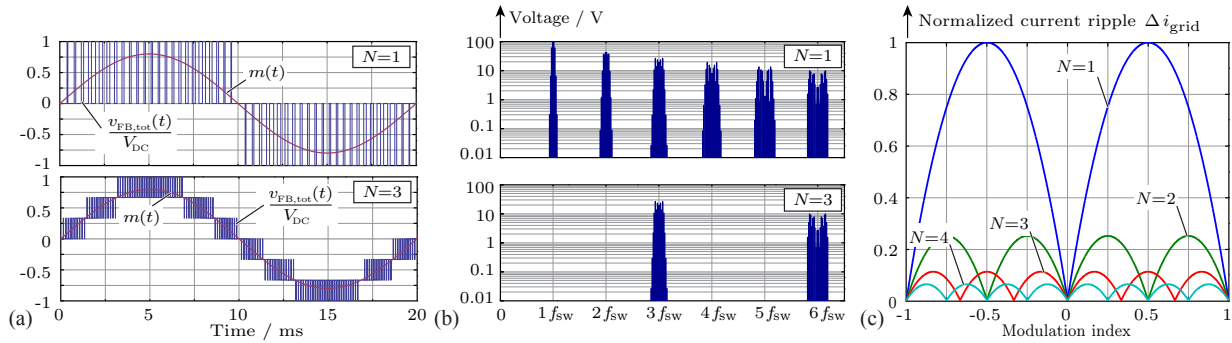


Fig. 2: Effect of multiple rectifier stages with phase-shifted modulation on the system behavior: (a) comparison of the switched voltage waveform between a multi-cell system with three cells and a single-cell converter system; (b) harmonic spectrum of a single rectifier stage with switching frequency f_{sw} (top) and harmonic spectrum of a system with three interleaved rectifier stages (bottom); (c) peak-to-peak current ripple of grid current i_{grid} (normalized to $V_{DC}/(4f_{sw}L_g)$) for different numbers of rectifier stages N in dependency of the modulation index $m = v_{FB,tot}/V_{DC}$.

A. Switching frequency and harmonic spectrum

The AC-DC stages of the multi-cell systems of **Fig. 1(b)** and **(c)** comprise multiple series connected full-bridge switching stages that are advantageously operated with a phase-shifted (interleaved) modulation scheme considering a phase shift of $\delta_{ph} = 2\pi/N$ with N being the number of converter cells. In the simplest case only one bridge leg of each cell is operated at switching frequency f_{sw} while the other bridge leg is operated at mains frequency f_g . This modulation method is commonly referred to as totem pole modulation. For a system with N series-connected and interleaved full-bridge cells, this results in an effective switching frequency $f_{sw,eff}$ of the entire rectifier stage which is N times higher than the switching frequency f_{sw} of a single cell, i.e. $f_{sw,eff} = N \cdot f_{sw}$. The total capacitor voltage V_{DC} required for the operation of the PFC rectifier (i.e. sufficiently above the peak value of the mains voltage \hat{V}_g) is distributed among N capacitors, each being charged to $V_{DC,i} = V_{DC}/N$. As a result, the voltage $v_{FB,tot}$ (i.e. sum of all rectifier stage voltages $v_{FB,i}$) comprises $2 \cdot N + 1$ possible voltage levels, as shown in **Fig. 2(a)**. This, in combination with the higher effective switching frequency, leads to a significantly reduced ripple of the mains current i_g for a given inductance of the line inductor L_g and also to an improved EMI behavior as described in the following.

Based on [6] the amplitude $\hat{V}_{FB,i}$ of a harmonic with order q of

the mains frequency $f_g = 1/T_g$ can be calculated for a single full-bridge stage for a modulation index $m(t) = v_{FB,tot}(t)/V_{DC}$ as

$$\hat{V}_{FB,i(q)} = \frac{-4 \cdot V_{DC} \cdot (1 - (-1)^k)}{n\pi T_g} \cdot \int_0^{T_g/4} \cos(k \cdot \omega_g \cdot t) \cdot \sin(n \cdot \pi \cdot m(t)) dt \quad (1)$$

with $q = n \cdot z + k$, $z = f_{sw}/f_g$ and $|k| \leq z/2$ where $n, k \in \mathbb{N}$, under the assumption of $z \gg 1$. In a system with N rectifier cells the time dependent waveform of a harmonic with order q of the converter input voltage $v_{FB,tot}$ can now be expressed as a sum of voltages of all cells, taking into account the phase-shifted carrier signals,

$$\hat{V}_{FB,tot(q)}(t) = \sum_{i=1}^N \frac{\hat{V}_{FB,1(q)}}{N} \cos\left(q \cdot \left(2\pi f_g t + \frac{2\pi}{z \cdot N} (i-1)\right)\right) \quad (2)$$

By assuming $z \rightarrow \infty$, the above mentioned formula converges to the simplified expression of

$$\hat{V}_{FB,tot,i(q)}(t) = \begin{cases} \hat{V}_{FB(q)} \cos(q \cdot (2\pi f_g t)), & \text{if } n = l \cdot N, l \in \mathbb{N} \\ 0, & \text{else.} \end{cases} \quad (3)$$

This means, that the harmonic spectrum of the multi-cell system can be derived from the spectrum of a single stage

by considering only the harmonics $q = n \cdot z + k$ with orders that are multiples of the number of converter cells N , i.e. $n = l \cdot N$, $l \in \mathbb{N}$, as visualized in **Fig. 2(b)** for a simplified system with three rectifier stages.

Furthermore, with a higher effective switching frequency and an improved harmonic spectrum of the rectifier voltage, also the current ripple Δi_g of the mains current i_g decreases. The current ripple can be calculated in dependency of the modulation index m by introducing an effective modulation index $m_{\text{eff}} = (m \text{ modulo } 1/N)$ with the relation of $v = L di/dt$ as

$$\Delta i_g(m_{\text{eff}}) = \frac{V_{\text{DC}}}{L_g f_{\text{sw}}} \cdot m_{\text{eff}} \cdot \left(\frac{1}{N} - m_{\text{eff}} \right). \quad (4)$$

(cf. [7]). This relation is shown in **Fig. 2(c)** normalized to $V_{\text{DC}}/(4f_{\text{sw}}L_g)$. The maximum peak-to-peak value of the grid current ripple can be found at $m_{\text{eff}} = 0.5$ as

$$\Delta i_{g,\text{max}} = \frac{V_{\text{DC}}}{4N^2 f_{\text{sw}} L_g}. \quad (5)$$

As a result, by increasing the number of cells, N , with the same switching frequency, the current ripple of the input current decreases quadratically for a given line inductor L_g .

B. Impedance of the commutation cells

In each converter cell of the multi-cell converter the switches and the attached DC-link capacitor create a commutation cell, which is shown for the simplified case of a unidirectional half-bridge with a constant current source of I_L in **Fig. 3(a)**. The commutation loop contains an inductance L_σ which represents all parasitic inductances of the commutation loop, i.e. inductances due to the semiconductor packages, the PCB or the capacitor leads. At the turn-off of the MOSFET the parasitic inductance L_σ causes an over-voltage Δv_0 , depending on the duration of the switching transition t_s and the load current I_L ,

$$\Delta v_0 = L_\sigma \cdot \frac{I_L}{t_s} \leq k \cdot V_0. \quad (6)$$

The overvoltage is related to the capacitor voltage V_0 such that a constraint for a maximum permissible overvoltage $k \cdot V_0$ is given, as visualized in **Fig. 3(b)**. By introducing the impedance $Z_0 = V_0/I_L$ this inequality can be rearranged to [8]

$$Z_0 = \frac{V_0}{I_L} \geq \frac{L_\sigma}{k \cdot t_s}. \quad (7)$$

Thus, for a given impedance of the converter cell the parasitic loop inductance has to be lower than a specific value, which is visualized for a relative overvoltage of 10% ($k = 0.1$) and different switching transition durations t_s in **Fig. 3(c)**. By paralleling converter cells the current I_L is split up among the converter cells, thus their impedance is increased

$$Z_{0,\text{par}} = \frac{V_0 \cdot N}{I_L} = N \cdot Z_0 \quad (8)$$

while connecting converter cells in series distributes the voltage among the converter cells and thus decreases the impedance

$$Z_{0,\text{ser}} = \frac{V_0}{I_L \cdot N} = \frac{Z_0}{N}. \quad (9)$$

As a result, it is especially important for series connected converter cells to keep the parasitic loop inductance limited to small values, for example by using lead-less semiconductor packages, in order to avoid transient over-voltages at the switches.

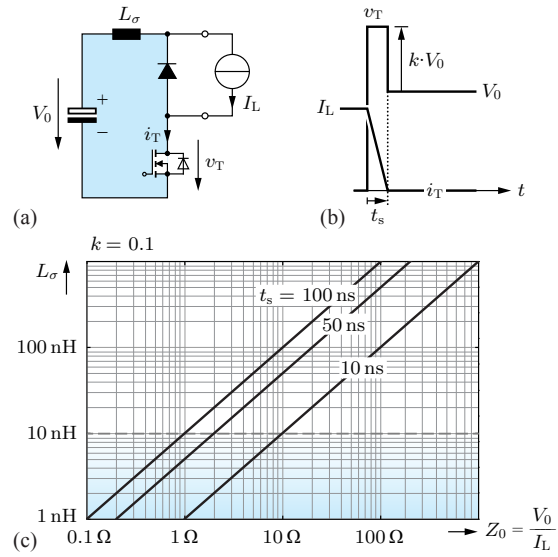


Fig. 3: Influence of the parasitic commutation loop inductance on the switching over-voltage during switching transients: (a) commutation cell consisting of a DC-link capacitor, a transistor, a freewheeling diode, an inductive load and a parasitic loop inductance L_σ ; (b) the turn-off transition of the transistor causes a voltage overshoot of kV_0 of the transistor voltage v_T during the time t_s of the switching transient; (c) maximum allowed loop inductance L_σ for different impedance values $Z_0 = V_0/I_L$ of the commutation cell and different values of the transition time t_s such that the voltage overshoot is below 10% of the DC-link voltage V_0 (i.e. $k = 0.1$).

C. Further scaling laws

The series and/or parallel connection of converter cells provides several advantages which are presented in [5] and are briefly summarized subsequently for the sake of completeness.

- **Conduction losses:** The series connection of converter cells with individual DC-links allows to use semiconductor devices with a blocking voltage of only V_{DS}/N . By considering the so-called Silicon limit it can be derived that the total $R_{\text{DS,on}}$ of multiple series connected MOSFETs shows a lower value of than given for a single MOSFET blocking the full voltage. This holds true also for the case that the total employed chip area of the series connected devices is equal to the chip area of the single semiconductor.
- **Switching losses:** For both series- and parallel-interleaved converter cells the switching losses scale advantageously with an increasing number of converter cells. This is due to the fact, that the voltage or the current, respectively, is split up among multiple semiconductors. For a given switching speed (i.e. di/dt and du/dt) the losses resulting from the overlap of current and voltage during the switching transients are reduced, as the switching speed is effectively increased.
- **Inductor volume:** For parallel connected converter cells the total amount of stored energy in the associated inductors decreases with increasing number of cells until the DC-value of the conducted current in each inductor becomes negligible compared to the current ripple. Since the stored energy in inductors is related to their volume [9], the total inductor volume in parallel-interleaved systems also decreases.
- **Heatsink volume:** In multi-cell converters the transferred

Tab. I: Specifications of the multi-cell telecom rectifier module.

Parameter	Variable	Value
Nominal grid voltage	$V_{\text{grid,RMS,nom}}$	230 V / 50 Hz
Grid voltage range	$V_{\text{grid,RMS}}$	180 V - 270 V
Rated output power	P_{out}	3.3 kW
Nominal output voltage	$V_{\text{out,nom}}$	48 V
Output voltage range	V_{out}	40 V - 60 V
Hold-up time	T_{hold}	10 ms at rated power
Switching freq. per cell	f_{sw}	≥ 18 kHz
Conversion efficiency	η	$\geq 98\%$
Power density	ρ	≥ 3 kW/dm ³
EMI standards		CISPR Class A and B

power and thereby also the losses are equally distributed among the converter cells if operated with a common duty-cycle. Due to the spreading of the losses among the cells the required thermal resistances of the heat-sinks for the semiconductors are substantially lower and in many cases, e.g. for low voltage MOSFETs, the heat transfer capabilities of the underlying PCB are sufficient such that no external heat-sinks are required.

III. CONVERTER OPTIMIZATION

In order to identify the Pareto performance limits of the proposed multi-cell telecom power supply module (the full set of specifications can be found in **Tab. I**) with respect to efficiency and power density, a comprehensive converter optimization has to be performed taking into account all available degrees of freedom. This requires to calculate for all possible converter designs the losses and volumes by means of analytical models of the losses and volumes of each type of components.

A. Optimization degrees of freedom

The most basic degree of freedom in the design of multi-cell converter system is the multi-cell topology itself, i.e. the interconnection of the converter cells. All multi-cell converters can be classified into one of the following categories: input series output parallel (ISOP), input series output series (ISOS), input parallel output parallel (IPOP) and input parallel output series (IPOS). In the case at hand the ISOP structure is selected since it inherently provides a step-down voltage conversion ratio of $1/N$, depending on the number of employed converter cells N as also utilized in [10] for a DC-DC power supply. Another benefit of the ISOP structure is that the input voltage and output current are naturally balanced among the converter cells [11], [12].

The choice of the converter topologies for the AC-DC and the isolated DC-DC stages is an additional degree of freedom. As already mentioned in **Sec. II**, the AC-DC rectifier stage is a full-bridge rectifier operated in totem pole mode. For the isolated DC-DC converter a phase-shifted full bridge converter with synchronous rectification is chosen, as it provides easy controllability and high efficiency.

Another degree of freedom offered by multi-cell systems is the number of converter cells N . With increasing N the benefits of the scaling laws of **Sec. II** are leveraged to a larger extent, however the communication overhead and the constant losses associated with each converter cell also increase. Thus, for the optimization algorithm the range for the number of cells

is limited to $N = [3...10]$.

The converter system and especially the DC-link capacitors have to be designed for the worst case such that it can still transfer power to the load during a grid outage of a mains half-period $T_{\text{hold}} = 10$ ms, i.e. hold-up time. This inevitably leads to a voltage drop in the DC-link, depending on the overall energy stored in the DC-link. Thus, a maximum permissible drop of the DC-link voltage has to be specified for the design of the system and is therefore an additional degree of freedom for the optimization.

Once the above specified global degrees of freedom are determined, the individual converter stages (i.e. the AC-DC and the DC-DC stage) can be optimized independently from each other, since the interface between the two stages is defined by the maximum drop of the DC-link voltage¹. For each converter stage, multiple optimization parameters/constraints can be identified:

AC-DC rectifiers:

- **Switching frequency:** The lower limit of the switching frequency of each cell is deducted from the audible frequency range and thus should not be lower than $f_{\text{sw}} \geq 18$ kHz. An upper boundary of the switching frequency is not inherently given; however, the CISPR EMI standards impose limits on the harmonics in the frequency range above $f_{\text{EMI}} \geq 150$ kHz [13]. Thus, an upper boundary of the switching frequency per cell can be derived as $f_{\text{sw}} < f_{\text{EMI}}/N$.
- **Boost inductor realization:** The boost inductor design constitutes an Pareto-optimization problem on its own. The design parameters of an inductor for a given value of inductance and peak current are the core material, core size, number of turns, conductor type, conductor size and the air-gap.
- **MOSFET chip-size and junction temperature:** For a given blocking voltage the MOSFETs can be optimized with respect to the total losses by adjusting the chip size [3]. Furthermore, the junction temperature is another degree of freedom which allows for a trade-off between conduction losses and heat-sink volume.
- **DC-link capacitor realization:** For a required capacitance of the DC-link, which is determined by the maximum drop of the DC-link voltage, different realizations in terms of number of capacitors and size of capacitors are possible. For the case at hand, electrolytic capacitors are chosen for the optimization. In the experimental setup some ceramic capacitors with low equivalent series inductance (ESL) will be used in addition to reduce the parasitic loop inductance of the commutation cells.
- **Input filter design:** The input filter which is needed to suppress harmonics such that the EMI standards are fulfilled can be designed with different numbers of stages.

Isolated DC-DC converters: The MOSFET optimization and the inductor optimization follow the same constraints as described above for the AC-DC rectifier and are therefore not mentioned below.

- **Switching frequency:** The switching frequency is an important parameter for the design of the DC-DC converter as it influences the transformer design, the output inductor design and to some extent also the losses in

¹The DC-link capacitors are allocated to the AC-DC stage.

the MOSFETs. The effective frequency at the output inductor is twice the switching frequency of the full-bridge rectification. The range of the switching frequency for the optimization is set to $f_{sw,DCDC} = [100...300 \text{ kHz}]$.

- Transformer realization: The design of transformers offers the same degrees of freedom as given for inductors with the additional option, that the conductor types and diameters for the primary and secondary winding can be different.

B. Component loss and volume models

In order to determine the performance of a converter design in terms of efficiency and power density, the losses and volumes of all employed components have to be calculated. This can be done with following component specific models:

- MOSFETs: In order to perform a chip-size optimization, the conduction and switching losses of the MOSFETs have to be described in dependence of the chip size A_{chip} . For the AC-DC rectifier, the losses have to be calculated as an average value over a mains period. The conduction losses can be calculated with the RMS current I_{RMS} of a MOSFET as

$$P_{MOSFET,cond}(T_{jct}, A_{chip}) = I_{RMS}^2 \cdot R_{DS,on}(T_{jct}, A_{chip}) \cdot \quad (10)$$

The switching losses of the MOSFETs depend on the specific layout of the commutation loop (e.g. the parasitic loop inductance) and thus are difficult to precisely calculate. However, a fairly good approximation can be obtained by taking into account different loss mechanisms of the switching process, such as the stored charge in the parasitic drain-source capacitances, the reverse recovery charge of the intrinsic body diodes and the gate drive losses [14], again in dependence of the chip size. Since the switching losses increase and the conduction losses decrease with larger chip size, an optimal value of the chip size leading to the lowest total losses can be found. The thermal resistance of the junction to the case is also influenced by the chip size. Thus, in the last step, the required heat-sink can be calculated based on the total MOSFET losses and the specified junction temperature. By considering the CSPI (cooling system performance index) for different types of heat-sinks, the volume of the heat-sink can be calculated based on the required value of $R_{Th,HS}$.

- Inductive components: The losses of inductors and transformers can be divided into winding and core losses. Analytical models are available to calculate both loss components. The core losses can be determined for arbitrary waveforms of the flux with the improved generalized Steinmetz equation (iGSE) and by use of loss maps also for DC offsets in the flux [15]. The winding losses consist of DC losses and AC current losses (skin and proximity effect) which can be calculated based on [16]. A thermal impedance network is applied to adequately model the heat-transfer within the inductive components which also impacts the losses in both the core and the windings.
- DC-link capacitors: The electrolytic DC-link capacitors have to carry an RMS current which creates losses in connection with the equivalent series resistance (ESR) of the capacitors. Since the ESR is frequency dependent,

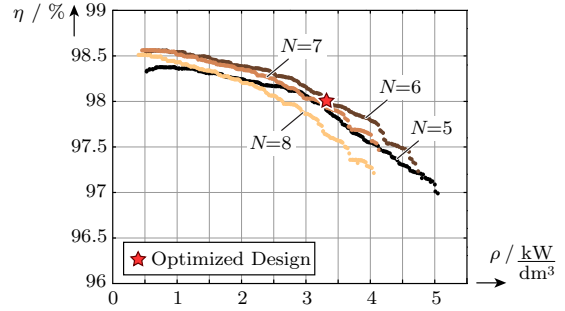


Fig. 4: Pareto-optimal (efficiency / power-density) designs of the multi-cell telecom power supply module for different numbers of converter cells and a drop of the DC-link voltage during the hold-up time of $k_{DC,drop} = 20\%$.

the total losses are the sum of the losses at twice the fundamental frequency and at the switching frequency of the AC-DC stage. Furthermore, each capacitor exhibits a leakage current which has to be taken into account, too.

- Input filter: The volume of the input filter has been taken into the optimization by models which translate the required filter attenuation for different number of filter stages into component volumes [17].
- Auxiliary electronics: For the losses attributed to auxiliary electronics (e.g. for a digital signal processor, voltage and current sensing) on each converter cell constant losses of $P_{cell,const} = 800 \text{ mW}$ are estimated and for the central controller constant losses of $P_{centr,const} = 1.2 \text{ W}$ are considered.

C. Optimization results

The Pareto-limits resulting from the optimization for the entire multi-cell converter system of **Fig. 1(b)** are depicted in **Fig. 4** for full load operation at the nominal operating point for different numbers of converter cells and a maximum permissible drop of the DC-link voltage during the hold-up time of $k_{DC,drop} = 20\%$. It can be seen that the optimum number of converter cells is $N_{opt} = 6$ where the target specifications of $\eta = 98\%$ and $\rho = 3.3 \text{ kW/dm}^3$ (calculated by summing up the boxed volumes of all components) are met. The full set of design parameters of the optimized system can be found in **Tab. II**. Even though the scaling laws of **Sec. II** suggest that increasing the number of cells improves the system performance, there are limiting factors which lead to a decline of the performance with larger numbers of converter cells:

- EMI filter: With a lower switching frequency limit of $f_{sw,cell} = 18 \text{ kHz}$ the effective switching frequency of the system with $N = 8$ cells is at $f_{sw,eff} = 144 \text{ kHz}$ and therefore already at the border to the EMI constrained frequency spectrum. With slightly larger cell switching frequencies, the effective switching frequency falls within the limited spectrum and the EMI filter increases due to a larger required attenuation.
- MOSFETs: Even though the silicon limit can be overcome with series connected MOSFETs, at some point with a larger number of devices, the gain is outweighed by the package resistances [18].
- DC-link capacitors: By increasing the number of cells, the voltage at each DC-link capacitor decreases. At

Tab. II: Design parameters of the final system with $N = 6$ converter cells. (All values given per component if not otherwise noted.)

AC-DC rectifier	
Switching frequency	$f_{sw,cell} = 23$ kHz
Boost inductance	AMCC-125, 2605SA1, 110 μ H
MOSFETs	2xBSC046N10NS3G, 100 V, 4.6 m Ω
DC-link cap.	5xEPCOS B41505, alum. elect., 80 V
EMI filter	3rd order, 7.4 μ H, 660 nF
DC-DC converter	
Switching frequency	$f_{sw} = 125$ kHz
Transformer	2xE34/14/9, N87, EPCOS
Inductance	E34/14/9, N87, EPCOS, 11 μ H
Prim. MOSFETs	2xBSC046N10NS3G, 100 V, 4.6 m Ω
Sec. MOSFETs	BSC046N10NS3G, 100 V, 4.6 m Ω

lower voltages, however, the energy density of electrolytic capacitors decreases and since the energy of the entire system stored in all DC-link capacitors is given by the hold-up requirement, i.e. does not change with the number of cells, the total volume of the DC-link capacitors increases with increasing number of cells.

- Parallel connected DC-DC converters: The total volume of the output inductors of the parallel connected DC-DC converters decreases since the stored energy reduces along with lower DC current values. However, with larger numbers of converter cells the DC component of the current becomes negligible and the stored energy is mainly defined by the ripple current and therefore constant. Thus, by further increasing the number of cells, the total energy and therefore also the total volume increase again.

An optimum value can also be found for the maximum permissible drop of the DC-link voltage during the hold-up time. In **Fig. 5(a)** the Pareto-optimal results are shown for the entire system for different values of $k_{DC,drop}$ for $N = N_{opt} = 6$. The results are examined in greater detail in **Fig. 5(b)** and **Fig. 5(c)** which depict the individual results for AC-DC rectifier stage and DC-DC conversion stage, respectively. Based on these results an optimum value of $k_{DC,drop,opt} = 20\%$ can be deduced. The trade-offs leading to this optimal value are described in the following:

- AC-DC rectifiers: In the AC-DC rectifier the value of $k_{DC,drop}$ mainly influences the losses and the size of the electrolytic DC-link capacitors. With a larger permissible voltage drop, lower capacitance values can be used within the cells. However, since the ESR of electrolytic capacitors increases with decreasing capacitance, the losses also

increase.

- DC-DC converters: The performance of the DC-DC converters deteriorates with larger values of $k_{DC,drop}$. This is due to the fact, that the transformer turns ratio has to be adjusted according to the lowest DC-link voltage value. Thus, at the nominal operating point a lower duty cycle of the DC-DC converter is required which results in larger RMS current values in the transformer and the input full bridge switches and therefore in higher losses.

In **Fig. 6(a)** and **(b)** a loss and volume breakdown, respectively, is provided for the optimized system operating at full load at nominal voltages.

IV. OPTIMAL CONTROL

Multi-cell converter systems in ISOP configuration are usually operated with a common duty cycle for all rectifier stages and all DC-DC converter stages, since the system possesses a natural balancing capability [11], [12]. This ensures an equal voltage sharing at the series connected inputs of the converter cells and an equal current sharing at the parallel connected outputs of the converter cells. The control and thus the duty cycles are adjusted according to the prevalent average quantities of an operating point. This means, that the output power determines the power which has to be delivered over a half-cycle of the mains period and all converter cells equally share the transferred power.

This modulation scheme, however, does not take into account the additional time-dependent degrees of freedom in the operation of a multi-cell converter that are provided by the time-varying input voltage and or input power of the system and the actual value of the load power which could be significantly lower than the rated power in part-load operation. Based on the instantaneous grid voltage and the required output power at a given point in time, the number of active rectifier cells and DC-DC converter stages, respectively, can be adjusted since the energy storage capability of the DC-link capacitors (designed for a hold-up requirement at rated power) allow to decouple the operation of both stages concerning the power flow. Thus, following degrees of freedom can be leveraged for improving the system performance [19]:

- Input voltage: At any given time the AC-DC rectifier stages have to provide a voltage $v_{FB,tot}(t)$ which is defined by the grid voltage, i.e. $v_g(t) = v_{FB,tot}(t)$ over a switching period. This allows to derive a minimum number of active rectifier stages $N_{v,min}$ that are required for the operation

$$N_{v,min} = \left\lceil \frac{v_g(t)}{V_{DC,i}} \right\rceil. \quad (11)$$

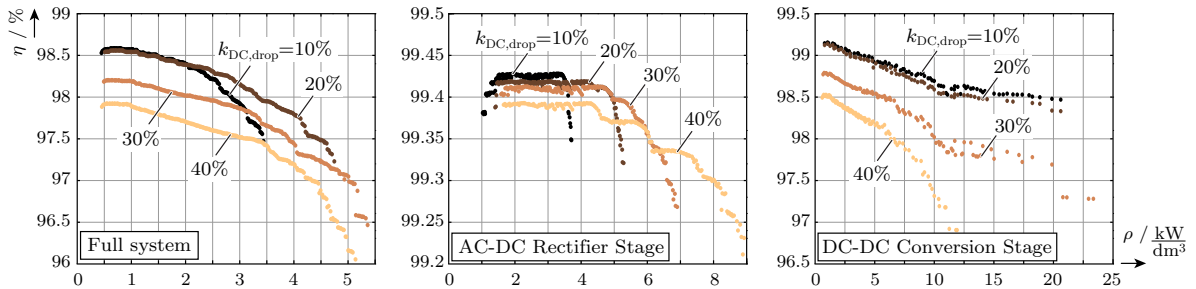


Fig. 5: Impact of different values of the maximum permissible drop of the DC-link voltage during the hold-up time on the achievable Pareto-optimal results of the entire system, the AC-DC rectifier stages and the DC-DC converter stages.

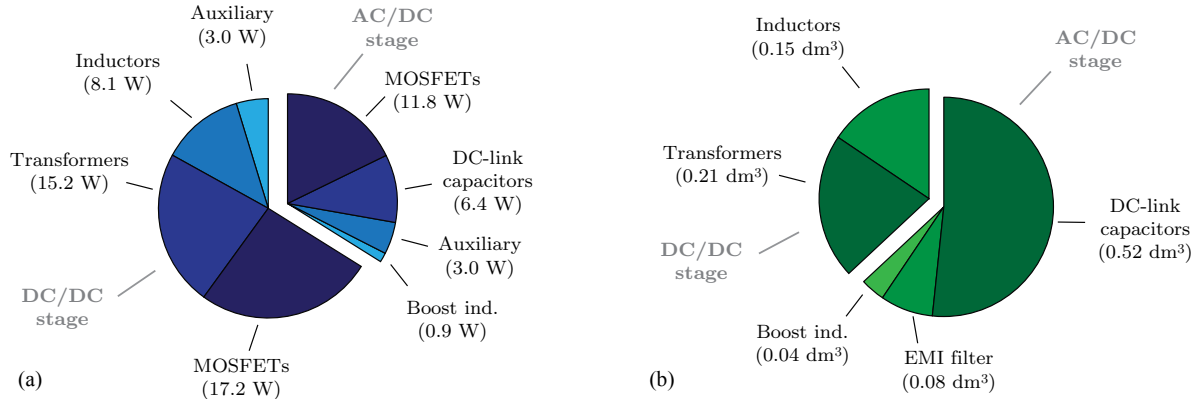


Fig. 6: Break-down of the losses (a) and the volume (b) for the optimized converter design of the multi-cell telecom power supply module.

However, any number of cells $N_{v,op}$ between the minimum number $N_{v,min}$ and the actual number of employed converter cells $N_{cells} = N$ can be used for the operation. In addition, the modulation indices m_i of the individual rectifier stages can be chosen to be different, the only mandatory condition that has to be fulfilled is the formation of the required total voltage during a switching period

$$v_{FB,tot}(t) = \sum_{i=1}^{N_{cells}} v_{FB,i}(t) . \quad (12)$$

Furthermore, the modulation technique used for the individual stages does not necessarily have to be the same. It might be possible, for example, to operate a subset of cells out of $N_{v,op}$ with fundamental frequency modulation while the remaining cells are operated with PWM technique [20], [21]. It is also possible to operate the PWM controlled cells with a time-varying switching frequency.

- Output current: The power $p_{con,tot}(t)$ which is transferred by the parallel connected DC-DC converters has to be equal to the power of the load $p_{load}(t)$ at any given time under the assumption of a negligible output capacitance

$$p_{load}(t) = p_{con,tot} = \sum_{i=1}^{N_{cells}} p_{FB,i}(t) . \quad (13)$$

Since each converter cell has a maximum power rating, a minimum number of converter cells $N_{p,min}$ required for the power transfer can be derived as

$$N_{p,min} = \left\lceil \frac{p_{load}(t)}{p_{con,max}} \right\rceil . \quad (14)$$

However, comparable to the input voltage criterion, any number of converter cells $N_{p,op}$ between the minimum number $N_{p,min}$ and the number of available cells, N_{cells} , can be operated. Furthermore, the cells $N_{p,op}$ can transfer different values of power. Even though a DC power quantity is requested by the load, the converter cells might operate at time-varying power levels, e.g. following a mission profile or operating in burst mode in order to reach a high efficiency [3], as long as (13) is satisfied.

- DC link capacitor: The capacitance of the DC-link capacitors allows a power flow of the rectifier stages different from the power flow of the DC-DC converters. This means, that by utilizing the energy storage capability of the DC-link capacitors the number of active AC-DC

rectifier stages $N_{v,op}$ can be different to the number of active DC-DC converter stages $N_{p,op}$. The only constraint is, that the average power transferred by the DC-link capacitors is zero on average over a certain time interval. But especially at low levels of the load power, the voltage variation of the DC-link is comparably small since the capacitance of the DC-link capacitors is designed for a worst case of a mains outage during half a mains period. In that case it might be sufficient to ensure the power transferred by the DC-link capacitors is equal to zero on average over a number of grid cycles.

In general, the above mentioned degrees of freedom can also be applied to other multi-cell converter configurations, since the voltage criterion of (12) is applicable to series connected converter cells whereas the power criterion of (13) is applicable to parallel connected converter cells.

For the ISOP multi-cell telecom power supply module an optimal control scheme can be derived taking the aforementioned degrees of freedom into account. For the parallel connected DC-DC converters the most efficient operation can be found by assuming a generic loss function of each converter cell depending on the output power as

$$p_{loss} = k_0 + k_1 \cdot p_{out} + k_2 \cdot p_{out}^2 \quad (15)$$

where k_0 models the constant losses (e.g. auxiliary electronics), $k_1 \cdot p_{out}$ the linearly dependent losses (e.g. a diode voltage drop) and $k_2 \cdot p_{out}^2$ the quadratically dependent losses (e.g. resistive losses). The total losses of the DC-DC converter stage comprising N_{cells} cells can thus be written as

$$p_{losses,tot} = N \cdot k_0 + k_1 \cdot \sum_{i=1}^{N_{cells}} p_{out} + k_2 \cdot \sum_{i=1}^{N_{cells}} p_{out}^2 . \quad (16)$$

By applying the Lagrangian method to the minimization problem of (16) under the constraint of (13) following solution can be found for the general case

$$p_{out,1,opt} = p_{out,2,opt} = \dots = p_{out,N,opt} = \frac{p_{out}}{N_{cells}} \quad (17)$$

under which the total losses are minimized. By inserting the solution of (17) in (16) the total losses can be simplified to

$$p_{losses,tot} = N_{cells} \cdot k_0 + k_1 \cdot p_{out} + k_2 \cdot \frac{p_{out}^2}{N_{cells}} . \quad (18)$$

The remaining optimization parameter is the optimum number of active DC-DC converters $N_{opt} \in [N_{p,min}, N_{cells}]$ used for the

power transfer for maximum efficiency. By differentiating (18) with respect to N and setting it equal to zero, the solution for the optimal number of active cells can be found as

$$N_{\text{opt}} = \sqrt{\frac{k_2}{k_0}} \cdot p_{\text{out}} \quad (19)$$

For the AC-DC rectifier stage, an optimum control scheme might not necessarily aim at a high efficiency. Since the converter is connected to the low-voltage grid the compliance with EMI standards is mandatory and thus an optimization goal might primarily focus on the lowest possible harmonic emissions. Thus, a control scheme with varying switching frequencies can lead to a spreading of the harmonics over a broader frequency range and, in consequence, to a smaller EMI filter.

Another concept uses the fact that during part-load operation one or more DC-DC converters might be inactive. Their connected full-bridge AC-DC rectifier cells in connection with the DC-link capacitors can then be used to create a switching frequency ripple compensation signal such that a closer approximation of a sinusoidal converter voltage is obtained, similar to the concept in [21].

V. CONCLUSION

A new approach towards a highly efficient and very compact telecom rectifier module beyond the limits of state-of-the-art systems is presented. Based on fundamental scaling laws, the benefits of a multi-cell converter system are derived in comparison to a single converter system. The degrees of freedom in the design procedure of a multi-cell telecom power supply module in ISOP configuration are outlined and the optimization process is described in detail. The optimization results show that a converter design with an efficiency of $\eta = 98\%$ and a power density of $\rho = 3.3 \text{ kW/dm}^3$ can be achieved. The results also reveal an optimum value of $N = 6$ for the number of converter cells and an optimum maximum permissible drop of 20% the DC-link voltage during the hold-up time. Furthermore, the degrees of freedom in the operation of multi-cell systems in general and the ISOP converter in particular are discussed. Based on these degrees of freedom, different new control concepts are presented which allow for an optimal operation of the converter system as will be theoretically and experimentally verified in the course of future research.

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