Power Electronic Systems
Laboratory

Proceedings of the 15th International Power Electronics and Motion Control Conference (ECCE Europe 2012), Novi Sad, Serbia, September 4-6, 2012

Three-Phase Harmonic Reducing Diode Rectifier

Y. Nishida,
H. Ohyama,
P. Pejovic,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Three-Phase Harmonic Reducing Diode Rectifier

Yasuyuki NISHIDA [1], Hiromichi. OHYAMA [1], Predrag PEJOVIC [2] and Johann W. KOLAR [3]

[1]Chiba Institute of Technology, Tsudanuma, Narashino, Chiba, Japan, E-mail: nishida_yas@nifty.com
[2]University of Belgrade, Belgrade, Serbia, E-mail: peja@etf.rs
[3]Swiss Federal Institute of Technology, Zurich, Switzerland, E-mail: kolar@lem.ee.ethz.ch

Abstract — Diode rectifiers are essential utility interfaces for several power converter systems and those provide useful characteristics such as cheap, light weight, compact, high efficiency, lower producing EMI noises, robust for fault high current and etc. Only the unwanted feature of the diode rectifiers is greatly distorted input current which may cause harmonic pollution in power systems. The authors propose a 24-pulse three-phase diode rectifier by means of a simple and unique topology. In this paper, the topology and operating principle are shown and the performance and the practicability are validated through experiments.

Keywords — diode rectifier, multi-pulse, PFC, utility interface, harmonics, total-harmonic-distortion

I. INTRODUCTION

Diode rectifiers are essential utility-interface for several power converter systems and those provide useful characteristics such as cheap, light weight, compact, high efficiency, lower producing EMI noises, robust for fault high current, low emission noises and etc. Only the unwanted feature of the diode rectifiers is greatly distorted input current which may cause harmonic pollution in power systems. To mitigate the harmonic pollution caused by rectifiers, several PFC schemes have been proposed and applied so far. The traditional multi-pulse scheme in three-phase diode rectifiers by means of isolation transformers for phase-shifting with full kVA (i.e., full power-conversion scale) and the modern PWM scheme are the major ones. This traditional multi-pulse scheme results in a bulky system due to the isolation transformer, while the PWM scheme results in lower reliability, lower robustness, higher cost, greater EMI noise. Instead of them, several simplified multi-pulse schemes have been proposed and practically applied recently. Unlike the traditional multi-pulse scheme with full kVA isolation transformer, this simplified multi-pulse schemes requires only an autotransformer of limited kVA and the size, weight, cost and efficiency are greatly improved compared with the traditional one[1]-[15].

Although 12-pulse and 18-pulse three-phase diode rectifiers with simplified topologies have been proposed and practically applied so far, a 24-pulse (or higher pulse number) diode rectifier is difficult to realize with a simple topology because the configuration of the autotransformer becomes very complicated and difficult to produce it with certain accuracy.

By the way, the authors have proposed the pulse-doubler scheme[15]-[23] for doubling pulse numbers of three-phase diode rectifiers (as well as voltage fed inverters). For example, a 6-pulse or a 12-pulse diode rectifier can be 12-pulse or 24-pulse one, respectively, by applying this pulse-doubler scheme, i.e., adding a small auxiliary circuit into the dc circuit of the original one. By hybridizing the simplified 12-pulse scheme with an autotransformer and the pulse doubler scheme with a small auxiliary circuit, we can obtain a simplified 24-pulse diode rectifier. In this study, the authors have applied the pulse-doubler scheme onto the simplified 12-pulse three-phase diode rectifier with the Line-Side Interphase Transformer (LIT) scheme[1]-[3], and this hybrid diode rectifier obtains the 24-pulse nature.

The theory to obtain the 24-pulse operation has been shown in this paper and it is confirmed through simulations and experiments.

II. CIRCUIT TOPOLOGY AND OPERATION

A. Circuit Topology

The topology of the new hybrid 24-pulse rectifier is shown in Figure 1. The rectifier circuit consists of two parts: the 12-pulse rectifier part with black color lines/parts and the pulse-doubler auxiliary part with blue color lines/parts.

The 12-pulse rectifier part consists of a three-phase voltage source (i.e., utility), an ac inductor L_{AC} to limit distortion of the utility currents (i_A, etc.), a LIT T_L, two three-phase diode bridge rectifiers (Rec.1 and Rec.2), a dc smoothing capacitor C_{DC} and a dc load R_O. By replacing the pulse-doubler part from the circuit and connecting the two dc output positive terminals (P_1 and P_2) directly to the dc output positive terminal P_O, this rectifier becomes the 12-pulse rectifier of LIT scheme. In this 12-pulse topology, the two diode rectifiers (Rec.1 and Rec.2) produce two sets of three-phase 6-pulse staircase voltages (υ_{XY1} etc. and υ_{XY2} etc.) on the ac-input side and the two three-phase voltages have phase displacement of 30 [deg] each other. The two sets of three-phase 6-pulse staircase voltages (υ_{XY1} etc. and υ_{XY2} etc.) are synthesized through the T_L and three-phase 12-pulse staircase voltages (υ_{XY0} etc.) are produced on the input of the T_L. Since the synthesized 12-pulse voltages (υ_{XY0} etc.) have much less distortion compared with a 6-pulse voltage, less inductance is required on the ac inductor L_{AC} to obtain utility line currents (i_A, etc) with certain quality of waveform (i.e., lower Total-Harmonic-Distortion (THD)).

The pulse-doubler part consists of only the DC-Side Interphase Transformer T_D with three intermediate taps

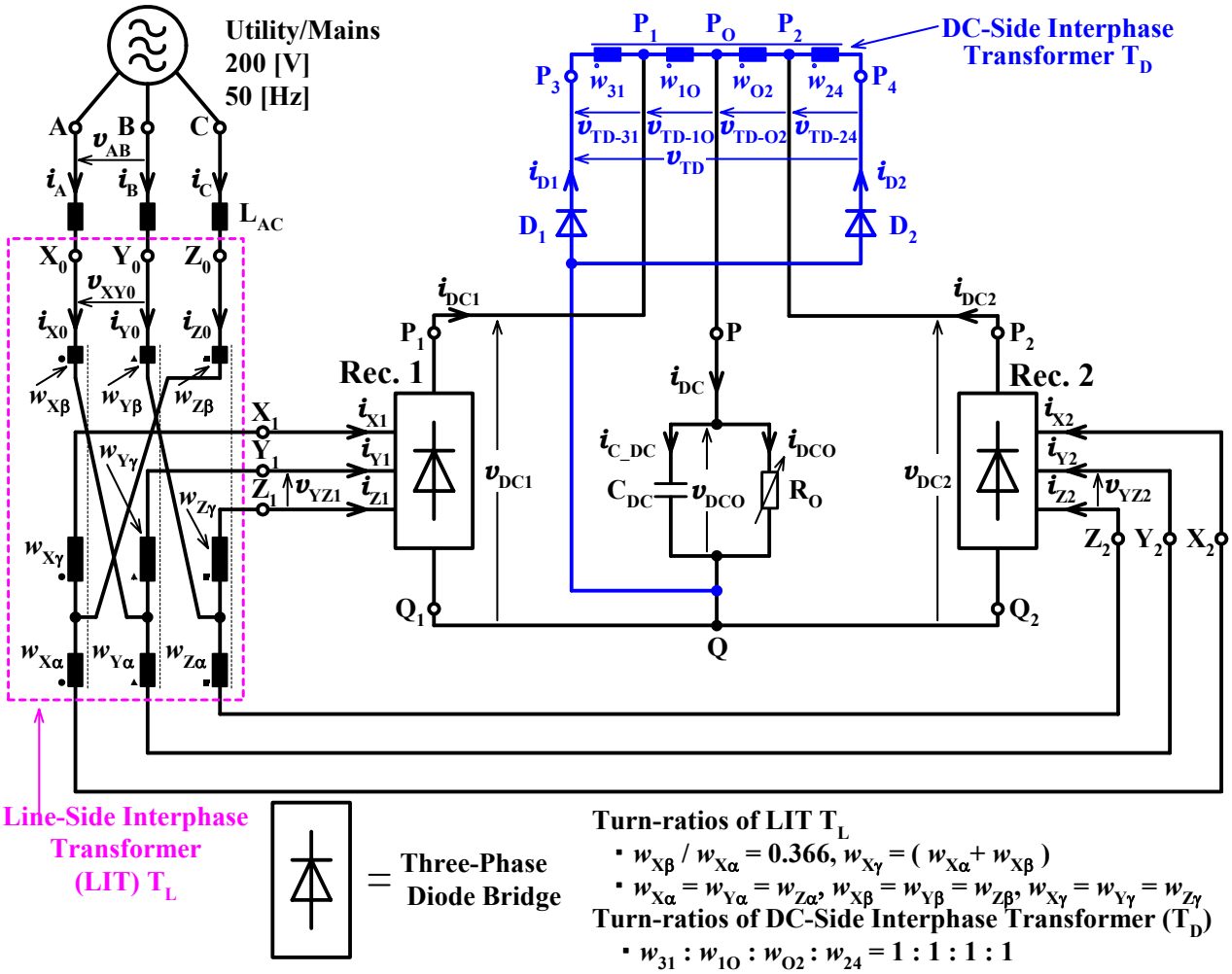


Fig.1. Circuit Topology for Three-Phase 24-Pulse Diode Rectifier

and two diodes. The theoretically optimum winding ratios[17] of each the windings are almost "w_{O1}:w_{O2}:w_{13}:w_{24}= 1:1:1:1."

B. Circuit Operation

Figure 2 shows operating waveforms under ideal condition in a graphical analysis of the proposed rectifier (and the traditional 12-pulse rectifier partially) shown in Fig. 1, where the utility voltages (v_{AB} etc.) are purely sinusoidal, the currents (i_A etc.) continuously flow and the dc output voltage v_{DCO} is completely smoothed as shown in Fig. 1 (a), (b) and (c).

Under the condition with ideal sinusoidal utility line currents (i_A etc.) (i.e., with continuous input line currents (i_{X1} etc. and i_{X2} etc.) of the diode rectifiers (Rec. 1 and Rec. 2), the output current i_{DC1} and i_{DC2} of the rectifier pulsate at six times of the utility/mains frequency (i.e., in every 60 [deg.]) as shown in Fig. 2 (b). As a result, the dc currents alternates the conditions of "$i_{DC1} < i_{DC2}$" (Mode 1) and "$i_{DC1} > i_{DC2}$" (Mode 2) at six times of the utility/mains frequency (i.e., in every 60 [deg.]) as shown Fig. 3 (e).

The total ampare-turn $AT_{TD\text{-}ALL}$ of the DC-Side Interphase-Transformer T_D produced by the dc-currents and the windings (w_{O1} etc.) must be zero at all the time as shown,

$$\begin{aligned} AT_{TD\text{-}ALL} &= AT_{TD\text{-}1O} + AT_{TD\text{-}31} + AT_{TD\text{-}O2} + AT_{TD\text{-}24} \\ &= w_{1O}(i_{DC1}+i_{D1}) + w_{31}i_{D1} \\ &\quad - w_{O2}(i_{DC2}+i_{D2}) - w_{24}i_{D2} \\ &= 0 \end{aligned} \quad ...(1)$$

Thus, only one of the auxiliary diodes D_1 or D_2 turns-on while the other turns-off under the dc current conditon of "$i_{DC1} < i_{DC2}$" or "$i_{DC1} > i_{DC2}$," respectively, as shown in Fig. 3 to realize Eq. (1). The circuit condition of "$i_{DC1} < i_{DC2}$" or "$i_{DC1} > i_{DC2}$" where the auxiliary diode D_1 or D_2 turns on and other turns off is called "Mode-1" or "Mode-2," respectively, hereafter. The circuit condition in Mode-1 and Mode-2 are shown in Fig. 3 (a) and (b), respectively.

Since the dc voltage v_{DCO} is applied on the widings w_{1O} and w_{31} of the DC-Side Interpase Transformer T_D in Mode-1 as seen in Fig. 3 (a), the following voltage equation is obtained.

$$v_{DCO} = -v_{TD\text{-}1O} - v_{TD\text{-}31} \quad ...(2)$$

Since the winding number of all the windings are the same, we obtain,

$$v_{TD\text{-}1O} = v_{TD\text{-}31} = v_{TD\text{-}O2} = v_{TD\text{-}24} = -v_{DCO}/2 \quad ...(3)$$

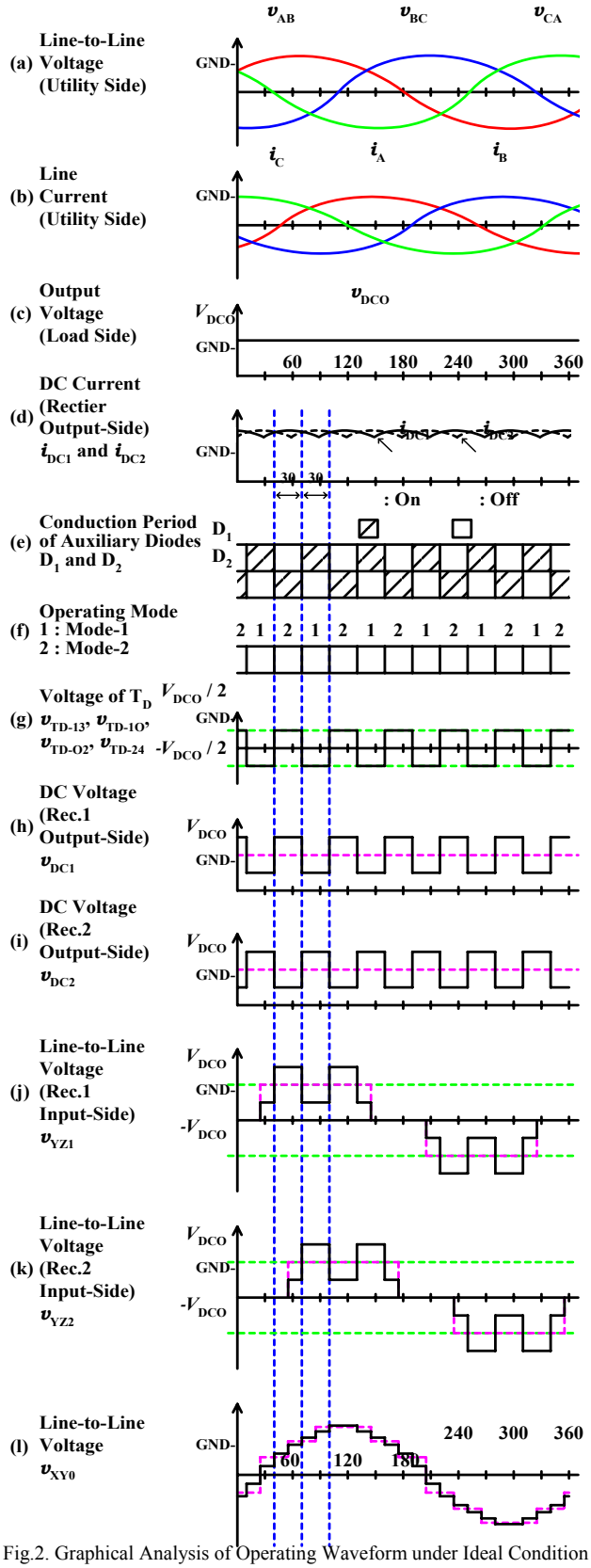


Fig.2. Graphical Analysis of Operating Waveform under Ideal Condition
(Horizontal: 30 [deg. / div.] @ 50 [Hz])
(w_{31} : w_{1O} : w_{O2} : w_{24} = 1 : 1 : 1 : 1)

As similar to the Mode-1, we obtain the following equation for the Mode-2.

$$v_{TD-1O} = v_{TD-31} = v_{TD-O2} = v_{TD-24} = v_{DCO}/2 \quad ...(4)$$

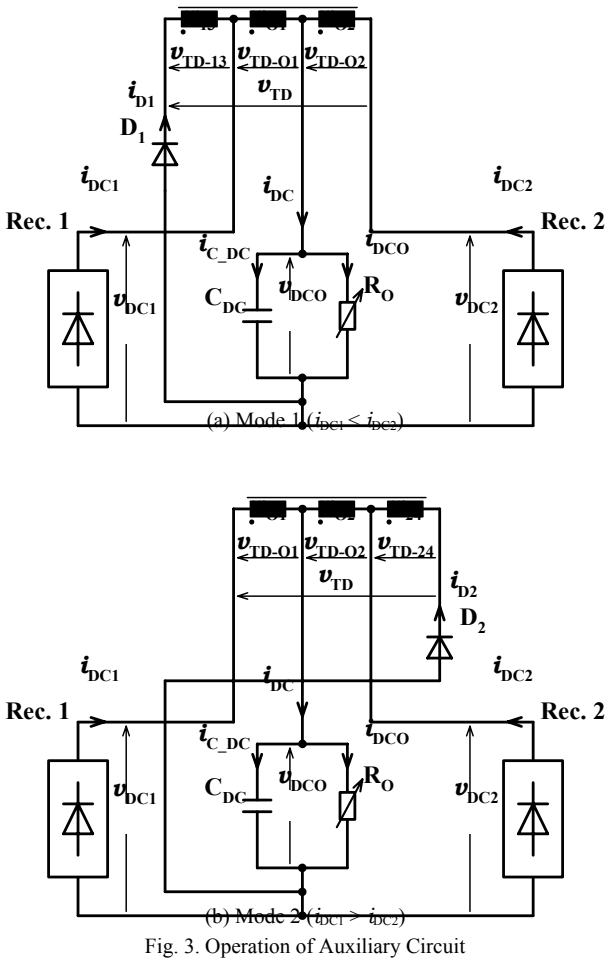


Fig. 3. Operation of Auxiliary Circuit

Referring to Eq. (3) and (4), it is known that the winding voltages (v_{TD-1O}, v_{TD-31}, v_{TD-O2} and v_{TD-24}) produce a 2-level rectangular waveform as shown in Fig. 2 (g).

Since the dc-voltages (v_{DC1} and v_{DC2}) are obtained,

$$v_{DC-1} = v_{DCO} + v_{TD1O} + v_{TD31} \quad ...(5)$$

$$v_{DC-2} = v_{DCO} - v_{TDO2} + v_{TD24} \quad ...(6)$$

By applying Eq. (3) and (4) to Eq. (5), we obtain,

$$v_{DC-1} = v_{DCO} - v_{DCO} \quad \text{(in Mode-1)} \quad ...(7)$$

$$v_{DC-2} = v_{DCO} + v_{DCO} \quad \text{(in Mode-1)} \quad ...(8)$$

$$v_{DC-1} = v_{DCO} + v_{DCO} \quad \text{(in Mode-2)} \quad ...(9)$$

$$v_{DC-2} = v_{DCO} - v_{DCO} \quad \text{(in Mode-2)} \quad ...(10)$$

By referring to Eq. (7) to (10), we obtain uneven dc voltages (v_{DC1} and v_{DC2}) of the Rec.1 or Rec.2 as shown with black lines in Fig. 2 (h) or (i), respectively. The smoothed waveforms with pink lines in the figure show the dc-side voltages (v_{DC1} or v_{DC2}) of the traditional 12-pulse rectifier.

By means of the unique operation of the LIT T_L, The two uneven dc voltages (υ_{DC1} and υ_{DC2}). The three-phase diode rectifiers (Rec.1 or Rec.2) synthesizes the dc-side voltages (υ_{DC1} or υ_{DC2}) and produce the ac-side voltages (υ_{YZ1} or υ_{YZ2}) as shown with black lines in Fig. 2 (j) or (k), respectively. The waveforms with pink lines show the ac-side voltages (υ_{YZ1} or υ_{YZ2}) of the traditional 12-pulse rectifier.

The LIT T_L synthesises the two ac-side voltages (υ_{YZ1} or υ_{YZ2}) by the unique operation and produces a 24-pulse line-to-line voltages υ_{XY0} as shown in Fig. 2 (l). The waveforms with pink lines show the ac-side voltages υ_{XY0} of the traditional 12-pulse rectifier.

The differece between the utility voltages (υ_{AB} etc.) (sinusoidal in most case) and the input line-to-line voltages (υ_{XY0} etc.) is applied on the ac inductors L_{AC} and the input line-to-line voltages (υ_{XY0} etc.) of the proposed 24-pulse rectifier involve much less harmonics especially in the lower order ones compared with the conventional 12-pulse rectifier. Thus, less inductance is required for the ac inductor in the proposed 24-pulse rectifier compared with the conventional 12-pulse rectifier to obtain utility line currnets (i_A etc.) with a certain quality of waveform (i.e., lower THD).

III. Simulations and Experiments

To confirm the validity of the theory of the new 24-pulse rectifier, the performance of the rectifier was evaluated through simulations. TABLE-I shows circuit constants and measured data in the simulations. The theory of the operation is based on "continuous current condition" and it realizes when the ac inductor L_{AC} has a large inductance. Thus, an ac inductor with a great inductance (i.e., 25.2 [mH] or *%IX* of 40.2 [%]) is employed in the simulations.

Figure 4 (a) or (b) show the line-to-line voltage υ_{XY0} or the line current i_A on the utility/mains side in the simulations, respectively. TABLE-II (a), (b-S) and (c-S) show harmonic contents of the ideal 6, 12, 18, and 24-pulse waveforms as well as the line-to-line voltage υ_{XY0} and the line current i_A in the simulations, respectively.

The line-to-line voltage υ_{XY0} in the simulation shown in Figure 4(a) draws an almost ideal staircase waveform of 24-pulse. The harmonic contents of the voltage is similar to those of the ideal 24-pulse waveform as seen in TABLE-II (a) and (b-S), and the THD (*THD*-υ_{XY0}) of the voltage is only 6.73% and this is almost the same to the ideal case (i.e., 7.5%).

From the waveform shown in Fig. 4(a) and the harmonic contents shown in TABLE-II (a) and (b-S), the line-to-line voltage υ_{XY0} can be recognized as a 24-pulse waveform. Thus the validity of the theory for synthesizing the 24-pulse voltage waveform in the proposed rectifier is confirmed.

Because of the fine waveform of the voltage υ_{XYO} and a large inductance of the line inductor L_{AC}, the line current i_A in the simulations shown in Fig. 4(b) draws an almost pure sinusoidal waveform. The THD (*THD*-i_A) of this current i_A is only 0.54%.

TABLE-I
CIRCUIT CONSTANNS OF SETUP AND MEASURED DATA OBTAINED FROM SIMULATIONS

Circuit Constants

AC side Inductor L_{AC} [mH]	25.20 (*%IX* = 40.2 [%])
DC side Capacitor C_{DC} [μF]	24,000

Measured Data

Measured Items	**Data**
(a) Utility / Mains Side	
Line-to-Line Voltage V_{AB} [V_{RMS}]	200.0
Line Current I_A [A_{RMS}]	8.75
Apparent power S [kVA]	3.03
Active power P [kW]	2.33
Total Harmonic Distortion of Line Current i_A $THD_{.iA}$ [%]	0.54
Total Power Factor TPF [%]	76.90
(b) DC Output Side	
Output Voltage V_{OUT} [V_{AVE}]	185.9
Output Current I_{OUT} [A_{AVE}]	10.80
Output Power P_{OUT} [kW]	2.01

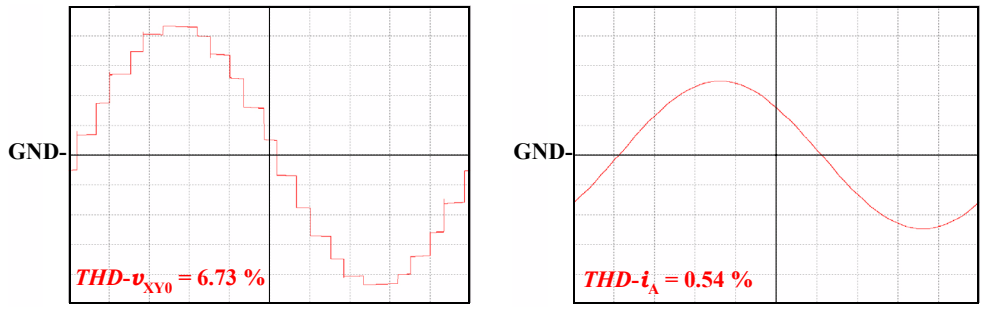
The line-to-line voltage υ_{XY0} in the experiments shown in Figure 5(a) draws a distorted waveform compared with the ideal one. The dominant reason of the phenomena seems to be errors of the winding ratios of the T_L and practical features of the component such as leakage inductance of the transformers. Detail analysis of the reason remains and under processing. Though, the step number of the line-to-line voltage υ_{XY0} is 24 and the step levels are reasonable. From the harmonic contents of the line-to-line voltage υ_{XY0} in experiments shown in TABLE-II (b-E), it is known that the voltage waveform is better than ideal 12-pulse waveform but worse than ideal 24-pulse waveform. The THD (*THD*-υ_{XY0}) of the voltage υ_{XY0} in experiments is 8.75 [%] and this value is much smaller than that of ideal 12-pulse waveform (i.e., 15 [%]) and slightly worse than that of ideal 24-pulse waveform (i.e., 7.5 [%]). Thus, effectiveness of the 24-pulse rectifier for reducing harmonics of the line-to-line voltage υ_{XY0} can be confirmed through the experimental results.

As a result of harmonic reduction of the line-to-line voltage υ_{XY0}, the line currents (i_A etc.) draw almost sinusoidal waveform in the experiments as shown in Fig. 5 (b). The THD of the current is only 1.48% in this case.

IV. Conclusions

To overcome the problem of conventional 18 and 24-pulse diode rectifier, i.e., necessity of phase-shifting transformers with very complicated windings, a 24-pulse diode rectifier with 12-pulse topology and pulse-doubler schemes hybrid has been proposed. The operating principle and experimental results are described and validity of the theory of the rectifier is briefly confirmed in this paper.

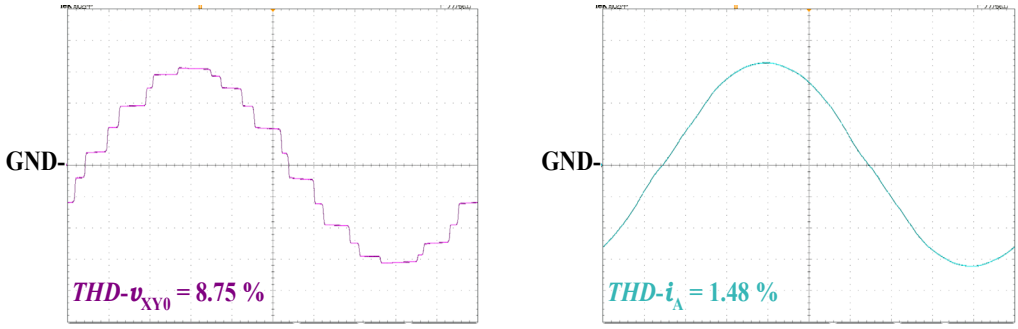
Detail practical study with higher power level is remained and now under preparation.



(a) Line-to-Line voltage v_{XYO}.
(Vertical: 50 [V/div.], Horizontal: 2 [ms/div.])

(b) Line Current i_A.
(Vertical: 5 [A/div.], Horizontal: 2 [ms/div.])

Fig.4. Operating Waveform Obtained from Simulations.
(Vertical: 50 [V/div.], Horizontal: 2 [ms/div.]; Output Power: P_{OUT} = 2 [kW] approx.)



(a) Line-to-Line voltage v_{XYO}.
(Vertical: 50 [V/div.], Horizontal: 2 [ms/div.])

(b) Line Current i_A.
(Vertical: 5 [A/div.], Horizontal: 2 [ms/div.])

Fig.5. Operating Waveform Obtained from Experiments.
(Vertical: 50 [V/div.], Horizontal: 2 [ms/div.]; Output Power: P_{OUT} = 2 [kW] approx.)

TABLE-II
HARMONICS CONTENT OF LINE CURRENT i_A AND LINE-TO-LINE VOLTAGE v_{XY0}

Harmonic Order K	(a) Harmonic Contents of Ideal 6-, 12-, 18- and 24-Pulse Waveforms $H_{(J,K)}$				(b) Harmonic Contents of LINE-TO-LINE VOLTAGE v_{XY0} in Proposed Rectifier $H_{V(K)}=V_{XY0(J,K)}/V_{XY0(1)}$		(c) Harmonic Contents of LINE CURRENT i_A in Proposed Rectifier $H_{I(K)}= I_{A(J,K)}/I_{A(1)}$	
	Pulse-Number J				(b-S) Simulations	(b-E) Experiments	(c-S) Simulations	(c-E) Experiments
	6	12	18	24				
1	1	1	1	1	1	1	1	1
2	0	0	0	0	0	0.002	0	0.001
3	0	0	0	0	0	0.006	0	0.002
4	0	0	0	0	0	0.002	0	0.001
5	**0.200**	**0**	**0**	**0**	**0.007**	**0.013**	**0.002**	**0.013**
6	0	0	0	0	0	0.002	0	0
7	**0.143**	**0**	**0**	**0**	**0.005**	**0.012**	**0**	**0.005**
8	0	0	0	0	0	0.007	0	0.001
9	0	0	0	0	0	0.004	0.001	0.001
10	0	0	0	0	0	0.005	0	0.001
11	**0.091**	**0.091**	**0**	**0**	**0.026**	**0.057**	**0.003**	**0.004**
12	0	0	0	0	0	0.002	0	0
13	**0.077**	**0.077**	**0**	**0**	**0.025**	**0.044**	**0.002**	**0.003**
14	0	0	0	0	0	0.007	0	0.001
15	0	0	0	0	0	0.004	0	0
16	0	0	0	0	0	0.006	0	0
17	**0.059**	**0.059**	**0.059**	**0**	**0.003**	**0.009**	**0**	**0**
18	0	0	0	0	0	0.002	0	0
19	**0.053**	**0.053**	**0.053**	**0**	**0.002**	**0.005**	**0**	**0**
20	0	0	0	0	0	0.006	0	0
21	0	0	0	0	0	0.003	0	0
22	0	0	0	0	0	0.004	0	0
23	**0.043**	**0.043**	**0**	**0.043**	**0.035**	**0.009**	**0.002**	**0**
24	0	0	0	0	0	0.002	0	0
25	**0.040**	**0.040**	**0**	**0.040**	**0.030**	**0.003**	**0.002**	**0**
***THD* [%]**	**30**	**15**	**11**	**7.5**	**6.73**	**8.75**	**0.54**	**1.48**

REFERENCES

[1] C. Niermann, "New Rectifier Circuits with Low Main Pollution and Additional Low Cost Inverter for Energy Recovery," Proc. of the 3rd European Power Electronics and Applications Conf. EPE, Vol. 3, pp. 1131 – 1136 (1989)

[2] M. Depenbrock and C. Niermann, "A New 12-Pulse Rectifier Circuit with Line-Side Interphase Transformer and Nearly Sinusoidal Line Currents" Proc. of the 6th Conference on Power Electronics and Motion Control (PEMC), Vol. 2, pp. 374 – 378 (1990)

[3] M. Depenbrock and C. Niermann, "A New 18-Pulse Rectifier Circuits with Line-Side Interphase Transformer and Nearly Sinsoidal Line Currents," Proc. of the International Power Electronics Conference (IPEC), Vol. 1, pp. 539 – 546 (1990)

[4] K. Oguchi, T. Yamada, "Novel 18-step diode rectifier circuit wiyh nonisolated phase shifting transformers, " IEE Proc. Electric Power Applications, Journal, Vol. 144, pp. 1 – 5 (1997)

[5] K. Oguchi, K. Fukushima, T. Kubota, "Comparative Studies on Line-Side Reactor-Coupled 12-Pulse Three-Phase Diode Rectifier," Domestic Technical Meeting of Semiconductor Power Converter (SPC), Paper#: SPC-99-15, pp. 1 – 6 (1999) (in Japanese)

[6] K. Oguchi, G. Maeda, N. Hoshi, T. Kubota, "Coupling Rectifier Systems With Harmonic Cancelling Reactors," IEEE Industry Applications Magazine, Vol. 7, July/August, pp. 53 – 63 (2001)

[7] K. Oguchi, "Autotransformer-based 18-pulse rectifiers without using dc-side interphase transformers: Classification and comparison," International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), pp. 760 – 765 (2008)

[8] A. Uan-Zo-li, R. Burgos, F. Wang, D. Boroyevich, F. Lacaux, A. Tardy, "Comparison of prospective topologies for aircraft autotransformer-rectifier units," Proc. of the 29th Annual Conference of the IEEE Industrial Electronics Society (IECON), Vol. 2, pp. 1122 – 1127 (2003)

[9] A. Uan-Zo-li, F. Lacaux, R.P. Burgos, F. Wang, D. Boroyevich, "Multi-level Modeling of Autotransformer Rectifier Units for Aircraft Applications," Proc. the International Power Electronics Conference (IPEC), Vol. 1, pp. 539 – 546 (2005)

[10] H. Mochikawa, J. Tsuda, M. Uesugi, T. Yamashita, "A New 18-Pulse Rectifier Circuit with Small Phase-Shifting Transformer," Proc. of the International Power Electronics Conference (IPEC), Vol. 1, pp. 1838 – 1842 (2005)

[11] P. Mysiak, P. Jankowski, "A Multi-Pulse Diode Rectifier with a Coupled Three-Phase Reactor - the Design Method and Results of the Simulation and Laboratory Tests," Electrical Power Quality and Utilisation, Journal, Vol. 11, No. 1, pp. 83 – 92 (2005)

[12] Xiao-hua Wu, Peng-peng Cai, Xiao-bin Zhang, "Design and Analysis of An Autotransformer Based 24-pulse Rectifier," Proc. of Electrical and Control Engineering (ICECE), pp. 3529 – 3532 (2010)

[13] S. Nakhaee, A. Jalilian, "Simulation of 24-Pulse Autotransformer Based AC-DC Converter Employing Pulse Multiplication with Direct Torque Controlled Induction Motor Drive Load," Proc. of the 2nd Power Electronics, Drive Systems and Technologies Conference (PEDSTC) pp. 593 – 598, (2011)

[14] Y. Nishida, "Passive and Hybrid PFC Rectifiers –A Survey and Exploration of New Possibilities–," IEEJ Industry Applications Society, Vol. 126, No.7, pp. 927 – 940, (2007)

[15] J.W. Kolar, T. Friedli, "The Essence of Three-Phase PFC Rectifier Systems," Proc. of the 33rd IEEE International Telecommunications Energy Conference (INTELEC), pp. 1 – 27 (2011)

[16] S. Iida, S. Masukarwa, S Miyairi and Y. Nishida, "A Method for Reducing Harmonics in Output Voltages of Double Connected Inverter," Proc. of EPE '89, Vol. II, pp. 555 - 559 (1989)

[17] Y. Nishida, S. Iida, S. Masukawa, S. Miyairi, "A Method for Reducing Harmonics in Input Currents of Double Connected Diode Rectifier," Proc. EPE '91, Vol. 1, pp. 349 – 354, (1991)

[18] S. Masukawa, "Improvement of a Double Connected Diode Rectifier with a Smoothing Capacitor by Using an Interphase Transformer," IEEJ Industry Applications Society, Vol. 116, No.5, pp. 538 – 545 (1996)

[19] Y. Nishida, M. Nakaoka, "A Study on Generalization of Ripple Component Injection Technique to Reduce AC-Side Harmonics and DC-Side Ripples in Three-Phase PAM Power Converters," Domestic Technical Meeting of Semiconductor Power Converter (SPC), Paper : SPC-96-113, pp. 1 – 10 (1996)

[20] Y. Nishida, M. Nakaoka, "A New Harmonic Reducing Three-Phase Diode Rectifier for High Voltage and High Power Applications," IEEE IAS '97 (the 1997 IEEE Industry Applications Society 32nd Annual Meeting), Vol. 2, pp. 1624 – 1632 (1997)

[21] Y. Nishida, "A Harmonic Reducing Scheme for 3-Phase Bridge 6-Pulse Diode Rectifier," Proc. of the 25th Annual Conference of the IEEE Industrial Electronics Society (IECON), Vol. 1, pp. 228 – 234 (1999)

[22] Y. Nishida, K. Mino, "A Method to Decrease Input Current Harmonics of Three-Phase Diode Rectifier by Pulse-Doubler Scheme," Proc. of the 32nd Annual Conference of the IEEE Industrial Electronics Society (IECON) pp. 1673 – 1678 (2006)

[23] P. Pejović, Y. Nishida, "A Current Injection Based Twelve-Pulse Rectifier," Proc. of the 32nd Annual Conference of the IEEE Power Electronics Specialists Conference (PESC), pp. 3603 – 3609 (2008)