Three-Phase Two-Third-PWM Buck-Boost Current Source Inverter System Employing Dual-Gate Monolithic Bidirectional GaN e-FETs

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***Abstract*— Latest dual-gate (2G) monolithic bidirectional (MB) gallium nitride (GaN) enhancement-mode field effect transistors (e-FETs) enable a performance breakthrough of current DC-link inverters, e.g. in terms of power conversion efficiency, power density, cost and complexity. In fact, a single 2G MB GaN e-FET can replace the two anti-series connected conventional power semiconductors required in this inverter topology, realizing a *four-quadrant* (AC) switch with bidirectional voltage blocking capability and allowing controlled bidirectional current flow. Furthermore, as shown in this paper in case of three-phase (3-Φ) buck-boost (bB) current source inverter (CSI) systems comprising a DC-link current impressing buck-type DC/DC input stage and a subsequent boost-type 3-Φ current DC-link inverter output stage, a variable DC-link current control strategy, based on a *Synergetic Control* concept, can be applied to significantly reduce the switching losses occurring in the 3-Φ inverter. This strategy is denominated *Two-Third Pulse-Width Modulation* (2/3-PWM), since by properly shaping the DC-link current with the input stage, the desired 3-Φ sinusoidal load phase currents can be generated by switching, in each switching period, only two out of the three phases of the output stage. Based on comprehensive circuit simulations and analytical calculations, a detailed explanation of the developed modulation and control schemes in different operating conditions is provided, and the reduction of losses enabled by 2/3-PWM is confirmed. Next, the seamless transition of the 3-Φ bB CSI system from 2/3-PWM to conventional 3/3-PWM is demonstrated. Finally, a $3.3\,\mathrm{kW}$ 3-Φ bB CSI system, applying 2/3-PWM and employing research samples of 2G MB GaN e-FETs in the 3-Φ inverter, is estimated to achieve an efficiency of $98.4\,\%$ and a power density of $18\,\mathrm{kW/dm^3}$ $(295\,\mathrm{W/in^3})$ at a switching frequency of $140\,\mathrm{kHz}$.**

***Index Terms*— Dual-Gate Monolithic Bidirectional Gallium Nitride Enhancement-Mode Field-Effect Transistor, Three-Phase Buck-Boost Current Source Inverter System, Variable DC-Link Current Control.**

I. Introduction

THE three-phase (3-Φ) voltage DC-link inverter is the industry preferred solution to perform compact and efficient DC/AC energy conversion in variable speed drives (VSDs) and/or grid connected power electronic applications. To comply with the electromagnetic (EM) regulations and, in case of VSDs, to avoid excessive losses in the electric machine, insulation stress and bearing wear-out [1], filter circuits are connected at the output of voltage DC-link inverters to generate continuous output voltage waveforms [2]–[4]. To limit the size and/or cost of the output filter, but also to increase the control bandwidth of the system, high frequency, e.g. $100\,\mathrm{kHz}$, VSDs are employed. In this context, wide band-gap (WBG) semiconductors, i.e. gallium nitride (GaN) and silicon carbide (SiC), become key technologies to preserve a high power conversion efficiency, even outperforming conventional silicon (Si) based solutions [5]. Additionally, when the supplying DC input voltage varies in a wide range, e.g. when it is provided by the traction battery of an electric vehicle (EV) [6] or by a string of photovoltaic (PV) panels [7], voltage DC-link inverters are preceded by a boost-type DC/DC converter input stage [8], which regulates the DC input voltage of the 3-Φ inverter. Hence, the so obtained two-stage converter (including the output filter), i.e. a 3-Φ boost-buck (Bb) voltage source inverter (VSI) system, can operate in a wide DC input voltage range and generate continuous output voltage waveforms, thus fulfilling the requirements of modern DC/AC power converters [1], [8].

The functionality of a 3-Φ Bb VSI system can alternatively be achieved with the quasi-dual approach, i.e. the 3-Φ buck-boost (bB) current source inverter (CSI) system [9]–[11] shown in **Fig. 1**. It comprises a DC-link current impressing buck-type DC/DC input stage (gray) and a subsequent boost-type 3-Φ current DC-link inverter output stage (black) [12]. Advantageously, the DC-link inductor L_{dc} forms, in combination with the output capacitors C_{o}, an integrated output filter; i.e., the 3-Φ bB CSI system naturally generates continuous output voltage waveforms.

Nevertheless, this quasi-dual solution is rarely adopted, mainly because of the higher count of power devices. In fact, a 3-Φ voltage DC-link inverter only requires six power semiconductors with unidirectional voltage blocking capability allowing controlled

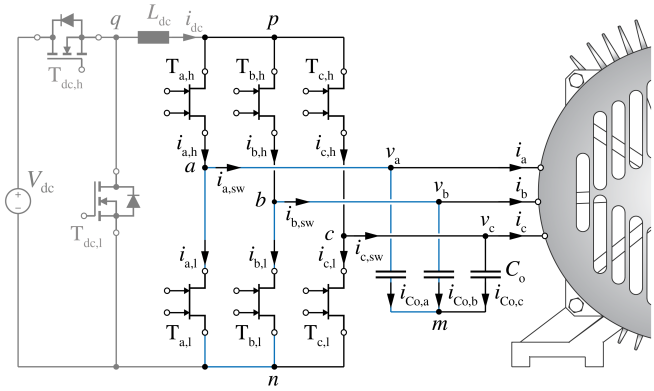


Fig. 1: Schematic of the three-phase (3-Φ) buck-boost (bB) current source inverter (CSI) system analyzed in this paper. The boost-type 3-Φ current DC-link inverter output stage (black) is formed by six 2G MB GaN e-FETs and connected to an electric machine, as in a variable speed drive (VSD) application. The buck-type DC/DC converter input stage (gray), connected to a supplying DC input voltage source, introduces the bB functionality and allows to control and shape the DC-link current i_{dc}.

bidirectional current flow, such as MOSFETs or IGBTs (with external anti-parallel diodes), which are the most widely used power devices. Consequently, VSI systems are often preferred and, especially when WBG power semiconductors are considered, high power conversion efficiencies and extreme power densities can be achieved at any power level [8], [13].

In contrast, a 3-Φ current DC-link inverter requires six power semiconductors with bidirectional voltage blocking capability, such as, e.g., symmetric GTOs. However, when design constraints demand switching frequencies in the 10-100 kHz range, these switches are preferably realized by anti-series connecting two discrete components, e.g. two power transistors (with external anti-parallel diodes) [14]. This ultimately causes an increase of chip area, cost, driving complexity and conduction losses, which disfavor CSI systems in comparison with VSI systems. However, the unprecedented performance of WBG devices, enabling a significant reduction of switching and conduction losses compared to Si MOSFETs at a given operating point, stimulate further research on current DC-link converters featuring GaN [15] or SiC [16] power semiconductors. Additionally, recent development in the power semiconductor industry culminated in the realization of monolithic bidirectional [17] (MB) GaN enhancement-mode field-effect transistor (e-FET) research prototypes [18]–[21] which feature bidirectional voltage blocking capability and allow a controlled current flow in both directions, i.e. excellently fit the requirements of current DC-link inverters. In particular, $\pm 600\,\mathrm{V}$ $26\,\mathrm{m\Omega}$ research samples of a dual-gate (2G) MB GaN e-FET [22] are available from a major manufacturer of power semiconductors. Preliminary tests on these devices are performed in [23], however, their potential in a 3-Φ bB CSI system still remains unclear.

Beside these new components, other intrinsic characteristics [15] of 3-Φ bB CSI systems motivate the research on this circuit topology. In fact, while voltage DC-link inverters switch a constant voltage and a variable current, the opposite is true for current DC-link inverters. Since the switching losses are typically stronger influenced by the switched voltage than by the switched current [24], lower switching losses might occur in the current DC-link approach for the same processed power [25], eventually resulting in overall higher efficiencies [26]. Moreover, although capacitors (voltage DC-links) have a higher energy storage density than inductors (current DC-links), a lower boundary for their volume is given by their current rating [27]. Differently, higher switching frequencies, i.e. WBG semiconductors, always enable the downsizing of magnetic components. Additionally, different costs, operating temperature ranges, critical environmental conditions, failure modes and failure rates are associated to capacitors and inductors. Hence, current DC-link inverters potentially show advantages over voltage DC-link inverters in certain applications.

In this paper, the operating principle of the 3-Φ bB CSI system is introduced in **Section II**. Ideal waveforms of the 3-Φ inverter support the explanation of a variable DC-link current control strategy denominated *Two-Third Pulse-Width Modulation* (2/3-PWM) [28]–[31]. Although the basic principle of 2/3-PWM is originally presented in [29], [30], this is as well briefly summarized in **Section III** to provide a common basis for the subsequent analysis, which focuses on its range of applicability, resulting stress on the circuit components, e.g. switching losses, and operation supported by comprehensive simulation results (also in case of non-unity load power factor and load steps). In particular, analytic calculations, performed in **Section IV**, highlight the performance improvement of the 3-Φ inverter enabled by this concept. The developed *Synergetic Control* scheme, employed for the 3-Φ bB CSI system, is described in **Section V** and circuit simulations prove its functioning in different operating conditions. The considered 2G MB GaN e-FET research prototypes are presented in **Section VI** and compared to state-of-the-art power semiconductors. A prediction of the efficiency and power density achievable by the 3-Φ bB CSI system precedes **Section VII**, which concludes the paper. Finally, an experimental hardware, designed to evaluate the switching performance of the 2G MB GaN e-FETs, is described and measured switching waveforms are discussed in the **Appendix**.

TABLE I: Nominal specifications of the 3-Φ bB CSI system shown **Fig. 1**.

	Description	Value
V_{dc}	supplying DC input voltage	$400\,\mathrm{V}$
$\hat{i}_{\mathrm{out}}$	peak sinusoidal load phase current	$11\,\mathrm{A}$
$\hat{v}_{\mathrm{out}}$	peak sinusoidal output voltage	$196\,\mathrm{V}$
f_{out}	output frequency	$50\,\mathrm{Hz}$
P_{out}	output power	$3.3\,\mathrm{kW}$

II. Power Converter Operation

As first step of a comprehensive analysis of the 3-Φ bB CSI system shown in **Fig. 1**, its operating range and operating principle are described in this section.

A. Operating Range

The direction of power flow in the 3-Φ bB CSI system shown in **Fig. 1** is defined by the sign of the DC-link current i_{dc}. In fact, since the output voltage of the buck converter v_{qn} is unipolar, i.e. it is limited between $0\,\mathrm{V}$ and the supplying DC input voltage $V_{\mathrm{dc}} > 0\,\mathrm{V}$, the average in a switching period of the input voltage of the 3-Φ inverter $\bar{v}_{\mathrm{pn}}$ must be positive to guarantee the controllability of i_{dc}, i.e. the stability of the system. However, still both directions of power flow are possible in the 3-Φ inverter, as only the sign of i_{dc} (and not the one of $\bar{v}_{\mathrm{pn}}$, as for a conventional system [32]) must be inverted for feeding power back to the supplying DC input voltage source.

Nevertheless, when $\bar{v}_{\mathrm{pn}}$ approaches $0\,\mathrm{V}$, i.e. when the peak value $\hat{v}_{\mathrm{out}}$ of the sinusoidal output voltages or the load power factor $\cos(\phi)$ of the supplied load are reduced [32], the controllability of i_{dc}, as well as the possibility to invert it, are limited. For this reason, the selected 3-Φ bB CSI system is particularly suited for VSDs supplying synchronous machines operated with high power factors or passive loads, e.g. pumps and fans [33], and, in the case of grid connected power electronic applications, for power factor correction (PFC) rectifiers and inverters, e.g. future bidirectional EV battery chargers, and PV inverters, i.e. for systems typically operating with $\cos(\phi) \approx \pm 1$.

Irrespectively of this limitation, the DC/DC buck-type input stage based 3-Φ bB CSI system (see **Fig. 1**) is preferred to the back-to-back AC/AC system comprising two DC-side connected 3-Φ inverters [32] to better suite the requirements of voltage DC-link systems and distributed voltage DC-link architectures, becoming more and more prominent in VSDs [34].

B. Input-Output Voltage Gain

The two main control variables of the 3-Φ bB CSI system are the duty-cycle of the buck converter

$$\bar{s}_{\mathrm{Tdc,h}} = \frac{\bar{v}_{\mathrm{qn}}}{V_{\mathrm{dc}}} = \frac{\bar{v}_{\mathrm{pn}}}{V_{\mathrm{dc}}}, \tag{1}$$

where $\bar{v}_{\mathrm{qn}}$ indicates the average in a switching period of v_{qn}, and the modulation index of the 3-Φ inverter

$$m_{\mathrm{dc/ac}} = \frac{\hat{i}_{\mathrm{out}}}{I_{\mathrm{dc}}} = \frac{\bar{v}_{\mathrm{pn}}}{\hat{v}_{\mathrm{out,ll}}} \frac{2}{\sqrt{3}}, \tag{2}$$

if constant $i_{dc} = I_{dc}$ and $\cos(\phi) = +1$ are assumed. In (2), $\hat{i}_{out}$ and $\hat{v}_{out,ll}$ correspond to the peak values of the sinusoidal load phase currents i_{out} and sinusoidal line-to-line output voltages $v_{out,ll}$ generated by the 3-Φ inverter, respectively. Combining (1) and (2), the voltage gain g_v of the 3-Φ bB CSI system can be calculated as

$$g_v = \frac{\hat{v}_{out,ll}}{V_{dc}} = \frac{\bar{s}_{Tdc,h}}{m_{dc/ac}} \frac{2}{\sqrt{3}}. \quad (3)$$

Since $0 \leq \bar{s}_{Tdc,h} \leq 1$ and $0 \leq m_{dc/ac} \leq 1$, g_v can assume any positive value, i.e. the bB capability of the system is confirmed.
Although different combinations of $\bar{s}_{Tdc,h}$ and $m_{dc/ac}$ result in the same g_v, $\bar{s}_{Tdc,h} = 1$ eliminates the switching losses in the buck converter (since $T_{dc,h}$ is permanently on), while $m_{dc/ac} = 1$ minimizes the losses of the overall system for a given operating point [35]. Accordingly, these are the preferred values of $\bar{s}_{Tdc,h}$ and $m_{dc/ac}$ for a given g_v; hence, two operating modes, namely the *Buck-Mode* ($0 \leq \bar{s}_{Tdc,h} < 1$, $m_{dc/ac} = 1$) and the *Boost-Mode* ($\bar{s}_{Tdc,h} = 1$, $0 \leq m_{dc/ac} < 1$), can be defined [28]. From (3), the boundary between the *Buck-Mode* and the *Boost-Mode* can be calculated as

$$V_{dc} = \frac{\sqrt{3}}{2} \hat{v}_{out,ll}. \quad (4)$$

In particular, for $V_{dc} > \sqrt{3}/2\, \hat{v}_{out,ll}$, the system is operated in the *Buck-Mode*, whereas, when $V_{dc} < \sqrt{3}/2\, \hat{v}_{out,ll}$, the buck converter can no longer control i_{dc}; consequently, the *Boost-Mode* is entered.

C. Simplified Operating Principle

The 3-Φ bB CSI system shown in **Fig. 1** is simplified to the circuit shown in **Fig. 2** (cf. **Fig. 13** in [32]) to explain its operation in the *Buck-Mode* and with power flowing from the supplying DC input voltage source to the supplied AC output load. For this purpose, the buck converter and L_{dc} are replaced by a current source $i_{dc} > 0$, whereas the 3-Φ inverter is represented by two *three-position* switches T_h and T_l. The two output terminals tapped by T_h and T_l define one state of the 3-Φ inverter out of overall $3^2 = 9$ possibilities; e.g., in **Fig. 2**, a transition from state [ab] to [ac] is illustrated. The three shoot-through states [aa], [bb] and [cc] are denominated *zero states* in contrast to the remaining six states denominated *active states*. In the *zero states*, the 3-Φ inverter short circuits the DC-link terminals p and n whereas, in the *active states*, it connects the load between them. Consequently, depending on the selected state, v_{pn} varies between 0 V (*zero states*) and the six $v_{out,ll}$ values, i.e. $\pm v_{ab}$, $\pm v_{bc}$ and $\pm v_{ca}$ (*active states*), while the switching stage output currents $i_{a,sw}$, $i_{b,sw}$ and $i_{c,sw}$ can either assume the value of 0 A (*zero states*) or of $\pm i_{dc}$ (*active states*). Hence, by appropriately switching T_h and T_l, and output filtering (through C_o), i_{dc} can be modulated and transformed into the sinusoidal load phase currents i_a, i_b and i_c.

III. Modulation Schemes

Two different modulation schemes, namely conventional *Pulse-Width Modulation* (3/3-PWM) and *Two-Third Pulse-Width Modulation* (2/3-PWM) [28]–[31] can be applied to the 3-Φ bB CSI system when operated in the *Buck-Mode*. Both approaches are described in this section with the support of idealized waveforms of the 3-Φ inverter, relative to its nominal operating point (see **Table I**).

A. Conventional Pulse-Width Modulation (3/3-PWM)

In the *Buck-Mode* (see **Section II-C**), the buck converter controls i_{dc}, while the 3-Φ inverter is responsible for generating i_a, i_b and i_c. In case 3/3-PWM is applied, i_{dc} is controlled to a constant value I_{dc}. The most significant waveforms of the 3-Φ inverter in these conditions are summarized in **Fig. 3(a)**, **4(a)** and **5(a)**, where the encircled numbers

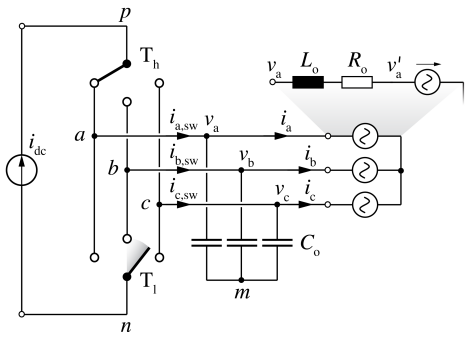


Fig. 2: Simplified representation of the 3-Φ bB CSI system shown **Fig. 1**. The two *three-position* switches T_h and T_l, modulating the DC-link current $i_{dc} > 0$ by alternately connecting the output terminals a, b and c to the DC-link terminals p and n, model the operation of the 3-Φ inverter.

define the six symmetric $\pi/3$-wide sectors of an AC output period.
In each interval of **Fig. 3(a)**, three of the six 2G MB GaN e-FETs forming the 3-Φ inverter are operated with PWM, i.e. are switched with switching frequency f_{sw}. For example in sector ①, characterized by $i_a > |i_b|$ and $i_a > |i_c|$, $T_{a,h}$ is permanently on, while $T_{b,h}$ and $T_{c,h}$ are permanently off, and all three low-side switches $T_{i,l}$ are alternately switched within a switching period. In other words, the states [aa], [ab] and [ac] are alternately applied since, as visible in the space vector diagram of **Fig. 6(a)**, these are (in this sector) the closest neighbors of the vector of the reference sinusoidal load phase current $\vec{i^*}$, having $|\vec{i^*}| = m_{dc/ac} I_{dc} = \hat{i}_{out}$. Hence, $\vec{i^*}$ can be expressed as

$$\frac{\vec{i^*}}{I_{dc}} = \delta_{[aa]} \cdot [aa] + \delta_{[ab]} \cdot [ab] + \delta_{[ac]} \cdot [ac], \quad (5)$$

where $\delta_{[xy]}$ indicates the duty-cycle of the state [xy]. Intuitively, all other $\delta_{[xy]} = 0$.
In **Fig. 3**, the gate control signal $s_{Ti,j}$ of each 2G MB GaN e-FET $T_{i,j}$ and its average within one switching period $\bar{s}_{Ti,j}$ are additionally shown. The conversion from $\delta_{[xy]}$ to $\bar{s}_{Ti,j}$ is immediately deduced from **Fig. 2** and can be expressed as

$$\bar{s}_{Ti,h} = \sum_{y = a, b, c} \delta_{[iy]}, \qquad \bar{s}_{Ti,l} = \sum_{x = a, b, c} \delta_{[xi]} \qquad (i = a, b, c). \quad (6)$$

Furthermore, from **Fig. 6(a)**, the duty-cycles of the *active states* $\delta_{[ab]}$ and $\delta_{[ac]}$ can be derived from the projections of $\vec{i^*}$ according to

$$\frac{|\vec{i^*}|}{I_{dc}} \begin{bmatrix} \cos\vartheta \\ \sin\vartheta \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} \delta_{[ac]} \\ \delta_{[ab]} \end{bmatrix} \quad (-\pi/6 < \vartheta < \pi/6), \quad (7)$$

where ϑ indicates the instantaneous phase angle of $\vec{i^*}$. The remaining fraction of the switching period is accounted for the *zero state*, whose duty-cycle $\delta_{[aa]}$ is calculated as

$$\delta_{[aa]} = 1 - (\delta_{[ac]} + \delta_{[ab]}) = 1 - m_{dc/ac} \cos\vartheta \geq 1 - \cos\vartheta \geq 0. \quad (8)$$

It should be noticed in (8), that even if $|\vec{i^*}| = I_{dc}$ as given for the *Buck-Mode* and applying 3/3-PWM, $\delta_{[aa]} > 0$ results (except for the point in time in the middle of ①, i.e. for $\vartheta = 0$, where $\delta_{[aa]} = 0$). Hence, a free-wheeling interval, i.e. an interval during which I_{dc} bypasses the load flowing through $T_{a,h}$ and $T_{a,l}$, is present during every switching period forming ①. Since (7) and (8) can be extended to the other five sectors (from ② to ⑥) based on symmetry considerations, it can be concluded that *zero states* are always necessary when 3/3-PWM is applied, i.e. the *zero state* and the two *active states* are occurring in each switching period.

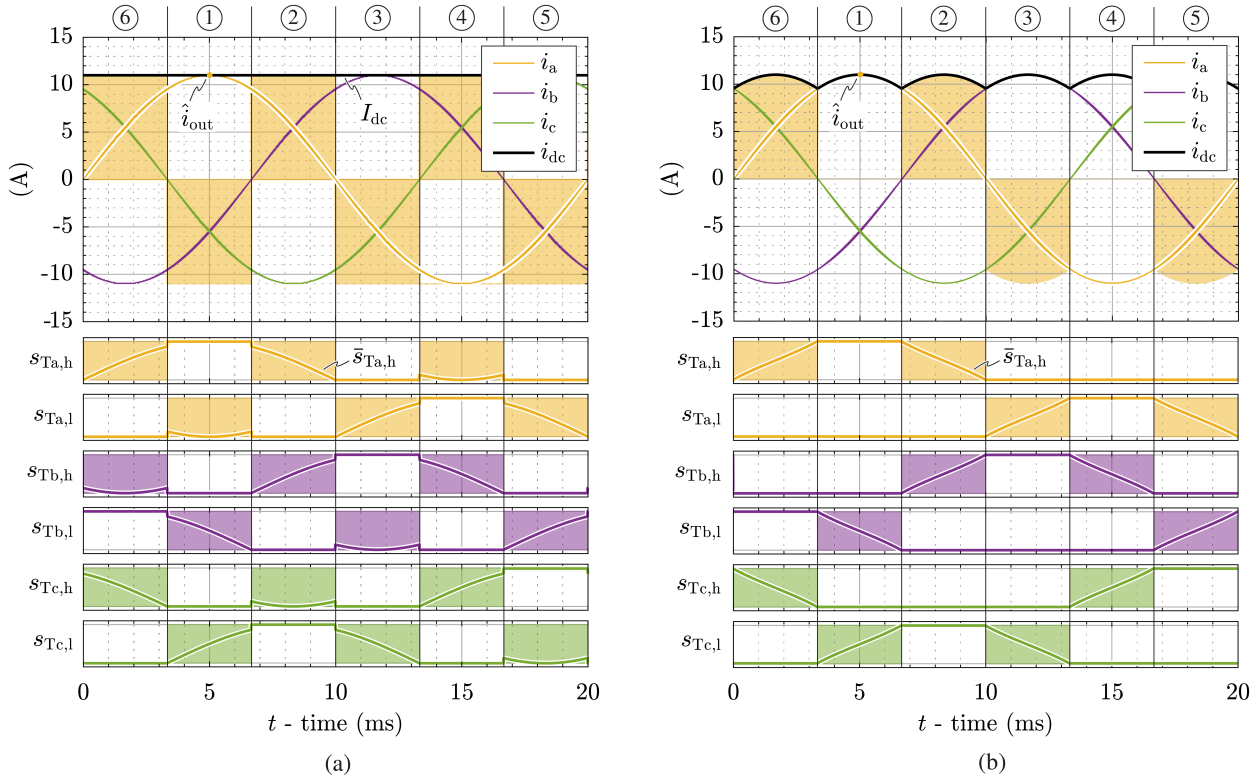


Fig. 3: DC-link current i_{dc}, sinusoidal load phase currents i_a, i_b and i_c with peak value $\hat{i}_{out}$ and gate control signals $s_{Ti,j}$ within one AC output period, in case **(a)** 3/3-PWM is applied ($i_{dc} = I_{dc}$) and **(b)** 2/3-PWM is applied ($i_{dc} = \max\{|i_a|, |i_b|, |i_c|\}$). The waveforms are given for the operating point specified in **Table I**. The encircled numbers, also indicated in **Fig. 4**, **5** and **6**, define the six symmetric $\pi/3$-wide intervals of an AC output period. The yellow area in the graphs of i_{out} indicates the switching stage output current of phase a, i.e. $i_{sw,a}$. The colored lines in the graphs of $s_{Ti,j}$ correspond to their average $\bar{s}_{Ti,j}$ in a switching period. Further details are shown in **Fig. 4** and **5**.

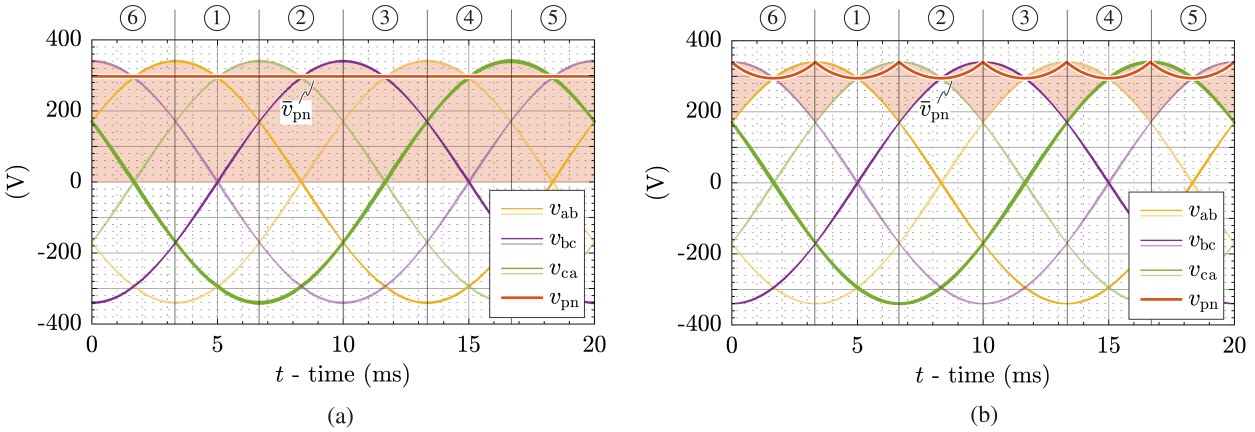


Fig. 4: Sinusoidal line-to-line output voltages $\pm v_{ab}$, $\pm v_{bc}$ and $\pm v_{ca}$, and input voltage of the 3-Φ inverter v_{pn} within one AC output period, in case **(a)** 3/3-PWM is applied and **(b)** 2/3-PWM is applied. The waveforms are given for the operating point specified in **Table I**. The red lines correspond to the average input voltage of the 3-Φ inverter $\bar{v}_{pn}$ in a switching period. Further details are shown in **Fig. 3** and **5**.

B. Two-Third Pulse-Width Modulation (2/3-PWM) [28]–[30]

According to **Section III-A**, a *zero state* free modulation should be preferred to maximize the efficiency of the 3-Φ bB CSI system. In fact, the transitions into (and out of) the *zero states* cause additional switching losses and, during the *zero states*, conduction losses occur even though no power is transferred to the load. Additionally, *zero states* are responsible for generating the highest common-mode voltage [36].

Hence, rewriting (8) for $\delta_{[aa]} = 0$,

$$i_{dc} = \hat{i}_{out} \cos\vartheta = i_a \qquad (-\pi/6 < \vartheta < \pi/6) \tag{9}$$

is obtained. For symmetry, (9) can be generalized to

$$i_{dc} = \max\{|i_a|, |i_b|, |i_c|\}, \tag{10}$$

which is valid for the entire AC output period, neglecting the currents flowing in C_o. In other words, if the buck converter controls and shapes i_{dc} to be equal to the instantaneous largest load phase current

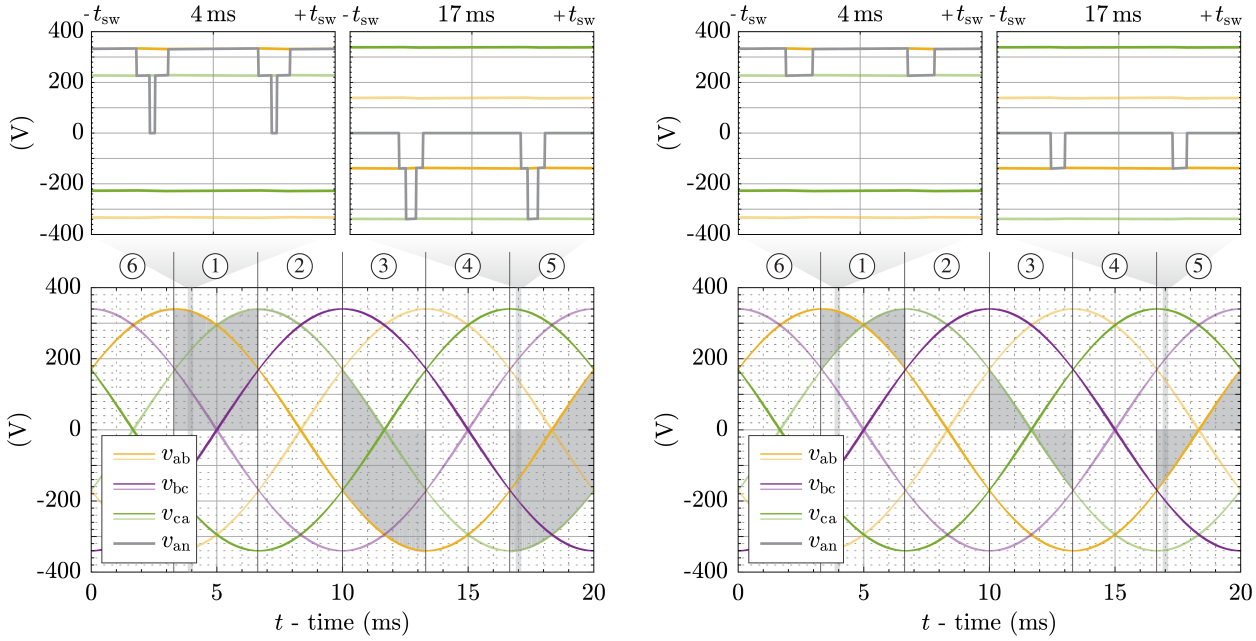


Fig. 5: Sinusoidal line-to-line output voltages $\pm v_{ab}$, $\pm v_{bc}$ and $\pm v_{ca}$, and voltage v_{an}, within one AC output period, in case **(a)** 3/3-PWM is applied and **(b)** 2/3-PWM is applied. The waveforms are given for the operating point specified in **Table I**. The graphs in the upper part offer a zoomed view of v_{an} during a switching period. Further details are shown in **Fig. 3** and **4**.

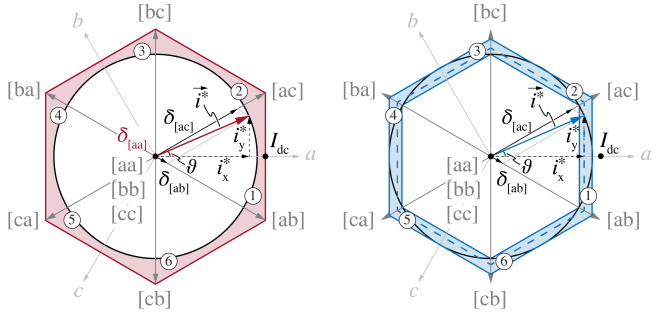


Fig. 6: Space vector diagram highlighting the nine states of the 3-Φ inverter and the vector of the reference sinusoidal load phase current $\vec{i}^*$, in case **(a)** 3/3-PWM is applied, i.e. the apothem of the hexagon is fixed to I_{dc} and **(b)** 2/3-PWM is applied, i.e. the size of the hexagon is scaled according to i_{dc}. The encircled numbers define the six symmetric $\pi/3$-wide intervals of an AC output period, as described in **Fig. 3**.

absolute value, e.g. to i_a during ①, the free-wheeling interval is avoided (since, e.g. again during ①, $i_{dc} - i_a = 0$). Adjusting i_{dc} as described translates, in the space vector plane shown in **Fig. 6(b)**, into a continuous scaling of the dimensions of the hexagon over time such that its perimeter matches the trajectory defined by $\vec{i}^*$, resulting in $\delta_{[ac]} + \delta_{[ab]} = 1$, i.e. $\delta_{[aa]} = 0$. Following this approach, only the two *active states* [ab] and [ac] (instead of all three states) must be applied within one switching period; consequently, $T_{a,l}$ is permanently off and only two ($T_{b,l}$ and $T_{c,l}$) instead of three 2G MB GaN e-FETs are alternately switched, as illustrated in **Fig. 3(b)**. Accordingly, this concept is named *Two-Third Pulse-Width Modulation* (2/3-PWM) and, as already speculated and further discussed in **Section IV-B**, it enables a significant reduction of switching losses.

As a consequence of (10), $\bar{v}_{pn}$ in **Fig. 4(b)** is not constant as in **Fig. 4(a)** but still guarantees a constant power $\bar{v}_{pn} i_{dc}$ at the input of the 3-Φ inverter. Moreover, since the *zero states* are avoided, v_{pn} never assumes the value of 0 V.

In **Fig. 5** the voltage v_{an} across $T_{a,l}$ is indicated for completeness. During ① in **Fig. 5(b)**, generated applying 2/3-PWM, v_{an} varies between v_{ab} and $-v_{ca}$, while in **Fig. 5(a)**, where 3/3-PWM is considered, it also reaches 0 V. The same reasoning can be extended to ⑤, where the three states of interest are [ca], [cb] and [cc] (see **Fig. 6**), yielding to v_{an} not assuming the value of $-v_{ca}$ in **Fig. 5(b)**. Repeating the calculations described in **Section II-B** with $i_{dc} = \hat{i}_{out} \cos\vartheta$, the range of applicability of 2/3-PWM can be determined as

$$V_{dc} > \frac{\sqrt{3}}{2} \frac{1}{\cos(\vartheta)} \hat{v}_{out,ll} \qquad (-\pi/6 < \vartheta < \pi/6). \tag{11}$$

Since $\sqrt{3}/2 < \cos(\vartheta) \leq 1$, (11) indicates that 2/3-PWM can be considered only if $V_{dc} > \hat{v}_{out,ll}$, i.e. in a subset of the *Buck-Mode* operating region. However, when $\sqrt{3}/2\, \hat{v}_{out,ll} < V_{dc} < \hat{v}_{out,ll}$, i.e. in the rest of the *Buck-Mode* region, 2/3-PWM and 3/3-PWM can be alternated depending on ϑ, as discussed more in detail in **Section V-B**. In practice, the range of applicability of 2/3-PWM should be defined in the design phase of the 3-Φ bB CSI system, opportunely selecting V_{dc} as function of $\hat{v}_{out}$.

IV. Analysis of the Two-Third Pulse-Width Modulation

Following the basic analysis of 2/3-PWM provided in **Section III-B**, the enabled reduction of conduction and switching losses in the 3-Φ inverter are calculated in the following.

A. Reduction of Conduction Losses

Since i_{dc} continuously flows through L_{dc} and two MB GaN e-FETs, the conduction losses occurring in the 3-Φ inverter are proportional to

the square of the root-mean-square (RMS) value of i_{dc}. Considering i_{dc} given by (10),

$$i_{dc,RMS} = \sqrt{\frac{1}{\pi/3}\int_{-\pi/6}^{+\pi/6} \hat{i}_{out}^2 \cos^2(\vartheta)\, d\vartheta} = 0.96\,\hat{i}_{out} \tag{12}$$

results. Consequently, for a given operating point, the conduction losses reduce by 8 % in case 2/3-PWM is applied. Similarly, the local average value of i_{dc} given by (10) can be calculated for each sector of an AC output period, obtaining $\langle i_{dc}\rangle = {}^{3}/_{\pi}\ \hat{i}_{out} = 0.95\,\hat{i}_{out}$.

B. Reduction of Switching Losses

To analyze the occurring switching losses, the 3-Φ bB CSI system illustrated in **Fig. 1** is simplified to the circuit schematic shown in **Fig. 7**. This representation is valid during ① but, according to the symmetry of the phases, similar diagrams can be derived for the rest of the AC output period.

Only the three low-side switches $T_{i,l}$ are considered in **Fig. 7**, since (during ①) the switching state of the three high-side switches $T_{i,h}$ is fixed, i.e. $T_{a,h}$ is permanently on, while $T_{b,h}$ and $T_{c,h}$ are permanently off. It can be recognized that the three line-to-line output voltages v_{xy} are applied across the corresponding pairs of low-side switches $T_{x,l}$ and $T_{y,l}$, and that one switch in turn conducts i_{dc}. Therefore, the series connection of $T_{x,l}$ and $T_{y,l}$ can be considered as a bridge-leg configuration supplied from v_{xy}, having the negative DC-link terminal n as switch node and i_{dc} as load current. Consequently, the switching transition between two states, e.g. from [ab] to [ac], is nothing else than the commutation of a bridge-leg, e.g. of the one formed by $T_{b,l}$ and $T_{c,l}$, and supplied by v_{bc}.

Assuming $i_{dc} > 0$ and practically constant, on the one hand the sign of v_{xy} determines whether a switching state change correspond to a zero voltage switching transition or a hard switching transition, while on the other hand the actual value of v_{xy} determines the occurring switching losses. Moreover, the sequence in which the states of the 3-Φ inverter, i.e. the three closest neighbors of the vector of the reference sinusoidal load phase current $\vec{i}^{*}$ (see **Section III**), are applied within one switching period ultimately defines which v_{xy} are switched [31]; e.g., v_{ab} and v_{bc} are involved in the state sequence [aa]-[ab]-[ac], whereas v_{ab} is replaced by v_{ca} in the state sequence [aa]-[ac]-[ab].

Accordingly, the switching losses occurring in the 3-Φ inverter can be approximated by calculating the average value of the switched v_{xy} over the considered ${}^{\pi}/_{3}$-wide interval of an AC output period, i.e. $\langle v_{sw}\rangle$, which is dependent on ϕ, on $\hat{v}_{out}$ and on the selected state sequence [37], [38]. For simplicity, only hard switching losses are considered in this analysis, i.e. zero voltage switching losses are neglected.

In case of 3/3-PWM, extending the procedure proposed in [38], it can be shown that the state sequence offering minimum switching losses [39] requires two hard switching transitions with an average voltage

$$\langle v_{sw,3/3}\rangle = \frac{3\sqrt{3}}{2\pi}\,\hat{v}_{out} \tag{13}$$

per switching period, independent of ϕ. In case of 2/3-PWM, instead, only the two *active states* [ab] and [ac] are applied within one switching period, i.e. the switched voltage, during ①, is always v_{bc}; hence, $\langle v_{sw,2/3}\rangle$ (the counterpart of $\langle v_{sw,3/3}\rangle$ for 2/3-PWM) can be calculated as the average of $|v_{bc}|$ over the considered ${}^{\pi}/_{3}$-wide interval of an AC output period [29]–[31], obtaining

$$\frac{\langle v_{sw,2/3}\rangle}{\hat{v}_{out}} = \begin{cases} \dfrac{3\sqrt{3}}{\pi}\,(2-\sqrt{3}\cos(\phi)) & ({}^{-\pi}/_{6} < \phi < {}^{+\pi}/_{6}) \\ \dfrac{3\sqrt{3}}{\pi}\,\sin(\phi) & ({}^{+\pi}/_{6} < |\phi| < {}^{+\pi}/_{2}). \end{cases} \tag{14}$$

The mathematical expressions (13) and (14) are visualized in **Fig. 8(a)**. The ratio between $\langle v_{sw,2/3}\rangle$ and $2\,\langle v_{sw,3/3}\rangle$ (where the factor 2 accounts for the fact that two hard switching transitions occur within one switching period in case of 3/3-PWM) is already an indicator of the reduction of switching losses enabled by 2/3-PWM; in particular

$$\frac{\langle v_{sw,2/3}\rangle}{2\,\langle v_{sw,3/3}\rangle} = 2-\sqrt{3}\cos(\phi) = 0.27 \tag{15}$$

is obtained for $\cos(\phi) = +1$.

More precisely, the hard switching losses $P_{sw} = E_{sw} f_{sw}$ occurring

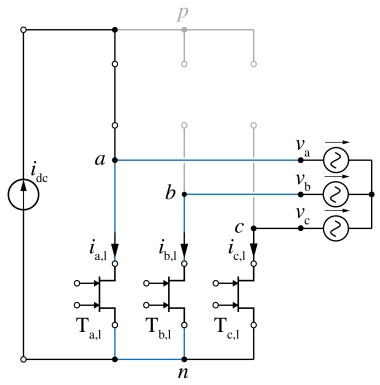


Fig. 7: Simplified representation of the 3-Φ bB CSI system shown in **Fig. 1** for the analysis of the switching losses in the 3-Φ inverter. Each pair of low-side switches forms a bridge-leg supplied from one of the sinusoidal line-to-line output voltages and having the DC-link current as load current.

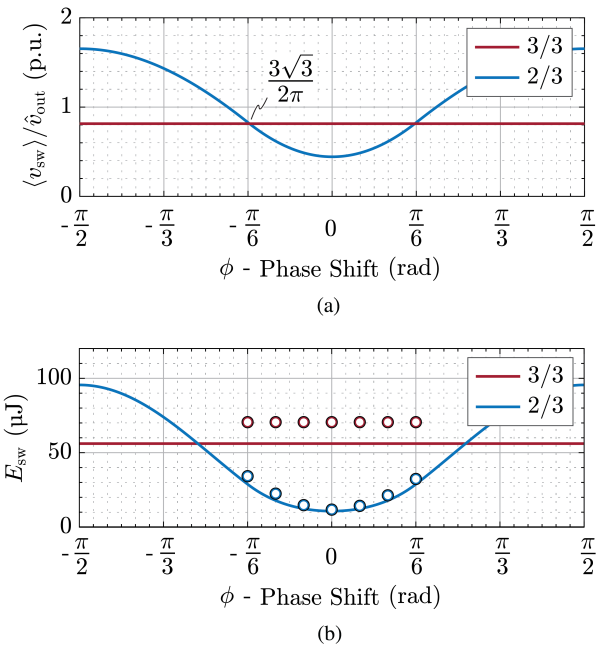


Fig. 8: **(a)** Normalized average (over the considered ${}^{\pi}/_{3}$-wide interval of an AC output period) line-to-line output voltages $\langle v_{sw}\rangle$ switched in the 3-Φ inverter, as function of the phase shift ϕ. **(b)** Switching energy E_{sw} dissipated in the 3-Φ inverter in one switching period, as function of ϕ and of the selected modulation scheme. The lines indicate the results of the simplified analytical calculations while the dots are obtained from circuit simulations.

in the 3-Φ inverter can be calculated according to the conventional VI-overlap switching loss model. Considering only the dependency on the switched voltage given by (13) and (14), since the switched current is practically constant, E_{sw} can be approximated with

$$E_{sw,3/3} = 2\left(k_1 \langle v_{sw,3/3}\rangle + k_2 \langle v_{sw,3/3}\rangle^2\right) \tag{16}$$

and

$$E_{sw,2/3} = k_1 \langle v_{sw,2/3}\rangle + k_2 \langle v_{sw,2/3}\rangle^2 \tag{17}$$

for the case of 3/3-PWM and 2/3-PWM, respectively. The values of k_1 and k_2 in (16) and (17) are determined by the considered operating point (see **Table I**) and by the switching performance of the power semiconductors employed for the realization of the 3-Φ inverter. $k_1 = 60\,\mathrm{A\,ns}$ and $k_2 = 720\,\mathrm{pF}$ [40] are selected as an example in **Fig. 8(b)**, where (16) and (17) are depicted for comparison. It can be observed that 2/3-PWM clearly outperforms 3/3-PWM, as already speculated, especially for low values of ϕ, i.e. in approximately ohmic load conditions. This originates from the fact that 2/3-PWM requires only one hard switching transition per switching period and, in addition, that the switched voltage $|v_{bc}|$ is the smallest among all $|v_{xy}|$ for low values of ϕ [31]. In particular

$$\frac{E_{sw,2/3}}{E_{sw,3/3}} = 0.19 \tag{18}$$

is calculated for $\cos(\phi) = +1$, i.e. in the typical operating conditions of VSDs supplying synchronous machines or passive loads, of PFC rectifiers and of inverters feeding renewable energy into the grid. The result of (18) is lower (and more accurate) than the one of (15) for the influence of the quadratic term present in (16) and (17).

Only for $\pi/3 < |\phi| < \pi/2$, $|v_{bc}|$ features a maximum; hence, all state sequences avoiding the transitions from [ab] to [ac] and vice versa result in lower switching losses. However, 2/3-PWM can nevertheless be applied and [aa] used only as a transitory state between [ac] and [ab], just to avoid the most lossy switching transition associated to the direct commutation from [ac] to [ab]. In this way, it is still possible to benefit from the reduction of conduction losses enabled by 2/3-PWM.

To prove the correctness of the developed analytic procedure, the switching energy E_{sw} is additionally calculated in a simulation environment. The same operating conditions (see **Table I**) and switching loss models (cf. (16) and (17)) are selected, but the exact switched voltage and current values are now considered. The so obtained numerical results are indicated with dots in **Fig. 8(b)**, confirming the accuracy of the analytical results. The discrepancy between calculations and simulations is attributed to the averaging of v_{xy} over the considered $\pi/3$-wide interval of an AC output period and to the neglection of the soft switching losses, as well as of the losses occurring in the switch not involved in the commutation of i_{dc} [41]. A more detailed (but more complex) analytic derivation of E_{sw}, offering a better matching with the numerical results, can be found in [31].

In summary, it should be pointed out that, in particular for $\phi \approx 0$, typical for VSDs employing synchronous machines and passive loads, and for PFC rectifiers and inverters, the reduction of switching losses in the 3-Φ inverter enabled by 2/3-PWM amounts up to 83 %.

V. Circuit Simulation

The detailed operation of the 3-Φ bB CSI system is discussed in this section through the analysis of circuit simulations, focusing on 2/3-PWM and on the developed *Synergetic Control* scheme.

A. Synergetic Control

A key requirement for the correct operation of the 3-Φ bB CSI system, in particular when 2/3-PWM is applied, is a precise control and shaping of i_{dc}; for this purpose, the control structure shown in **Fig. 9** is proposed and described in the following.

The input of the controller, indicated on the left, is the reference speed of the driven electric machine ω^*, assuming a VSD application. Comparing ω^* with the measured speed ω, a reference for the torque and hence for the sinusoidal load (motor) phase currents i_a^*, i_b^* and i_c^* are generated. Since this analysis focuses only on the operation of the 3-Φ bB CSI system, the speed and torque controller (typically implemented in a rotating dq-coordinate frame) is not discussed further.

The central part of the control structure determines the reference switching stage output currents $i_{a,sw}^*$, $i_{b,sw}^*$ and $i_{c,sw}^*$ from i_a^*, i_b^* and i_c^* and compensates for the currents $i_{Co,a}$, $i_{Co,b}$ and $i_{Co,c}$ flowing through C_o. As this part is identical for all the phases, the phase quantities i_a^*, i_b^* and i_c^* are unified in the generic reference sinusoidal load phase current i_{out}^*. Comparing i_{out}^* with the measured i_{out}, i.e. with the measured i_a, i_b and i_c, the error on the sinusoidal load phase current $e_{i,out}$ is calculated. Through a proportional-integral (PI) controller, $e_{i,out}$ is transformed into the reference sinusoidal output voltage v_{out}^* to be applied across C_o. Eventually, an estimation of

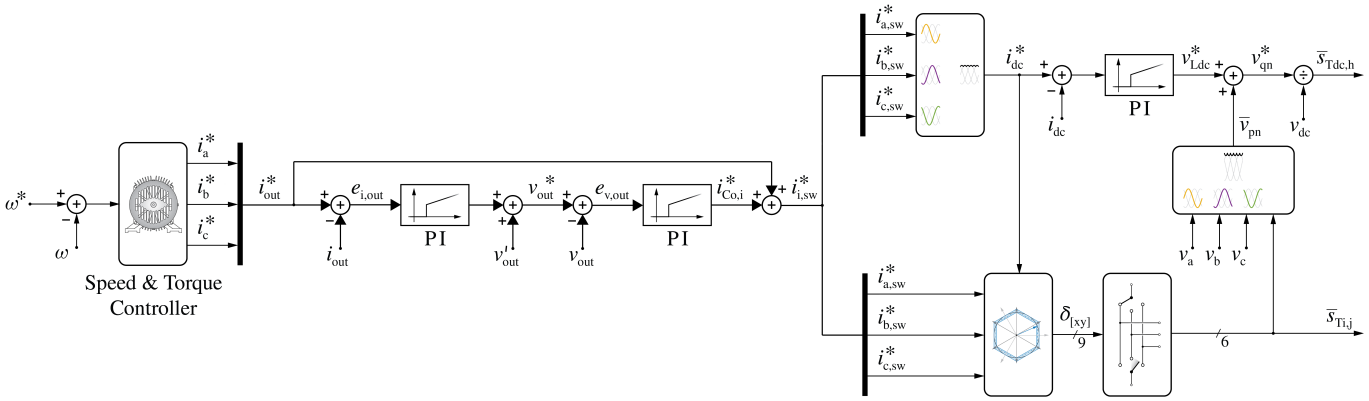


Fig. 9: Structure of the *Synergetic Control* combining the regulation and shaping of i_{dc} with the generation of sinusoidal load phase currents. The input of the controller (left) is the reference speed of the driven electric machine ω^*, while the outputs (right) are the duty-cycle of the buck converter $\bar{s}_{Tdc,h}$ and the nine gate control signals (average in a switching period) of the 3-Φ inverter $\bar{s}_{Ti,j}$. The illustrated control structure is applicable in the *Buck-Mode* (both for 2/3-PWM and for 3/3-PWM) and can be extended to the *Boost-Mode* as described in [28].

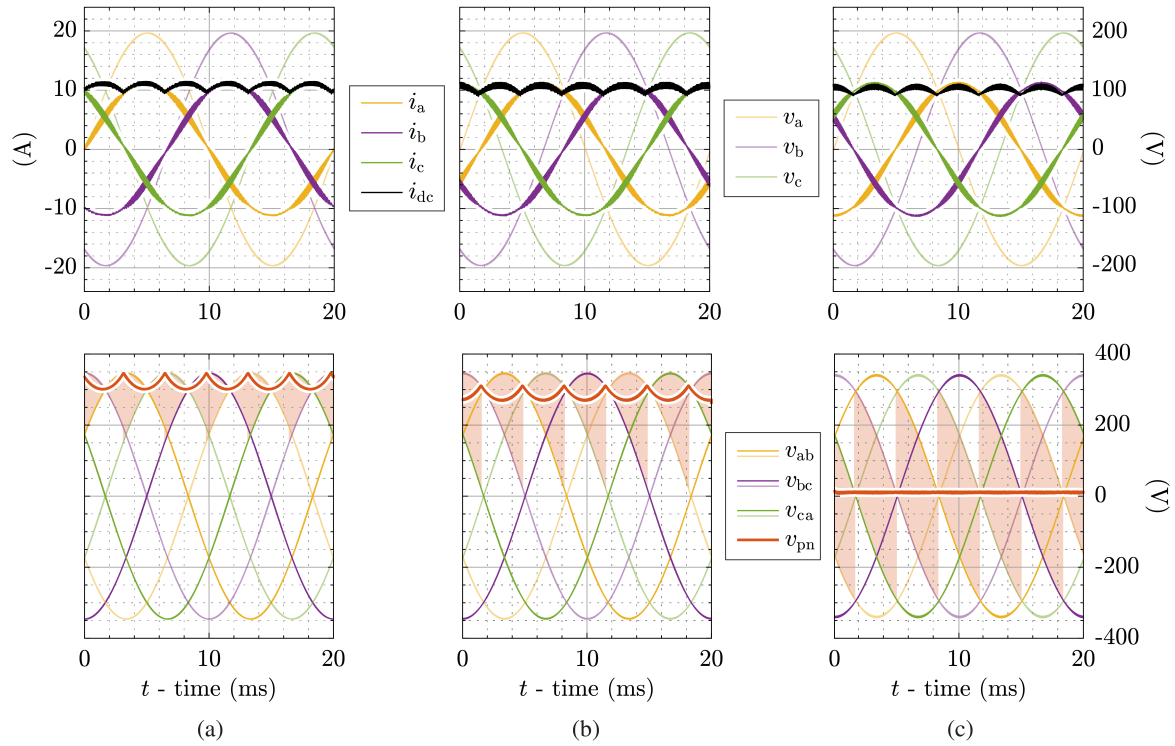


Fig. 10: DC-link current i_{dc}, sinusoidal load phase currents i_a, i_b and i_c, sinusoidal output voltages v_a, v_b and v_c, sinusoidal line-to-line output voltages $\pm v_{ab}$, $\pm v_{bc}$ and $\pm v_{ca}$, and input voltage of the 3-Φ inverter v_{pn} within one AC output period, in case 2/3-PWM is applied, for **(a)** phase shift of the sinusoidal load phase currents and sinusoidal output voltages $\phi \approx 0$, **(b)** $\phi \approx \pi/6$ and **(c)** $\phi \approx \pi/2$. Independently of the value of the load power factor $\cos(\phi)$, a constant peak value $\hat{i}_{out}$ of the sinusoidal load phase currents is maintained. The red lines in the graphs of $v_{out,ll}$ correspond to the average input voltage of the 3-Φ inverter $\bar{v}_{pn}$ within a switching period.

v_{out}, i.e. v'_{out}, can be feed-forwarded to improve the performance of the current controller. In case of VSDs, v'_{out} (see **Fig. 2**), i.e. the back-electromotive force of the electric machine, can be obtained multiplying ω with the speed constant of the considered electric machine. Similarly as for the case of i_{out}, comparing v^*_{out} with the measured v_{out}, the error on the sinusoidal output voltage $e_{v,out}$ is calculated. Again, through a PI controller, $e_{v,out}$ is transformed into the reference filter capacitor current $i^*_{Co,i}$ (i = a, b, c). Summing i^*_{out} with $i^*_{Co,i}$, the reference switching stage output current $i^*_{i,sw}$ (i = a, b, c) is finally obtained.

Phase quantities are necessary in the right part of the block diagram; hence $i^*_{i,sw}$ is transformed back into $i^*_{a,sw}$, $i^*_{b,sw}$ and $i^*_{c,sw}$. This part is divided in two sub-parts: one provides the duty-cycle of the buck converter $\bar{s}_{Tdc,h}$, while the other one determines the average (within one switching period) gate control signals of the 3-Φ inverter $\bar{s}_{Ti,j}$.

In the upper part, $i^*_{a,sw}$, $i^*_{b,sw}$ and $i^*_{c,sw}$ are first combined to generate the reference DC-link current i^*_{dc}, as defined in (10). Comparing i^*_{dc} with the measured i_{dc}, the reference voltage to be applied across L_{dc}, i.e. v^*_{Ldc}, is determined through the third PI controller. Summing v^*_{Ldc} with $\bar{v}_{pn}$, obtained from the lower part of the block diagram, the reference output voltage of the buck converter v^*_{qn} is obtained. Finally, dividing v^*_{qn} with v_{dc}, also $\bar{s}_{Tdc,h}$ is determined.

In the lower part, $i^*_{a,sw}$, $i^*_{b,sw}$, $i^*_{c,sw}$ and i^*_{dc} are first inserted in (7) to determine the nine duty-cycles $\delta_{[xy]}$. For example, for $\vartheta = 0$ (during ①), $\delta_{[ac]} = \delta_{[ab]} = 0.5$ (and all other $\delta_{[xy]} = 0$) results. Thus, the nine $\delta_{[xy]}$ are converted to the six $\bar{s}_{Ti,j}$, as indicated in (6). In the example, $\delta_{[ac]} = \delta_{[ab]} = 0.5$ translates into $\bar{s}_{Ta,h} = 1$, $\bar{s}_{Tb,l} = \bar{s}_{Tc,l} = 0.5$ and all other $\bar{s}_{Ti,j} = 0$. Finally, the six $\bar{s}_{Ti,j}$ are combined with the measured v_a, v_b and v_c to obtain

$$\bar{v}_{pn} = \sum_{i\,=\,a,\,b,\,c} \left(\bar{s}_{Ti,h} - \bar{s}_{Ti,l}\right) v_i, \tag{19}$$

required in the upper part of the control. In the example, (19) expands to $\bar{v}_{pn} = v_a - 0.5\,(v_b + v_c)$.

As clarified with this explanation, the control scheme shown in **Fig. 9** is considered as *Synergetic*, since the upper and lower parts mutually contribute to the correct operation of the 3-Φ bB CSI system, i.e. the buck converter shapes i_{dc} in support of the generation of sinusoidal load phase currents, finally performed by the 3-Φ inverter. This control concept is applicable in the *Buck-Mode*, but can be easily extended to the *Boost-Mode* [28].

To conclude, it should be additionally noticed that, the same exact control structure can be considered for 3/3-PWM, except for (10). In case of 3/3-PWM, in fact, i^*_{dc} is constant and $i^*_{dc} = I^*_{dc} \geq i^*_{i,sw}$ (i = a, b, c) is necessary. As shown in the next section, this allows a seamless transition between 3/3-PWM and 2/3-PWM and viceversa.

B. Simulation Results

The functioning of the *Synergetic Control* scheme described in **Section V-A** is verified in the following analyzing the results of closed-loop circuit simulations of the 3-Φ bB CSI system, in different operating conditions.

In particular, in the upper part of **Fig. 10(a)**, **(b)** and **(c)**, the simulated waveforms of i_{dc} and i_{out} are shown together with the ones of v_{out}, for $\phi \approx 0$, $\pi/6$ and $\pi/2$. Differently from the ideal case considered in **Fig. 3(b)**, a small discrepancy between i_{out} and i_{dc}, due to $i_{Co,i}$, can be observed here. Although the same values of $\hat{i}_{out}$ (hence i_{dc}) and $\hat{v}_{out}$ are considered in these three plots, the different

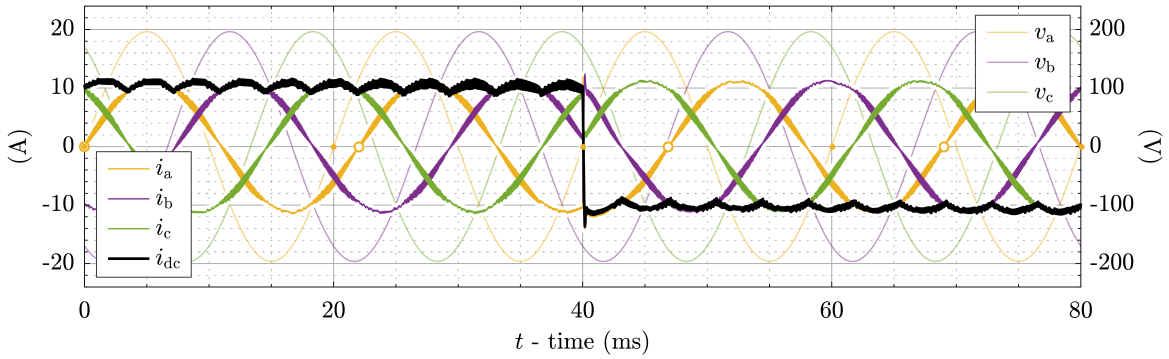


Fig. 11: DC-link current i_{dc}, sinusoidal load phase currents i_a, i_b and i_c, sinusoidal output voltages v_a, v_b and v_c within four AC output periods, in case 2/3-PWM is applied, and for load power factor $\cos(\phi)$ decreasing linearly from $+1$ to -1. Independently of the value of $\cos(\phi)$, a constant peak value $\hat{i}_{out}$ of the sinusoidal load phase currents is maintained. At time $t = 40\,\text{ms}$, $\cos(\phi)$ reaches 0 and subsequently changes sign, i.e. the direction of power flow is swapped and i_{dc} must be inverted accordingly.

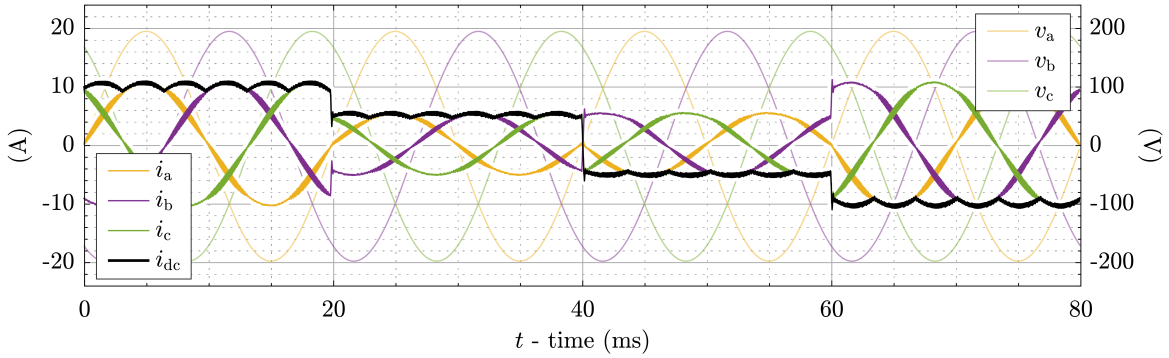


Fig. 12: DC-link current i_{dc}, sinusoidal load phase currents i_a, i_b and i_c, sinusoidal output voltages v_a, v_b and v_c within four AC output periods, in case 2/3-PWM is applied, for load power factor $\cos(\phi) = +1$ for time $t < 40\,\text{ms}$ and $\cos(\phi) = -1$ for $t > 40\,\text{ms}$, and for different peak values $\hat{i}_{out}$ of the sinusoidal load phase currents, i.e. for full and half rated output power P_{out}.

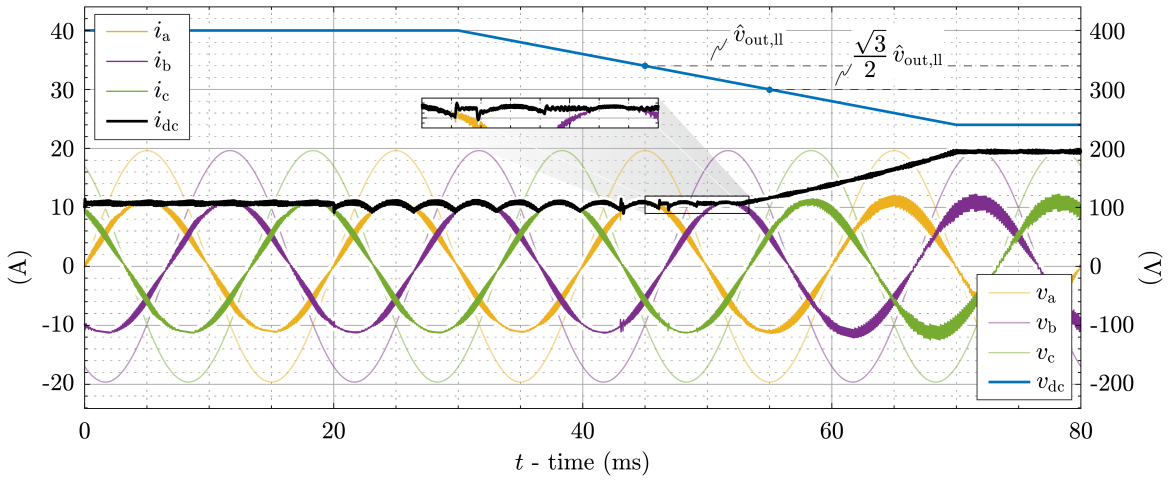


Fig. 13: DC-link current i_{dc}, sinusoidal load phase currents i_a, i_b and i_c, sinusoidal output voltages v_a, v_b and v_c, and supplying DC input voltage v_{dc} within four AC output periods, for load power factor $\cos(\phi) = +1$. By reducing v_{dc}, a transition from the *Buck-Mode* to the *Boost-Mode* occurs; additionally, both 3/3-PWM and 2/3-PWM are applied in the *Buck-Mode*.

values of $\cos(\phi)$ result in different values of the output power P_{out}. Accordingly, the reduction of $\bar{v}_{pn}$, directly proportional to the one of P_{out}, is highlighted in the lower part of **Fig. 10(a)**, **(b)** and **(c)**. For completeness, the simulated waveforms of i_{dc}, i_{out} and v_{out}, for $-1 \leq \cos(\phi) \leq +1$, are shown in **Fig. 11**. The smooth decrease of $\cos(\phi)$ can be noticed observing how, e.g. the waveforms of i_a and v_a, are in phase at time $t = 0\,\text{s}$ and in phase opposition at $t = 80\,\text{ms}$. To guarantee the controllability of i_{dc}, i.e. to guarantee that $\bar{v}_{pn}$ is sufficiently positive when the direction of power flow is inverted (see **Section V-A**), ϕ instantaneously varies from $\pi/2 - \pi/8$ to $\pi/2 + \pi/8$ at $t = 40\,\text{ms}$. The same waveforms are summarized in **Fig. 12**, for $\cos(\phi) = \pm 1$, and for different values of $\hat{i}_{out}$, to analyze the dynamic response of the *Synergetic Control* scheme. Finally, the two operating modes described in **Section II-B**, i.e. the *Buck-Mode*

and the *Boost-Mode*, and the two modulation schemes presented in **Section III**, i.e. 3/3-PWM and 2/3-PWM, are jointly shown in **Fig. 13**, for $\cos(\phi) = +1$. At $t = 0\,\mathrm{s}$, the supplying DC input voltage $v_{\mathrm{dc}} > \hat{v}_{\mathrm{out,ll}}$ allows both 3/3-PWM and 2/3-PWM in the *Buck-Mode*; hence, both modulations are independently applied in the first and second AC output periods, respectively. At $t \approx 40\,\mathrm{ms}$, $v_{\mathrm{dc}} < \hat{v}_{\mathrm{out,ll}}$; thus, although still in the *Buck-Mode*, 2/3-PWM can be used only in combination with 3/3-PWM, depending on the instantaneous value of v_{out}. When $v_{\mathrm{dc}} > \sqrt{3}/2\,\hat{v}_{\mathrm{out,ll}}$ after $t \approx 60\,\mathrm{ms}$, the *Boost-Mode* is entered.

To summarize, in all the operating conditions of interest, i.e. for different values of $\cos(\phi)$ and $\hat{i}_{\mathrm{out}}$, the 3-Φ bB CSI system outputs the desired current and voltage waveforms and can be successfully operated with 2/3-PWM.

VI. Aspects of Practical Realization

In this section, after introducing research samples of 2G MB GaN e-FETs, a prediction of the efficiency and power density achievable by the 3-Φ bB CSI system is provided.

A. Dual-Gate Monolithic Bidirectional GaN e-FET

The power devices selected for the realization of the 3-Φ inverter are $\pm 600\,\mathrm{V}$ $26\,\mathrm{m\Omega}$ 2G MB GaN e-FETs [23]. The main characteristics of this switch (currently only available as research sample) are compared in **Table II** with the ones of the best-in-the-market conventional GaN power transistor in the same voltage class, i.e. a $650\,\mathrm{V}$ $25\,\mathrm{m\Omega}$ GaN e-FET [42].

To extend the operation of the conventional devices to *four-quadrants*, while maintaining the same overall on-state resistance $R_{\mathrm{ss,on}}$, two anti-series and two parallel devices must be connected as shown in **Fig. 14(a)**; this massively increases costs and, as highlighted by **Fig. 14(b)**, the required PCB area with respect to the solution based on the MB switch. Additionally, due to the increased parasitic output capacitance C_{oss}, the Figure of Merit (FoM) [13] of the so obtained AC-switch becomes almost three times worse than the one of the MB device. To summarize, the considered 2G MB GaN e-FET is expected to allow a performance breakthrough of 3-Φ bB CSI systems, and

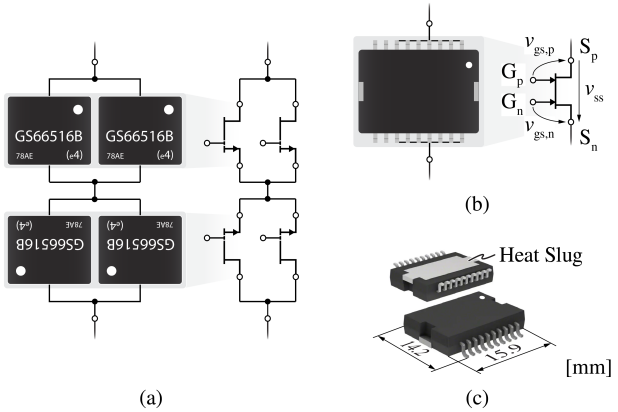


Fig. 14: Conventional realization of a switch with bidirectional voltage blocking capability and allowing controlled bidirectional current flow, i.e. a *four-quadrant* (AC) switch, with **(a)** two anti-series/two parallel $650\,\mathrm{V}$ $25\,\mathrm{m\Omega}$ GaN e-FETs [42] compared with **(b)** a single $\pm 600\,\mathrm{V}$ $26\,\mathrm{m\Omega}$ 2G MB GaN e-FET [23] (geometric proportions of the packages are preserved). Both solutions **(a)** and **(b)** achieve approximately the same voltage blocking capability and overall on-state resistance, however **(b)** enables a massive saving in terms of package size. **(c)** Perspective view of the 20-pin package of the 2G MB GaN e-FET.

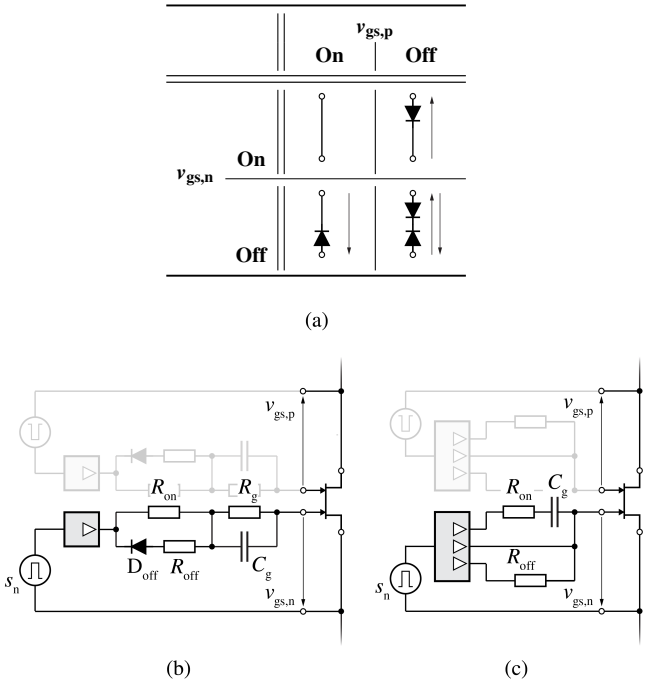


Fig. 15: (a) Equivalent circuit of the 2G MB GaN e-FET depending on the applied gate voltages $v_{\mathrm{gs,n}}$ and $v_{\mathrm{gs,p}}$. **(b)** Conventional gate driver circuit adapted to GITs [44] based on a commercial IC and **(c)** gate driver circuit for GITs based on a specialized IC featuring a dedicated pin for the supplying of the constant gate current [45].

potentially of all circuit topologies requiring AC-switches as, e.g., AC/AC matrix converters.

In order to simultaneously control the bidirectional voltage blocking and current flow capabilities of the 2G MB GaN e-FET (see **Fig. 15(a)**), two gate voltages $v_{\mathrm{gs,n}}$ and $v_{\mathrm{gs,p}}$ must be separately applied to the 2G structure, as indicated in **Fig. 14(b)**. Alternatively, if only one gate is controlled, only unidirectional current flow is possible. The gate voltages $v_{\mathrm{gs,n}}$ and $v_{\mathrm{gs,p}}$ must be isolated from each other because of the common-drain structure (split-source structure) which, based on a single drift layer, yields to lower values of $R_{\mathrm{ss,on}}$ compared with the alternative common-source structure [20]. Additionally, the potential of the substrate must be left floating, while it is typically connected to the only source potential available in conventional GaN power transistors; different switching behaviors of the 2G MB GaN e-FET are observed when the substrate is connected to the one or the other source potentials, and are currently under investigation.

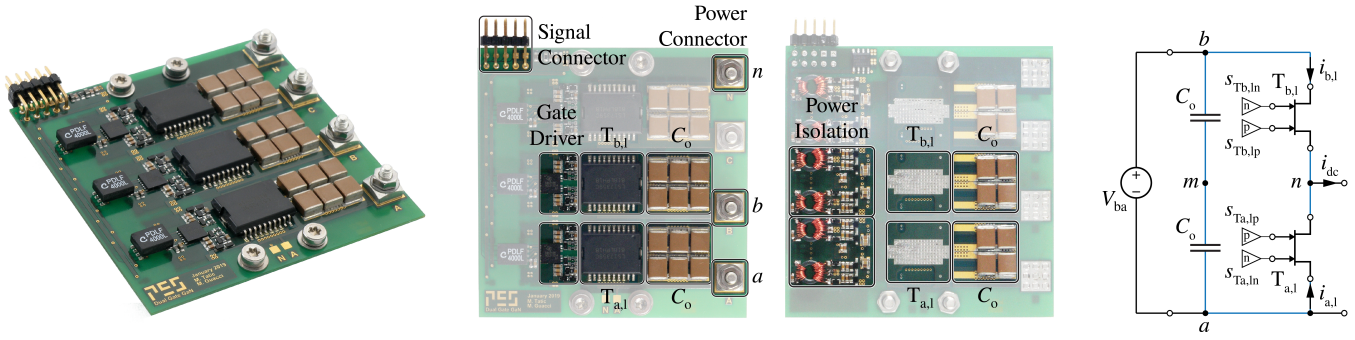
Since the device is of *Gate Injection Transistor* (GIT) type [43], constant currents (in the mA-range) must flow through the gates to modulate the conductivity of the two-dimensional electron gas (2DEG) channel during on-state. As visible in **Fig. 15(b)**, conventional gate driver circuits can be modified to include this feature [44]; alternatively, an *ad hoc* integrated circuit (IC) [45], i.e. featuring a dedicated pin for the supplying of the constant gate current, can be used. Adopting the latter approach, the compact gate driver design illustrated in **Fig. 15(c)**, requiring only three discrete components between the IC and the gate terminal, can be realized.

B. Performance Estimation of the 3-Φ bB CSI System

The presented 2G MB GaN e-FETs, whose operation is verified in the **Appendix**, together with the simulation results discussed in **Section V-B**, demonstrate the feasibility of the 3-Φ bB CSI system operated with 2/3-PWM, and rise the interest in estimating its key

TABLE II: Main characteristics of the selected 2G MB GaN e-FET compared to the best-in-the-market conventional GaN power transistor in the same voltage class as a single device (1x) and in the two anti-series/two parallel configuration (4x).

Power Semiconductor			$V_{ss,MAX}$	$I_{ss,MAX}$ @ 25 °C	$R_{ss,on}$ @ 25 - 150 °C	$C_{oss,Q}$ @ 400 V	$C_{rss,Q}$ @ 400 V	FoM = $(R_{ss,on}C_{oss,Q})^{-1}$ @ 25 °C - 400 V	Package Size
Panasonic Co.	EDLS06SMD		±600 V	92 A	26 - 43 mΩ	190 pF	40 pF	202 GHz	2.3 cm²
GaN Systems Inc.	GS66516	(1x)	650 V	60 A	25 - 65 mΩ	281 pF	8 pF	142 GHz	1.0 cm²
		(4x)	±650 V	120 A		562 pF	16 pF	71 GHz	4.0 cm²



(a) (b) (c) (d)

Fig. 16: **(a)** Perspective view, **(b)** top view and **(c)** mirrored bottom view of the test bench PCB comprising the three 2G MB GaN e-FETs $T_{i,l}$ forming the low-side of the 3-Φ inverter, their respective gate drivers [45] with isolated signal transmission and isolated power supply, and a fraction of the overall output filter capacitors C_o [46], in addition to robust power and signal connectors. The PCB is squared, with each edge measuring 7.1 cm (2.8 in). **(d)** Bridge-leg formed by $T_{a,l}$ and $T_{b,l}$ on which the waveforms shown in **Fig. 17** are measured. The blue line should help to recognize this bridge-leg structure in **Fig. 1** and **Fig. 7**.

performance indexes, i.e. the achievable efficiency and power density, e.g. for the specifications given in **Table I**.

In particular, the design of the 3-Φ bB CSI system analyzed in the simulation environment (see **Fig. 10**) is estimated to achieve an efficiency $\eta = 98.4\,\%$, a volumetric power density $\rho = 16\,\mathrm{kW/dm^3}$ ($260\,\mathrm{W/in^3}$) and a gravimetric power density $\beta = 6.1\,\mathrm{kW/kg}$ at a switching frequency $f_{sw} = 140\,\mathrm{kHz}$, if a cooling system performance index CSPI $= 15\,\mathrm{W/K\,dm^3}$ is considered [47]. The power density figures are mainly limited by the volume ($81\,\mathrm{cm^3}$) and weight (240 g) of $L_{dc} = 550\,\mu\mathrm{H}$ [48]. Accordingly, if the allowed peak-to-peak current ripple on i_{dc} is increased from 10 %, as selected for **Fig. 10** (in order to clearly describe the operation of the 3-Φ inverter) to 30 %, L_{dc} can be reduced to 185 µH, resulting in a more compact and lighter inductor design, i.e. in a volume of $50\,\mathrm{cm^3}$ ($3.0\,\mathrm{in^3}$) and in a weight of 115 g; thus, for the same $\eta = 98.4\,\%$, the power density figures increase to $\rho = 18\,\mathrm{kW/dm^3}$ ($295\,\mathrm{W/in^3}$) and $\beta = 7.7\,\mathrm{kW/kg}$. If 3/3-PWM is applied to the same design, η drops below 98 %; an even more significant reduction is observed for higher values of f_{sw}, when the switching losses dominate the loss breakdown.

In all designs, the buck converter is realized with the best-in-the-market conventional GaN power transistor listed in **Table II**, whose performance are reported in [40]; moreover the same switching frequency is considered for the buck converter and for the 3-Φ inverter [28].

VII. Conclusion

A 3-Φ bB CSI system employing a variable DC-link current control strategy denominated *Two-Third Pulse-Width Modulation* (2/3-PWM) and 2G MB GaN e-FETs in its boost-type 3-Φ current DC-link inverter output stage is analyzed in this paper. Circuit simulations are performed to verify the operation of the 3-Φ bB CSI system, considering 2/3-PWM and the developed *Synergetic Control* concept. Moreover, analytic calculations quantify a reduction of conduction losses of 8 % and a massive reduction of switching losses of 83 % (in case of unity load power factor), for 2/3-PWM in comparison with conventional 3/3-PWM. The operation of the 2G MB GaN e-FETs, which are suitable for any topology requiring AC-switches, is verified in a hardware prototype, where voltages up 400 V and currents up to 10 A are continuously switched. These novel devices, in combination with 2/3-PWM, have the potential to significantly enhance the performance of 3-Φ bB CSI systems, ultimately favoring their usage in place of 3-Φ Bb VSI systems; in particular, a 3-Φ bB CSI system, rated for an output power $P_{out} = 3.3\,\mathrm{kW}$, is estimated to simultaneously achieve an efficiency $\eta = 98.4\,\%$ and a volumetric power density $\rho = 18\,\mathrm{kW/dm^3}$ ($295\,\mathrm{W/in^3}$) at a switching frequency $f_{sw} = 140\,\mathrm{kHz}$ when 2/3-PWM is applied.

Appendix

A test bench for the 2G MB GaN e-FETs introduced in **Section VI-A** is realized as illustrated in **Fig. 16(a)**, **(b)** and **(c)**. It implements the three switches forming one side (e.g. the low-side) of the 3-Φ inverter, since, as clarified in **Section IV-B**, this is sufficient, due to symmetry properties, to quantify the losses occurring in the entire 3-Φ inverter. In addition to the three $T_{i,l}$, the realized PCB includes the associated gate drivers [45] (see **Fig. 15(b)**) with isolated signal transmission and isolated power supply, and a fraction of the overall C_o [46].

In particular, the bridge-leg formed by $T_{a,l}$ and $T_{b,l}$, highlighted in **Fig. 16 (d)**, is considered in the following. This bridge-leg is operated connecting a supplying DC input voltage source V_{ba} between the terminals b and a, and a resistive-inductive load at the switch node n to sink the load current i_{dc}. Measured waveforms of the switch node voltage v_{na} and of i_{dc} are recorded and plotted in **Fig. 17(a)** for $V_{ba} = 400\,\mathrm{V}$ and $\langle i_{dc} \rangle = 5\,\mathrm{A}$ (blue) and 0 A (red) in soft (zero voltage and zero current) switching and hard switching conditions. No significant overvoltage or oscillations are observed on v_{na}, while turn-off zero current and hard switching transitions are performed at

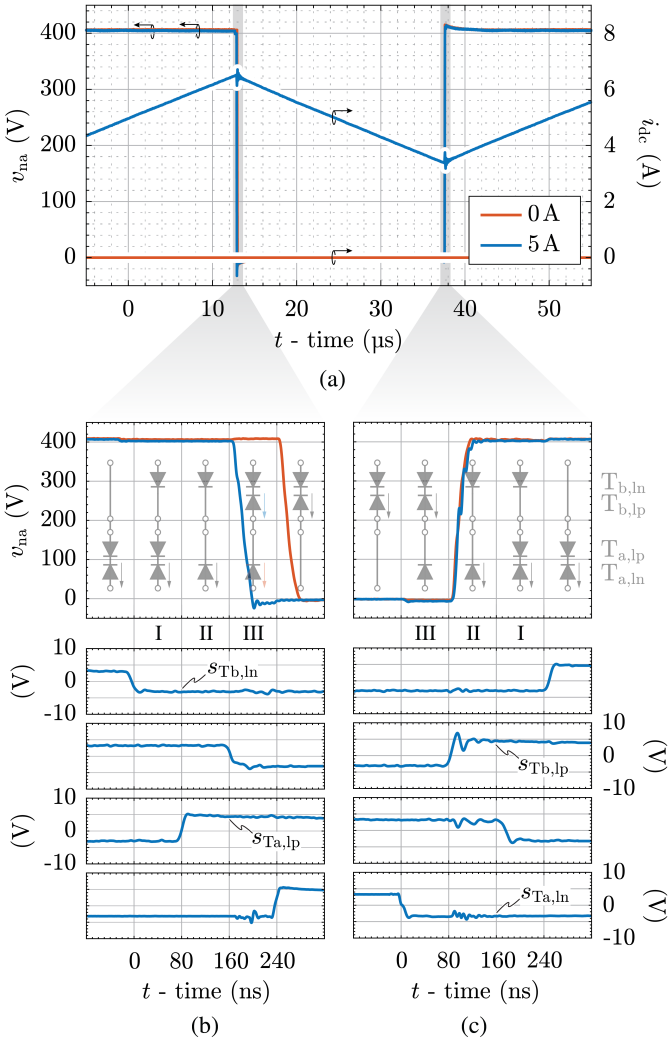


Fig. 17: **(a)** Measured waveforms of the switch node voltage v_{na} and of the load current i_{dc} during continuous operation of the bridge-leg shown in **Fig. 16 (d)**, for a supplying DC input voltage $V_{ba} = 400\,\mathrm{V}$ and an average output current $\langle i_{dc} \rangle = 5\,\mathrm{A}$ (blue) and $0\,\mathrm{A}$ (red). **(b)**-**(c)** Zoomed view of v_{na} during a turn-on zero voltage switching transition (blue in **(b)**), a turn-on zero current switching transition (red in **(b)**), a turn-off zero current switching transition (red in **(c)**), and a turn-off hard switching transition (blue in **(c)**), associated gate signals $s_{Ti,lp}$ and $s_{Ti,ln}$ determined according to the current sign dependent multi-step commutation strategy, and equivalent circuit of the bridge-leg.

switching speeds $^{dv}/_{dt}$ of about $15\,^{V}/_{ns}$ (red and blue in **Fig. 17(c)**, respectively). Moreover, the voltage slope occurring for the turn-on zero voltage switching transition (blue in **Fig. 17(b)**) confirms the expected $C_{oss,Q}$ value according to $2\,C_{oss,Q} = {}^{i_{dc}}/_{dv/dt}$ (cf. **Table II**). For 2G MB GaN e-FETs (and AC-switches in general), particular care must be taken during the switching transition, such that always a path for the switched current is provided while one of the two switches involved in the commutation blocks the bipolar switched voltage (see **Fig. 15(a)**). Hence, the four gate signals $s_{Ti,lp}$ and $s_{Ti,ln}$ are generated according to a current sign dependent multi-step commutation strategy [23], as illustrated in the lower part of **Fig. 17(b)** and **(c)** for the case of $i_{dc} > 0$. Additionally, the zoomed view of the measured v_{na} is overlapped with the equivalent circuits of the bridge-leg (I, II and III) determined by $s_{Ti,lp}$ and $s_{Ti,ln}$ (see **Fig. 15(a)**). These plots highlight how, depending on the type of switching transition, i.e. zero voltage, zero current or hard, the commutation takes place at different instants of the multi-step sequence.

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