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G. Knabben,
D. Neumayr,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

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Gustavo C. Knabben, Dominik Neumayr and Johann W. Kolar
Power Electronic Systems Laboratory
ETH Zurich, Switzerland
{knabben,neumayr,kolar}@lem.ee.ethz.ch

***Abstract*—Despite the increasing performance of power semiconductors and passives components, limited timing resolution in off-the-shelf available digital control hardware often prevents the switching frequency in kW-scale dc/ac power conversion to be increased above several MHz for the sake of extreme power densities. In this paper an alternative approach to generate a sinusoidal output voltage, based on constant duty cycle frequency shift control of a high frequency resonant inverter stage and a subsequent synchronous cycloconverter, is analyzed. The design of the presented converter is facilitated by means of a derived mathematical model. A novel closed-loop control system is proposed which achieves tight regulation of the output voltage by means of controlling the switching frequencies of the involved bridge legs operated in resonant mode. Characteristic waveforms of the dc/ac converter during steady-state and load transients are presented. Two distinct implementations of the resonant inverter stage, constituting an intermediate voltage or intermediate current link, are analysed and compared.**

***Index Terms*—Dc/Ac Inverter, Soft-Switching, Resonant Converter, Cycloconverter, Frequency Shift, Phase Shift.**

I. Introduction

Extremely compact power conversion systems are a key technology in the automotive and telecom industry and the design of compact power electronics has recently been promoted by Google and IEEE in the Little Box Challenge, an open competition to build the world's smallest $2\,\mathrm{kW}$ PV inverter. As can be seen from the technical documentation of the LBC finalists [1], [2], the majority of approaches relied on a single-stage full-bridge based PWM inverter topology with time-varying duty cycle for sinusoidal output voltage generation. A constant or variable switching frequency in the range of $0.1\,\mathrm{MHz}$ – $1\,\mathrm{MHz}$ was selected by the finalists, where several teams employed sophisticated triangular current mode (TCM) control to enable soft-switching and push the frequency up to the MHz. Apart from the residual switching loss, despite employing latest GaN semiconductor technology and zero voltage switching (ZVS) [3], and the limited performance of magnetics at high frequency (HF), today's existing off-the-shelf digital control hardware (microcontrollers, FPGAs, PWM controller ICs) prevents the switching frequency to be increased above $2\,\mathrm{MHz}$ – $3\,\mathrm{MHz}$ due to unacceptably low duty cycle resolution. Now, keeping the expected performance improvement of WBG semiconductors and magnetic core materials [4] in mind, a dc/ac conversion topology which supports switching frequencies up to ten MHz, while achieving both a low THD and tight regulation of the ac voltage with reasonable digital control effort, is needed.

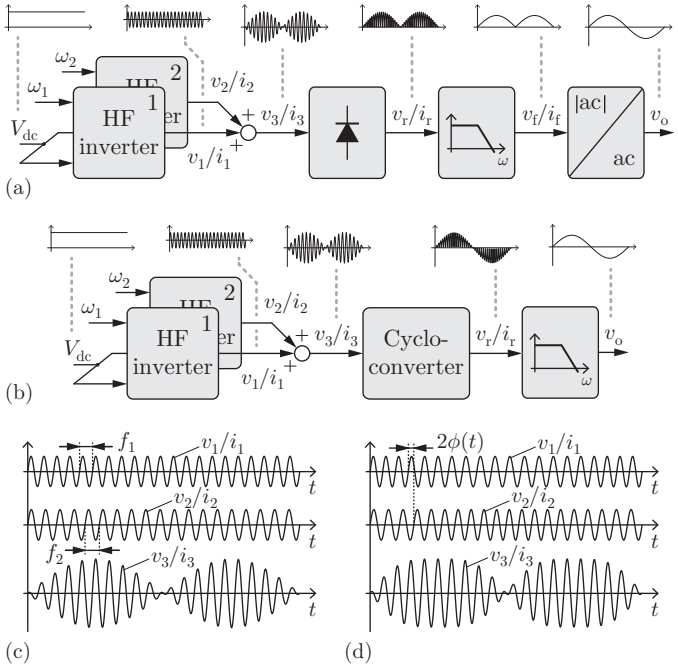

Fig. 1: (a) Generic concept of a voltage- or current-based sine amplitude modulation (SAM) high frequency (HF) link dc/ac converter with diode rectification, low-pass filter and unfolding stage. The diode rectifier and LF unfolding stages can also be replaced with a cycloconverter (b). The HF inverter stages are controlled by means of either (c) sine-wave frequency shift ($\omega_{1,2}^{\mathrm{FS}} = \omega_s t \pm \omega_o t$) or (d) phase shift ($\omega_{1,2}^{\mathrm{PS}} = \omega_s t \pm \phi(t)$), generating an intermediate HF voltage or current link (depending on the selected inverter implementation) with sinusoidally varying amplitude (SAM).

Two alternative concepts to generate a low frequency (LF) sinusoidal voltage from a dc source are schematically shown in Fig. 1 (a) (b). Two resonant inverter stages, HF inverter 1 and 2, are controlled such that the respective sinusoidal output voltages, v_1 and v_2, exhibit either (i) a slight difference in

frequency or (ii) a time-varying phase-shift. The voltage difference of v_1 and v_2 constitutes the voltage v_3 of a HF voltage link which exhibits a sine amplitude modulation (SAM), i. e. the envelope of v_3 changes over time and resembles a rectified sinusoid with the desired output frequency. As shown in Fig. 1 (a) the SAM voltage link is rectified and the HF content removed by a subsequent low-pass filter. The sinusoidal output voltage is then obtained by means of a $|\text{ac}|/\text{ac}$ unfolding stage. This three-stage approach has been proposed in [5]–[7]. The diode rectifier and LF unfolder can also be replaced with a cycloconverter as depicted in Fig. 1 (b). This two-stage approach with resonant link has been studied by the authors in [8]–[10]. It should be noted that, depending on the selected topology to implement the HF inverter stages, the generated HF link can also feature impressed currents (i_1,i_2,i_3) rather than voltages (v_1,v_2,v_3). A similar dc/ac conversion approach including a HF current link with fixed amplitude and a half-wave cycloconverter is described in [11]. By means of phase-control of the cycloconverter with respect to the resonant current a very efficient power delivery to the mains is achieved. The modulation concept of operating the HF resonant inverters with constant $50\,\%$ duty cycle but slightly different frequency, termed sine-wave frequency shift (FS) in literature [9], is depicted in Fig. 1 (c) showing two sine waves v_1 and v_2 of same amplitude $\hat{V}$ but different angular frequencies,

$$\begin{aligned} v_1 &= \hat{V}\sin\left(\omega_1 t\right) = \hat{V}\sin\left(\omega_\mathrm{s} t + \omega_\mathrm{o} t\right), \\ v_2 &= \hat{V}\sin\left(\omega_2 t\right) = \hat{V}\sin\left(\omega_\mathrm{s} t - \omega_\mathrm{o} t\right). \end{aligned} \tag{1}$$

The difference between v_1 and v_2 then forms the SAM HF voltage link,

$$v_3 = v_1 - v_2 = 2\hat{V}\sin\left(\omega_\mathrm{o} t\right)\cos\left(\omega_\mathrm{s} t\right), \tag{2}$$

with center frequency $\omega_\mathrm{s} = 2\pi f_\mathrm{s}$ and with $\omega_\mathrm{o} = 2\pi f_\mathrm{o}$ sinusoidally varying amplitude, where f_o is the desired frequency of the ac output. Although the duty cycle can be kept constant in case of FS, there is still a high requirement on the available resolution of the modulator. Given the ratio of switching frequency and clock frequency of the implemented modulator (microcontroller or FPGA),

$$N = \frac{f_\mathrm{clk}}{f_\mathrm{s}}, \tag{3}$$

the smallest difference in frequency which can be set is

$$\Delta f_s = \frac{f_\mathrm{clk}}{N(N+1)}. \tag{4}$$

For a clock frequency of $150\,\mathrm{MHz}$ and $\Delta f_s = 0.5\,\mathrm{Hz}$ Eq. (4) can be solved to find $N = 17320$. Thus, a frequency resolution of $0.5\,\mathrm{Hz}$ can only be achieved if the switching frequency of the HF inverter stage is kept below roughly $8.7\,\mathrm{kHz}$. However, this apparent limitation to use FS modulation for above MHz operation can be resolved if dedicated clock generation or direct digital synthesis (DDS) ICs are employed in addition to standard microcontroller or FPGA hardware. By means of such frequency and/or phase shift programmable ICs, control signals up to hundreds of MHz with frequency resolution better than $0.1\,\mathrm{Hz}$ can be generated [12], [13]. Another option to generate a voltage link with sinusoidally varying envelope is to operate both HF inverters with identical frequency but apply a time-varying phase shift (PS), $\phi(t)$, between the respective control signals such that,

$$\begin{aligned} v_1 &= \hat{V}\sin\left(\omega_\mathrm{s} t + \phi(t)\right), \\ v_2 &= \hat{V}\sin\left(\omega_\mathrm{s} t - \phi(t)\right), \\ v_3 &= v_1 - v_2 = 2\hat{V}\sin\left(\phi(t)\right)\cos\left(\omega_\mathrm{s} t\right), \end{aligned} \tag{5}$$

as analyzed thoroughly in [8]. Compared to FS, sine-wave PS is a more generic method which allows to generate envelopes of arbitrary shape and frequency and is the preferred technique by the authors in [6], [7], [14]–[21]. Nevertheless, since PS modulation at very high frequency also requires dedicated ICs for control signal generation and because the phase shift between the control signals must be continuously updated over time, sine-wave FS is the preferred choice in this work.

In this paper a two-stage HF resonant link based dc/ac converter employing sine-wave FS control is analysed in detail. Two variants of the HF inverter stage, a SAM voltage and current link, are introduced in Sec. II and the basic operation of the topology is explained. A comprehensive mathematical model of the converters is derived in Sec. III in order to identify optimal values for the passive components. Moreover, a novel control system is proposed for tight regulation of the output voltage by means of FS. Section IV presents typical waveforms of the converter with proposed FS control at stationary operation and during load transients obtained from simulations. Furthermore, the studied HF voltage and current link converters are compared to a single-stage TCM inverter by means of several performance indicators, highlighting the benefits and drawbacks of the respective topologies.

II. SAM HF Link Converter

The dc/ac converter topologies analyzed in this paper are shown in Fig. 2. The SAM voltage link based converter is depicted in Fig. 2 (a), where the HF inverter stage is implemented by means of two parallel resonant converters (PRC). Each PRC is formed by a bride-leg with a LC resonant tank connected between the respective switch node (A or B) and the split dc-link midpoint O. Bridge-leg A and B are operated with $50\,\%$ duty-cycle and frequencies ω_1 and ω_2 slightly above the resonance frequency of the resonant tank to reduce load dependency of the voltage gain, as discussed in Sec. III-A, and to enable ZVS.

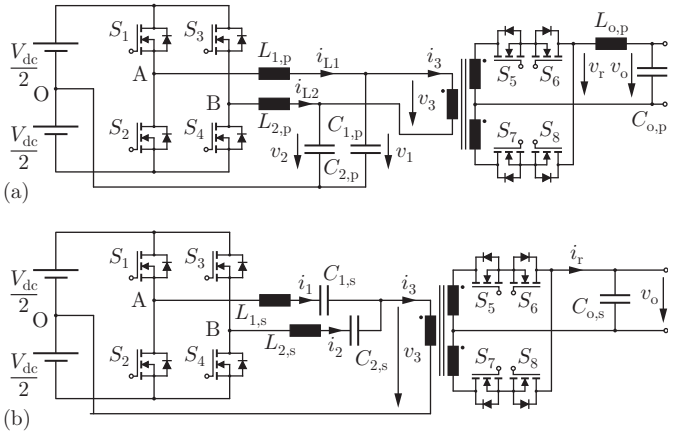

Fig. 2: Voltage- (a) and current-based (b) SAM HF link converter topologies with isolation transformer and center-tapped cycloconverter.

As described in the introduction, ω_1 and ω_2 differ precisely by twice the output frequency in order to establish the SAM voltage link v_3 which is constituted by the difference of v_1 and v_2. For increased conversion efficiency and to support reactive power transfer, a two-stage approach with cyclcoconverter (cf. Fig. 1 (b)) is preferred. Although galvanic isolation might not be required by the application, the transformer turns-ratio introduces an additional degree of freedom in the design of the respective inverter stage which helps to reduce the currents in the resonant tank (cf. Sec. III-A). Among several options to implement the cycloconverter, the double-winding center-tapped realization allows full-wave cycloconversion (power transfer in the positive and negative half-wave of v_3) with only two four-quadrant power switches. Zero current switching (ZCS) applies to the cycloconverter (synchronous cycloconversion) as long as the control signals are well synchronized to the voltage link v_3. The output inductor behaves as a current source, which requires a commutating strategy to ensure a path for the impressed current in $L_{\mathrm{o,p}}$ during switching stage transitions. One possible strategy is to keep S_6 and S_8 turned-off when the current in $L_{\mathrm{o,p}}$ is positive and to operate S_5 and S_7 at high frequency. During the pos. half-wave of v_3, S_5 is turned-on and S_7 is off. Slightly after the zero-crossing of v_3, S_7 is turned-on, initiating a current commutation between S_5 and S_7 and allowing S_5 to be turned on subsequently with zero current. The switching frequency of the cycloconverter is set to the center frequency obtained from the output voltage controller (cf. Sec. III-B) and, in order to synchronize, the carrier signal of the modulator is reset at the start of every new v_3 period. This can be achieved in practice by detecting the zero-crossing of v_3 by means of a high-bandwidth comparator circuit. To facilitate swift current commutation between the switches, the reset of the carrier signal is slightly delayed with respect to the v_3 zero crossing.

The second analysed topology in this paper is shown in Fig. 2 (b) where the HF inverter stage is implemented by means of two series resonant converters (SRC) which constitute a SAM current link i_3 and require an impressed voltage at the output of the cycloconverter ($C_{\mathrm{o,s}}$). The SRCs are also operated slightly above resonance frequency to achieve ZVS in all operating points. Now, the control of the cycloconverter must be synchronized to the current link i_3 to achieve ZVS in S_5-S_8. Since detecting the zero crossing of a current is more challenging at very high frequency, the SAM current link based topology with cycloconverter has a clear downside compared to the voltage link based topology.

In the next section a mathematical model of the converters is presented which allows to identify optimal values for the resonant tank elements and transformer turns-ratio.

III. Converter Design and Control Strategy

A. Mathematical Model and Converter Design Procedure

Applying the first harmonic approximation (FHA), the cycloconverter and the low-pass filter (cf. Fig. 2 (a) and (b)) can be represented by a single resistor R_3 as indicated in Fig. 3 (a) and (b) [22], [23]. R_3 is calculated according to

$$R_{3,\mathrm{p}} = \frac{\pi^2}{8 n_{\mathrm{p}}^2} R, \qquad R_{3,\mathrm{s}} = \frac{8}{\pi^2 n_{\mathrm{s}}^2} R, \tag{6}$$

where subscripts (p) and (s) denominate the parallel (voltage HF link) and series (current HF link) resonant circuits, $R = V_{\mathrm{o}}^2 / P_{\mathrm{o}}$ represents the load connected to the output of the converter and $n_{\mathrm{p}}/n_{\mathrm{s}}$ is the turns-ratio of the employed transformer.

The equivalent circuits depicted in Fig. 3 (a) and (b) are further simplified as shown in Fig. 3 (c) and (d) by means of introducing a time-variant resistance $R_1(t)$. In case of the PRC, the instantaneous power $p_{1,\mathrm{p}} = v_1 i_3 = v_1 \frac{v_3}{R_{3,\mathrm{p}}}$ provided to the output can be written as

$$p_{1,\mathrm{p}} = 2 \frac{\hat{V}^2}{R_{3,\mathrm{p}}} \cos(\omega_{\mathrm{o}} t) \sin(\omega_{\mathrm{s}} t) \sin(\omega_{\mathrm{s}} t + \omega_{\mathrm{o}} t), \tag{7}$$

substituting v_3 with Eq. (2). The time variant resistance shown in Fig. 3 (c) is calculated by means of averaging $p_{1,\mathrm{p}}$ over the resonant period

$$P_{1,\mathrm{p}} = \langle p_{1,\mathrm{p}} \rangle_{T_{\mathrm{s}}} = \frac{1}{T_{\mathrm{s}}} \int_0^{T_{\mathrm{s}}} p_{1,\mathrm{p}} dt = \frac{\hat{V}^2}{R_{3,\mathrm{p}}} \sin^2(\omega_{\mathrm{o}} t), \tag{8}$$

and then substituting (8) in $R_{1,\mathrm{p}} = \frac{\hat{V}^2}{2 P_{1,\mathrm{p}}}$ which leads to

$$R_{1,\mathrm{p}}(t) = \frac{R_{3,\mathrm{p}}}{2} \frac{1}{\sin^2(\omega_{\mathrm{o}} t)}. \tag{9}$$

It can be inferred that $R_{1,\mathrm{p}}(t)$ varies periodically with the output frequency f_o between a nominal value $R_{3,\mathrm{p}}/2$ and open-circuit.

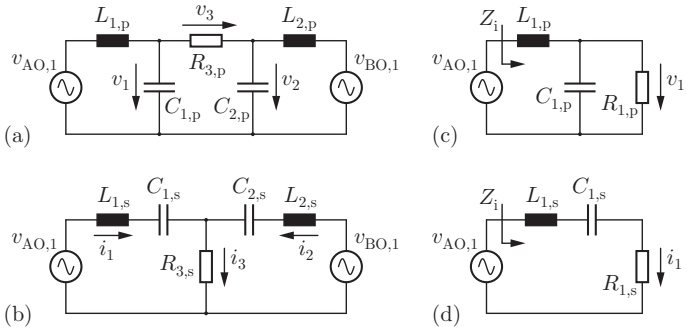

Fig. 3: Simplified circuits that facilitate mathematical analysis and passive component design. Equivalent resistance $R_{3,p}/R_{3,s}$ represents both cycloconverter and load resistor R. Circuits in (a) and (b) can be further simplified as shown in (c) and (d) by introducing a time-variant resistance $R_{1,p}(t)/R_{1,s}(t)$.

Following the same line of thought, Eq. (10) results for the equivalent resistance of the SRC model shown in Fig. 3 (d),

$$\begin{aligned} p_{1,\mathrm{s}} &= i_1 i_3 R_{3,s} = 2\hat{I}^2 R_{3,\mathrm{s}} \cos(\omega_\mathrm{o} t)\sin(\omega_\mathrm{s} t)\sin(\omega_\mathrm{s} t+\omega_\mathrm{o} t)\,, \\ P_{1,\mathrm{s}}(t) &= \langle p_{1,\mathrm{s}}\rangle_{T_\mathrm{s}} = \frac{1}{T_\mathrm{s}}\int_0^{T_\mathrm{s}} p_{1,\mathrm{s}}dt = \hat{I}^2 R_{3,\mathrm{s}}\cos^2(\omega_\mathrm{o} t)\,, \\ R_{1,\mathrm{s}}(t) &= 2R_{3,\mathrm{s}}\frac{1}{\cos^2(\omega_\mathrm{o} t)}. \end{aligned} \tag{10}$$

Using the basic expression for quality-factor and natural frequency of the series and parallel resonant circuit, the component values of the resonant tank elements are given by Eq. (11) for the PRC and by Eq. (12) for the SRC, where in a worst-case consideration, the minimum value of $R_{1,\mathrm{p}}$ and $R_{1,\mathrm{s}}$ over time was selected,

$$\begin{aligned} L_{1,\mathrm{p}} &= \frac{R_{3,\mathrm{p}}}{2\omega_\mathrm{n} Q_\mathrm{p}} = \frac{\pi^2 R}{16 n_\mathrm{p}^2 \omega_\mathrm{n} Q_\mathrm{p}}, \\ C_{1,\mathrm{p}} &= \frac{2Q_\mathrm{p}}{\omega_\mathrm{n} R_{3,\mathrm{p}}} = \frac{16 n_\mathrm{p}^2 Q_\mathrm{p}}{\omega_\mathrm{n}\pi^2 R}, \end{aligned} \tag{11}$$

$$\begin{aligned} L_{1,\mathrm{s}} &= \frac{Q_\mathrm{s} 2R_{3,\mathrm{s}}}{\omega_\mathrm{n}} = \frac{16 Q_\mathrm{s} R}{\pi^2 n_\mathrm{s}^2 \omega_\mathrm{n}}, \\ C_{1,\mathrm{s}} &= \frac{1}{\omega_\mathrm{n} Q_\mathrm{s} 2R_{3,\mathrm{s}}} = \frac{\pi^2 n_\mathrm{s}^2}{16\omega_\mathrm{n} Q_\mathrm{s} R}. \end{aligned} \tag{12}$$

Now, the required transformer turns-ratio to meet the output voltage requirement for given dc input voltage and resonant tank parameters is calculated for the HF voltage link dc/ac converter (cf. Fig. 2 (a)). The peak value of the envelope of the rectified HF voltage at the output of the cycloconverter is related to the output voltage according to

$$\hat{V}_\mathrm{r} = \frac{\pi\sqrt{2}}{2} V_\mathrm{o}. \tag{13}$$

Reflecting $\hat{V}_\mathrm{r}$ to the primary side of the transformer and observing from Eq. (2) that $\hat{V} = \frac{\hat{V}_3}{2}$ yields

$$\hat{V} = \frac{\pi\sqrt{2}}{4 n_\mathrm{p}} V_\mathrm{o}. \tag{14}$$

Introducing the voltage gain of the parallel resonant tank,

$$|H_\mathrm{p}| = \frac{1}{\sqrt{\left[1-\left(\frac{\omega_\mathrm{s}}{\omega_\mathrm{n}}\right)^2\right]^2 + \left(\frac{\omega_\mathrm{s}}{\omega_\mathrm{n} Q_\mathrm{p}}\right)^2}}, \tag{15}$$

and considering the expression for the first harmonic of v_{AO}, $V_{\mathrm{AO,1}} = \frac{2}{\pi} V_{\mathrm{DC}}$, allows to relate the peak value of the resonant capacitor voltage to the dc-link voltage,

$$\hat{V} = |H_\mathrm{p}|\,\hat{V}_{\mathrm{AO,1}} = |H_\mathrm{p}|\,\frac{2V_\mathrm{dc}}{\pi}. \tag{16}$$

Substituting Eq. (14) in Eq. (16) and rearranging results in an expression for the turns-ratio,

$$n_\mathrm{p} = \frac{\pi^2\sqrt{2} V_\mathrm{o}}{8\,|H_\mathrm{p}|\,V_\mathrm{dc}}. \tag{17}$$

The same analysis is applied to find n_s, in which

$$\hat{I} = \frac{n_\mathrm{s}\pi\sqrt{2}}{4} I_\mathrm{o}, \qquad \hat{I} = |H_\mathrm{s}|\,\frac{2V_\mathrm{dc}}{\pi}, \tag{18}$$

and the series resonant tank gain is written as

$$|H_\mathrm{s}| = \frac{1}{R_1}\frac{\frac{\omega_\mathrm{s}}{\omega_\mathrm{n} Q_\mathrm{s}}}{\sqrt{\left[1-\left(\frac{\omega_\mathrm{s}}{\omega_\mathrm{n}}\right)^2\right]^2 + \left(\frac{\omega_\mathrm{s}}{\omega_\mathrm{n} Q_\mathrm{s}}\right)^2}}, \tag{19}$$

resulting in the desired turns-ratio expression

$$n_\mathrm{s} = \frac{8\,|H_\mathrm{s}|\,V_\mathrm{dc}}{\pi^2\sqrt{2} I_\mathrm{o}}. \tag{20}$$

Now according to the technical specification given in Tab. I (P_o,V_o,V_dc,f_o,f_s), the resonant tank parameters $L_{1,p}/L_{1,s}$ and $C_{1,p}/C_{1,s}$ can be computed depending on the design-space variables f_n and Q. In a next step, the occurring resonant tank current and voltage are computed depending on f_n and Q. Then, for a maximal allowed voltage across the resonant capacitor, the optimal value of f_n and Q is determined by minimizing the resonant tank current. Based on the equivalent circuits in Fig. 3 (a) and (b), analytical expressions for the peak capacitor voltage and peak inductor current ($\hat{V}_{\mathrm{C1}}$,$\hat{I}_{\mathrm{L1}}$) of both parallel and series resonant converters can be derived. For the PRC, voltages v_1 and v_2 can be related to the sinusoidal excitations $v_{AO,1}$ and $v_{BO,1}$ according to Eq. (21) and Eq. (22),

$$\begin{bmatrix} k_1 & k_2 \\ k_2 & k_1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} v_{AO,1} \\ v_{BO,1} \end{bmatrix}, \tag{21}$$

$$k_1 = 1 - {\omega_\mathrm{s}}^2 L_1 C_1 + \frac{j\omega_\mathrm{s} L_1}{R_{3,p}} \quad \text{and} \quad k_2 = -\frac{j\omega_\mathrm{s} L_1}{R_{3,p}}. \tag{22}$$

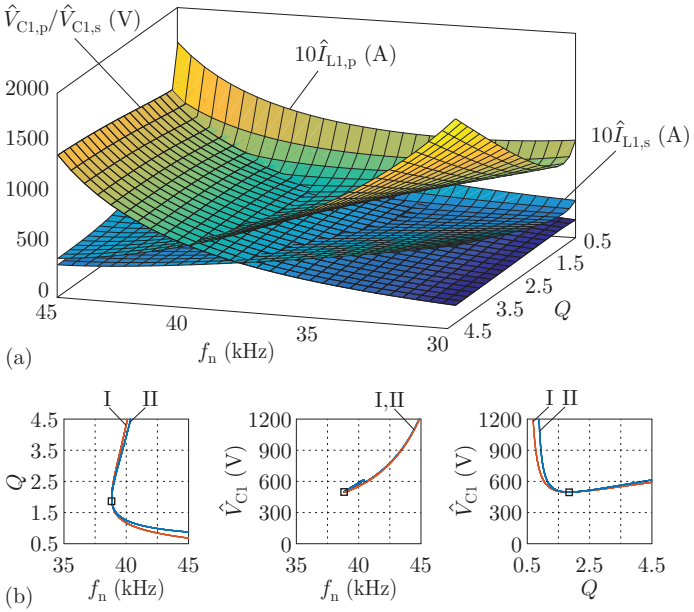

Fig. 4: (a) Resonant tank capacitor peak voltage $\hat{V}_{C1}$ and inductor peak current $\hat{I}_{L1}$ as a function of f_n and Q for both voltage (p) and current (s) SAM HF links. $\hat{V}_{C1}$ surfaces for both topologies are identical ($\hat{V}_{C1,p} = \hat{V}_{C1,s} = \hat{V}_{C1}$). The current-based link presents less inductor peak current if compared to the voltage-based link for the same capacitor peak voltage. (b) Intersection curves where (I) $\hat{V}_{C1} = 10\,\Omega \cdot \hat{I}_{L1,p}$ and (II) $\hat{V}_{C1} = 15.6\,\Omega \cdot \hat{I}_{L1,s}$, exhibiting a common optimum point of f_n = 38.9 kHz and Q = 1.81.

Solving the linear system for v_1 and v_2 results in

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} k_3 & k_4 \\ k_4 & k_3 \end{bmatrix} \begin{bmatrix} v_{AO,1} \\ v_{BO,1} \end{bmatrix}, \tag{23}$$

$$\text{where} \quad k_3 = \frac{k_1}{k_1^2 - k_2^2} \quad \text{and} \quad k_4 = \frac{-k_2}{k_1^2 - k_2^2}. \tag{24}$$

This allows to express the capacitor voltage and the inductor current,

$$v_{C1} = k_3 v_{AO,1} + k_4 v_{BO,1}, \tag{25}$$

$$i_{L1} = \frac{v_{AO,1} - v_{C1}}{j\omega_s L_1} = v_{AO,1} \frac{1 - k_3}{j\omega_s L_1} - v_{BO,1} \frac{k_4}{j\omega_s L_1}, \tag{26}$$

which can be rewritten using $\hat{V}_{AO,1} = \hat{V}_{BO,1} = 2V_{dc}/\pi$ in order to find the maximum value of the involved quantities,

$$\hat{V}_{C1,p} = \frac{2V_{DC}}{\pi} \left(|k_3| + |k_4| \right) \tag{27}$$

and

$$\hat{I}_{L1,p} = \frac{2V_{DC}}{\pi} \left(\left| \frac{1 - k_3}{j\omega_s L_1} \right| + \left| \frac{k_4}{j\omega_s L_1} \right| \right). \tag{28}$$

The same analysis is applied to compute the peak capacitor voltage

$$\hat{V}_{C1,s} = \frac{2V_{DC}}{\pi} \left(\left| \frac{k_3}{j\omega_s C_1} \right| + \left| \frac{k_4}{j\omega_s C_1} \right| \right), \tag{29}$$

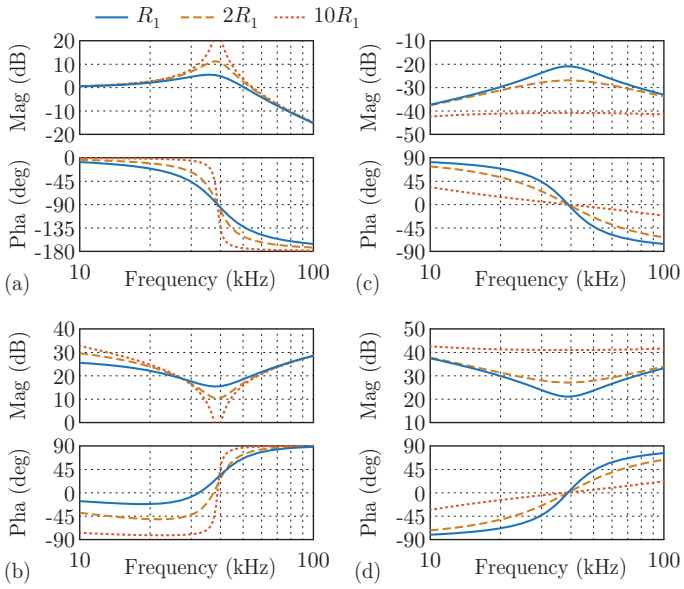

Fig. 5: Transfer function (a,c) and input impedance (b,d) Bode plots of the parallel (a,b) and the series (c,d) resonant converter depending on the equivalent resistance R_1.

and peak inductor current

$$\hat{I}_{L1,s} = \frac{2V_{DC}}{\pi} \left(|k_3| + |k_4| \right) \tag{30}$$

of the SRC.

The derived expressions allow to plot $\hat{V}_{C1,p}/\hat{V}_{C1,s}$ and $\hat{I}_{L1,p}/\hat{I}_{L1,s}$ for several values of f_n and Q. The plot of Fig. 4 (a) reveals the trade-off between $\hat{V}_{C1}$ and $\hat{I}_{L1}$ for the voltage and the current link based topology and shows that the peak current is substantially lower in the current link based converter.

TABLE I: Technical specifications.

Output power (P_o)	2 kW
Output RMS voltage (V_o)	230 V
DC-link voltage (V_{dc})	450 V
Output frequency (f_o)	50 Hz
Switching frequency (f_s)	50 kHz
Nominal output load resistance (R)	26.5 Ω

The optimal resonant tank parameter f_n and Q are listed in Tab. II and have been obtained from the intersection curves plotted in Fig. 4 (b). The shown intersection curves are $\hat{V}_{C1} = 10\,\Omega \cdot \hat{I}_{L1,p}$ in case of the PRC and $\hat{V}_{C1} = 15.6\,\Omega \cdot \hat{I}_{L1,s}$ in case of the SRC, where the scaling factors for both topologies were chosen such that the max. allowed 500 V across the resonant capacitor is attained for the optimal values of f_n and Q in order to minimize resonant tank current.

TABLE II: Optimal resonant tank parameter.

Maximum tank capacitor voltage ($\hat{V}_{C1,p}/\hat{V}_{C1,s}$)	500 V
Resonant tank natural frequency (f_n)	38.9 kHz
Resonant tank quality factor (Q)	1.81

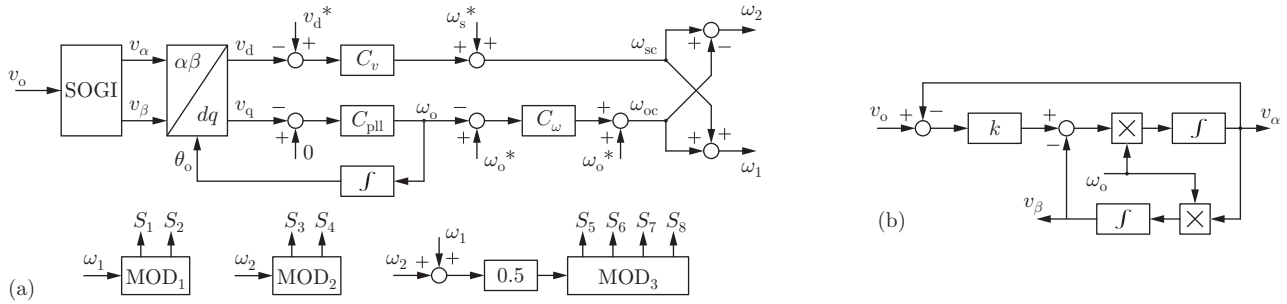

Fig. 6: (a) Combined amplitude and frequency control loop. A second-order generalized integrator (SOGI) phase locked loop (PLL) measures the output frequency ω_o and feeds a controller C_ω to impose the correct desired frequency-shift between ω_1 and ω_2. A second controller C_v changes both frequencies ω_1 and ω_2 simultaneously to compensate output voltage amplitude variations. The block diagram of (b) details the SOGI block internal structure.

Once optimum values for f_n and Q are found, the quantities n, L_1 and C_1 are calculated with Eq. (6)-(20) according to the specifications in Table I. The optimized circuit parameters are summarized in Table III.

TABLE III: Voltage (p) and current (s) based links main parameters.

Transformer turns ratio (n_p)	0.860
Tank inductance ($L_{1,\text{p}}$)	49.9 µH
Tank capacitance ($C_{1,\text{p}}$)	336 nF
Output inductance ($L_{\text{o,p}}$)	500 µH
Output capacitance ($C_{\text{o,p}}$)	2 µF
Transformer turns ratio (n_s)	1.96
Tank inductance ($L_{1,\text{s}}$)	82.4 µH
Tank capacitance ($C_{1,\text{s}}$)	203 nF
Output capacitance ($C_{\text{o,s}}$)	4 µF

The input impedance (Z_i) and transfer functions (v_1/v_{AO} and i_1/v_{AO}) Bode plots of both parallel and series resonant converters with optimized circuit parameters are depicted in Fig. 5. An increase in the equivalent tank resistance R_1 represented by dashed lines in the plots reveals how the magnitude and the phase changes with varying load. The PRC transfer function gain near the natural frequency f_n increases for higher R_1 values, while the opposite behaviour is found in the SRC. Since $R_1(t)$ varies over the output period (cf. Eq. (9) and Eq. (10)) it is not feasible to operate the converters with $f_\text{s} = f_\text{n}$ where the magnitude varies strongly with R_1. The operation above resonance is the preferred option (positive phase of Z_i) since it also enables ZVS of the half-bridge MOSFETs. The Bode plot of the PRC and SRC transfer functions in Fig. 5 (a) and Fig. 5 (c) also exhibit a difference in the slope of the magnitude above resonance frequency. In case of the PRC the magnitude decreases with $-40\,\text{dB/dec}$ while the SRC features a slope of just $-20\,\text{dB/dec}$. The selectivity (quality factor) of the PRC improves with increasing resistance R_1 while it decreases in case of the SRC. Thus, the PRC features better harmonic attenuation and more sinusoidal HF-link waveforms. This renders the PRC better suited for applications that require very low THD in the output voltage, particularly at light loads.

B. Proposed control strategy

Using FS modulation, the resonant links are excited by square-wave voltage waveforms with frequency $\omega_1 = (\omega_\text{s}+\omega_\text{o})$ and $\omega_2 = (\omega_\text{s}-\omega_\text{o})$, respectively. The center frequency of both resonant links,

$$\omega_\text{s} = (\omega_1 + \omega_2)/2, \tag{31}$$

sets the prevailing gain of the PRC and SRC transfer functions (cf. Eq. (15) and Eq. (19)) and allows to adjust the amplitude of the output voltage v_o. The angular frequency of the output voltage,

$$\omega_\text{o} = (\omega_1 - \omega_2)/2, \tag{32}$$

can be controlled by precisely adjusting the difference between ω_1 and ω_2.

Fig. 6 depicts the developed control system to regulate the output voltage v_o. A phase-locked-loop (PLL) [24] algorithm is applied to determine the angular frequency ω_o of the output voltage v_o. A deviation of ω_o from its reference value ω_o^* is compensated by means of PI controller C_ω with additional feed-forward term (ω_o^*). The amplitude of the output voltage v_o is obtained from the dq-transformation (v_d) and controlled to meet the amplitude reference v_d^* by means of compensator C_v with additional feed-forward of the angular switching frequency value (ω_s^*). The excitation frequencies of the respective bridge-legs, ω_1 and ω_2, are then computed according to Eq. (31) and Eq. (32). The control signals of the HF link MOSFETs, S_1-S_4, are then obtained from PWM with $50\,\%$ duty cycle and the respective frequency. The PWM unit generating the control signals for the cycloconverter stage, S_5-S_8, is parametrized with ω_s in order to synchronize the cycloconversion to HF voltage v_3, as explained in Sec. II.

IV. Simulation Results and Performance Comparison

Fig. 7 illustrates circuit simulation results of the voltage based SAM HF link converter designed in Sec. III for stationary operation at rated output power. The characteristic voltage waveforms are shown in Fig. 7 (a) over a mains period and in Fig. 7 (b) over two resonant periods. Considering Fig. 7 (a), it can be seen that the individual resonant tank voltages, v_1 and v_2, exhibit a fluctuating amplitude with twice the output frequency which can be explained by the time-varying equivalent resistance $R_1(t)$ (cf. Sec. III-A) which essentially alters the transfer characteristics of the resonant tank over time (cf. Fig. 5 (a)). Note, that this fluctuation would become more severe if the resonant tank would be operated closer to its resonance frequency. Voltage v_3 presents the desired SAM shape, which is then cycloconverted (v_r) and low-pass filtered to generate v_o. The waveforms with respect to the resonant period are depicted in Fig. 7 (b). Exciting the resonant tank above the resonance frequency, the input impedance becomes inductive (positive phase) and an increasingly triangular rather than sinusoidal shape of the currents i_{L1} and i_{L2} can be recognized. Note, that the results of the HF current link based converter are omitted since the waveforms are very similar to the voltage link based converter and the main discrepancies are highlighted in the performance comparison presented at the end of this section. The performance of the voltage link based converter subject to several stepwise load changes is shown in Fig. 8, demonstrating the excellent performance of the proposed FS control system described in Sec. III. At $t = 25\,\mathrm{ms}$ a stepwise decrease to $50\,\%$ of the load is initiated followed by another $25\,\%$ reduction at $85\,\mathrm{ms}$. At $t = 145\,\mathrm{ms}$, a stepwise increase of the load back to $2\,\mathrm{kW}$ rated power is shown. It can be seen that even under severe load changes, the output voltage is controlled tightly. Also shown in Fig. 8 are the computed control variables, switching (f_{sc}) and output (f_{oc}) frequencies, required to ensure the correct output frequency and amplitude. The low values of converter passive components explain the fast dynamic response of the circuit, which leads to v_o spikes during abrupt load transients. Also note, how the amplitude fluctuation of $v_1$and v_2 depends on the prevailing load.

TABLE IV: TCM inverter parameters.

Inductance	$62.2\,\mu\mathrm{H}$
Capacitance	$26.6\,\mu\mathrm{F}$
Lower current boundary	$5\,\mathrm{A}$
Lower switching frequency	$50\,\mathrm{kHz}$

In order to compare the performance of the voltage and current SAM HF link converters, several performance indicators were computed. The performance of a two-level full-bridge inverter operating in triangular current mode (TCM)

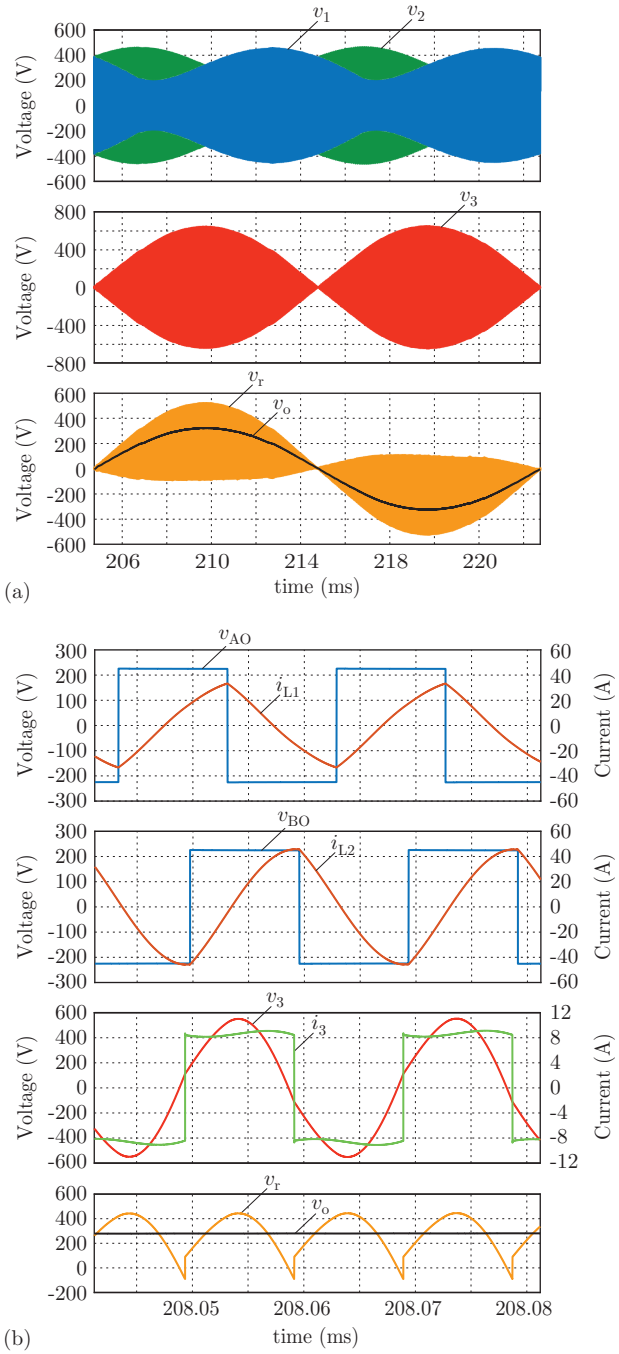

Fig. 7: Steady-state simulation results of the voltage-based SAM HF link inverter at rated output power for a mains period (a) and two resonant periods (b).

[25] is included as a benchmark, designed for the technical specifications shown in Table I which results in the parameter values summarized in Table IV. Since TCM features a variable switching frequency, the inductance value is chosen such that the minimum switching frequency corresponds to the $50\,\mathrm{kHz}$ of the SAM converter for a similar size of the passives. Fig. 9 shows the performance indicators with respect to output power and in the form of a radar chart. The indicators were chosen in order to easily recognize features and drawbacks of each

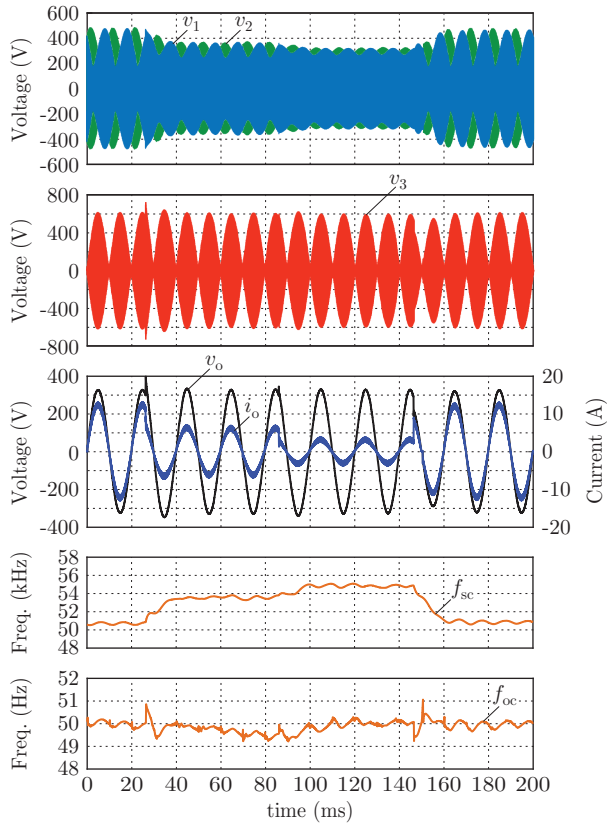

Fig. 8: Transient response simulation results for a 50 % stepwise load reduction after 25 ms followed by another 25 % reduction at 85 ms and a final stepwise increase to the 2 kW rated power at 145 ms, demonstrating the performance of the proposed control strategy.

topology. The inductor RMS current (I_{L1}/I_{L2}), the switching frequency (f_s) and the output voltage THD (THD_{vo}) provide a gauge of the conduction losses, switching losses and harmonic distortions, respectively. The average switching frequency over a v_o period was computed in case of the TCM inverter.

Concerning conduction losses, the current link inverter presents a better figure of merit compared to the voltage link due to the lower tank inductor RMS currents (I_{L1}/I_{L2}). The output voltage THD is around 2 % at rated power, but increases drastically in case of the current link converter if P_o is reduced below 1 kW, exceeding typical THD limits when operating at light loads. This is explained by the huge dependency of the SRC tank gain on the output load (cf. Fig. 5), which requires a large increase of f_s to keep the amplitude of v_o at its nominal value under light load. In contrast, the THD_{vo} in case of the voltage link converter is almost independent of the output power. Finally, regarding the f_s indicator, it can be seen that the average switching frequency of the TCM inverter is clearly above both SAM converters.

V. Conclusions

In this paper an alternative approach to conventional PWM with varying duty cycle to generate a low frequency sinusoidal output voltage in dc/ac converter applications is studied in detail. By means of constant duty cycle frequency shift (FS) control of a HF inverter stage at the dc side, an intermediate HF voltage or current link is established which exhibits a sinusoidally varying amplitude at the desired output frequency. A second cycloconversion stage with subsequent low-pass filter yields the desired ac output. Two variants of the HF inverter stage, a voltage or current link implemented by means of parallel or series resonant converters, respectively, have been analyzed. Based on a derived mathematical model of the converter, the resonant tank passives and transformer turns-ratio were chosen considering a minimization of the current stress for a given maximum resonant capacitor voltage in a 2 kW 400 V dc/ac application. A novel close-loop control systems is proposed which allows to tightly regulate the frequency and amplitude of the ac voltage. A dq-transformation based PLL and two individual PI controllers are implemented to compensate both amplitude and frequency deviations by adjusting the switching frequency of the respective HF inverters. The presented simulation results show excellent transient performance of the converter. In case of the PRC-based HF inverter, an abrupt load step of 75 % of nominal power settles within an output period and requires a shift of the center frequency (avg. frequency of both HF inverters) by roughly 4 kHz. Moreover, the performance of PRC and SRC implementations were compared to a single-stage TCM inverter regarding current stress, THD of the output voltage and switching frequency. Interestingly, the resonant inductor current is significantly higher in case of the PRC implementation compared to the SRC which exhibits values just slightly above the TCM inverter. As a consequence high conduction losses must be expected in case of the PRC implementation which leads to reduced efficiency particularly at light loads since the current stress in the resonant stage remains high. At nominal output power both HF inverter implementation show low output voltage THD values in the same range as the TCM inverter. Unfortunately, in case of the SRC implementation the THD increases significantly at light loads. It can be concluded that the HF current link based converter with FS control is a viable option to realize above MHz, kW-scale dc/ac power conversion. However, dedicated timing ICs are needed to realize FS control and the exact synchronization of the cycloconverter to the HF current link by means of current zero-crossing detection is crucial.

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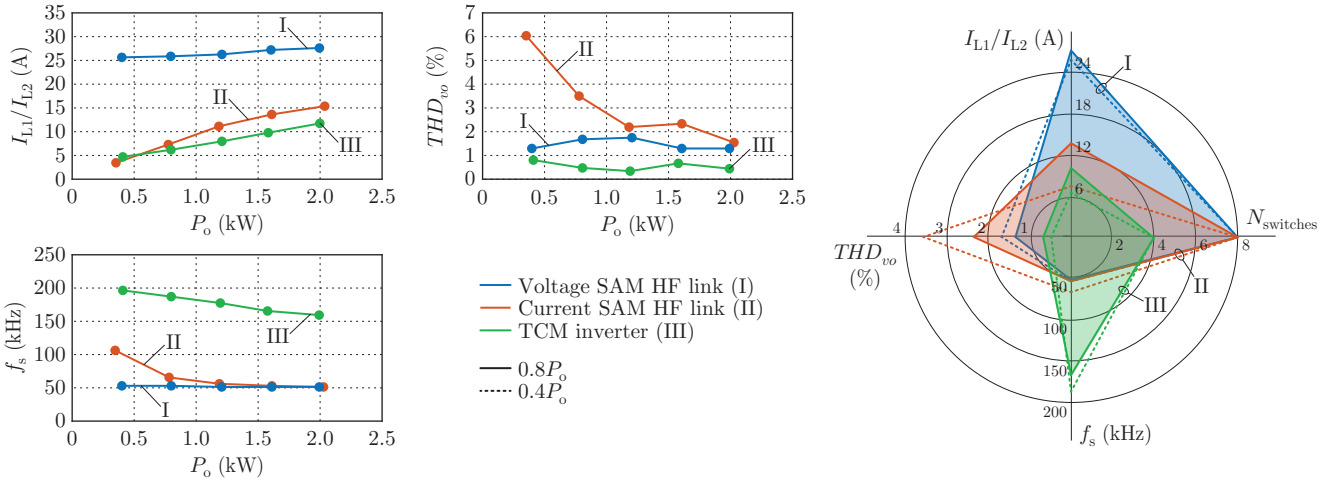

Fig. 9: Performance indicators for comparing both voltage (I) and current (II) SAM HF link converters and the triangular current mode (TCM) inverter (III) [25]. The current-based inverter shows better results regarding tank inductor RMS current values (I_{L1}/I_{L2}) which leads to lower conduction losses. In contrast, the voltage-based inverter has lower output voltage total harmonic distortion (THD_{vo}).

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