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20.3 A Feedforward Controlled On-Chip Switched-Capacitor Voltage Regulator Delivering 10W in 32nm SOI CMOS

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On-chip (or fully integrated) switched-capacitor (SC) voltage regulators (SCVR) have recently received a lot of attention due to their ease of monolithic integration [1-4]. The use of deep trench capacitors can lead to SCVR implementations that simultaneously achieve high efficiency, high power density, and fast response time [5]. For the application of granular power distribution of many-core microprocessor systems, the on-chip SCVR must maintain an output voltage above a certain minimum level $V_{out,min}$ in order for the microprocessor core to meet setup time requirements. Following a transient load change, the output voltage typically exhibits a droop due to parasitic inductances and resistances in the power distribution network. Therefore, the steady-state output voltage is kept high enough to ensure $V_{out}>V_{out,min}$ at all times, thereby introducing an output voltage overhead that leads to increased system power consumption. The output voltage droop can be reduced by implementing fast regulation and a sufficient amount of on-chip decoupling capacitance. However, a large amount of on-chip decoupling capacitance is needed to significantly reduce the droop, and it becomes impractical to implement owing to the large chip area overhead required.

Interleaving of SC converters greatly reduces or even eliminates the need for on-chip decoupling capacitors, and SC converters can be designed to have multiple conversion ratios to cover a wider input and/or output voltage range. The design reported in [1] achieves a 76mV droop with a sub-nanosecond response time controller and without using on-chip decoupling capacitors. In [3], 25mV of droop is achieved for a single-digit nanosecond response time controller, which uses on-chip decoupling capacitors. In previous work [5], 94mV droop is reported with a sub-nanosecond response time controller without using on-chip decoupling capacitors. Accordingly, the droop is caused neither by the regulation loop being too slow, nor by the lack of on-chip decoupling capacitance. Instead, the input node of the on-chip SCVR experiences a much larger droop than the output node. This input voltage droop is found to be the root cause of the output voltage droop. For example, a 2:1 SC converter can ideally regulate the output voltage from half the input voltage and less. If the input voltage droop results in $V_{in}<2V_{out}$, the SCVR is limited by the conversion ratio and cannot maintain the output voltage required by the application. This paper presents a feedforward control scheme that significantly reduces the output voltage droop in the presence of a large input voltage droop following a transient event. This in turn reduces the required output voltage overhead and may lead to significant overall system power savings.

Figure 20.3.1 shows the equivalent model of an SC converter consisting of a transformer with a fixed conversion ratio M and an equivalent output resistance R_{eq}. The typical feedback regulation scheme for SCVRs regulates R_{eq} – typically by modulating the switching frequency – to achieve the desired output voltage [1-5]. The proposed feedforward control, which can be implemented with a reconfigurable SC converter, dynamically changes the configuration to a higher voltage conversion ratio $M_2>M_1$ when a large input voltage droop is detected. Once the external VRM has recovered the input node of the on-chip SCVR, the configuration changes back to M_1, where the converter operation is more efficient.

Figure 20.3.2 shows the complete overview of the SCVR implemented. A 64-phase interleaving scheme of a 2:1 and 3:2 reconfigurable SC converter is employed. The feedback control is implemented as a single-bound hysteretic controller comprising a clocked comparator (strong-arm latch) and a digital clock interleaver [5]. The feedforward control is implemented using a clocked comparator and a gear controller that dynamically changes the configuration (gear) of the SC converter. An on-chip programmable load is also incorporated. Finally, the converter is designed to deliver 10W maximum output power to highlight the feasibility of high-power on-chip SCVRs.

The implementation of the feedforward control for an example 4-phase SCVR is shown in Fig. 20.3.3. Simulations show that changing the configuration of all 64 SC converters at once leads to unnecessarily high ripples at the output node. Therefore, the feedforward control is designed to change the configuration one at a time. The input voltage V_{in} is compared with a reference $V_{in,ref}$ by a clocked comparator having both positive (gp) and negative (gn) outputs. The gear signals are governed by a bi-directional shift register, where the direction is controlled by the select signal (sel). A rising edge of gp appears when $V_{in}<V_{in,ref}$, thereby triggering sel to go high, and logic 1 is stored in the first flip-flop, causing gear0 to go high. Consecutive gp triggers cause the subsequent gear signals to go high, and when all gear signals are high, subsequent gp triggers have no further impact. Once $V_{in}>V_{in,ref}$, a rising edge on gn appears, thereby triggering sel to go low, and storing logic 0 in the last flip-flop, causing gear3 to go low. Again, consecutive gn triggers cause the gear signals to go low one at a time. From simulations, it is found that pulse skipping of gn (denoted gn') leads to the smoothest transition back to the original conversion ratio.

A test chip is realized in a 32nm SOI CMOS technology that features the deep trench capacitor. The measured transient results are shown in Fig. 20.3.4. Although the sub-nanosecond feedback control maintains the output voltage for a short duration following the transient event, without the feedforward control, the collapse of the input voltage causes the output node to experience a large droop, leading to a relatively low $V_{out,min}$. With the feedforward control, the converter dynamically changes from the 2:1 to the 3:2 configuration when the input voltage gets too low, thereby significantly reducing the droop and leading to a higher $V_{out,min}$. Although not shown, the converter transitions back to the more efficient 2:1 configuration once the transient has settled completely.

For steady-state measurements, the on-chip input and output voltages are measured using Kelvin contacts, and the input current is directly measured from the input supply. The resistance of the programmable load is measured using a 4-point measurement setup. Also, the on-chip load resistance is characterized over temperature, and a thermal model is used to predict the on-chip temperature during operation. For each measurement point, the on-chip load resistance value at the specific operating temperature is used to estimate the output power and the converter efficiency.

Figure 20.3.5 shows the efficiency over output power for four different output voltages at V_{in}=1.8V. As can be seen, the 10W output power is achieved at full load for V_{out}=1.1V. The efficiency at nominal load in the 2:1 configuration for V_{out}=0.85V is 82.7% at 1.9W/mm^2 power density. For the same load with V_{out}=1.1V, the efficiency is 85.1% at 3.2W/mm^2 power density.

This SCVR design is compared with recent SCVR designs in Fig. 20.3.6. Having no on-chip decoupling capacitors, the 30mV voltage droop achieved in this work is comparable with the design of [3] that uses precious chip area for on-chip decoupling capacitors. For the designs without on-chip decoupling capacitors [1,4,5], the droop achieved in this work is reduced from more than 76mV in [1] to 30mV in this design. The 10W maximum output power is more than 6 times higher than previous designs. The 10W on-chip SCVR micrograph is shown in Fig. 20.3.7. The total converter area including gate driver and controller is 1.96mm^2.

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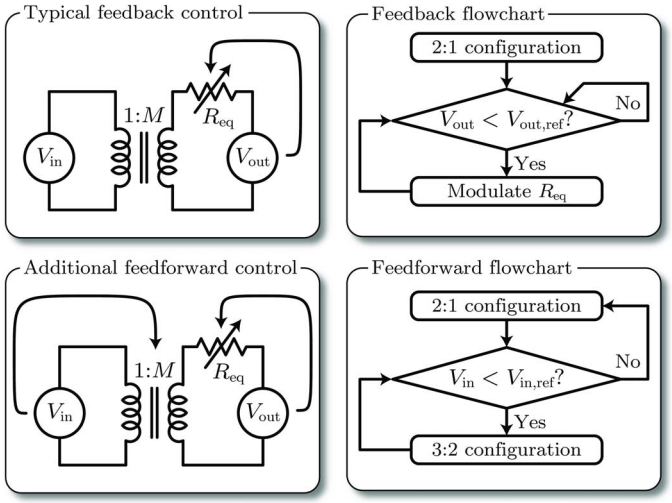

Figure 20.3.1: Switched-capacitor equivalent model showing how the feedforward control dynamically changes the conversion ratio *M* in conjunction with the typical feedback control that modulates R_{eq}.

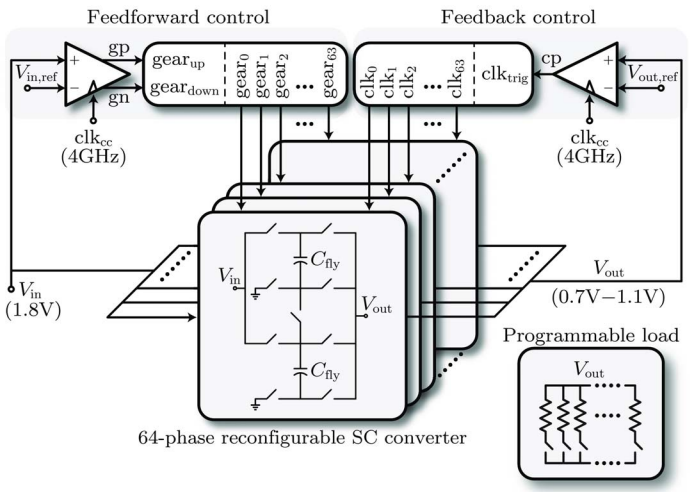

Figure 20.3.2: System overview of the 64-phase 2:1 and 3:2 reconfigurable switched-capacitor voltage regulator (SCVR) implemented.

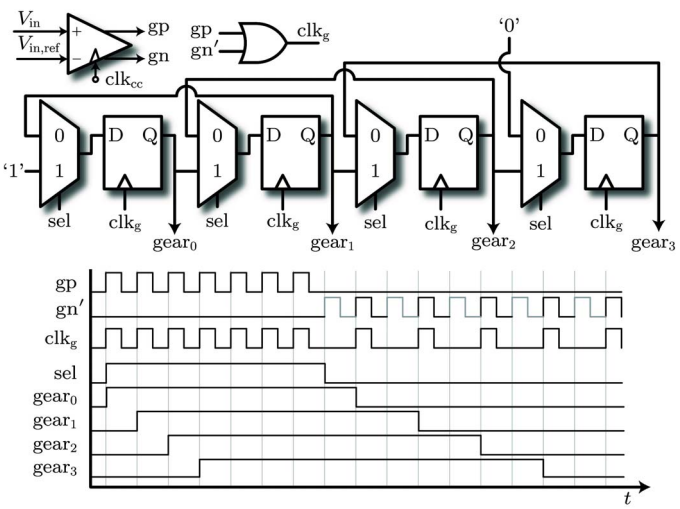

Figure 20.3.3: Example 4-phase implementation of the feedforward control that dynamically changes the configuration (gear) when an input voltage droop is detected by the clocked comparator.

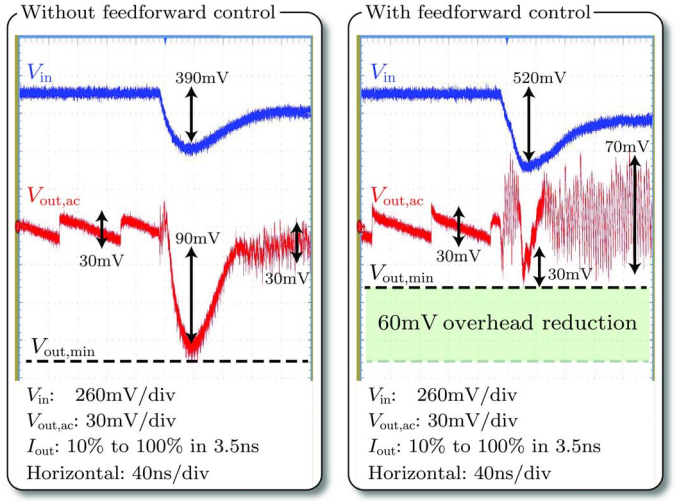

Figure 20.3.4: Transient response for V_{out}=850mV at V_{in}=1.8V. The feedforward control effectively reduces the voltage overhead required to maintain a certain $V_{out,min}$.

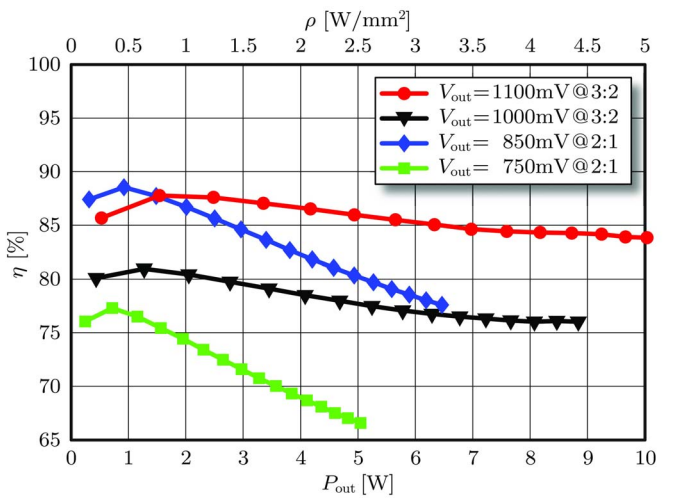

Figure 20.3.5: Measured efficiency over output power for four different output voltages at V_{in}=1.8V. The maximum output power is 10W.

Design	This Work	Le [1] ISSCC 2013	El-Damak [2] ISSCC 2013	Jain [3] VLSI 2013	Meyvaert [4] ECCE 2011	Andersen [5] ISSCC 2014
Technology	**32nm SOI**	65nm Bulk	32nm SOI	22nm Tri-Gate	90nm Bulk	32nm SOI
Conversion ratio (*M*)	**2:1, 3:2**	5:2, 3:1	3:1, 2:1 3:2, 1:1	2:1, 3:2 5:4, 1:1	2:1	2:1, 3:2
Capacitor technology	**Deep trench**	MOS	Ferroelectric	MIM	MOS	Deep trench
Interleaving	**64**	18	4	8	21	16
C_{fly} / C_{out}	**1nF / 0**	3.88nF / 0	1nF / 10nF	– / 100pF	0.57nF / 0	1nF / 0
V_{in}	**1.8V**	3V – 4V	1.5V	1.23V	2.35V – 2.6V	1.8V
V_{out}	**0.7V – 1.1V**	1V	0.4V – 1.1V	0.45V – 1V	1.03V	0.7V – 1.1V
$P_{out,max}$	**10W**	121mW	1.1mW	88mW	1.65W	840mV
$t_{response}$	**<1ns**	<1ns	<1ms	3ns – 5ns	<15µs	<1ns
V_{droop}	**30mV**	76mV	–	25mV	95mV	94mV
$V_{ripple,pp}$	**30mV**	–	–	43mV	–	30mV
η_{max} per *M*	**82.7%, 85.1%**	71.5%, 73%	90%, 91% 93%, 80%	82%, 71% 73%, 68%	69%	86%, 90%
ρ [W/mm²] @ η_{max}	**1.9, 3.2**	0.19, 0.19	0.0006, 0.0010 0.0013, 0.0016	0.062, 0.100 0.126, 0.243	0.42	2.2, 3.7

Figure 20.3.6: Performance summary and comparison with recently published on-chip SCVRs.

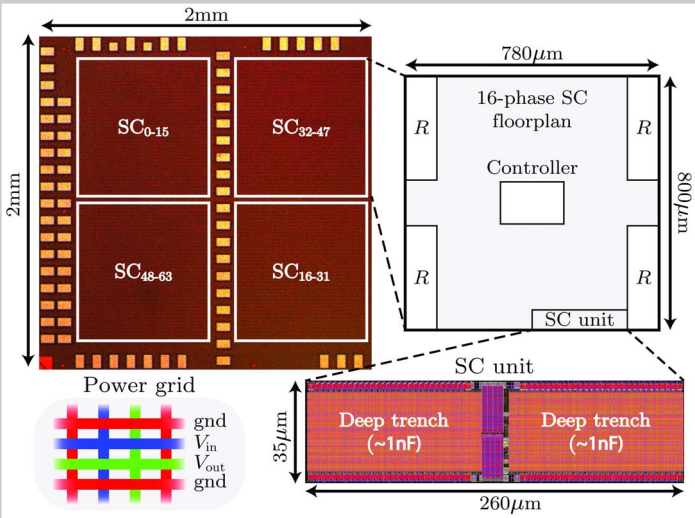

Figure 20.3.7: Chip micrograph of the 10W SCVR implemented in a 32nm SOI CMOS technology with deep trench capacitors. The total active converter area is 1.968mm².

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