Synthesis of Low-Switch-Count Power Converter Topologies

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***Abstract*—A systematic method is presented for synthesizing power converter topologies, using only a low number of semiconductor devices. The method is based on a single-switch elementary converter that can be used as a power converter building block. It is shown, that many well known converter topologies can be synthesized using the method. Furthermore, two novel single-phase power factor correction (PFC) rectifier topologies are synthesized, their basic control principles are demonstrated and results from circuit simulations are provided, verifying the functionality. The newly found topologies require only half the number of semiconductor devices, compared to conventional solutions, while still providing clamped voltages to all power semiconductors during their off state. The proposed synthesizing method can be applied to AC-DC, DC-DC, isolated and non-isolated, dual- and multi-port converters.**

***Index Terms*—Converter topology synthesis, elementary single-switch converter, low-switch-count converter topologies, single-phase PFC rectifiers.**

I. Introduction

The half-bridge, i.e., two series-connected switches in parallel to a capacitor, is the basic building block implementing the switching function of many converter topologies. However, there are some well known exceptions that do not use half-bridges:

- The flyback converter, an isolated buck-boost DC-DC converter with only one active switch, is often used for low-power auxiliary converters [1]–[4].
- The single-ended quasi-resonant inverter, a single-switch converter, is used in induction cookers [5], [6] and inductive power transmission [7], [8] for DC to high-frequency (HF) AC conversion.
- The push-pull current-doubler rectifier is a popular choice for high-current, low-voltage AC-DC conversion [9]–[12].
- The Ćuk converter [13], [14] and the single-ended primary-inductor converter (SEPIC) [15]–[17], both non-isolated buck-boost DC-DC converters, are other well-known but less common examples without a half-bridge transistor arrangement.

Disadvantages of the above-mentioned topologies include DC current in transformer windings, high MOSFET voltage stress, and the need for a snubber limiting the transistor switching overvoltage. Nevertheless, some of them are widely used for low-power and cost-sensitive applications because of their low switch count. Therefore, the question remains whether there are other, so far unknown, low-switch-count converter topologies that might be useful for certain applications.

There are existing methods for synthesizing power converter topologies, but they are based on complementary pairs of switches resulting in topologies with a multiple of two switches [18]–[20] or only apply to fixed-conversion-ratio switched-capacitor converters [21], [22].

This paper presents a systematic method for synthesizing low-switch-count topologies from a single-switch elementary converter, following an engineering rather than a basic rigorous mathematical approach. From specific input/output requirements, all kinds of converter types (AC-DC and DC-DC, isolated and non-isolated, dual- and multi-port) can be synthesized. The method is introduced in **Section II**, used to synthesize some well-known topologies in **Section III**, and finally results in two novel topologies of single-phase PFC AC-DC converters in **Section IV**. The functionality of the derived topologies is verified by circuit simulations. **Section V** concludes the paper.

II. Method

Is there a basic circuit, i.e., an elementary converter cell that most power converter topologies can be built from? Because if such a circuit exists, one could simply combine the lowest possible number of cells needed to realize a specified functionality and thus find a low-switch-count topology.

A. Elementary Converter

The obvious answer is that the half-bridge is such a basic circuit [18]. However, the topologies listed in the introduction are not built from half-bridges. So is there an even more basic circuit from which half-bridges can be built? To answer that question let's have a closer look at the DC-DC boost converter shown in **Fig. 1a**.

As known since the 1960s, the power flow in a switched-mode DC-DC power converter can be thought of consisting of both, DC and AC components [23], which has been rigorously analyzed and proved using graph theory by Wolaver in his seminal 1972 paper [24]; a more recent discussion of the power flows in converters can be found in [25]. Following [24], it is thus useful to define *apparent* DC and AC powers for the switching elements: Considering ideal, lossless MOSFETs and diodes, the instantaneous power at these elements is zero

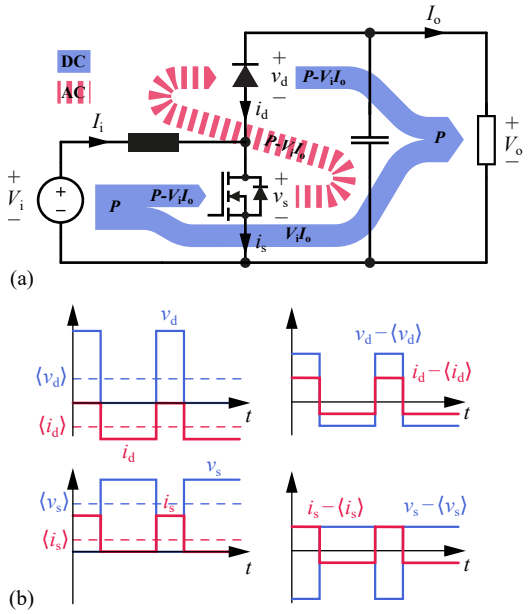

Fig. 1. (a) Boost converter circuit and power flows and **(b)** idealized switch and diode voltage and current waveforms separated into their DC and AC components.

because the non-zero intervals of the (idealized) voltage and current waveforms do not overlap, i.e.,

$$v_s i_s \stackrel{!}{=} 0 \quad \text{and} \quad v_d i_d \stackrel{!}{=} 0. \tag{1}$$

However, for the voltage across the MOSFET we have $v_s \geq 0$ and, as the MOSFET turns on and off in each switching period, v_s contains a non-zero DC component that corresponds to its local average value over one switching period, $\overline{v}_s = \langle v_s \rangle$, where $\langle x \rangle = 1/T_s \int_0^{T_s} x\, dt$ and T_s is the switching period. Accordingly, the AC component can be described as $\tilde{v}_s = v_s - \langle v_s \rangle$. Similar considerations can be made for i_s, v_d, and i_d. As suggested in [24], the voltages and currents at the switching devices are then expressed in terms of their DC and AC components (see also **Fig. 1b**):

$$v_s = \overline{v}_s + \tilde{v}_s, \;\; i_s = \overline{i}_s + \tilde{i}_s, \;\; v_d = \overline{v}_d + \tilde{v}_d, \;\; \text{and} \;\; i_d = \overline{i}_d + \tilde{i}_d. \tag{2}$$

Then, the local average power of the MOSFET becomes

$$\begin{aligned} \langle v_s i_s \rangle &= \langle (\overline{v}_s + \tilde{v}_s)(\overline{i}_s + \tilde{i}_s) \rangle \\ &= \underbrace{\langle \overline{v}_s \overline{i}_s \rangle}_{P_{dc,s}} + \underbrace{\langle \overline{v}_s \tilde{i}_s \rangle}_{0} + \underbrace{\langle \tilde{v}_s \overline{i}_s \rangle}_{0} + \underbrace{\langle \tilde{v}_s \tilde{i}_s \rangle}_{P_{ac,s}} \stackrel{!}{=} 0, \end{aligned} \tag{3}$$

i.e., $P_{dc,s} = -P_{ac,s}$, and likewise, $P_{dc,d} = -P_{ac,d}$ results for the diode. This suggests that each switching element absorbs a certain (apparent) DC power and emits an equal (apparent) AC power (or vice-versa) [23], [24], i.e., behaves like a DC-AC (or an AC-DC) converter.

For the specific example of the boost converter,

$$\overline{v}_s = V_i, \quad \overline{i}_s = d I_i, \quad \overline{v}_d = V_o - V_i, \quad \text{and} \quad \overline{i}_s = -(1-d) I_i, \tag{4}$$

where $d = 1 - V_i/V_o$ is the duty cycle, and V_i, I_i, V_o, and I_o are the input and output DC voltages and currents. With the total

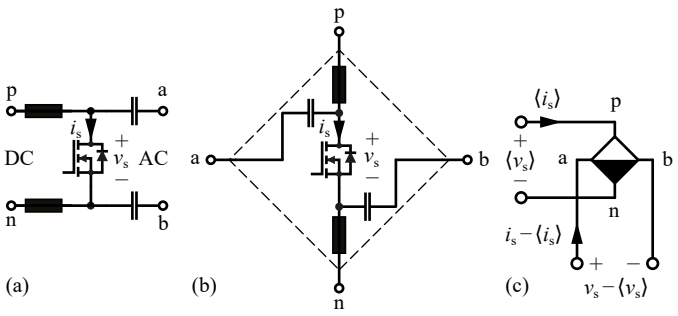

Fig. 2. Elementary converter. **(a)** Circuit structure and **(b)** re-arrangement leading to **(c)** schematic symbol of the elementary converter with DC terminals p, n, and AC terminals a, b.

input and output power $P = V_i I_i = V_o I_o$ (lossless converter) we find

$$\begin{aligned} P_{dc,s} &= P - V_i I_o \geq 0 \quad \text{and} \\ P_{dc,d} &= -P + V_i I_o \leq 0, \end{aligned} \tag{5}$$

where the inequalities follow from $V_i \leq V_o \wedge I_o \leq I_i \Leftrightarrow V_i I_o \leq P$ (equality results for the trivial case of $V_o = V_i$). It thus looks like the MOSFET is absorbing DC power ($P_{dc,s} > 0$) and the diode is emitting the same amount of DC power ($P_{dc,d} < 0$). Furthermore, note that

$$P_{dc,s} = -P_{ac,s} = P_{ac,d} = -P_{dc,d}, \tag{6}$$

i.e., the MOSFET absorbs DC power, converts it to AC power, which is then transferred to the diode. The diode converts the AC power back to DC power that it then emits to the output, see also the power flows indicated in **Fig. 1a**. Note further that there exists another, *direct* power flow, $V_i I_o$, which is never converted to an intermediate (apparent) AC power; this is consistent with [23], [24], and also with a more recent discussion on power flows in converters [25].

Thus, each semiconductor in a switched-mode converter acts like a DC-AC or an AC-DC converter. Up to this point, DC and AC components are separated only mathematically and DC and AC power are only terms of definition, as established in [24]. However, using inductors and capacitors as filter elements, this separation can also be realized physically. This idea leads to the circuit of the elementary converter, a single-switch DC-AC converter, shown in **Fig. 2**. As each elementary converter acts as a DC-AC converter, a single switching device (e.g., a MOSFET), and a DC and an AC port, i.e., four terminals, are needed. Further, there should be no AC power flow into the DC port. Hence, an inductor must be placed in series with the DC port; the inductor is transparent for DC. Similarly, no DC power should flow into the AC port. Hence, a series capacitor must be present; the capacitor is transparent for AC. Finally, the AC and DC ports should also be decoupled regarding common-mode (CM) signals; hence, the inductors and the capacitors should be arranged symmetrically as indicated in **Fig. 2**.

B. Systematic Synthesis of Converter Topologies

With the elementary converter, a single-switch AC-DC converter is found. Obviously, a DC-DC converter can be assembled

from two elementary converters. One to convert from DC to AC and the other converting back from AC to DC. The following method provides a systematic approach for designing converter circuits based on this idea. Each of the five steps is directly applied to the systematic synthesis of the (already considered) boost converter (see **Fig. 1a**); further examples are given in **Section III**.

1. DC circuit: A circuit consisting only of elementary converters (**Fig. 2c**) must be found. Only the DC ports shall be connected, the AC ports must be left open. The elementary converters' DC ports can be used as if they were unipolar (positive voltage only), controllable current sources. If bipolar (positive and negative) voltages are required at a converter port, two elementary converters can be connected in anti-series. The total power supplied by all elementary converter DC ports in the circuit must be zero ($\sum_k P_{\mathrm{dc},k} = 0$). This implies that at least two elementary converters and hence two switching devices are needed for any converter; this is consistent with [24].

*Boost converter example (**Fig. 3-1**):* Assuming a converter is required that generates an output voltage that is higher than the input voltage, the difference between output and input voltage can be provided by a first (top) elementary converter in series to the input voltage source. To meet the requirement of $\sum_k P_{\mathrm{dc},sk} = 0$, a second (bottom) elementary converter is connected in parallel to the input source, which absorbs the required power.

2. Net-zero-power sets: Next, each elementary converter must be assigned to a net-zero-power set. The total power of all elementary converter DC ports in a set must be zero, the number of net-zero-power sets should be maximized; this minimizes the number of elementary converters per set and thus the number of AC ports that must be connected with each other in step 3.

*Boost converter example (**Fig. 3-2**):* There is only one set of elementary converters with $\sum_k P_{\mathrm{dc},sk} = 0$.

3. AC circuit: The AC ports of all elementary converters within a net zero power set must be connected with each other to establish power transfer between them. The straightforward approach is to series-connect the AC ports of all elementary converters in a loop: and blocking voltage values as described here. Terminal b of the first elementary converter must be connected to terminal a of the next and so on, until terminal b of the last converter is connected to terminal a of the first, thus closing the AC loop.

Of all the switches within an AC loop, only one switch is blocking at any given time, while the others are conducting. This is required to make sure that there is always a low-impedance path for each inductor current to flow. If two or more switches would be off at the same time, the body diodes of all but one switch would be conducting, depending on the DC port currents. If all switches within an AC loop would be on, the loop capacitors would be shorted, typically resulting in destruction of the switches.

So it is preferred to control the set of switches $\mathcal{S}$ within an AC loop with duty cycles d_k that meet

$$\sum_{k\in\mathcal{S}} (1 - d_k) = 1. \tag{7}$$

The duty cycles of the switches are

$$d_k = 1 - \frac{\langle v_{\mathrm{s},k} \rangle}{v_{\mathrm{s,off}}}, \tag{8}$$

with the off-state voltage

$$v_{\mathrm{s,off}} = \sum_{k\in\mathcal{S}} \langle v_{\mathrm{s},k} \rangle. \tag{9}$$

Because thus each additional series-connected AC port increases the off-state voltage of all switches in the loop, parallel connections should be the preferred alternative. However, a parallel connection of two AC ports is only possible if the two elementary converters' duty cycles and DC port voltages are equal. If the duty cycles are equal but the DC port voltages are not, AC ports can be paralleled using a transformer with a turns ratio matching their DC port voltage ratio.

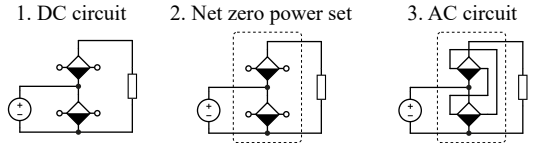

Fig. 3. Systematic synthesis of the boost converter (steps 1…3; note that step 4 is not applicable to the boost converter example).

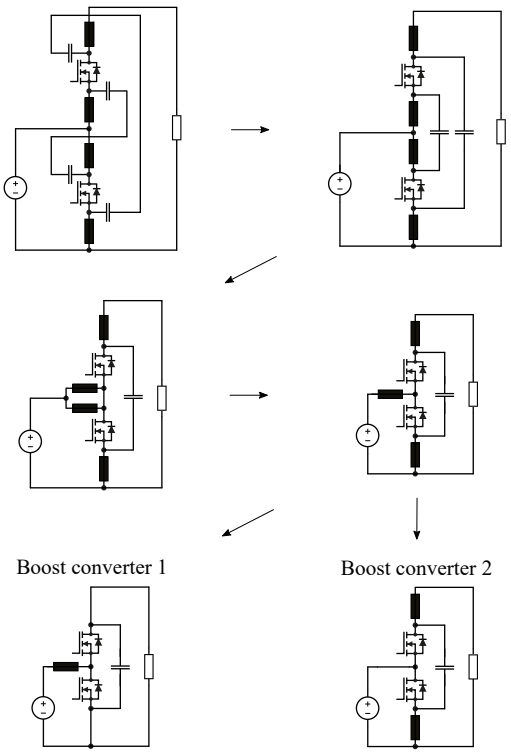

Fig. 4. Systematic synthesis of the boost converter (step 5): Simplification of the converter circuit obtained in **Fig. 3**; note that in the last step two different final results with identical terminal behavior can be achieved by shorting either one or two of the inductors.

*Boost converter example (**Fig. 3-3**):* Except for the special case of a voltage doubler, the voltages at the DC ports of the two elementary converters are different. Therefore, their AC ports are connected in series.

4. Clamp switches: In the off state, the voltage at a switch must be defined (clamped). To ensure this, the following criteria must be met for each elementary converter:

- The AC port must be part of a loop, that connects terminal b to terminal a only via capacitors, voltage sources, or other AC ports being passed from terminal a to terminal b.
- For the switches $\mathcal{S}$ within this loop, $\sum_{k\in\mathcal{S}}(1-d_k)=1$ must hold.

Otherwise, additional elementary converters must be added and their AC ports connected to close open AC loops.

Boost converter example: The AC path criterion is met, no additional elementary converters required; see the discussion of the Flyback converter in **Section III**, **Fig. 7** for an example.

5. Simplification: Replace all elementary converter symbols with the circuit in **Fig. 2a**. Simplify the resulting circuit by shorting inductors with zero AC voltage and capacitors with zero DC voltage, and by removing (i.e., replacing with an open circuit) capacitors with zero AC current and inductors with zero DC current. Integrate inductors with transformers if possible.

*Boost converter example (**Fig. 4**):* After replacing the elementary converter symbol with the actual circuit, the series-connected capacitors in the AC loop can be combined. There is zero DC voltage at one of them because its terminals are connected via inductors; it is replaced by a short circuit. Next, the two parallel inductors are combined. There is still redundancy: Either one or two of the three inductors may be shorted without affecting the circuits behavior. Finally, this leads to two results that contain no more redundant components. One is the expected well-known boost converter (Boost converter 1), the other is functionally equivalent but requires two inductors, see [26].

III. Derivation of Basic Converter Topologies

In the following, the method for systematic synthesis of topologies described above is applied to a few other simple DC-DC conversion problems, resulting in some well-known converter topologies.

A. Buck-Boost and Ćuk Converter

The method shall be applied to the problem of generating a negative output voltage from a positive input voltage, see **Fig. 5**. The negative output voltage may be provided by a single elementary converter in parallel to the load. A second elementary converter for establishing the power balance of the circuit is connected in parallel to the input voltage. The AC ports of the two elementary converters must be connected in series. Simplifying the resulting circuit results in either the buck-boost or the Ćuk converter, depending on which inductors are removed during the simplification.

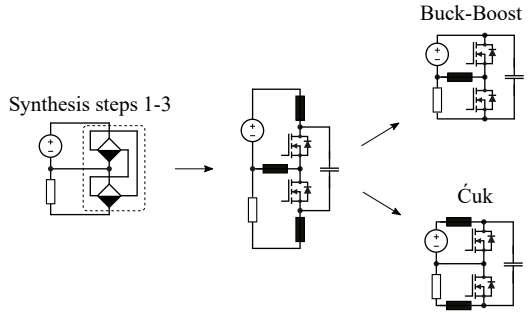

Fig. 5. Synthesis of an inverting buck-boost converter results in either the buck-boost converter or the Ćuk converter, depending on which of the redundant inductors are removed.

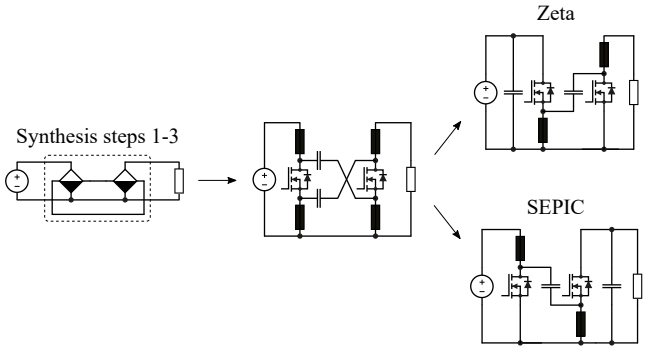

Fig. 6. Synthesis of a non-inverting buck-boost converter results in either the Zeta converter or the SEPIC converter, depending on which of the redundant inductors are removed.

B. SEPIC and Zeta Converter

An output voltage shall be generated that can be higher or lower than the input voltage, but must refer to the same ground, i.e., non-inverting buck-boost functionality is desired. One simple solution is to connect one elementary converter in parallel to the input and the other in parallel to the output, see **Fig. 6**. Again, simplification produces two results: the Zeta converter [27] and the SEPIC [15]. Due to the single-switch structure of the elementary converter, only the two lowest switch count non-inverting buck-boost converter topologies are obtained and not the commonly used half-bridge-based four-switch variant [28].

C. Flyback Converter

The previous examples did not require galvanic isolation. So finally the method is applied to the problem of providing an adjustable, galvanically isolated DC output voltage in **Fig. 7**.

1. DC circuit: One elementary converter is used to absorb the power from the input and another one to provide it to the load.

2. Net-zero-power sets: There is only one net-zero-power set.

3. AC circuit: Because the input/output voltage ratio must be adjustable, the voltages at the DC ports of the two elementary converters are not proportional. Therefore, their AC ports must be connected in series with a transformer for providing the galvanic isolation and, if necessary, voltage adaption.

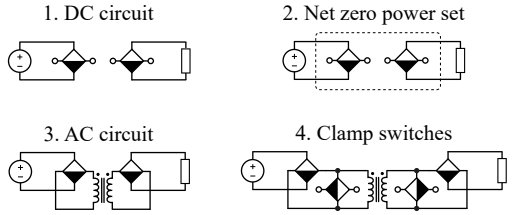

Fig. 7. Systematic synthesis of the flyback converter (steps 1…4).

4. Clamp switches: Two further elementary converters must be added and their AC ports connected in parallel to the windings to meet the AC path criterion.

5. Simplification: In **Fig. 8** the elementary converter symbols are replaced with their actual circuit. Series-connected components are combined and floating components removed. It is observed[1] that the AC voltages at the transformer primary winding and at the input inductor are equal. Therefore, the transformer primary winding can be connected in parallel to the input inductor; the same applies to the secondary winding and the output inductor. Because the inductors are now connected in parallel to the transformer magnetizing inductance, they can be eliminated. The resulting circuit resembles a flyback converter with clamp switches, which define the voltage at the other switches in off-state and prevent overvoltage spikes [29].

Due to step 4 (introducing clamp switches), defined off-state voltages are ensured for all topologies synthesized with the proposed method. For low power applications, however, the clamp switches are often replaced by snubber networks or avalanche-rated devices to save cost.

IV. Derivation of Novel Low-Switch-Count Topologies

In this section, two novel low-switch-count topologies are synthesized. Circuit simulations are presented to verify the results, and for the sake of completeness also the control of the topologies is explained.

A. Buck-Boost Single-Phase PFC Rectifier

Consider the typical example of a non-isolated single-phase battery charger for electric vehicles. For compatibility with various mains voltages and car types, wide input and output voltage ranges are required, which are typically overlapping, i.e., the maximum input voltage amplitude exceeds the minimum battery voltage. Therefore, a simple boost PFC rectifier cannot be used for this application and an additional buck stage is necessary. Assuming a bridge-less PFC rectifier followed by a buck converter, the resulting circuit employs a total of six power semiconductor devices. Applying the method proposed in Section II shows that only three switches are required to provide the same function.

1) Synthesis:

1. DC circuit: An anti-series connection of two elementary converters can be used to match the AC input voltage as shown in **Fig. 9**. A third elementary converter is used to provide the output current to the battery.

[1]By shorting all elements with zero AC voltage (voltage source, load resistor, capacitors).

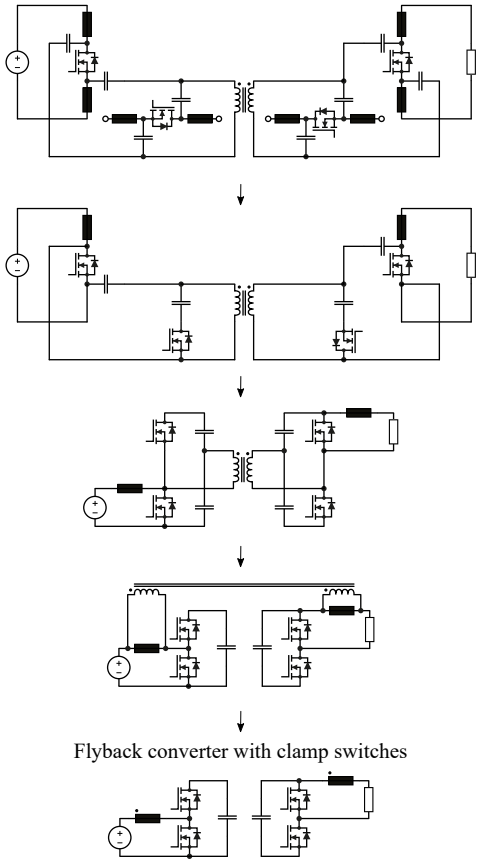

Fig. 8. Systematic synthesis of the flyback converter (step 5): Simplification of the circuit obtained in **Fig. 7** results in the circuit of a flyback converter with clamp switches. Note that the two inductors of the final circuit are magnetically coupled.

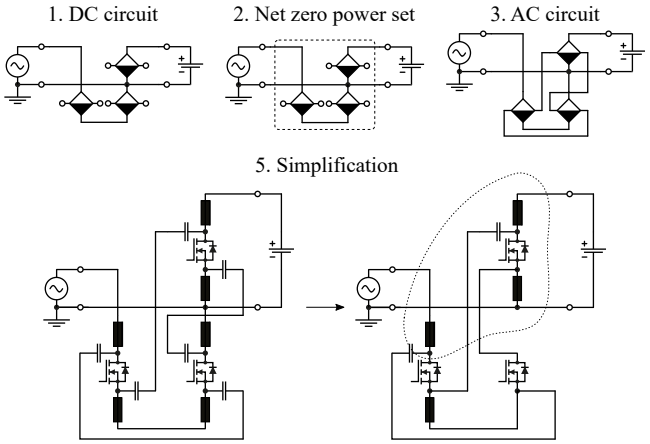

Fig. 9. Synthesis of a novel non-isolated single-phase buck-boost AC-DC converter. One of the three encircled inductors is redundant and can be shorted, leading to three different circuit variants; one is shown in **Fig. 10**.

2. Net-zero-power sets: To meet the power balance criterion, all elementary converters must be assigned to the same set.

3. AC circuit: All the three DC port voltages are different. Therefore, all AC ports are connected in series to form the AC loop. Although any connecting sequence works, it is

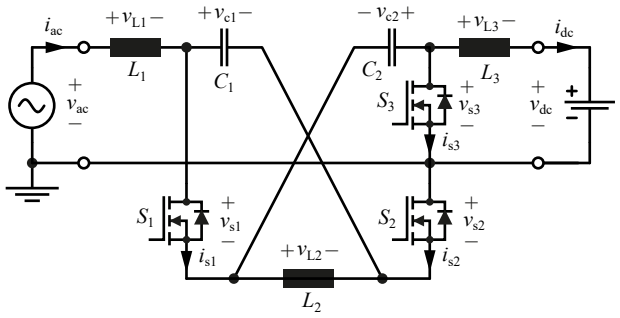

Fig. 10. Final simplified circuit obtained from the synthesis of a novel non-isolated single-phase buck-boost AC-DC converter in **Fig. 9**.

advantageous to connect terminals a and b of two elementary converters whose respective ports p and n are also connected, because this allows to short the two capacitors at the connected AC terminals a and b, and to merge the two inductors at the connected DC terminals p and n (see also the boost converter example in **Fig. 3** and **Fig. 4**).

4. Clamp switches: The AC path criterion is met and thus no additional elementary converters required.

5. Simplification: First, all series or parallel connected components are combined and capacitors with zero DC voltage are shorted. One of the three encircled inductors in the resulting circuit may be removed.[2] The one that's connected to the neutral line is selected (the other two are in series to the input and output terminal, respectively, and can thus advantageously contribute to EMI filtering) and finally the circuit shown in **Fig. 10** is obtained.

2) Control and Simulation: All the three switches are part of the (butterfly shaped) AC loop (see **Fig. 10**), because all elementary converter AC ports have been connected in series. According to (7), only one of them must be turned off at any given time, i.e.,

$$(1-d_1)+(1-d_2)+(1-d_3)=1. \tag{10}$$

No matter which one of the switches is off, it is blocking $v_{s,off}=v_{c1}+v_{c2}$. At each switch k, the average voltage $\langle v_{s,k}\rangle = (1-d_k)(v_{c1}+v_{c2})$ can be adjusted between 0 and $v_{c1}+v_{c2}$ using the duty cycle d_k.

Because the maximum blocking voltage of the switches must not exceeded a certain value $V_{s,max}$, one needs to control $v_{c1}+v_{c2}$ to that value. This is achieved by setting the duty cycle of S_3 according to

$$1-d_3=\frac{v_{dc}}{V_{s,max}}, \tag{11}$$

where v_{dc} is the DC output voltage.

To control the input current of the rectifier to follow a sinusoidal reference value $i_{ac,set}$, a simple proportional controller with gain k_p that applies $\langle v_{L1}\rangle = k_p(i_{ac,set}-\langle i_{ac}\rangle)$ to the inductor L_1 can be used. Taking into account the voltage ratio, $\langle v_{L1}\rangle/\langle v_{L2}\rangle = L_1/L_2$, this is achieved by setting d_1 and d_2 according to

$$(1-d_1)-(1-d_2)=\frac{\langle v_{ac}\rangle - k_p\frac{L_1+L_2}{L_1}(i_{ac,set}-\langle i_{ac}\rangle)}{\langle v_{c1}\rangle+\langle v_{c2}\rangle}. \tag{12}$$

The explicit expressions for the three duty cycles result from (10), (11) and (12).

[2]The three inductors are the only three connections between two circuit sections, hence the sum of the inductor currents must be zero; the same applies to the sum of the inductor voltages and thus one voltage can be set to zero by removing the corresponding inductor.

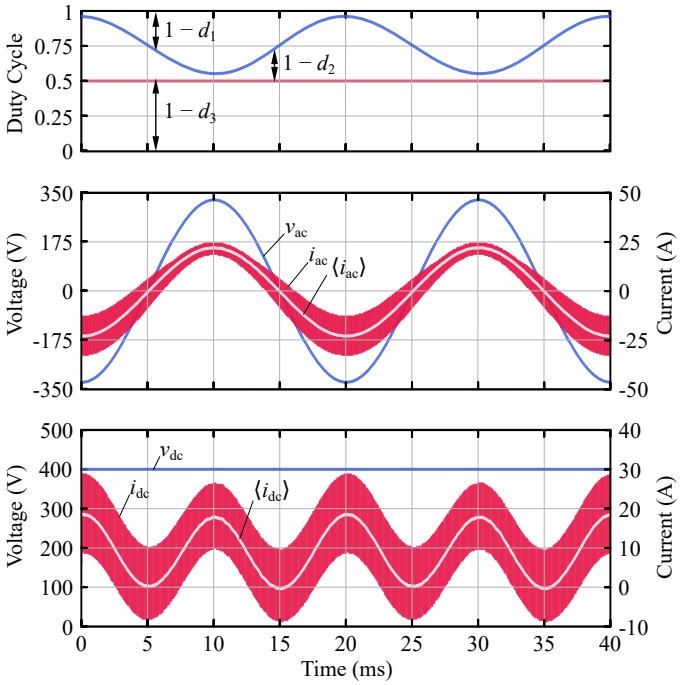

Fig. 11. Simulated input/output waveforms of the non-isolated single-phase buck-boost PFC rectifier in **Fig. 10**.

To verify the theoretical considerations, a circuit simulation with the component values $L_1=L_2=L_3=100\,\mu H$, $C_1=C_2=5\,\mu F$, $f_s=100\,kHz$ switching frequency, 230 V RMS mains voltage (50 Hz), 400 V battery voltage and 3.6 kW output power is carried out. The waveforms of two mains periods are shown in **Fig. 11**. Manual tuning of the current controller gain shows that $k_p=\frac{L_1 f_s}{2}=4\,\Omega$ provides good results.

The switch signals when zooming in at 7 ms are shown in **Fig. 12**. A single sawtooth carrier with two compare levels is used to generate the three gate signals. The blocking voltage of each switch in the off-state is reaching $V_{s,max}=800\,V$. After switch 1 turns on, the current is already positive, so this is a hard turn-on. When switch 3 turns off, the current is negative, so this is a hard hard-switching transition. The other turn-on and turn-off transitions are soft. To get rid of the hard switching, the inductance values could be reduced to achieve triangular-current-mode (TCM) operation, but that comes at the price of higher RMS current and the need to vary the switching frequency over the mains period.

B. Isolated Single-Phase PFC Rectifier

Usually, battery chargers are required to provide galvanic isolation. A conventional solution would be a PFC rectifier followed by an LLC resonant converter [30]. With a bridge-less

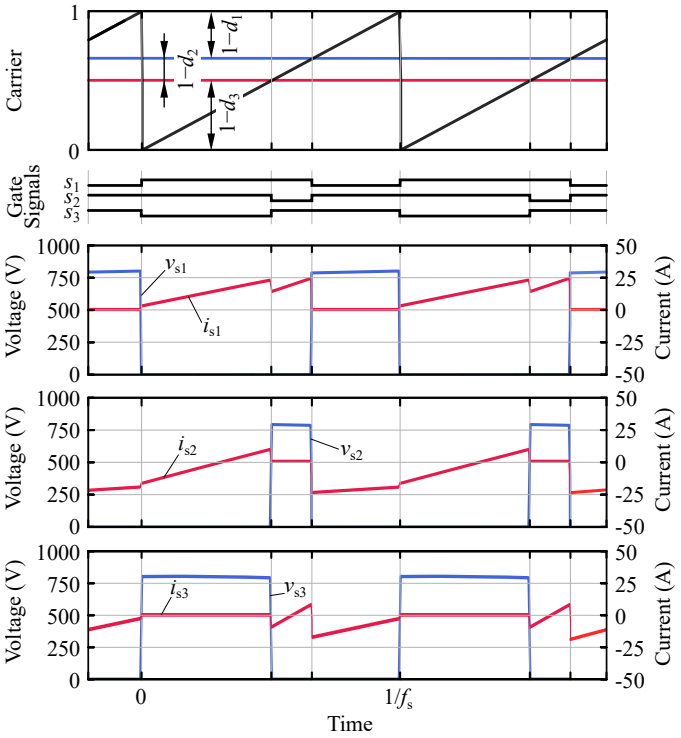

Fig. 12. Simulated switch waveforms (at 7 ms into the mains period) of the non-isolated single-phase buck-boost PFC rectifier in **Fig. 10**.

PFC and a half-bridge based LLC, the charger would consist of eight semiconductor devices. In the following it is shown that four semiconductor devices can provide the same functionality.

1) Synthesis:

1. DC circuit: On the primary side, an anti-series connection of two elementary converters is required for the AC interface, see **Fig. 13**. On the secondary side, two elementary converters are connected in series to charge the battery.[3]

2. Net-zero-power sets: To meet the power balance criterion, all elementary converters must be assigned to the same set.

3. AC circuit: The DC port voltages of the two primary-side elementary converters are different because the voltage *difference* must be equal to the input voltage. Therefore, their AC ports must be connected in series. The *sum* of the two primary-side elementary converter DC port voltages can be set to any value higher than $|v_{ac}|$. Setting it to a value that is proportional to the battery voltage allows to connect each AC port of the secondary-side elementary converters in parallel to one of the primary elementary converters via a transformer.

4. Clamp switches: To meet the AC path criterion, the AC ports of the two secondary-side elementary converters can be series connected to form a loop. This is possible without using a clamp switch.

5. Simplification: The two transformers are connected in parallel on the primary and secondary sides, so one of them

[3]Although not strictly necessary at this point, using two elementary converters allows to parallel-connect their AC ports and thus ultimately reduces the blocking voltage of the semiconductors on the secondary side.

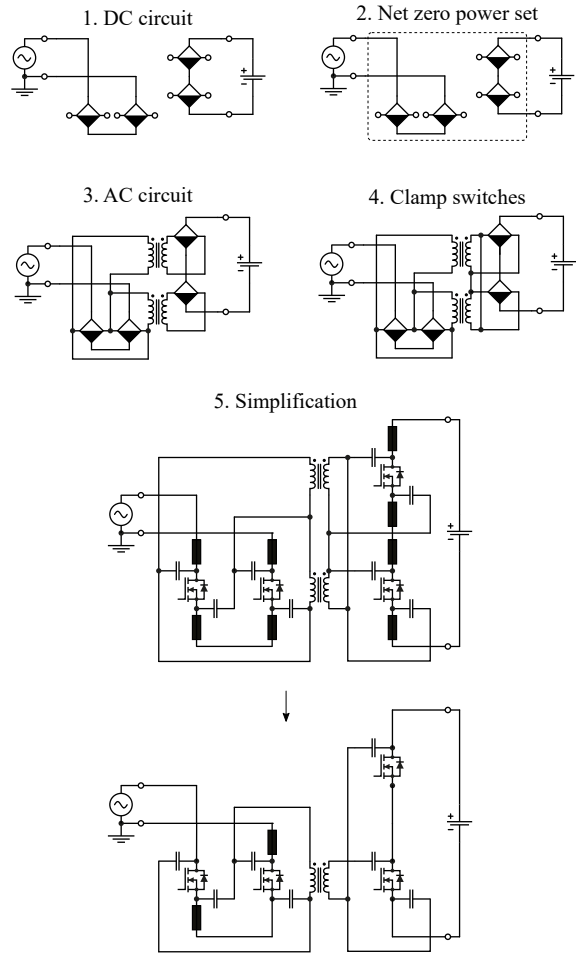

Fig. 13. Synthesis of an isolated single-phase PFC rectifier.

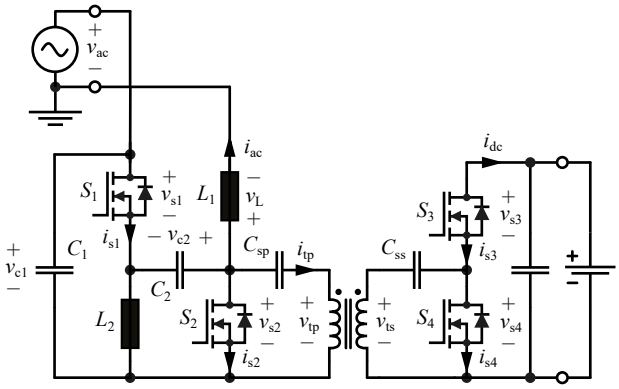

Fig. 14. Simplified circuit of the isolated single-phase PFC rectifier in **Fig. 13**.

can be removed. The primary-side circuit can be simplified in the same way as the SEPIC in **Fig. 6** and the secondary side simplification follows the same steps as in the derivation of the boost converter in **Fig. 4**. Finally, after rearranging the components, the circuit in **Fig. 14** is obtained.

2) Control and Simulation: In step 4 of the synthesis in **Fig. 13**, the AC ports of the primary-side elementary converters are connected in series, forming a loop; the same is done on the secondary side. Applying (7) requires $(1-d_1)+(1-d_2) = 1$ and

$(1-d_3)+(1-d_4)=1$. According to step 3 of the method, the duty cycles of parallel-connected AC ports must be equal. So the parallel connection via the transformers requires that $d_1 = d_3$ and $d_2 = d_4$. Therefore, the primary-side and secondary-side MOSFETs are controlled as complementary pairs with the same duty cycle

$$d = d_1 = (1-d_2) = d_3 = (1-d_4). \tag{13}$$

Additionally, also the phase shift g between the primary-side and secondary-side pairs of switches can be adjusted. So there are two controllers: One controlling the input current using the duty cycle d, the other controlling the power transfer between primary and secondary side using the phase shift g.

To control the input current, assuming again a simple proportional controller, the local average (over one switching period) voltage at the input inductor must be set to

$$\langle v_\mathrm{L}\rangle = k_\mathrm{p}(i_\mathrm{ac,set} - \langle i_\mathrm{ac}\rangle). \tag{14}$$

Thus, the switching period average voltage at S_1 must be set to

$$\langle v_\mathrm{s1}\rangle = \langle v_\mathrm{ac}\rangle - \langle v_\mathrm{L}\rangle + \langle v_\mathrm{c2}\rangle \tag{15}$$

by applying a duty cycle of

$$d = \frac{\langle v_\mathrm{s1}\rangle}{\langle v_\mathrm{c1}\rangle + \langle v_\mathrm{c2}\rangle} = \frac{\langle v_\mathrm{ac}\rangle - k_\mathrm{p}(i_\mathrm{ac,set} - \langle i_\mathrm{ac}\rangle) + \langle v_\mathrm{c2}\rangle}{\langle v_\mathrm{c1}\rangle + \langle v_\mathrm{c2}\rangle}, \tag{16}$$

where v_ac is the input AC voltage. The phase-shift controller, controls the power flow via the transformer in order to maintain a voltage ratio between primary-side and secondary-side elementary converters, which matches the turns ratio as required by step 3 of the method. With the turns ratio n as defined in the transformer equivalent circuit in **Fig. 15a**, the phase-shift controller aims to control the primary-side off-state voltage $(v_\mathrm{c1}+v_\mathrm{c2})$ to be equal to the secondary-side off-state voltage referred to the primary side $(\frac{v_\mathrm{dc}}{n})$ in order to achieve voltage waveforms at the transformer that ideally look as in **Fig. 15b**.

This is realized by transferring

$$P_\mathrm{t} = v_\mathrm{ac} i_\mathrm{ac,set} + k_\mathrm{t}\left((v_\mathrm{c1}+v_\mathrm{c2})^2 - \left(\frac{v_\mathrm{dc}}{n}\right)^2\right) \tag{17}$$

from the primary to the secondary side. This is a proportional controller with gain k_t and a feed-forward term for the power at the input. Basic analysis yields the equation for the transferred power as function of duty cycle d and phase shift g as

$$P_\mathrm{t} = \mathrm{sign}(g)\frac{(v_\mathrm{c1}+v_\mathrm{c2})v_\mathrm{dc}}{2f_\mathrm{s}L_\mathrm{s}n}\left(2d(1-d)|g| - g^2\right). \tag{18}$$

This equation is only true for $|g| < \min(d, 1-d)$, which is sufficient because the maximum power is obtained at $g = \pm d(1-d)$. Solving (18) for the phase-shift results in

$$g = \mathrm{sign}(P_\mathrm{t})\left(d - d^2 - \sqrt{d^4 - 2d^3 + d^2 - \frac{2f_\mathrm{s}L_\mathrm{s}nP_\mathrm{t}}{(v_\mathrm{c1}+v_\mathrm{c2})v_\mathrm{dc}}}\right). \tag{19}$$

Simulated waveforms during two mains cycles are shown in **Fig. 16** for the same operating point as used above (230 V RMS

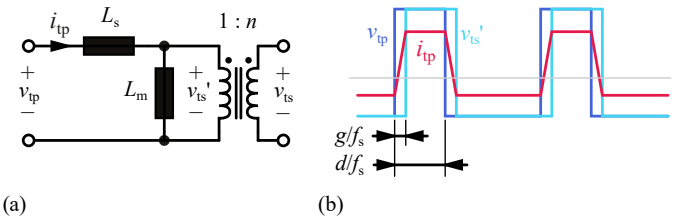

Fig. 15. **(a)** Transformer equivalent circuit and **(b)** idealized transformer voltage and current waveforms of the isolated rectifier in **Fig. 14**.

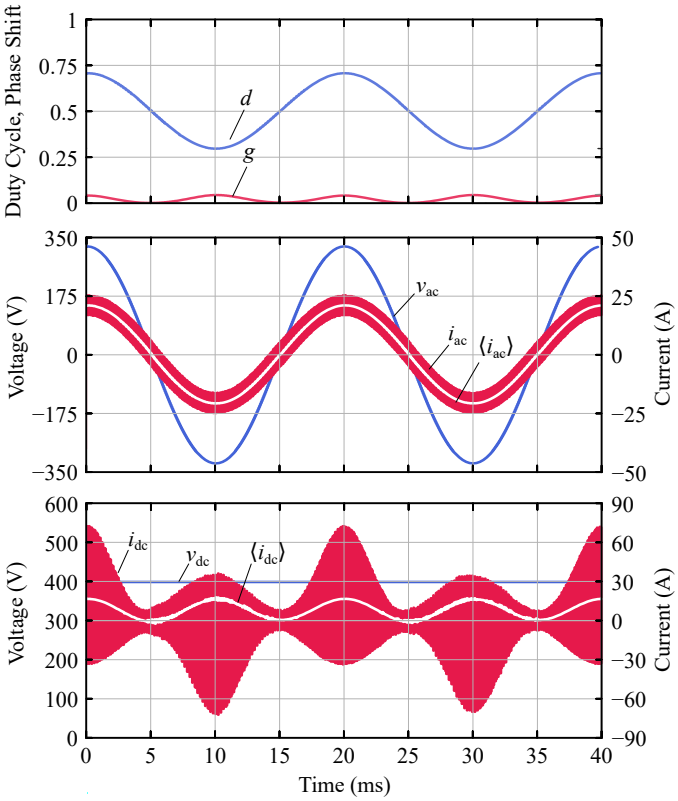

Fig. 16. Simulated input/output waveforms of the isolated single-phase PFC rectifier in **Fig. 14**.

mains, 400 V DC output, and 3.6 kW load) and $f_\mathrm{s} = 100\,\mathrm{kHz}$, $L_1 = L_2 = L_\mathrm{m} = 200\,\mu\mathrm{H}$, $L_\mathrm{s} = 4\,\mu\mathrm{H}$, $n = 0.5$, $C_1 = C_2 = 5\,\mu\mathrm{F}$ and $C_\mathrm{sp} = C_\mathrm{ss} = 10\,\mu\mathrm{F}$. A close-up of the signals during a switching period at 20 ms is shown in **Fig. 17**. Note that the switches on the DC side are soft-switching, while there is a hard-switching commutation on the AC side. The amount of phase-shift required to transfer a certain power can be reduced by reducing the leakage inductance. Because the loop voltages on the AC and the DC side are controlled to match the turns ratio, also very low leakage inductance values can be used, which can be an advantage for the design of the transformer.

For practical applications two modifications of the circuit in **Fig. 14** are interesting: First, if only unidirectional power flow is required, the secondary-side MOSFETs may be replaced by diodes. The secondary-side capacitors should be tuned to compensate the leakage inductance of the transformer at the switching frequency. With $C_\mathrm{sp} = 500\,\mathrm{nF}$ and otherwise

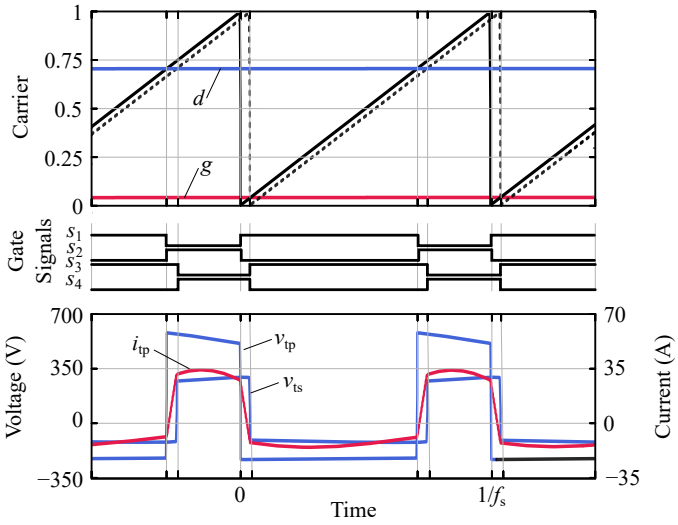

Fig. 17. Simulated gate signals and transformer waveforms (at 20 ms) of the isolated single-phase PFC rectifier in **Fig. 14**.

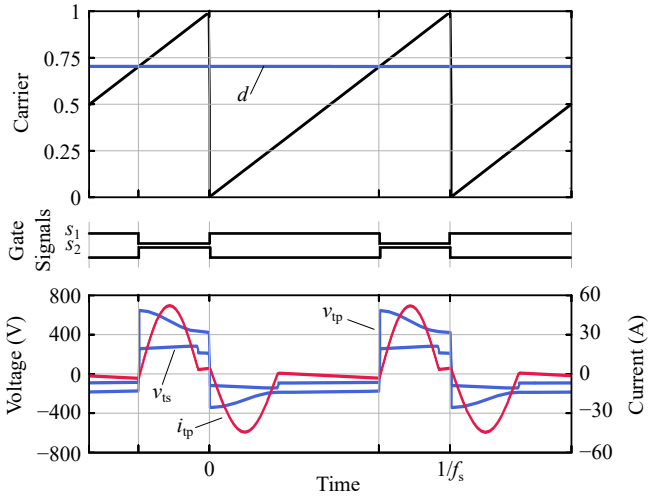

Fig. 18. Simulated gate signals and transformer waveforms of the isolated rectifier in **Fig. 14** with diodes instead of MOSFETs on the secondary side and series compensated transformer leakage inductance.

the same values as above, the resonant waveforms shown in **Fig. 18** result. Then, the power flow through the transformer is automatically obtained, similar as in a series-resonant "DC transformer" (DCX) [31], and the circuit can be controlled only via the duty cycle.

A further simplification of the circuit can be made by integrating the two inductors and the transformer into a single component. This is straight-forward with the winding polarities shown in **Fig. 19**; all windings are wound around the same magnetic core.

V. Conclusion

A method for synthesizing low-switch-count power converter topologies from specific electric requirements is presented. The method is based on an elementary converter that can be used as a building block. First, it is used to derive the topologies of the boost, buck-boost, Ćuk, SEPIC, Zeta and fly-back converters. Next, two novel AC-DC converter topologies are derived: A non-isolated buck-boost single-phase rectifier with three semiconductor devices and an isolated single-phase rectifier with four semiconductor devices.

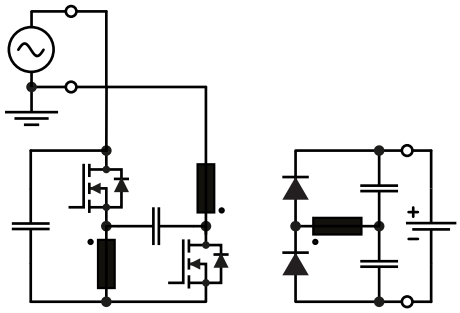

Fig. 19. Unidirectional circuit variant of the isolated single-phase PFC rectifier from **Fig. 14** with integrated transformer; note that all inductors are magnetically coupled.

For the derived topologies, waveforms from circuit simulations are shown and the control principles are briefly outlined. Although using fewer switches is not in general more efficient (in terms of losses), there are other advantages. This is mainly the lower complexity of the gate driver and control circuitry, which is important for low-power, low-cost applications. Also, one could employ parallel or series interleaving with any of the low-switch-count topologies to reduce the size of the passive components with still an acceptable total number of switches.

The method presented in this paper is intended to find suitable topologies for special applications, such as direct AC-DC conversion and/or multi-port converters. Although the method requires some engineering choices, it will always result in a working converter topology. Therefore, it could be interesting to apply it as part of a software framework for converter topology synthesis and optimization.

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