Power Electronic Systems
Laboratory

Proceedings of the 31st Applied Power Electronics Conference and Exposition (APEC 2016), Long Beach, CA, USA, March 20-24, 2016

Gate Signal Jitter Elimination and Noise Shaping Modulation for High-SNR Class-D Power Amplifiers

M. Mauerer
A. Tüysüz
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Gate Signal Jitter Elimination and Noise Shaping Modulation for High-SNR Class-D Power Amplifiers

M. Mauerer, A. Tüysüz and J. W. Kolar
Power Electronic Systems Laboratory, ETH Zürich, Switzerland
Email: mauerer@lem.ee.ethz.ch

***Abstract*—Two important aspects of switched-mode (Class-D) amplifiers providing a high signal to noise ratio (SNR) for mechatronic applications are investigated. Signal jitter is common in digital systems and introduces noise, leading to a deterioration of the SNR. Hence, a jitter elimination technique for the transistor gate signals in power electronic converters is presented and verified. Jitter is reduced tenfold as compared to traditional approaches to values of 25 ps at the output of the power stage. Additionally, digital modulators used for the generation of the switch control signals can only achieve a limited resolution (and hence, limited SNR) due to timing constraints in digital circuits. Consequently, a specialized modulator structure based on noise shaping is presented and optimized which enables the creation of high-resolution switch control signals. This, together with the jitter reduction circuit, enables half-bridge output voltage SNR values of more than 100 dB in an open-loop system.**

I. Introduction

Low-noise switched-mode amplifiers are required in different industry applications, amongst them integrated circuit manufacturing, where such amplifiers are used to drive various kinds of actuators of high-precision motion systems [1]. These systems have to provide positioning accuracies in the nanometer range, which requires the amplifiers to provide output currents of extremely low noise and high precision in order to avoid disturbing forces or torques in the actuators. It is estimated that the output current signal to noise ratio (SNR) of the power amplifiers needs to increase by approximately 20 dB every five years in order to keep track with the industry's growing requirements [2]. Therefore, a current SNR in excess of 110 dB is desired. State-of-the-art systems usually achieve SNR values in the range of $80 - 100\,\mathrm{dB}$ [2], [3].

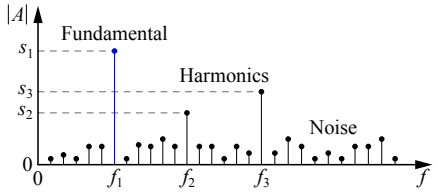

Fig. 1: Discrete amplitude spectrum of a noisy, periodic signal. The signal to noise ratio (SNR) relates the fundamental power $p(s_1)$ to the noise power $p(n)$ in a certain frequency range.

As the amplifiers target mechatronic applications, their output must be of low noise and high precision only in a limited frequency range from DC to $\approx$10 kHz, as the mechanical systems provide sufficient damping at higher frequencies and are thus less sensitive to high-frequency signal distortion or noise in the actuator's currents.

Digital control of such amplifiers is desired for the reasons of development and maintainability. Accordingly, this paper deals with two main aspects that are required to enable digitally controlled low-noise power amplifiers: jitter, which deteriorates the achievable SNR, and digital modulators, which, although operating with a coarse duty cycle resolution in order to achieve a given PWM switching frequency, are still capable of creating gate signals with a high SNR.

The SNR relates the power of a desired signal $p(s_1)$ to the power of unwanted signals $p(n)$, such as noise, in a given frequency range. The desired signal can be, e.g., the fundamental frequency component of an amplifier output voltage- or current signal, which can also contain low-order harmonics and noise. **Fig. 1** exemplarily illustrates the spectrum of a periodic signal that contains the desired fundamental with amplitude s_1, some integer harmonics s_x, and wideband noise. The signal's SNR is defined as:

$$\mathrm{SNR} = 10\log_{10}\left(\frac{p(s_1)}{p(n)|_{s_2,s_3,s_x=0}}\right), \tag{1}$$

where the noise power $p(n)$ is calculated in a given frequency range $[f_a \dots f_b]$ and the harmonics are excluded from the noise power calculation. If they were included, the figure would be called signal to noise and distortion ratio (SINAD) [4]. This work uses the SNR, as the investigated processes (jitter and PWM) cause few harmonics (if at all) of negligible power. The Fast Fourier Transform can be used to obtain the signal and noise powers from simulations or measurements [5], [6].

Although mechatronic amplifiers need to provide output currents of high SNR to create low-noise torques in the actuators, this work analyzes the SNR of the switching stage's output voltage in order to present a concise analysis of distortion and noise originating from the fundamental building blocks of the power converter, as a distorted voltage finally translates to current distortion in filter inductors or actuators.

Section II presents sources of jitter in power electronic converters and proposes a simple new circuit for generating isolated, low-jitter gate signals. The circuit is also immune to fast common-mode voltage transients across the isolation barrier and its functionality is experimentally verified. **Section III** details advanced modulation structures which outperform conventional pulse-width modulators. Their performance is also demonstrated with a prototype system. Finally, **Section IV** summarizes the achieved results and presents an outlook.

978-1-4673-9550-2/16/$31.00 ©2016 IEEE

II. Signal Jitter and its Elimination in a Gate Driver Circuit

Electrical signal jitter has various classifications and, due to its often stochastic nature, can be modeled like noise [7]. **Fig. 2** shows a periodic digital signal with jitter, which expresses itself as the time-dependent deviations Δt_i of the signal's edge positions from their ideal positions [8].

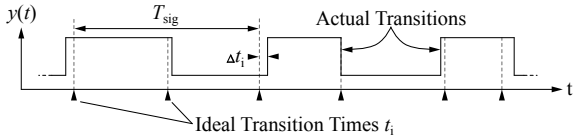

Fig. 2: A digital, periodic signal $y(t)$ shows jitter if its edges occur at time instants different from the ideal transition times. The time difference Δt_i between actual and ideal edge is often of stochastic nature.

In digital signals, where information is encoded in the time instants of its edges, jitter alters the information and introduces wideband noise [4]. For high-precision PWM applications with targeted SNRs in excess of 100 dB and pulse frequencies $f_{\mathrm{PWM}} = 1/T_{\mathrm{PWM}}$ in the range of $50 \ldots 200$ kHz, even jitter figures (Δt_i) in the picosecond range can introduce significant noise and limit the SNR as the equation from [9] shows:

$$\mathrm{SNR}_{\max} = 20 \log_{10} \left(\frac{m}{4\sqrt{2} \cdot T_{\mathrm{Jit,RMS}}} \sqrt{\frac{T_{\mathrm{PWM}}}{f_{\mathrm{BW}}}} \right) \qquad (2)$$

Fig. 3 illustrates eq. (2) for different pulse frequencies f_{PWM}. The bandwidth f_{BW} in which the noise power is assessed is 10 kHz (cf. eq. (1)) and the modulation index m of the PWM modulator approaches 1 ($0 \leq m \leq 1$). $T_{\mathrm{Jit,RMS}}$ is the RMS jitter and denotes the stationary RMS value of the time deviations Δt_i. As these deviations follow a stochastic distribution, a sufficient amount of samples, depending on the underlying stochastic process, must be considered in order to correctly calculate their RMS value.

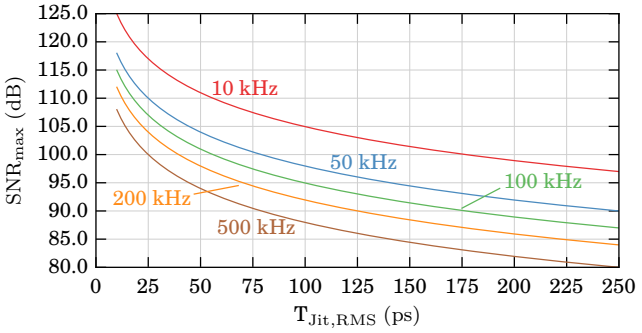

Fig. 3: Plots of eq. (2): Maximum achievable SNR for a given PWM frequency in dependence of the RMS jitter. The modulation index is $m \to 1$ and the bandwidth for which the SNR is calculated is 10 kHz.

A. Sources of Jitter in Power Electronics

Fig. 4 depicts a half-bridge (HB) leg which is a typical building block of Class-D amplifiers and consists of two power transistors, T_1 and T_2 and their respective gate driver circuits. Both drivers require an isolated supply and an isolated gate control signal path in order to allow any control system reference potential between the potentials U_{POS}, U_{NEG} of the DC link rails.

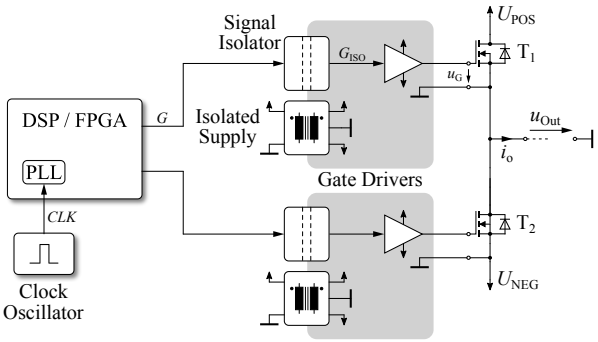

Fig. 4: Conventional half-bridge topology with two power transistors, their isolated gate drivers and a digital gate signal generator.

Every functional element in the gate signal path is a potential source of jitter. In this regard, the clock oscillators of digital signal processors (DSPs) or field programmable gate arrays (FPGAs), both being widely used to generate the gate control signals, as well as the signal routing in an FPGA, add jitter. However, the most prominent jitter source is the signal isolator, which is commonly realized using optocouplers or non-optical digital signal isolators[1].

B. Gate Driver with Reduced Jitter

Existing jitter minimization techniques reduce the jitter of a (periodic) clock signal with phase locked loops (PLL) or filters, and are usually applied in low-power digital-to-analog converters [11]. This work proposes the circuit depicted in **Fig. 5** to reduce the jitter of the (potentially non-periodic) gate control signals which includes a basic concept proposed in [12], but extends it by a system that renders the gate drivers immune to fast output voltage transients, i.e., it prevents faulty switching actions of the power transistors in case the signal isolator emits erroneous signals during short output voltage transients of high $\mathrm{d}u/\mathrm{d}t$.

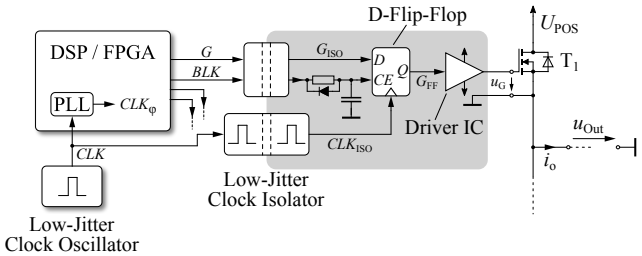

Fig. 5: Improved gate driver which significantly reduces jitter and is immune to output voltage transitions with a high $\mathrm{d}u/\mathrm{d}t$. (The isolated supply and the second identical driver are not drawn).

[1]Digital signal isolators feature shorter propagation delay times, stricter propagation delay tolerances and a higher $\mathrm{d}u/\mathrm{d}t$ withstand capability than optocouplers and are thus expected to perform better in low-distortion applications where the signal integrity is of importance [10].

The key component of this circuit is a low-jitter clock isolator, which, in this work, is made of a small signal transformer made for clock frequencies greater than 100 MHz, driven by a high-speed differential driver. The circuit transmits the clock signal to the gate driver where it clocks a flip-flop which re-synchronizes the gate control signal to this low-jitter clock CLK_{ISO}. **Fig. 6** depicts the timing waveforms of this method. In order to meet the setup and hold times of the flip-flop, the clock used for the DSP/FPGA, CLK_{φ}, must potentially be shifted in phase relative to the isolated clock CLK_{ISO}, which can be accomplished by, e.g., using the FPGA's on-chip clock manager.

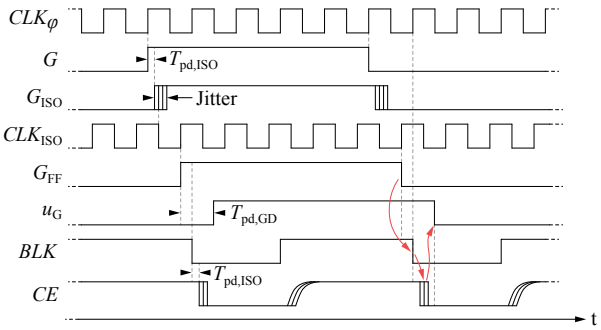

Fig. 6: Timing waveforms of the proposed circuit. CLK_{φ} is used by the digital control system. *BLK* and *CE* are used to render the system immune to bridge leg output transitions with a high $\mathrm{d}u/\mathrm{d}t$. $T_{\mathrm{pd,ISO}}$ and $T_{\mathrm{pd,GD}}$ are the propagation delays of the signal isolator and the gate driver IC. The required sequencing of G_{FF}, *BLK* and *CE* is indicated with arrows.

C. Output Transient Withstand Capability

In order to reduce distortion, amplifier output signals ($u_{\mathrm{Out}}(t)$ in **Fig. 4**) require a short output transition time to approximate the ideal square waveform [13]. However, the signal isolators can only withstand a certain $\mathrm{d}u/\mathrm{d}t$, caused by bridge leg output voltage transitions, across their isolation barrier without producing erroneous output signals (usually $< 50\,\mathrm{kV\,\mu s^{-1}}$ [14]). The circuit presented in **Fig. 5** is designed to prevent faulty control signals to be transmitted to the driver IC during fast output voltage transients. The method utilizes a blanking signal, *BLK*, which is forwarded to the clock-enable (*CE*) input of the flip-flop via an RC low-pass filter. As long as the *CE* input is low, the flip-flop conserves its state regardless of its potentially faulty input (G_{ISO}).

The low-pass filter prevents temporary (ns range) faulty signals that are potentially emitted by the signal isolator during output transients from affecting the *CE* input. In order to be able to quickly pull the *CE* input low, a diode is placed across the low-pass filter. The waveforms of this method are also illustrated in **Fig. 6**. The required sequencing of the control signals G_{FF}, *BLK* and *CE* is indicated with arrows. It is essential that the *CE* input is pulled low before the gate driver changes the gate voltage u_{G}, as afterwards, the function of the signal isolator might not be guaranteed during the output transient. This can be achieved as the gate driver has a given propagation delay of usually $5 - 30\,\mathrm{ns}$ during which the *CE* input is pulled low. The blanking sequence is always executed simultaneously by both gate driver circuits in a half-bridge whenever any of the two bridge leg gate drivers changes its transistor's gate voltage, as the output voltage transient may occur only when the complementary transistor switches, depending on the bridge leg's output current direction.

This system limits the minimum dead time (i.e., the time required, after a transistor has switched, before the complementary transistor may be switched, to prevent a short-circuit of the DC link rails) and minimum duty cycle, as time must be allotted for the blanking cycle and the low-pass filter, during which the bridge leg's output state cannot be changed. Experiments show that with a clock frequency of 100 MHz, the minimum dead time is $\approx 50\,\mathrm{ns}$.

D. Jitter Measurements

The circuit from **Fig. 5** has been implemented in a hardware demonstrator (without the power transistors) in order to verify its basic functionality. **Fig. 7** shows the system which features two isolated gate drivers, an FPGA and a low-jitter clock oscillator which serves as the FPGA's clock source. The isolated supplies of the gate drivers create adjustable positive and negative supply voltages.

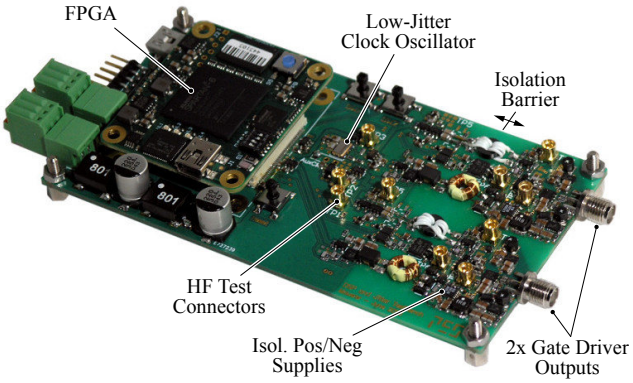

Fig. 7: Hardware demonstrator featuring two isolated gate drivers with the jitter reduction circuitry. The clock isolator comprises a 5.95 mm *Fair-Rite 5943000101* toroid core with $N_1 = N_2 = 4$ turns, being driven by an LVDS driver. The digital signal isolator is an *SI8620*, the gate driver IC is an *LM5114* and the clock oscillator an *FXO-HC536R-100*. The flip-flop is a *74LVC1G79GV* and its *CE* functionality is implemented using an AND-gate at its clock input.

Using this prototype, the signal jitter (Δt_i) along the gate signal path is measured. **Fig. 8** illustrates such a measurement in the time domain for the rising edges of the signals G_{ISO} and G_{FF} (cf. **Fig. 5**), with each edge transition being made visible using the oscilloscope's infinite screen persistence. A high-bandwidth oscilloscope must be used to minimize the influence of its own time base jitter, which is usually in the low ps range [15].

For each signal transition, the time deviation from the ideal edge position (Δt_i, cf. **Fig. 2**) is recorded and the RMS value of the deviations is calculated. **Tab. I** lists the RMS jitter values of different signals along the gate signal path. For these measurements, a square wave is created by the FPGA and transmitted to the gate drivers. The clock frequency of the low-jitter oscillator is 100 MHz. Using eq. (2), the maximum achievable SNR, which is calculated using the measured jitter

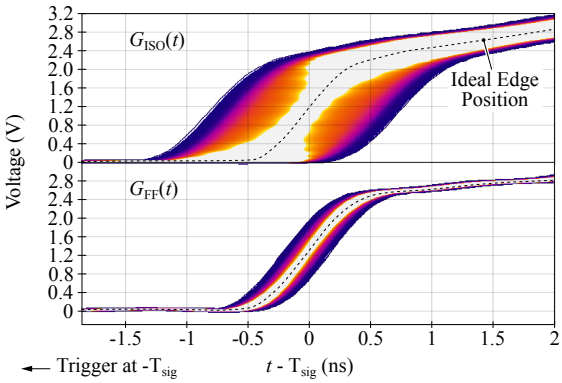

Fig. 8: Persistent oscilloscope waveforms of two different signals (G_{ISO} and G_{FF}, cf. **Fig. 5**), visualizing their jitter. Brighter colors represent more signal transitions. The oscilloscope has a 1 GHz analog bandwidth and samples with 10 GHz (*R&S RTO1014*).

values, is also listed ($f_{\mathrm{PWM}} = 100\,\mathrm{kHz}$, $f_{\mathrm{BW}} = 10\,\mathrm{kHz}$, cf. **Fig. 3**). It is evident that the signal isolator adds the most jitter (215 ps) to the gate signal. The clock isolator only contributes 5.7 ps to the clock jitter. The remaining jitter contributions arise from the re-synchronization flip-flop and the gate driver IC.

Signal	$T_{\mathrm{Jit,RMS}}$ (ps)	$\mathrm{SNR_{max}}$ (dB)
CLK	3.3	124.6
CLK_{ISO}	9.0	115.9
G	33.5	104.4
G_{ISO}	248	87.1
G_{FF}	24.7	107.1
u_{G}	25.1	107.0
[2]u_{Out} (400 V)	25.6	106.8

TABLE I: Measured RMS values of the time differences Δt_i of signals along the gate signal's path. The max. achievable SNR is derived from eq. (2) and calculated for a PWM frequency of 100 kHz, a bandwidth of 10 kHz and a modulation index of $m \to 1$.

Due to the stochastic nature of jitter, a visualization with a histogram is typically done. **Fig. 9** depicts the jitter (Δt_i) of G_{ISO} and G_{FF}. It reveals that the jitter of G_{FF} can be approximated by a normal distribution with a standard deviation of 24.7 ps. This does not apply to the distribution of G_{ISO}, which shows a more triangular shape.

These measurements prove the necessity and functionality of the proposed circuit. As expected, the signal isolator adds a high amount of jitter to the signal. After the resynchronization flip-flop, the RMS jitter is reduced tenfold and the achievable SNR can be increased from 87 dB to 107 dB.

E. Transient Withstand Capability Verification

As section II-C explains, the proposed gate driver circuit is capable of withstanding an output voltage transient with a high $\mathrm{d}u/\mathrm{d}t$ across its isolation barrier without producing erroneous switch signals. In order to verify this functionality, a half-bridge comprising two *GaN Systems GS66508T* gallium nitride (GaN) enhancement-mode HEMTs (high electron mobility transistor,

[2]Power transistors are connected to the drivers and the jitter of u_{Out} is measured, cf. sec. II-E

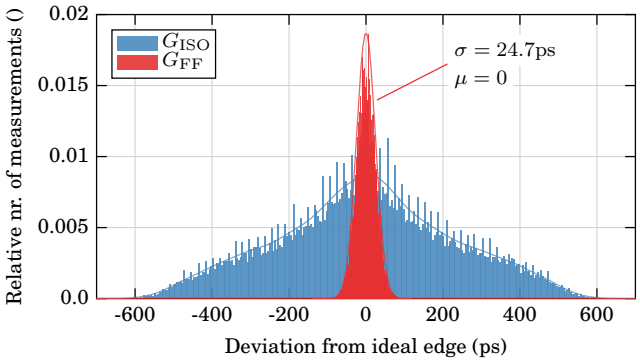

Fig. 9: Histogram of two signals with jitter as measured on the hardware demonstrator. G_{ISO} is the signal after the digital isolator and G_{FF} is the same signal after the re-synchronization flip-flop.

650 V, 30 A, 55 mΩ) is connected to the hardware demonstrator (cf. **Fig. 7**). This setup allows the generation of half-bridge output voltage transitions with a high $\mathrm{d}u/\mathrm{d}t$ in both double-pulse experiments as well as under a constant operation in a buck converter. **Fig. 10** (a) and (b) illustrate the hard- and soft-switched output voltage transitions respectively as they were obtained during double-pulse experiments with a half-bridge output current of 20 A. The $\mathrm{d}u/\mathrm{d}t$ values observed are in the

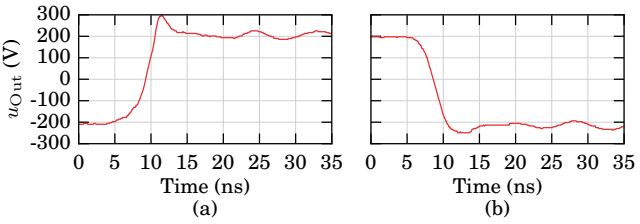

Fig. 10: GaN Half-bridge output voltage transitions with a load current of 20 A. (a): Hard-switched transition. $\mathrm{d}u/\mathrm{d}t_{(10\%-90\%)}$: $83.2\,\mathrm{kV\,\mu s^{-1}}$. Max. $\mathrm{d}u/\mathrm{d}t$: $221\,\mathrm{kV\,\mu s^{-1}}$. (b): Soft-switched transition. $\mathrm{d}u/\mathrm{d}t_{(10\%-90\%)}$: $-93.2\,\mathrm{kV\,\mu s^{-1}}$. Max. $\mathrm{d}u/\mathrm{d}t$: $-115\,\mathrm{kV\,\mu s^{-1}}$.

range of $80-220\,\mathrm{kV\,\mu s^{-1}}$ and easily exceed the signal isolator's rating of $50\,\mathrm{kV\,\mu s^{-1}}$ [14]. Consequently, an erroneous behavior of this device is likely. This demonstrates the need for an isolated signal transmission system which is capable of dealing with fast voltage transitions across its isolation barrier.

In order to verify the reliability of the gate driver circuit, the same half-bridge has also been continuously operated in a buck converter ($P = 1.9\,\mathrm{kW}$, $U_1 = 400\,\mathrm{V}$, $U_2 = 200\,\mathrm{V}$, $f_{\mathrm{PWM}} = 100\,\mathrm{kHz}$, $\eta_{\mathrm{tot}} = 98.5\%$). During this operation, with a load current of ≈10 A, the RMS jitter of the switched, 400 V output voltage remained at ≈26 ps, and no faulty switching actions occurred. However, fast switching transients across the signal isolator's dielectric can lead to its deterioration during longer operation due to capacitive displacement currents. A low-capacitance common-mode filter in series to the signal isolator input can potentially reduce these dielectric currents [16].

This chapter demonstrated the functionality and performance of the proposed gate driver circuit. In the following, a digital modulation scheme is presented which creates high-resolution (low-noise) switch control signals that utilize the full potential of the low-jitter gate drivers.

III. Noise Shaping PWM

This chapter addresses specialized digital signal processing techniques that allow the creation of high-resolution (and hence, low-noise) pulse width modulated (PWM) switch control signals.

A. Digital PWM Resolution Limits

In digital systems, PWM signals are commonly created with, as **Fig. 11** (a) shows, a counter that counts (with the clock frequency f_{Clk}) during one switching period ($T_{\mathrm{PWM}} = 1/f_{\mathrm{PWM}}$) from zero to a predefined value (*TOP*), and, in case of double-sided modulation, back down to zero. Whenever the counter value is lower than a compare value *CMP*, the PWM output is high and otherwise, it is low (assuming two switching levels), leading to a modulation of the output signal by *CMP* [17].

Each counter step represents a possible PWM duty cycle and hence, the duty cycle is amplitude-quantized with the number of available counter steps. As the duty cycle is only changed once every switching period, the PWM signal is also time-quantized (i.e., sampled, with f_{PWM}). The achievable SNR of the PWM signal is limited due to the amplitude-quantization error present in signals of finite amplitude resolution [18]. The SNR of a sinusoidal, amplitude-quantized and sampled signal with a resolution of n bits can be approximated by:

$$\mathrm{SNR} = 6.02n + 1.76\ \mathrm{dB}, \tag{3}$$

where the frequency range is from DC to $f_{\mathrm{PWM}}/2$ [4]. Eq. (4) emphasizes the relationships between the PWM resolution, the PWM frequency f_{PWM} and the counter frequency f_{Clk} (cf. **Fig. 11** (a)):

$$\mathrm{PWM}_{\mathrm{Res}}(\mathrm{Bits}) = n = \frac{\ln(TOP)}{\ln(2)} = \frac{\ln\left(\frac{f_{\mathrm{Clk}}}{2f_{\mathrm{PWM}}}\right)}{\ln(2)}. \tag{4}$$

This shows that for high-SNR PWM signals and a given PWM frequency, a high digital clock frequency is required, e.g., for a PWM signal with $f_{\mathrm{PWM}} = 20\,\mathrm{kHz}$ and a resolution of $n = 16$ bits, a clock frequency $f_{\mathrm{Clk}} > 2.6\,\mathrm{GHz}$ is necessary. This is unfeasible for practical implementations as high-resolution counters cannot easily be implemented in digital hardware at such high clock rates. The limit for configurable logic is usually below 500 MHz [19]. Therefore, the following section presents a DSP technique which can create low-noise digital signals despite using low-resolution signals.

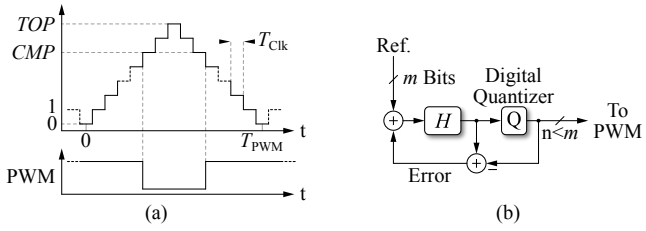

Fig. 11: (a): Counter-based PWM modulator. Each counter step represents a possible duty cycle. (b): Simplified noise shaping principle. The quantization error is fed back into the system whereas its frequency components are shaped by the transfer function H.

B. Noise Shaping

In audio engineering, high-resolution amplitude-quantized signals with up to 24 bits need to be fed to a PWM modulator in Class-D amplifiers with switching frequencies in excess of 300 kHz [20], [21]. This is accomplished by using a nonlinear DSP technique named oversampled noise shaping (NS), which can convert a high-resolution, amplitude-quantized signal to a signal of lower amplitude resolution such that a counter-based PWM modulator can be used while still achieving little quantization noise in a given frequency band (i.e., the baseband) [22], [23]. These techniques shift the quantization noise created by the reduction of signal resolution to higher frequencies, where they can be attenuated by a low-pass filter or where they are of no concern for the target application.

Fig. 11 (b) illustrates a simplified structure of a noise shaping system. The reference signal has a high amplitude resolution of m bits. The digital quantizer reduces the resolution to n bits such that $n < m$. The quantization error is fed back into the system and its spectrum is shaped by a transfer function H such that the quantization noise is significantly reduced in the baseband, resulting in a low-noise output. This signal can now be fed to a PWM modulator with a resolution of also n bits.

Assuming that the quantizer adds the quantization noise additively, its spectral behavior in a noise shaping system can be described by the so-called noise transfer function (NTF), whereas the influence of the noise shaper on the desired signal can be described by the signal transfer function (STF) [22]. The block diagram in **Fig. 12** visualizes this approach. These transfer functions are implemented by the noise shaper's internal structure. **Fig. 12** also illustrates an exemplary NTF. The baseband ranges from DC to 10 kHz in which the amplitude-quantization noise gets attenuated by ≈75 dB. At higher frequencies, the quantization noise increases (high-pass characteristic).

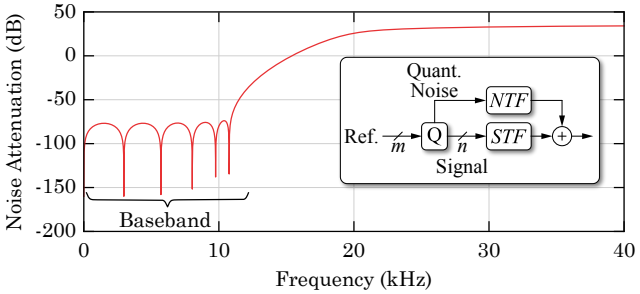

Fig. 12: Amplitude plot of an exemplary noise transfer function (NTF) with 11 poles and 11 zeros. The high-pass characteristic shifts the quantization noise to higher frequencies.

For a typical mechatronic amplifier, noise above ≈10 kHz is not critical as the inertia of the mechanical systems introduces sufficient attenuation. Hence, such NS techniques can be applied with a baseband ranging from DC to ≈10 kHz.

Fig. 13 depicts the simulated output signal response of a noise shaper to an arbitrary, varying input signal in the time domain. In this case, the signal transfer function is $STF = 1$, which is visualized by the perfect tracking performance of the noise shaper's output. The difference of the input and output

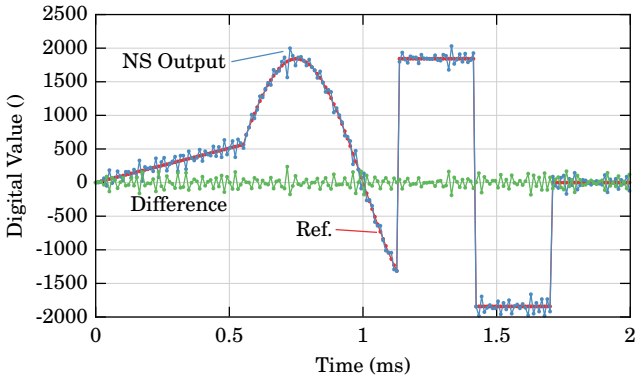

Fig. 13: Exemplary time-domain behavior of a noise shaper. The input signal has an amplitude resolution of 12 bits and the output of the noise shaper is 9 bits wide. The output is rescaled (multiplied by 2^{12-9}) such that the input and output are directly comparable.

is the quantization error whose spectrum is shaped by the NTF (cf. **Fig. 12**). As a noise shaper employs feedback, the system can potentially become unstable. Due to their nonlinear nature (due to the quantizer and digital saturation or overflow effects), noise shapers can only be well investigated using computer simulations. This is done to assess its performance or stability with different input signals.

Noise shaping can be employed in different ways to obtain the switch control signals. **Fig. 14** illustrates two possible signal flow paths in a noise shaping DSP system. The goal of the structure is to replicate the reference signal with a physical signal (i.e., voltage or current) in the amplifier's power stage. The reference signal is created digitally (e.g., by an overlaying amplifier control system) with a high resolution of m bits and a sampling rate f_S. This sampling rate is usually lower than the PWM modulator's sampling rate f_PWM and consequently, there must be a digital upsampling block which performs interpolation and increases the reference signal's sampling rate to f_PWM, which is also the noise shaper's sampling rate. The ratio between f_PWM and f_S is the oversampling ratio (OSR). After the upsampling block, there are two options of how to create the power transistor's switching signal, which can have k levels ($k \geq 2$), depending on the power stage topology.

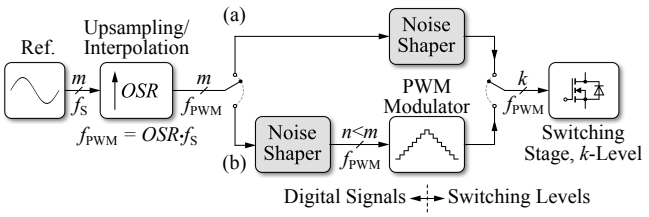

Fig. 14: Two possible signal flow paths in a digital, noise shaping modulation system for power electronic converters. (a): The noise shaper directly creates the switching signals. (b): The noise shaper feeds a PWM modulator which creates the switching levels.

In the first option, the noise shaper outputs a very low-resolution signal which is directly used as the switch control signal, e.g., a 1-bit signal in the case of a $k = 2$-level switching stage (cf. **Fig. 14** (a)). In the other option (cf. **Fig. 14** (b)), the noise shaper forms an output signal with a resolution of several bits (e.g., $n = 8$) that is fed to a counter-based PWM modulator which creates the switch signals as illustrated in **Fig. 11** (a). This lower-resolution modulator can easily be implemented in digital hardware with clock frequencies not exceeding several hundred MHz (cf. eq. (4)).

Computer simulations with common noise shaper implementations [24] have been performed in order to determine which of the two options results in the lowest baseband (DC-10 kHz) quantization noise. The results show that option (b) generally performs better. This is due to the fact that the noise shapers with the low output resolution as used in **Fig. 14** (a) become unstable more easily than noise shapers with a higher output resolution. This limits their ability to attenuate the quantization noise sufficiently.

In the following, the structure of the evaluated noise shaper and its performance are presented in more detail.

C. Noise Shaper Implementation

Different common noise shaping structures [24] have been simulated with a signal flow path as illustrated in **Fig. 14** (b) and compared with respect to their achievable performance and stability. The structure presented in [25], named noise-coupled noise shaper (NCS), performed best and simulations verify its robust performance. **Fig. 15** (a) illustrates this noise shaper structure.

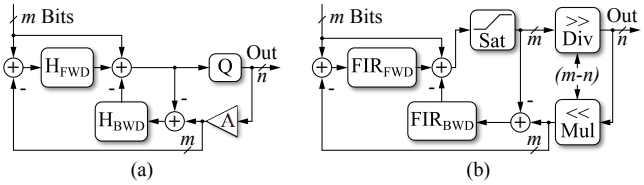

Fig. 15: (a): The noise-coupled noise shaping structure (NCS) used in this work. The transfer functions $\mathrm{H_{FWD}}$ and $\mathrm{H_{BWD}}$ define the noise transfer function (NTF) and can be implemented as FIR filters. (b): Digital implementation of the noise-coupled shaper.

The signal transfer function of this structure is $STF = 1$, which means that the desired signal passes the noise shaper without alteration. The NTF is given by

$$NTF = \frac{1 - \mathrm{H_{BWD}}}{1 + \mathrm{H_{FWD}}}. \tag{5}$$

If $\mathrm{H_{FWD}}$ and $\mathrm{H_{BWD}}$ have just zeros but no poles, they can be implemented as FIR filters. Furthermore, $\mathrm{H_{BWD}}$ then determines the zeros of the NTF and $\mathrm{H_{FWD}}$ its poles. Consequently, if the NTF is given, $\mathrm{H_{BWD}}$ and $\mathrm{H_{FWD}}$ are found by comparing the coefficients. The order of the noise shaper is determined by the number of coefficients in $\mathrm{H_{FWD}}$ and $\mathrm{H_{BWD}}$. A higher-order noise shaper shows a better noise suppression, but is more prone to unstable behavior [22]. The gain block A (cf. **Fig. 15** (a)) simply rescales the quantizer output to the corresponding value in the quantizer's input range (multiplication by 2^{m-n}).

Fig. 15 (b) illustrates the digital implementation of the NCS. Only simple structures like FIR filters or bit shifts (division/multiplication by powers of 2) are required. The quantization noise is introduced when the quantizer (the divider) shifts the lower bits out of the signal (division without remainder).

D. Noise Shaper Optimization

The poles and zeros of the NTF can be optimally arranged such that the noise level is minimized in the baseband [22], [24]. Furthermore, the order of the noise shaper is an additional degree of freedom which influences the performance. However, the stability of different NS configurations with different input signals must be assessed using computer simulations. Such optimizations and stability assessments have been performed for the noise-coupled shaper (cf. **Fig. 15**) with the aim of finding stable configurations (i.e., zero/pole placement and order) with the best possible quantization noise suppression from DC to 10 kHz.

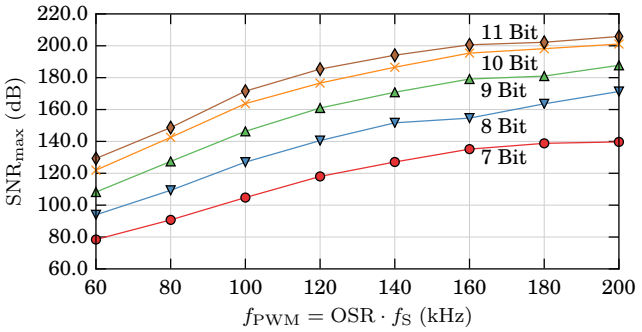

Fig. 16: Best achievable SNR of stable noise-coupled shapers with different output resolutions from DC to 10 kHz. The reference input signal is a 80 Hz sinus with a resolution of 35 bits and a modulation index of $m = 0.9$.

Fig. 16 illustrates the optimization results. The best achievable SNR of the noise-coupled shapers is plotted for different OSR and noise shaper output bit widths n. The different noise shaper configurations feature orders ranging from 7 to 14.

E. Noise Shaper Verification

The NCS structure presented above has been implemented in an FPGA in order to verify its functionality. The testbench presented in **Fig. 7** is used together with the half-bridge setup described in section II-E to create a low-distortion and low-noise digital output signal. The supply of the half-bridge is fed by batteries (9 V) to minimize external noise sources and it is buffered by large DC link capacitors in order to minimize supply harmonics [13]. The noise shaper has an order of 11, an output resolution of $n = 9$ bit and the PWM switching frequency is $f_{PWM} = 97.7$ kHz. The digital reference signal is a 170 Hz sinus with a resolution of 26 bits and a modulation index of $m = 0.85$. The noise shaper is optimized for a baseband from DC to ≈10 kHz. The reference signal is sampled with f_{PWM} in order to eliminate the need for an upsampling/interpolation stage.

Fig. 17 shows the computer simulated amplitude spectra of the signals after this noise shaper and after the PWM modulator ($k = 2$ switching levels). The spectra are rescaled such that the fundamentals match in amplitude. At frequencies higher than 10 kHz, the quantization noise increases significantly, as designed. The SNR of the noise shaper output signal from DC to 10 kHz is 138 dB. The spectrum of the PWM output contains two harmonics. These originate from the non-naturally sampling PWM modulator, as the duty cycle is updated once every switching period [17]. Pre-distortion techniques can potentially be used to reduce these harmonics [20], [26]. Additionally, the noise floor of the PWM output starts to rise at frequencies lower than 10 kHz. This is an effect caused by intermodulation distortion at the PWM modulator's nonlinearities which leads to noise being folded back into the baseband [20]. The SNR of the PWM output is 97.8 dB and its total harmonic distortion (THD, [13]) is −103 dB.

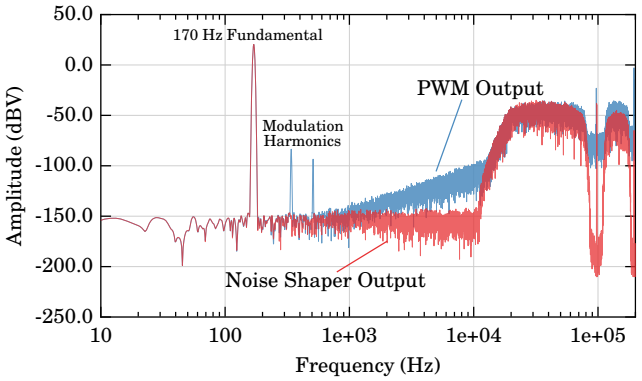

Fig. 17: Simulated amplitude spectra of the digital signal at the noise shaper output and the 1-bit switch signal from the PWM modulator's output. Rescaled in amplitude to match the fundamentals.

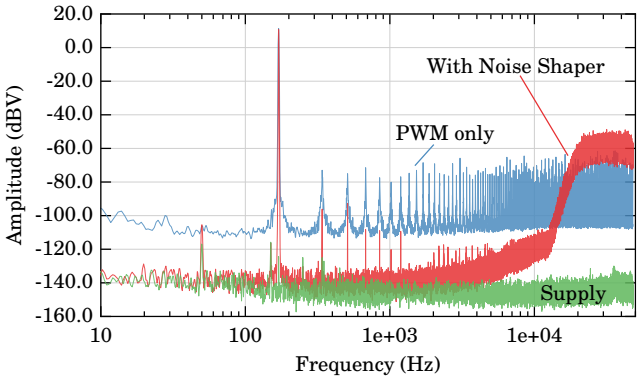

Fig. 18: Spectra obtained from a switched half-bridge output operated with and without the noise-coupled noise shaper (cf. **Fig. 15** and sec. III-E). The supply spectrum is measured at the input of the half-bridge.

In order to measure such low-noise signals, specialized equipment is required (*R&S UPV* Audio Analyzer). **Fig. 18** depicts the measurement of this noise shaper performed on the hardware demonstrator at the half-bridge output. If only a 9-bit PWM modulator would be used without noise shaping, the quantization noise would be significant and the SNR in the baseband from DC to 10 kHz would only be 65.8 dB. As expected from the simulation results, the noise shaper can increase this figure to 97 dB. There are, however, more harmonics in the noise-shaped spectrum than predicted by the simulations. This is due to the nonzero switching times of the power transistors, dead time and the non-ideal supply [13]. The THD of the noise-shaped signal is −102 dB (considering only the first two harmonics), which is a close match with the

simulation. Note that an RMS jitter of ≈26 ps is still present in the switched output waveform. This limits the best achievable SNR in the 10 kHz baseband to 106 dB (cf. eq. (2)), which is close to what is shown by the measurement.

In order to compare the measurement with the simulation, as the spectra are computed with different FFT windows and lengths, **Fig. 19** shows the power spectrum densities (PSD) of the measured signal and the simulation, which allows a direct comparison of the noise levels [6]. At frequencies from DC to ≈2 kHz, the noise floor of the measurement is higher than the simulation's due to the remaining RMS jitter of ≈26 ps at the half-bridge output. Otherwise, the measurement matches the simulation well which verifies the effectiveness of the noise shaper.

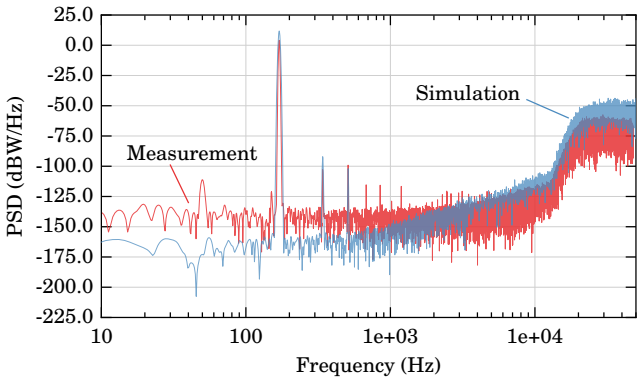

Fig. 19: Power spectrum densities of the measured half-bridge output and its computer simulation. Reference impedance: 1 Ω.

IV. Conclusion & Outlook

Two systems which allow the creation of high-SNR, low-noise, PWM modulated output signals for a switched-mode amplifier are presented. A special gate driver can significantly reduce jitter at the output of a 400 V GaN half-bridge from values of ≈250 ps to values under 30 ps while being immune to repeated common-mode transients in excess of 200 kV μs^{-1} across its isolation barrier.

A digital modulator based on noise shaping, which reduces quantization noise in a given frequency band through feedback action, can create high-SNR PWM signals which exceed the noise performance of traditional modulators. The quantization noise is shifted to higher frequencies, where it can be low-pass filtered and where it is of no concern to the mechatronic actuators. Using these techniques, open-loop half-bridge output voltage SNR figures of nearly 100 dB (DC-10 kHz) are achieved.

These results are obtained in an open-loop voltage output system. The overall distortion at the amplifier output (in both voltage and current) can be improved by employing feedback, which attenuates unwanted harmonics or noise. As an output current with an SNR in excess of 110 dB is desired by the industry, specialized low-noise and highly linear current sensors are required. Furthermore, in order to obtain a complete high-power, and low-noise mechatronic amplifier system, the supply of the power stage must provide an output of low noise and low parasitic series impedance in order to minimize distortion at the amplifier output [13].

References

[1] R. Munnig Schmidt, G. Schitter and J. van Eijk, *The Design of High Performance Mechatronics*. Delft University Press, 2011, ISBN: 978-1-60750-825-0.

[2] J.M. Schellekens, "A Class of Robust Switched-Mode Power Amplifiers with Highly Linear Transfer Characteristics," *PhD Thesis, University of Eindhoven*, 2014, ISBN: 978-94-6259-400-5.

[3] L. Risbo and T.Mørch, "Performance of an All-Digital Power Amplification System," in *Proc. of the 104th Audio Engineering Society Convention*, May 1998.

[4] W. Kester, *The Data Conversion Handbook*. Elsevier, 2005, ISBN: 0-7506-7841-0.

[5] W.B. Davenport, Jr., and W.L. Root, *An Introduction to the Theory of Random Signals and Noise*. McGraw-Hill, Lincoln Laboratory, Massachusetts Institute of Technology, 1958.

[6] G. Heinzel, A. Rüdiger and R. Schilling, "Spectrum and Spectral Density Estimation by the Discrete Fourier Transform (DFT), including a Comprehensive List of Window Functions and some New Flat-Top Windows," *Max-Planck-Institut für Gravitationsphysik*, 2002.

[7] M. Shimanouchi, "An Approach to Consistent Jitter Modeling for Various Jitter Aspects and Measurement Methods," in *Proc. of the International Test Conference*, 2001, pp. 848–857.

[8] M. Peng Li, *Jitter, Noise, and Signal Integrity at High-Speed*. Prentice Hall, 2007, ISBN: 978-0-13-242961-0.

[9] B. Kelleci, E. Sanchez-Sinencio and A.I. Karsilayan, "THD+Noise Estimation in Class-D Amplifiers," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2007, pp. 465–468.

[10] K. Gingerich and C. Sterzik, "The ISO72x Family of High-Speed Digital Isolators," January 2006, TI Application Report SLLA198.

[11] M.J. Hawksford, "Dynamic Jitter Filtering in High-Resolution DSM and PWM Digital-to-Analog Conversion," in *Proc. of the Audio Engineering Society Convention*, Feb 1994.

[12] M.A. Alexander, "PWM Re-Clocking Scheme to Reject Accumulated Asynchronous Jitter," June 2014, US Patent US8742841 B2.

[13] M. Mauerer, A. Tüysüz and J.W. Kolar, "Distortion Analysis of Low-THD/High-Bandwidth GaN/SiC Class-D Amplifier Power Stages," in *Proc. of the Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 2563–2571.

[14] Silicon Labs, "Si861x/2x Data Sheet," Rev. 1.6.

[15] Rohde&Schwarz, "Jitter Analysis with the R&S RTO Digital Oscilloscope." August 2013, Application Note 1TD03_2e.

[16] J.W. Kolar, J. Miniböck and M. Baumann, "Three-Phase PWM Power Conversion - The Route to Ultra High Power Density and Efficiency," in *Proc. of the CPES Annual Seminar/Industry Review*, April 2003.

[17] D.G. Holmes and T.A. Lipo, *Pulse Width Modulation for Power Converters - Principles and Practice*. Wiley-IEEE, 2003, ISBN: 978-0-471-20814-3.

[18] W.R. Bennett, "Spectra of Quantized Signals," in *Bell System Technical Journal*, 1948.

[19] *Xilinx LogiCORE IP Binary Counter v11.0 - DS215*, Xilinx, 2011.

[20] P. Craven, "Toward the 24-bit DAC: Novel Noise-Shaping Topologies Incorporating Correction for the Nonlinearity in a PWM Output Stage," *Journal of the Audio Engineering Society*, vol. 41, no. 5, pp. 291–313, 1993.

[21] J.M. Goldberg and M.B. Sandler, "Noise Shaping and Pulse-Width Modulation for an All-Digital Audio Power Amplifier," *Journal of the Audio Engineering Society*, vol. 39, no. 6, pp. 449–460, 1991.

[22] S. R. Norsworthy, R. Schreier and G.C. Temes, *Delta-Sigma Data Converters*. Wiley-IEEE, 1996, ISBN: 0-7803-1045-4.

[23] M. Norris, L.M. Platon, E. Alarcon and D. Maksimovic, "Quantization Noise Shaping in Digital PWM Converters," in *Proc. of the IEEE Power Electronics Specialists Conference (PESC)*, June 2008, pp. 127–133.

[24] R. Schreier and G.C. Temes, *Understanding Delta-Sigma Data Converters*. Wiley-IEEE, 2005, ISBN: 0-471-46582-2.

[25] K. Lee, M. Bonu and G.C. Temes, "Noise-coupled ΔΣ ADCs," *Electronics Letters*, vol. 42, no. 24, pp. 1381–1382, November 2006.

[26] M.O.J. Hawksford, "Dynamic Model-Based Linearization of Quantized Pulse-Width Modulation for Applications in Digital-to-Analog Conversion and Digital Power Amplifier Systems," *Journal of the Audio Engineering Society*, vol. 40, no. 4, pp. 235–252, 1992.