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Novel iGSE-C Loss Modelling of X7R Ceramic Capacitors

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***Abstract*—Due to the large relative permittivity of Class II dielectrics, ceramic capacitors from these materials promise significant volume and weight reductions in inverter and rectifier sine-wave filters, and are especially attractive in mobile applications that demand ultra-high power density. While previous literature found large low-frequency losses in these components, no extensible loss model was proposed to accurately characterize these ferroelectric losses. In this work, we take advantage of prior art on ferro*magnetic* components in power electronics to propose a Steinmetz parameter-based loss modelling approach for X7R ceramic capacitors, named the Improved Generalized Steinmetz Equation for ceramic Capacitors, or iGSE-C. This model is verified using the Sawyer-Tower circuit to measure losses in a commercially-available X7R capacitor across excitation magnitude, DC bias, temperature, excitation frequency, and harmonic injection. Losses are shown to scale according to a power law with charge, with the resulting Steinmetz coefficients valid across DC bias and slightly varying as the temperature is increased. The iGSE-C accurately predicts losses for typical non-sinusoidal phase voltage waveforms with an error under $8\,\%$.**

Finally, the loss modeling technique is demonstrated for the sine-wave output filter of a bridge-leg arrangement with both low- and high-frequency excitations, with total capacitor losses predicted within $12\,\%$ accuracy.

***Index Terms*—DC-AC power converters, AC-DC power converters, inverters, rectifiers, power capacitors, ceramic capacitors, large-signal excitation, Steinmetz loss modeling, iGSE, iGSE-C.**

I. Introduction

In the push towards ultra-compact power converters for emerging applications, including electric vehicles and more-electric aircraft, electromagnetic interference (EMI) filter volume and weight represent a key bottleneck to ever-higher volumetric and gravimetric power density. In switched-mode converters, these filters are unavoidable to protect the mains from high-frequency conducted emissions and to comply with the relevant harmonic standards, and a path towards both miniaturization and weight reduction is sought.

For the sine-wave filters of, e.g., three-phase rectifiers or motor drive systems with low high-frequency stresses (to reduce bearing currents and/or increase feasible cable lengths), a variety of filtering techniques – both Common Mode (CM) and Differential Mode (DM) – are employed to filter switching harmonics while passing the fundamental frequency, as shown in **Fig. 1**. Due to their low cost and high quality factor [1], film capacitors are predominantly used in these applications, comprising approximately $50\,\%$ of the overall filter volume [2].

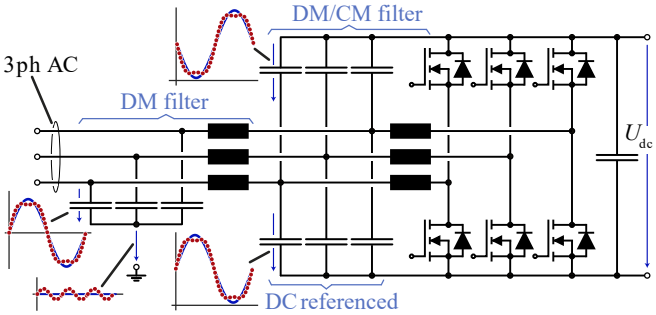

Fig. 1. Illustration of a common sine-wave filter structure for a three-phase inverter or PFC rectifier: open-star-point DM filter and combined DM/CM DC-link referenced filter. The resulting low-frequency voltage waveforms across the filter capacitors for standard sinusoidal PWM operation with constant DC offset (solid line) and with additional $1/6$ 3^{rd} harmonic injection [3] (dotted line) for maximum utilization of the linear modulation range are shown.

To reduce the filter volume and weight in applications highly sensitive to power density, Ceramic Capacitors (CCs) are an attractive replacement for film capacitors [4]. For a $1\,\text{kV}$, $470\,\text{nF}$ capacitor, the volume can be reduced by over $75\times$ by moving from an off-the-shelf film capacitor (metallized polypropylene, KEMET PHE844RD6470MR30L2) to an off-the-shelf CC (X7R, Knowles Syfer 2220Y1K00474KETWS2), as shown in **Table I**. With this one-for-one replacement, the capacitor contribution to the filter volume becomes negligible, allowing the inductor size to be increased (reducing losses and improving efficiency) and/or a reduction in overall converter size and weight. As such, CCs are the preferred capacitor technology for ultra-compact converters, including those built for the Google Little Box Challenge [5,6] and/or for any application, where the benefits of compactness outweigh the cost increase of the ceramic replacement (costs given in **Table I**).

In particular, X7R CCs have extremely high capacitance and energy density [1], originating from the large relative permittivity of ferroelectric Class II dielectrics [7]. X7R capacitors have excellent properties in the high-frequency range for filtering switching harmonics, with a constant capacitance value over a wide frequency range, low Effective Series Resistance (ESR), and a compact geometry that enables a low-inductance realization with a high self-resonant frequency (see the small-signal impedance measurements

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TABLE I
COMPARISON OF A FILM AND A CERAMIC CAPACITOR

Dielectric	V_n	C_n	Volume	Price
Film (PP)	1 kV	470 nF	9.87 cm^3	1.94 $
Ceramic (X7R)	1 kV	470 nF	0.13 cm^3	6.69 $

of the 2220Y1K00474KETWS2 capacitor in **Fig. 2a-c**). With increasing voltage bias, however, X7R CCs exhibit (similar to magnetic components) dielectric saturation [8] and a decrease in capacitance, as measured in **Fig. 2d**, well-known in the literature (e.g. [9]), and reported in capacitor datasheets.

In the context of line-frequency filtering, the effective capacitance is then highly dependent on the low-frequency voltage waveforms, and therefore on the filter configuration itself. To highlight these voltage waveforms, **Fig. 1** shows both a combined DM/CM DC-link referenced LC-filter, which was proposed in [10] specifically to reduce the capacitance variation in a line cycle, and a pure DM filter structure. In motor drive applications, alternative modulation schemes employed to expand the modulation range and/or to decrease semiconductor losses [11] introduce additional harmonics (e.g. 3rd harmonic injection [3] or Discontinuous Pulse Width Modulation (DPWM) [12]), which further impacts the voltages applied to the filter capacitors. **Fig. 1** accordingly includes the resulting low-frequency capacitor voltages for both standard sinusoidal modulation and additional 3rd harmonic injection. Lastly, the filter capacitors connected to the DC-link rails in **Fig. 1** also face the triangular switching-frequency currents of the power inductors, causing a voltage variation and losses on a switching frequency level. Further, high-frequency stresses are possible in alternative topologies such as the three-phase Y-inverter [13], where the filter capacitors are subject to both low-frequency voltage waveforms with a DC offset and rectangular switching-frequency currents.

Recent work has found an elevated dissipation factor in CCs operating at low frequencies that is highly dependent on both DC bias and the large-signal excitation frequency and waveshape [14,15]. These unexpectedly-high losses – as high as $10\,\mathrm{W/cm^3}$ at 120 Hz [14] – cannot be predicted from the small-signal measurement data provided by manufacturers (in the datasheet or with online tools), and indeed Ref. [16] describes that small-signal measurements are fundamentally insufficient to characterize a ferroelectric capacitor. Within the context of elevated large-signal excitation losses, the compactness of CCs becomes a double-edged sword: although the loss contribution of CCs in a converter system may still be relatively small, substantial capacitor heating can result, eventually limiting, for example, the maximum fundamental frequency (and hence speed) for a motor drive system. In light of these unmodeled and substantial large-signal losses, we desire a method – extensible across voltage waveshape – to measure, characterize, and predict these losses in CCs.

For *magnetic* components, which also exhibit loss mechanisms that must be characterized under large-signal conditions, Steinmetz parameters [17] are commonly provided to

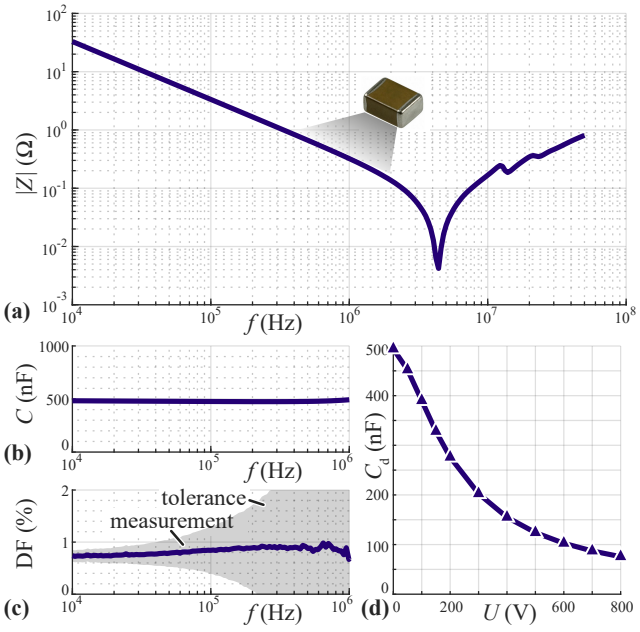

Fig. 2. Small-signal measurements of **(a)** impedance, **(b)** capacitance, and **(c)** dissipation factor of the 1 kV, 470 nF, X7R Ceramic Capacitor (CC) under test (Knowles Syfer 2220Y1K00474KETWS2) at room temperature (25 °C) and with 0.5 $\mathrm{V_{rms}}$ AC excitation. Self-resonance occurs at 4.4 MHz. The small-signal capacitance dependence on voltage is shown in **(d)**, where an AC excitation of 5 $\mathrm{V_{rms}}$ with 100 Hz was applied on top of the reported DC bias voltage U.

allow engineers to calculate core losses under a particular operating condition. In contrast, Refs. [14,15] only provide loss look-up tables for the reported CCs under a sine-wave excitation at a few frequencies and a multitude of DC bias points, leaving extensibility across DC voltage, AC waveshape, frequency, and part number unanswered. The current state of the art, then, requires additional measurements to design CC filters with losses that can be predicted *a priori* (excluding the coincidence when the filter capacitor, frequency, and selected part all exactly align with a reported measurement point).

Given these shortcomings and the attractiveness of CCs for converters with high power density, there is a clear need for a loss model for ferroelectric capacitors in power electronics. In this work, we propose a Steinmetz-based loss modeling approach for CCs under large-signal excitation, called the Improved Generalized Steinmetz Equation for ceramic Capacitors (iGSE-C), in **Section II**, which is verified with the measurement technique of **Section III** on a commercially-available ferroelectric capacitor in **Section IV**. This particular capacitor, or the Device Under Test (DUT), is the 1 kV, 470 nF X7R CC of **Table II**, which was employed in a hardware prototype for an ultra-compact industrial motor drive with large observed low-frequency excitation losses. Low-frequency losses are characterized across excitation magnitude, DC bias, temperature, and 3rd harmonic content. Next, high-frequency losses are added for a complete picture of X7R CC losses in switched-mode power converters, which is validated in **Section V** with straightforward and extensible design guidelines for loss prediction *in situ* based on the iGSE-C. **Section VI** summarizes the key findings and the

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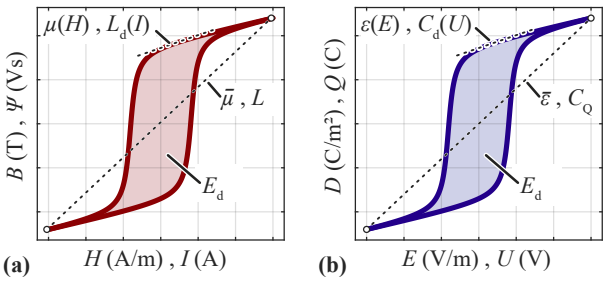

Fig. 3. Illustration of a **(a)** ferro*magnetic* and **(b)** ferroelectric hysteresis loop, with instantaneous (L_d, C_d) inductances and capacitances highlighted separately from average large-signal values (L, C_Q).

proposed iGSE-C model, and **Appendix A** surveys alternative calorimetric-based loss measurement techniques.

II. Modelling Approach

For adoption and adaptability, the ferroelectric capacitor loss modeling approach must be extensible across voltage waveshape, excitation magnitude, and DC bias. A Steinmetz-based capacitor loss model is developed analogously to the well-known large-signal approach for ferro*magnetic* components, and we first review the conventional [17] and Improved General [18] Steinmetz Equations for inductors to ground the proposed model.

A ferromagnetic hysteresis loop is shown in **Fig. 3a**, where the magnetic field strength H (or current I) and flux density B (or flux linkage, Ψ, given by the time integral of the excitation voltage U) are linked by the permeability $\mu(H)$ (or differential inductance $L_\mathrm{d}(I)$) as:

$$L_\mathrm{d}(I) = \frac{U}{dI/dt} = \frac{d\Psi}{dI}, \quad \mu(H) = \frac{dB}{dH}. \tag{1}$$

For a given hysteresis curve, both the average permeability $\overline{\mu}$ (or large-signal inductance L) and instantaneous permeability $\mu(H)$ can be calculated, and these are shown on **Fig. 3a** as the appropriate slopes. The enclosed area E_d represents the energy dissipated in a single charge-discharge cycle, where hysteresis (caused by irreversible magnetization), eddy current, and residual losses are the main underlying loss mechanisms [19].

The time-averaged losses P of magnetic materials under a sinusoidal flux excitation depend on both frequency f and the peak magnetic flux density, B_pk, and empirically follows the power law given by the familiar Steinmetz Equation (SE) [17]:

$$P = k \cdot f^\alpha \cdot B_\mathrm{pk}^\beta, \tag{2}$$

where k, α, and β are material-specific constants characterized under large-signal excitation (note that f^α was not in the original equation, but was added later and is now standard [18]).

For a non-sinusoidal excitation – the condition in most power converters – a number of loss-modeling methods have been proposed. The Improved Generalized Steinmetz Equation (iGSE) [18] is the most established method, and one with parameters directly extractable from the given Steinmetz parameters. The losses are assumed to depend both on the peak-to-peak flux density ΔB and the flux density change rate dB/dt within a period T, as:

$$P = k_\mathrm{i} \cdot \Delta B^{\beta-\alpha} \cdot \frac{1}{T}\int_0^T \left|\frac{dB}{dt}\right|^\alpha dt, \tag{3}$$

with the coefficient k_i derived from the SE parameters as:

$$k_\mathrm{i} = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^\alpha 2^{\beta-\alpha} d\theta}. \tag{4}$$

If multiple minor hysteresis loops occur within a single period T, (3) is summed for each loop j separately to find average core losses as:

$$P_\mathrm{avg} = \sum_j P_j \frac{T_j}{T}. \tag{5}$$

With the SE and iGSE well-established for magnetic materials, we seek to develop an analogous loss modeling method for ferroelectric capacitors, including the ceramic components highlighted here. **Fig. 3b** shows a ferroelectric hysteresis loop, where the electric field strength E (or voltage U) and displacement field D (or charge Q) are linked by the permittivity $\varepsilon(E)$ (or differential capacitance $C_\mathrm{d}(U)$) as:

$$C_\mathrm{d}(U) = \frac{I}{dU/dt} = \frac{dQ}{dU}, \quad \varepsilon(E) = \frac{dD}{dE}. \tag{6}$$

For a given hysteresis curve, both the average permittivity $\overline{\varepsilon}$ (or charge-equivalent capacitance C_Q) [20] and instantaneous permittivity $\varepsilon(E)$ can be calculated, and these are shown in **Fig. 3b** as the appropriate slopes. Again, the area enclosed by the loop E_d represents the energy dissipated in a single charge-discharge cycle. In [21], a summary of capacitor losses mechanisms is provided, where ferroelectric Class II CCs hysteresis losses result (similar to the hysteresis losses in magnetics) due to irreversible polarization processes [22,23].

Ref. [24] proposed a Steinmetz power law to model ferroelectric capacitor losses under small-signal excitation with a fit on the peak sinusoidal voltage, $\hat{U}$. The same voltage-based Steinmetz template was used for losses in semiconductor output capacitance in [25,26], where multiple sets of Steinmetz parameters were required to accurately describe the losses over the excitation voltage range. With the curve of **Fig. 3b**, however, we see that a power law fit on excitation voltage (or field strength E) cannot hold in a ferroelectric capacitor due to the charge saturation with increasing voltage magnitude. Steinmetz also worked on dielectric hysteresis and expected, based on theoretical considerations only, the losses to scale with $P = kfD_\mathrm{pk}^2$ for a peak charge density excitation D_pk [27]. In contrast to magnetic materials, the field quantity D of commercial CCs cannot be easily calculated, as the internal structure, and therefore the effective amount of dielectric material and electrode area per device volume, is not known (cf. **Fig. 4**). However, the charge Q *can* be measured without in-depth knowledge of the exact CC realization.

Therefore, and in analogy with the ferromagnetic SE of (2), we propose to describe the losses in ferroelectric

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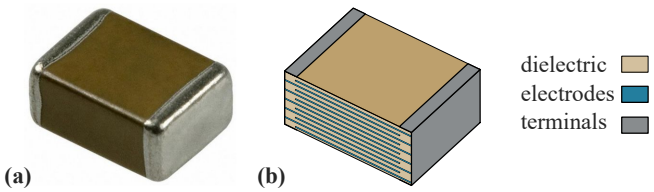

Fig. 4. (a) Picture of the 1 kV, 470 nF, X7R Ceramic Capacitor (CC) under test (Knowles Syfer 2220Y1K00474KETWS2) and **(b)** illustration of the internal structure of a CC consisting of several electrode and dielectric layers. The resulting capacitance value depends on the employed dielectric and the number, arrangement, and thickness of the electrodes [9]. These parameters are not known for commercial devices.

capacitors with a *peak charge based* (Q_{pk}) SE as:

$$P = k \cdot f^{\alpha} \cdot Q_{\mathrm{pk}}^{\beta}, \tag{7}$$

where k, α, and β are to be fitted under large-signal excitation. We note that SE parameters found for one CC cannot directly be employed for another product (even when the same dielectric is employed), as the charge density D is not known. However, in future datasheets, device manufacturers could provide the SE parameters of the employed dielectric and the dielectric volume density for each product to support loss calculations.

For non-sinusoidal excitations, an iGSE approach could again be applied, where for a peak-to-peak charge ΔQ the losses can be described:

$$P = k_{\mathrm{i}} \cdot \Delta Q^{\beta-\alpha} \cdot \frac{1}{T} \int_0^T \left|\frac{dQ}{dt}\right|^{\alpha} dt \tag{8}$$

and k_{i} is again given by the SE parameters and (4), where (8) collapses to (7) in the case of a sinusoidal excitation. This proposed loss model is named the Improved Generalized Steinmetz Equation for ceramic Capacitors, or the iGSE-C.

III. Measurement Method and Setup

With a modelling approach proposed, we turn to characterizing the losses in the selected X7R CC of **Table II.** Firstly, a measurement method must be selected that can evaluate the known loss dependencies outlined in **Section I** of:

- Large-signal excitation (sinusoidal and non-sinusoidal),
- DC bias,
- Frequency,
- High-frequency currents, and
- Temperature.

Ideally, this measurement method produces rapid measurements that can be applied to transient conditions, can measure losses at constant temperature, is applicable across a wide frequency range, and is valid with non-sinuosoidal waveforms. We briefly survey potential electric and calorimetric methods.

A. Potential Measurement Techniques

Voltage-Current Electric Measurement: A voltage-current electric measurement that measures instantaneous power with a voltage and current probe is one candidate for loss characterization. This method fulfills the need for fast, quasi-pulse measurements in a time period that avoids a substantial increase of the DUT temperature, and Ref. [14] used a Yokogawa WT3000 power analyzer to measure the losses in two ferroelectric capacitors under 120 Hz large-signal excitation. Ref. [15] used a similar measurement approach to validate a calorimetric measurement and calculate volumetric energy storage at low frequencies.

This direct measurement method introduces a number of challenges, however. For a high-quality factor CCs, avoiding a phase error between the voltage and current probes is paramount and, unfortunately, difficult to maintain across excitation frequency and when non-sinusoidal waveforms are applied. To overcome this problematic calibration step, currents could be measured with a precision shunt and a voltage probe to simplify phase matching. With the current of a capacitor scaling linearly with frequency (for a constant voltage), however, a large number of shunts would be required to achieve a good signal-to-noise ratio for a frequency range of several orders of magnitude.

Sawyer-Tower (ST) Electric Measurement: The ST method was introduced in 1930 [28] to evaluate Rochelle salt as a dielectric, and operates by adding a well-characterized, low-loss reference capacitor in series with the DUT to calculate the charge in the DUT. This method has been employed in various power electronics applications, including to characterize capacitors for microprocessor applications [29] and to measure soft-switching losses (up to the MHz frequency range) in silicon superjunction MOSFETs [25], SiC MOSFETs [30], and GaN-on-Si HEMTs [26]. For semiconductor-specific measurements, the ST circuit was improved and simplified in [31].

The ST measurements are conducted with passive voltage probes, and with the voltage ratio between the DUT and the reference capacitor constant over frequency, a single ST setup can be used to cover the whole frequency range of interest.

Calorimetric Measurements: Calorimetric measurement techniques achieve excellent accuracy independent of frequency and the ratio of reactive to active power, and have been used to characterize capacitor losses [15,32,33]. **Appendix A** surveys three calorimetric measurement types (*(a)* steady-state, *(b)* indirect transient, and *(c)* direct transient), finding that none are attractive for the application, due to the temperature dependence of the losses of CCs for *(a)*, the slow speed of calorimetric measurements for *(b)* , and the lack of a known loss calibration point in a capacitor in case of *(c)*.

Therefore, with the ease of calibration, extensibility across waveforms, and transient measurement capability, the ST method is the preferred candidate for this measurement suite, and the circuit operation is covered in detail below.

B. Sawyer-Tower Measurement

The ST circuit is shown in **Fig. 5a**, with both the voltage across the linear reference capacitor C_{ref} (u_{ref}) and the excitation voltage u_{ac} measured. Depending on the position of the mechanical switch, either the lossy and non-linear DUT or the calibration capacitor C_{cal} is measured, where C_{cal} is ideally linear and lossless and serves to calibrate the ST setup. The component selection for the realization of C_{ref} and C_{cal} is discussed in further detail at the end

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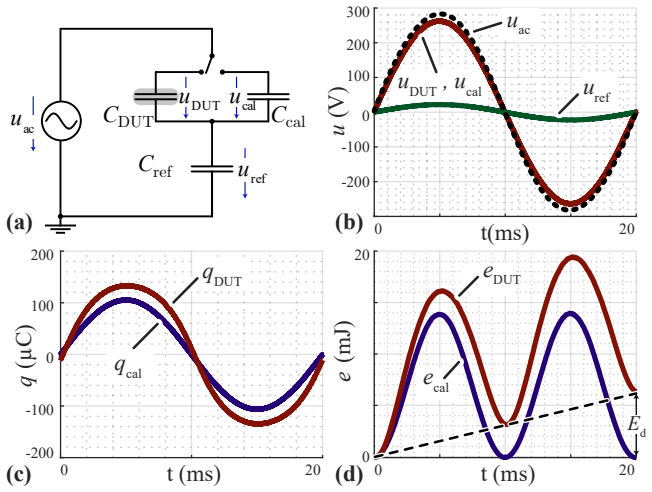

Fig. 5. **(a)** Schematic circuit of the employed Sawyer-Tower measurement setup (either the DUT or a calibration capacitor is connected in series to the reference capacitor) for AC voltage excitation. Resulting time domain waveforms for the ST measurement: **(b)** voltage, **(c)** calculated charge, and **(d)** calculated stored energy. For the lossless calibration capacitor, the stored energy e_{cal} is fully recovered within an AC period, giving identical initial and final energy. For the lossy DUT, however, some portion of the stored energy is dissipated, yielding a final e_{DUT} larger than the initial e_{DUT} (the distance of which is represented by E_{d}).

of this section, where non-ferroelectric C0G capacitors with a 20 x-30 x lower Dissipation Factor (DF) than the class II ferroelectric CCs of interest are employed (cf. **Table II**).

The measured voltage waveforms are shown for operation with both C_{cal} and C_{DUT} in **Fig. 5b**, and the component values according to **Table II.** With the charge q (c.f. **Fig. 5c**) in series capacitors equal, we can write (note that the following loss equation is derived for the DUT, but the same equations and procedure apply for the calibration capacitor C_{cal}):

$$u_{\mathrm{DUT}}(t) = u_{\mathrm{ac}}(t) - u_{\mathrm{ref}}(t) \tag{9}$$

$$q_{\mathrm{DUT}}(t) = q_{\mathrm{ref}}(t) = u_{\mathrm{ref}}(t) \cdot C_{\mathrm{ref}}. \tag{10}$$

With C_{ref} selected as much higher capacitance than C_{DUT} or C_{cal}, only a small fraction of the applied voltage u_{ac} appears across it (cf. **Fig. 5b**).

Integrating the instantaneous power, the energy stored in the non-linear DUT (cf. **Fig. 5d**) can be calculated using the calculated charge q_{DUT} (10) as:

$$e_{\mathrm{DUT}}(t) = \int_0^t u_{\mathrm{DUT}}(\tau) \cdot i_{\mathrm{DUT}}(\tau) d\tau$$

$$= \int_0^t u_{\mathrm{DUT}}(\tau) \cdot \frac{dq_{\mathrm{DUT}}}{d\tau} d\tau = \int_{q_{\mathrm{DUT}}(0)}^{q_{\mathrm{DUT}}(t)} u_{\mathrm{DUT}} dq_{\mathrm{DUT}}. \tag{11}$$

For a signal periodic with T (i.e. $u_{\mathrm{DUT}}(0) = u_{\mathrm{DUT}}(T)$ and $q_{\mathrm{DUT}}(0) = q_{\mathrm{DUT}}(T)$) and starting with the global charge minima $q_{\mathrm{DUT}}(0) = q_{\mathrm{min}}$, the dissipated energy E_{d} (i.e. the area enclosed by the U-Q hysteresis loop in **Fig. 3b**) of one cycle can be calculated, which yields the active power:

$$P = \frac{E_{\mathrm{d}}}{T} = \frac{1}{T}\Bigg(\underbrace{\int_{q_{\mathrm{DUT}}(0)}^{q_{\mathrm{DUT}}(T/2)} u_{\mathrm{DUT}} dq_{\mathrm{DUT}}}_{\text{charge}} + \underbrace{\int_{q_{\mathrm{DUT}}(T/2)}^{q_{\mathrm{DUT}}(T)} u_{\mathrm{DUT}} dq_{\mathrm{DUT}}}_{\text{discharge}} \Bigg) \tag{12}$$

E_{d} is highlighted in **Fig. 5d** for the DUT, which stands in contrast to the calibration capacitor (in the same figure) where all of the stored energy is recovered. The dissipation factor is defined by the ratio of dissipated E_{d} and stored E_{stored} energy

$$DF = \frac{E_{\mathrm{d}}}{2\pi \cdot E_{\mathrm{stored}}}, \tag{13}$$

and is a good measure for the loss-rate of non-linear CCs. For a linear capacitor (or a non-linear capacitor with small-signal excitation), the DF is identical to the the loss tangent $\tan(\delta)$ (i.e. the ratio of active and reactive power).

When C_{cal} is measured, two linear capacitors are excited by the sinusoidal voltage u_{ac}, resulting in the sinusoidal charge waveform q_{cal} of **Fig. 5c**. The non-linearity of C_{DUT}, however, causes the charge waveform q_{DUT} not to be purely sinusoidal, shown for contrast in **Fig. 5c**.

The selection of C_{ref} is critical for the accuracy of the ST measurements, and we highlight the key characteristics here. Firstly, C_{ref} takes a certain fraction of the applied AC voltage, which should be kept relatively small, such that the DUT sees the majority of the excitation voltage U_{ac}. This can be achieved with $C_{\mathrm{ref}} >> C_{\mathrm{DUT}}$, where a reasonable choice might be $C_{\mathrm{ref}} \approx 10 \cdot C_{\mathrm{DUT}}$. Secondly, if the DUT and the reference capacitor show the same loss tangent, the two measured voltages (u_{ac} and u_{ref}) will be in phase, resulting in no measured $U - Q$ hysteresis and zero measured losses. The reference capacitor, therefore, must have substantially lower $\tan\delta$ than the DUT. Lastly, the ST is fundamentally reliant on the linearity of C_{ref} to calculate the charge from voltage (see (10)), and the reference capacitors should be highly linear, i.e. a ferroelectric Class II capacitor should not be used for C_{ref}.

In light of these requirements, C_{ref} and the calibration capacitors C_{cal} are realized with low-loss, Class I C0G capacitors with extremely stable dielectrics. The key properties are summarized in **Table II,** with the DF of C_{ref} and C_{cal} at least an order of magnitude below the DUT (which was directly measured under small-signal conditions in **Fig. 2c**). For the C0G reference and calibration capacitors, the small-signal DF accurately approximates the large-signal DF, and the impact of the small-but-non-zero DF of C_{ref} is neglected in the following loss measurements.

With this simple and extensible technique, losses in ferroelectric capacitors can be characterized across voltage, temperature, waveform shape, DC bias, and frequency, and we move to validate the proposed loss model of **Section II** with measurements on the selected DUT.

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TABLE II
EMPLOYED COMPONENTS

Component	Dielectric	Manufacturer	Part Number	V_n	C_n	N(parallel)	C_{tot}	DF
C_{cal}	C0G	TDK	CAA572C0G2J204J640LH	650 V	200 nF	2	400 nF	$< 0.02\,\%$
C_{ref}	C0G	TDK	C5750C0G2A154J230KE	100 V	150 nF	32	4.8 µF	$< 0.03\,\%$
C_{DUT}	X7R	Knowles Syfer	2220Y1K00474KETWS2	1 kV	470 nF	1	470 nF	$> 0.71\,\%$

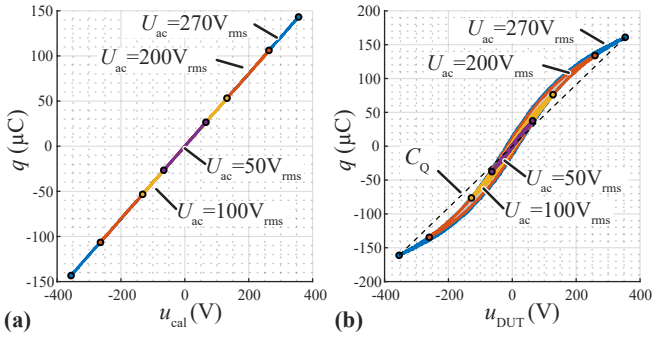

Fig. 6. $U-Q$ hysteresis recorded at 50 Hz for a range of excitation voltages for **(a)** the calibration capacitor, which shows no hysteresis and has a constant $C_Q = C_d$ at all voltages, and **(b)** the DUT, which exhibits increasing hysteresis and losses with increasing excitation voltage. C_Q highlighted for $U_{ac} = 270\,V_{rms}$. Measured $U-Q$ curves are identical at 50 Hz and 100 Hz.

IV. EXPERIMENTAL RESULTS

A sinusoidal AC excitation is applied to the circuit of **Fig. 5a** with an AC power source ($U_{ac,max} = 270\,V_{rms}$), with the initial calibration measurements shown at 50 Hz for a range of excitation voltages in **Fig. 6**.

With the calibration C0G capacitor (**Fig. 6a**), the capacitance is linear for all magnitudes, resulting in a constant C_Q across voltage and $C_Q = C_d$. There is no measurable hysteresis between the charging and discharging curves at a given voltage, resulting in negligible losses that are verified with no heating of C_{cal} during the test procedure. This "zero-loss" reading also validates a proper deskew of the voltage probes.

For the same excitation voltages at 50 Hz, **Fig. 6b** shows the measured ferroelectric $U_{DUT} - Q$ hysteresis curves for the X7R DUT capacitor. At $50\,V_{rms}$, the capacitor is approximately linear ($C_Q \approx C_d$), but clearly starts saturating for higher excitation amplitude. C_Q changes across applied voltage, and C_d deviates from C_Q at different voltages along the $U_{DUT} - Q$ curve. With an increasing voltage, further, the hysteresis area between the charging and discharging curves expands (especially near the zero-crossing, as we return to later), indicating an increase in losses with excitation voltage.

Even at the line frequency of 50 Hz, these hysteretic losses total as high as 0.5 W per DUT capacitor, and the large-signal DF is nearly an order-of-magnitude higher than the small-signal DF measured in **Fig. 2c**. These significant losses, validated by [14,15], justify a deeper investigation of the key loss drivers, and we evaluate the impact of frequency and excitation magnitude based on the proposed SE (**Section IV-A**), harmonic injection based on the proposed iGSE-C (**Section IV-B**), DC bias (**Section IV-C**), temperature (**Section IV-D**), and, finally, the impact of the high-frequency excitations necessarily imposed by the switching frequency current ripple of the inductors connected to the half-bridge switched nodes in **Fig. 1** (**Section IV-E**).

A. Impact of AC Excitation Magnitude and Frequency

The impact of low-frequency excitation voltage and frequency are evaluated from, respectively, $50\,V_{rms} - 250\,V_{rms}$ and $50\,Hz - 250\,Hz$. These measurements are recorded at room temperature (25 °C) with a measurement time of 1 s to avoid self-heating of C_{DUT} and to isolate any impact of temperature on the losses. The impact of temperature is investigated later in **Section IV-D**, where we find that self-heating of up to 10 °C changes the losses by no more than ≈5 % for the operating points considered here.

The measured losses are shown in **Fig. 7**. Firstly, we note the measured DF exceeds 7.0 % under certain operating conditions, far above the 0.7 % predicted by the small-signal characterization of **Fig. 2c** and resulting in losses as large as 2 W. **Fig. 7a.i-c.i** highlights the impact across frequency, and we find a linear scaling of losses with f, supporting the finding of $\alpha = 1$ from [24] for the SE of (7). C_Q and DF do not vary across this frequency range (with the slight measured deviations attributed to measurement error and heating of the DUT). This linear loss-frequency relationship (and the identical $U-Q$ hysteresis curves across frequency) are supported by the stable capacitance value of the DUT across frequency, as observed under both small-signal (**Fig. 2a-b**) and large-signal (**Fig. 7b.i**) conditions. Therefore, when increasing the frequency for a given excitation amplitude, the same ferroelectric hysteresis curve (cf. **Fig. 6**) is traversed more often, dissipating a constant amount of energy per cycle and accordingly resulting in a linearly-increasing power.

Across varying excitation voltage (highlighted in **Fig. 7a.ii-c.ii**), however, we observe significant deviations from the expected behavior of the X7R DUT capacitor. At low excitation voltage, DF approaches the small-signal value (0.7 %), increases up to 7.0 % at $100\,V_{rms}$, then saturates and even slightly decreases as the magnitude is further increased (**Fig. 7c.ii**). This voltage-dependent trend follows the other surprising finding that C_Q *increases* up to $100\,V_{rms}$ (**Fig. 7b.ii**) – for all X7R capacitors, we expect the capacitance to steadily *decrease* with voltage, as shown by the calculated charge-equivalent capacitance derived from the small-signal measurements of **Fig. 2d** (dotted line in **Fig. 7b.ii**). The peak capacitance is over 600 nF, more than 20 % greater than the measured value at zero DC bias. This effect of increasing capacitance with AC magnitude is also described in Ref. [9].

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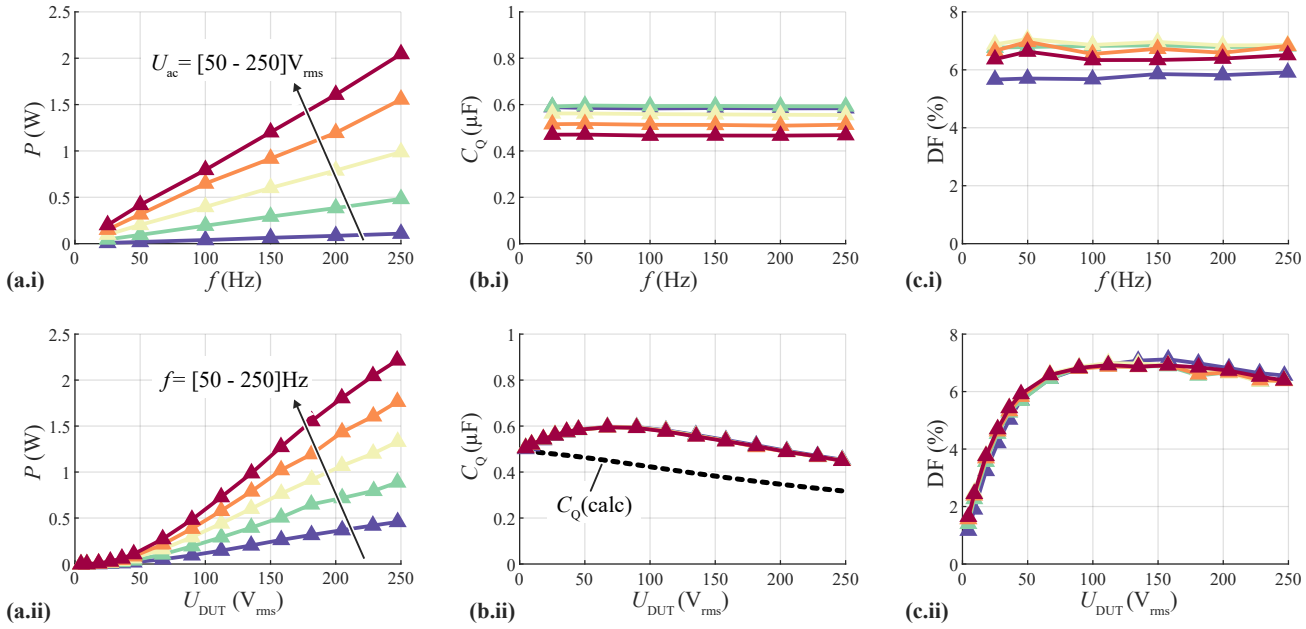

Fig. 7. Measured losses in the X7R CCs DUT using the Sawyer-Tower circuit of **Fig. 5a** across AC excitation voltage and AC excitation frequency. Dissipation factor is nearly an order-of-magnitude larger than expected from the small-signal measurements (**Fig. 2c**) and capacitance *increases* up to $U_{\mathrm{DUT}} = 100\,\mathrm{V_{rms}}$. Losses linearly increase with frequency equivalent to an SE parameter of $\alpha = 1$. **(a)** Losses P, **(b)** AC charge equivalent capacitance C_{Q} (the expected value $C_{\mathrm{Q}}(\mathrm{calc})$ derived from **Fig. 2d** is represented by the dashed line, and in **(b.ii)** all capacitance curves are overlapping), and **(c)** dissipation factor DF, plotted against **(i)** frequency and **(ii)** DUT voltage rms value.

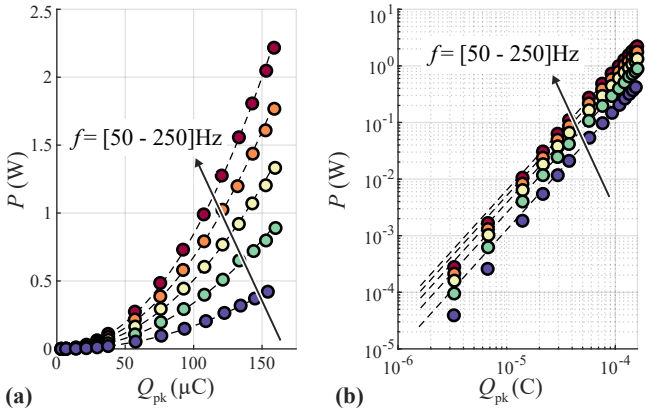

Fig. 8. Measured losses, from **Fig. 7**, plotted against measured charge Q_{pk} for AC frequencies from $50\,\mathrm{Hz} - 250\,\mathrm{Hz}$ and AC voltages from $50\,\mathrm{V_{rms}} - 250\,\mathrm{V_{rms}}$. Dotted lines are derived Steinmetz parameters ($k = 1.06 \cdot 10^6, \alpha = 1$, and $\beta = 2.12$) in (7), which show excellent agreement with the measured data. **(a)** Linear representation and **(b)** logarithmic representation.

The additional capacitance indicates a large-signal polarization mechanism around the voltage zero-crossing that is not captured by measurements with small AC magnitudes. While this phenomenon is investigated more in **Section IV-C**, we note here that the extra capacitance is undesired for filtering. The fundamental reactive currents in the capacitor are $I_{\mathrm{Q}} = 2\pi f C_{\mathrm{Q}} U_{\mathrm{DUT}}$, so a larger C_{Q} large-signal capacitance maps to increased conduction losses in the inductors and semiconductors of the converter while the capacitance available for switching-frequency filtering remains limited to the appropriate small-signal value of **Fig. 2d**.

Finally, we return to the proposed charge-based SE modeling to evaluate whether the measured losses are appropriately captured by (7). In **Fig. 8**, the measured losses are scattered against the measured charge excitation amplitude of $Q_{\mathrm{pk}} = C_{\mathrm{ref}} \cdot U_{\mathrm{ref,pk}}$ (cf. (10)) on both linear (**Fig. 8a**) and logarithmic (**Fig. 8b**) scales. Steinmetz parameters are fit from the measured data and plotted using (7) as dotted lines on both scales, with selected values of $k = 1.06 \cdot 10^6, \alpha = 1$, and $\beta = 2.12$. This fitting matches the measured data extremely well, with discrepancies only at very low excitation magnitudes where the measurement precision is low (losses in the $10\,\mu\mathrm{W}$ range), strongly supporting the proposed charge-based SE modeling approach. We note that a voltage-based power law relationship (proposed in [24] for small-signal excitation) cannot accurately capture the measured losses, as the losses have two distinct scaling regions with voltage (exponential below $50\,\mathrm{V_{rms}}$, linear above $50\,\mathrm{V_{rms}}$) that are clearly seen in **Fig. 7a.ii**.

Our characterization of losses across voltage magnitude and frequency confirm the proposed SE fitting, finding a strong dependence of losses on peak charge (more than quadratic, with $\beta = 2.12$) and a large-signal polarization near the zero-crossing that increases both converter conduction losses and the losses in the capacitor itself. With the charge-based SE approach confirmed, we next add superimposed harmonics to evaluate the iGSE-C extension of ferroelectric capacitor losses.

B. Impact of Harmonic Injection and iGSE Modelling

Generally, the modelling approach must be valid for non-sinusoidal waveforms. For filter capacitors in motor drive inverter or three-phase PFC rectifier applications, in particular, the 3rd harmonic (and its multiples) of the fundamental frequency is often used to extend the modulation range of the PWM scheme [11]. In the proposal of the iGSE loss modeling approach for magnetic materials [18], the method

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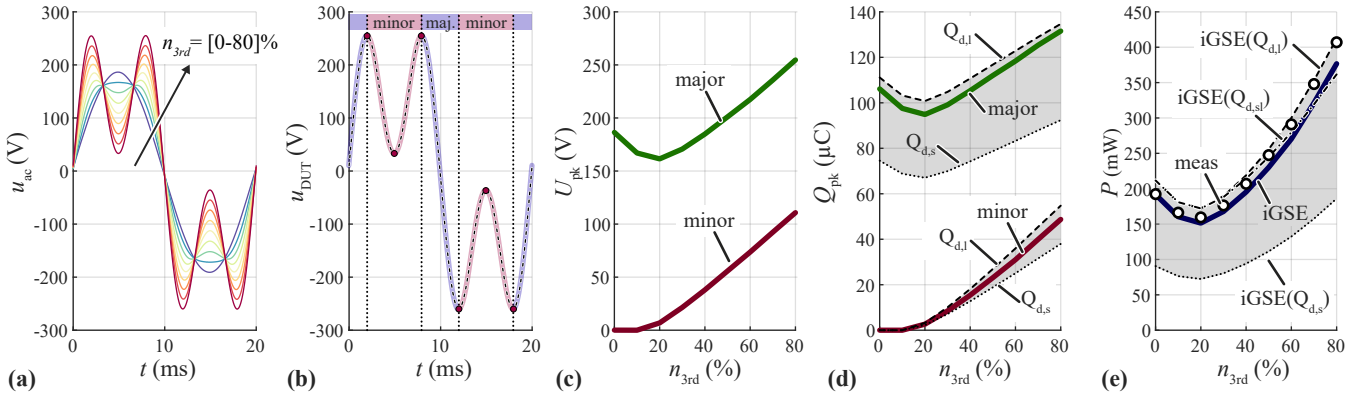

Fig. 9. Measurements under 3^{rd} harmonic injection conditions to validate the proposed iGSE-C modeling approach for non-sinusoidal voltage waveforms. **(a)** Measured excitation voltage waveforms with the 3^{rd} harmonic injection of variable magnitude ($n_{3\text{rd}}$) superimposed upon the $50\,\text{Hz}$, $150\,\text{V}_{\text{rms}}$ fundamental voltage excitation. For $n_{3\text{rd}} > 20\%$, minor loops result (the splitting of major and minor loops is highlighted for $n_{3\text{rd}} = 80\%$ in **(b)**). **(c)** Measured peak voltage amplitude U_{pk} of major and minor loops over $n_{3\text{rd}}$. **(d)** Measured peak charge amplitude Q_{pk} of major and minor loops over $n_{3\text{rd}}$, as well as the calculated charge from the large-signal ($Q_{\text{d,l}}$) and small-signal ($Q_{\text{d,s}}$) differential capacitance curves of **Fig. 15**. **(e)** Measured (scatter points) and calculated losses from (8) and (5) based on the measured charge (iGSE) or based on the calculated charge from the large-signal (iGSE($Q_{\text{d,l}}$)) and small-signal (iGSE($Q_{\text{d,s}}$)) differential capacitance curves of **Fig. 15**, or with the hybrid approach using large- and small-signal capacitance (iGSE($Q_{\text{d,sl}}$)) for each loop separately (cf. **Sec. V-A**). Accuracy between measured and calculated losses is within $7.6\,\%$ when using the measured charge.

was verified by superimposing a 3^{rd} harmonic component of varying magnitude upon the fundamental frequency excitation. Analogously, the ferroelectric iGSE-C proposed here in (8) is tested with the DUT under 3^{rd} harmonic injection.

Methodology: The DUT is excited with a single phase of a pre-existing buck-type three-phase inverter that complies with CISPR class A, making the high-frequency noise negligible at the DUT and supporting a variable-magnitude 3^{rd} harmonic injection. A fixed fundamental $150\,\text{V}_{\text{rms}}$, $50\,\text{Hz}$ sinusoidal excitation is applied to DUT and the 3^{rd} harmonic component is gradually increased from $0\,\% - 80\,\%$ of the fundamental amplitude, as shown in **Fig. 9a**.

With the linear loss dependence on frequency ($\alpha = 1$) found in **Section IV-A**, the integral term in (8) simplifies to twice the peak charge excitation magnitude Q_{pk} and the equation collapses to (7) for each loop. The losses can be straightforwardly calculated with (5) using major and minor loop splitting. In **Fig. 9b**, an example of this major and minor loop splitting is shown for $n_{3\text{rd}} = 80\,\%$, with the peak voltage U_{pk} in each harmonic loop shown across the tested $n_{3\text{rd}}$ values in **Fig. 9c**.

Measured Results: With the SE parameters defined and the iGSE-C modeling known, the final step in predicting losses under non-sinusoidal excitations is to determine the correct peak stored charge, Q_{pk}, to use in (7). **Fig. 9d** shows three methods of estimating the charge in each loop: the directly-measured charge (solid lines), the charge calculated from the large-signal differential capacitance ($Q_{\text{d,l}}$), and the charge calculated from the small-signal differential capacitance ($Q_{\text{d,s}}$). The large- and small-signal predictions are necessary for extensibility to arbitrary excitation waveforms and voltages, but we see that these two predictions differ widely in charge estimation, and therefore in loss prediction, with the large-signal $Q_{\text{d,l}}$ overestimating stored charge and the small-signal $Q_{\text{d,s}}$ underestimating the measured charge. This discrepancy – and an appropriate technique to estimate charge from an arbitrary voltage waveform – is investigated in depth in **Section V**.

Fig. 9e shows the calculated losses under 3^{rd} harmonic injection conditions with these different charge calculations, with a maximum error of $7.6\,\%$ between the measured and calculated losses using the proposed iGSE-C modeling with the measured charge. At low harmonic injection magnitudes, the voltage waveforms consists of a single major loop with decreasing peak amplitude, resulting in a decrease in measured losses. Above $20\,\%$ harmonic injection, two identical minor loops start to appear. For $n_{3\text{rd}} > 20\,\%$, the peak charge of the major loop starts to increase again, thereby increasing the measured and predicted losses.

While the agreement between the measured losses and predicted losses constitute a validation of the proposed iGSE-C loss modeling approach, the estimation of peak charge is again seen to be fundamental to the *a priori* loss prediction in **Fig. 9e**. This figure highlights the discrepancy in SE loss estimation between using the measured charge (excellent accuracy, denoted as SE), the calculated large-signal differential capacitance $C_{\text{d,l}}$ curve (again fairly accurate, $SE(Q_{\text{d,l}})$), and the calculated small-signal differential capacitance curve $C_{\text{d,s}}$ (significant underestimate of losses, $SE(Q_{\text{d,s}})$). In **Section V**, we propose a hybrid approach that calculates the large- and small-signal capacitance for each loop separately ($Q_{\text{d,sl}}$) and gives the most accurate and extensible results to estimate peak charge and therefore to predict losses (cf. **Fig. 9e**).

C. Impact of DC Bias

For magnetic materials, a DC premagnetization has a significant impact on the losses [34] that is not captured by the iGSE. To overcome this shortcoming, Ref. [35] provided Steinmetz Premagnetization Graphs (SPGs) for several magnetic materials to quantify the dependency of the Steinmetz parameters on the premagnetization current bias. Naturally, and especially with the well-known voltage dependence of X7R capacitors (as measured for the DUT in **Fig. 2d**), the impact of a DC voltage offset on the CC losses must be

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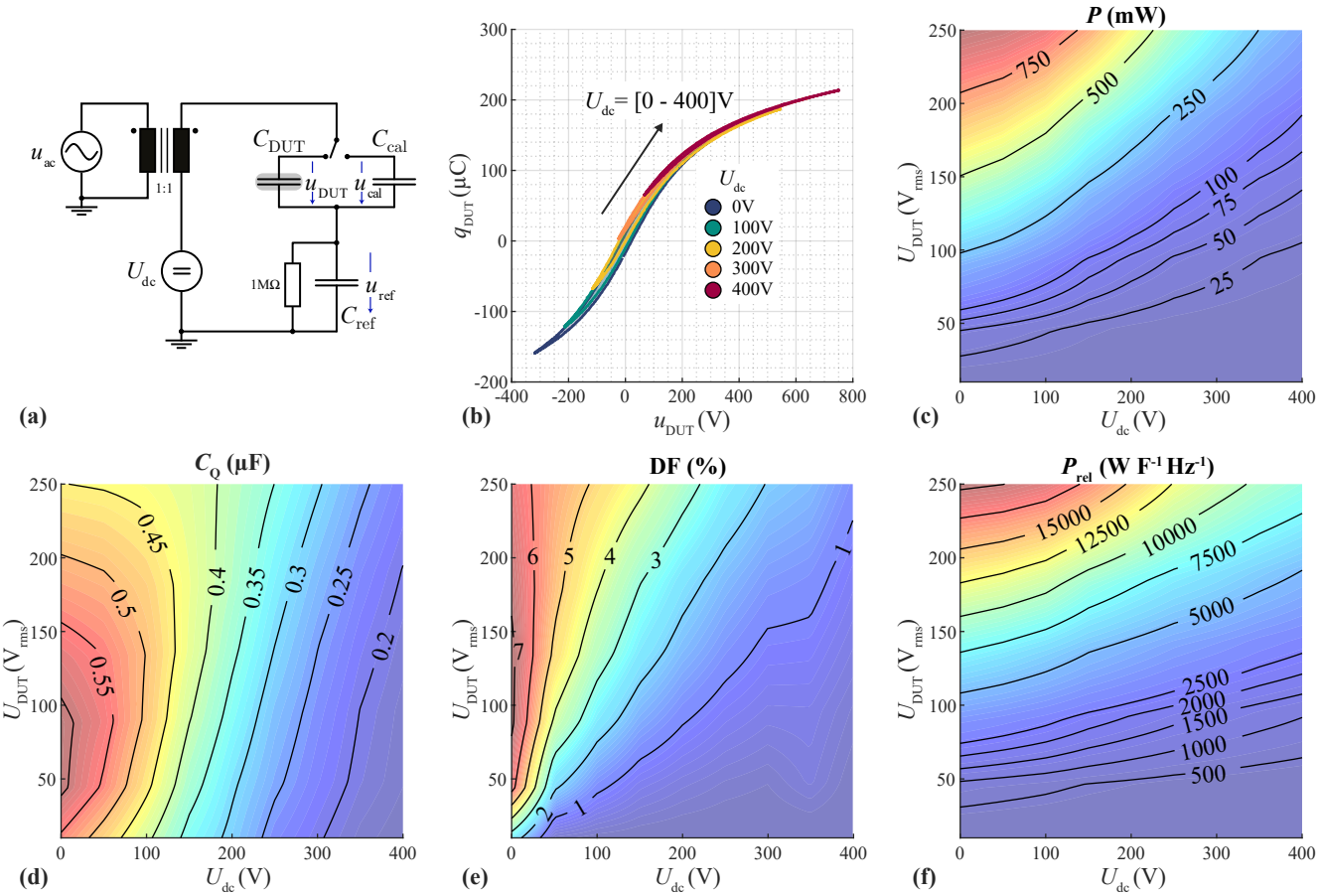

Fig. 10. Measured losses with varying DC bias and AC excitation voltage in the X7R CC under test (frequency fixed at 100 Hz for all measurements). Increasing DC bias decreases the losses in the DUT but simultaneously decreases the effective capacitance. Under the proposed charge-based SE loss model, DC bias has no impact on losses if peak charge is held constant (see **Fig. 11**). **(a)** Schematic circuit of a Sawyer-Tower measurement setup with AC voltage excitation and DC voltage bias. All measurements are conducted with an AC frequency of 100 Hz. The employed components are given in **Table II**. **(b)** Measured hysteresis curves for constant AC amplitude of 250 V_{rms} and increasing DC bias from 0 V − 400 V. Due to the parallel resistor of the reference capacitor, only the AC charge can be evaluated. As a function of AC voltage U_{DUT} and DC bias voltage, measured: **(c)** losses P, **(d)** charge-equivalent AC capacitance C_Q, **(e)** dissipation factor DF, and **(f)** losses P_{rel} normalized by measured AC capacitance and frequency, $P_{rel} = P/(C_Q \cdot f)$.

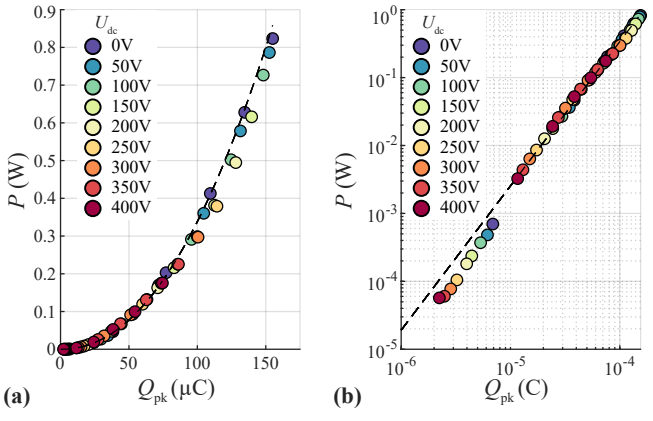

Fig. 11. Measured losses, from **Fig. 10c**, plotted against measured charge Q_{pk} for 100 Hz AC frequency, AC voltages from 50 V_{rms} − 250 V_{rms}, and DC bias from 0 V − 400 V. Dotted lines are derived Steinmetz parameters ($k = 1.06 \cdot 10^6, \alpha = 1$, and $\beta = 2.12$) in (7), which show excellent agreement with the measured data even under DC bias. The same Steinmetz fitting holds under DC bias conditions, indicating that the losses in the DUT are not dependent on DC bias, unlike in magnetic components. **(a)** Linear representation and **(b)** logarithmic representation.

investigated. We find here that the DC bias has no impact on the charge-loss relation found in **Section IV-A**, and that the same SE parameters can be employed to calculate the losses with a DC bias.

Methodology: The Sawyer-Tower circuit of **Fig. 5a** is modified slightly, as shown in **Fig. 10a**, to add a variable DC bias to the DUT. The DC bias source U_{dc} is referenced to protective earth with the AC excitation (from the AC power source) applied on top with an insulating transformer. A 1 MΩ resistor is added across the reference capacitor to ensure that the whole DC bias is applied to the DUT (otherwise, the DC voltage sharing is only defined by the capacitor leakage currents and the passive voltage probe resistances, i.e. poorly controlled parameters). As a result, only the AC charge excitation is captured by the Sawyer-Tower measurement, and the DC charge offset is added by integrating the previously-measured (in **Section IV-A**) large-signal differential capacitance to the DC bias voltage. The DC bias is varied from 0 V − 400 V with AC excitations at 100 Hz from 0 to 250 V_{rms}.

Measurement results: **Fig. 10b** shows the measured hysteresis curves for a constant AC excitation voltage of 250 V_{rms} and a DC bias increased in 100 V increments from

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$0\,\mathrm{V} - 400\,\mathrm{V}$. With a positive bias, the hysteresis becomes non-symmetric due to the voltage-dependent non-linearity of the capacitor. The peak-to-peak charge excitation shrinks with increasing DC bias, especially when the large-signal polarization around $0\,\mathrm{V}$ is avoided, and consequently both the losses and the large-signal capacitance (C_Q) decrease.

Fig. 10c-f show contour maps of measured losses, large-signal capacitance, dissipation factor, and normalized losses across varying excitation magnitude (U_DUT) and DC bias (U_dc). **Fig. 10c** shows the measured losses, with the zero DC bias results (along the y-axis) matching the results of **Fig. 7a.ii** with a maximum of $823\,\mathrm{mW}$. As expected from the curves of **Fig. 10b**, the hysteresis area and the losses drop with increasing DC bias for a given AC excitation.

The large-signal capacitance also decreases with increasing DC bias, as shown in **Fig. 10d**. The maximum AC capacitance is shifted towards higher AC amplitudes as the DC bias is increased, with the maximum occurring only when the curve encloses a voltage zero-crossing that results in large-signal polarization (explored in depth in **Section V**). **Fig. 10e** shows the dissipation factor, which continuously decreases with increasing DC bias (for a given AC excitation magnitude). We find, then, that a DC-referenced filter structure with a DC bias voltage and strictly positive capacitor voltages (cf. **Fig. 1**) would yield lower overall losses than a filter with zero DC bias, although more parallel capacitors would need to be employed to achieve the same effective capacitance value.

To visualize this tradeoff between losses (improving with DC bias) and capacitance (decreasing with DC bias), **Fig. 10f** normalizes the losses by AC capacitance and frequency, allowing a direct comparison of filter losses for an effective capacitance requirement. For a given AC excitation amplitude, the losses are either relatively constant across DC bias or decrease slightly at higher excitation amplitudes (where the zero crossing can be avoided with a large DC bias). We return to the Steinmetz fitting to more rigorously assess the effect of DC bias on losses and capacitance.

Steinmetz fitting: The measured losses across DC bias from **Fig. 10c** are scattered against the Steinmetz excitation parameter of (7), Q_pk (which is here derived from the charge-equivalent AC capacitance C_Q and U_DUT) in **Fig. 10d**, in both linear (**Fig. 11a**) and logarithmic (**Fig. 11b**) scales. The scatter color represents the DC offset voltage. The same Steinmetz fitting from **Section IV-A** ($k = 1.06 \cdot 10^6$, $\alpha = 1$, and $\beta = 2.12$) is plotted as a dotted line in each plot.

Fig. 11 clearly shows that the losses still follow the identical power law fit obtained from the AC-only measurement results, with discrepancies again only evident for loss magnitudes below $1\,\mathrm{mW}$. In contrast to magnetic materials, the DC bias has no impact on CC losses *for a given charge excitation amplitude* in the considered frequency range. While the bias has a major impact on the differential capacitance, as shown in **Fig. 10c**, only the charge magnitude is needed to calculate losses. This greatly simplifies the loss modeling of CCs and again validates the proposed charge-based SE and iGSE-C approaches.

D. Impact of Temperature

Thus far, short measurement times were used to maintain the DUT near room temperature ($25\,^\circ\mathrm{C}$) and measure consistent loss data, but with Ref. [14] showing that the losses of X7R CCs are highly temperature dependent, the impact of temperature on the measured and modeled losses needs to be evaluated.

Methodology: To assess the impact of temperature on losses, the DUT capacitor is now allowed to self-heat with a long measurement time. The measurement results from **Section IV-A** revealed losses of $9\,\mathrm{mW/Hz}$ or a loss density of $69\,\mathrm{mW/Hz/cm^3}$ at the maximum excitation voltage of $270\,\mathrm{V_{rms}}$, and hence substantial capacitor heating is expected.

Electrical (via the Sawyer-Tower circuit) and thermal measurements (via a high-frame rate thermal camera, the FLIR A655sc) are recorded simultaneously. Voltages are recorded with a large-memory oscilloscope, with memory sufficient to record $28\,\mathrm{s}$ of data with losses on an individual cycle basis extractable in post-processing (tests were stopped after $28\,\mathrm{s}$ or if the DUT reached $90\,^\circ\mathrm{C}$). To synchronize the electrical and thermal measurements, we assume a small thermal capacitance (C_th) of the DUT and align the oscilloscope trigger with the first increase of temperature. Similarly, the turn-off of the electrical source and the peak temperature happen simultaneously (noting that the device does not reach thermal steady-state in any of our test conditions), providing another synchronization verification. The excitation voltage is fixed at $270\,\mathrm{V_{rms}}$ and the frequency is varied from $100\,\mathrm{Hz} - 500\,\mathrm{Hz}$ with $100\,\mathrm{Hz}$ steps.

To provide a secondary loss verification with temperature, additional short-pulse (no self-heating) measurements (similar to **Section IV-A**) are recorded with the DUT fixed to a heating plate at variable temperature. These losses are recorded at $500\,\mathrm{Hz}$.

Measurement results: The recorded temperature and measured losses across elapsed time are shown in **Fig. 12a-b**, with the short-duration hot-plate measurements overlaid as scatter points. These short-pulse measurements are close to, but constantly slightly below, the losses measured in the transient measurement, which can be explained by the unavoidable self-heating implicit in the short-duration tests that shifts the real dielectric temperature slightly higher. The losses near $t = 0\,\mathrm{s}$ are close to the measured results and Steinmetz predictions of **Section IV-A**. Overall, these verifications indicate both that the synchronization is accurate and the temperature-dependent losses can be accurately measured under transient conditions.

Measured losses (normalized to the room-temperature value), large-signal capacitance, and dissipation factor are plotted with respect to temperature in **Fig. 12c-e**. We observe that both losses and effective capacitance drop substantially with increasing temperature (also shown in [14]), with losses declining faster than capacitance and dissipation factor therefore declining at higher dielectric temperature.

While the charged-based SE parameters for CCs do not depend on DC bias, these results indicate that operating temperature is an important factor that must be considered for loss prediction. In **Fig. 12c**, for example, the dashed line of best fit is plotted to represent the change of losses as

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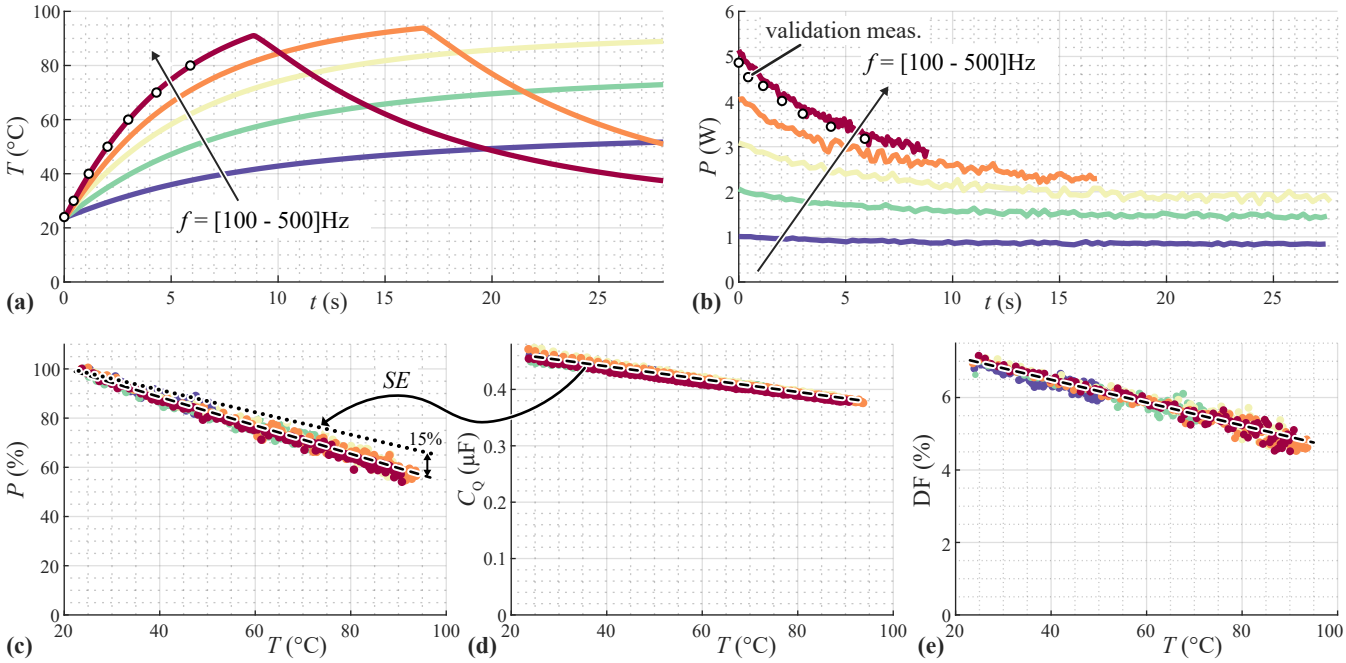

Fig. 12. Electrically measured losses under transient conditions with varying DUT temperature and excitation frequency from 100 Hz – 500 Hz (excitation magnitude fixed at 270 V_{rms} for all measurements). Scattered circles show measurements without self-heating (a hot-plate was used to control the device temperature and short-pulse measurements, like those reported in **Section IV-A**, were conducted), which match the transient measurements closely and validate the methodology. Losses and effective capacitance decrease with temperature, but losses decrease faster than C_Q and DF therefore decreases. **(a)** Measured DUT temperature and **(b)** losses over time for a constant AC voltage $U_{ac} = 270\,V_{rms}$ and increasing frequency f from 100 Hz – 500 Hz. Scatter points show hot-plate measurements to validate the transient method. **(c)** Losses relative to the initial value at room temperature (25 °C), **(d)** measured large-signal capacitance, and **(e)** dissipation factor as a function of temperature T. The decrease of charge-equivalent capacitance in **(d)** reduces the SE-predicted losses to those shown by the dotted line in **(c)**, with a maximum overestimation of 15 % over the measured losses at high temperature.

$P_{rel}(T) = 1 - 0.58\,\%/K \cdot (T - T_0)$ (with $T_0 = 20.28\,°C$). At high temperatures, the room-temperature SE parameters overpredict the measured losses by a maximum of 15 %, as shown with the dotted line in **Fig. 12c**. This indicates two separate temperature-related effects: firstly, the decrease in charge-equivalent capacitance with increasing temperature (**Fig. 12d**) results in lower predicted losses based on lower Q_{pk} (the SE line in **Fig. 12c**), but there appears to be an additional change to the dielectric loss mechanism with temperature that accounts for an additional 15 % of loss reduction. This discrepancy could eventually be obviated by means of an SE coefficient $k(T)$ that scales linearly with temperature, but with a small resulting deviation, this is not further considered.

Transient calorimetric capacitor loss measurement: This work was originally motivated by unexpectedly-high filter capacitor losses in an existing converter prototype. In these existing systems, a Sawyer-Tower circuit cannot be directly employed and the designer may be seeking to select the optimal filter capacitor or quantify the losses. From transient calorimetric techniques (e.g. [36]), we know that the device temperature and device losses are linked by the thermal resistance R_{th} and thermal capacitance C_{th}, and fitting these to the loss measurements of **Fig. 12** may enable *in situ* calorimetric loss measurements. This transient technique is introduced here and again used for two filter capacitors in **Section V**.

To perform an *in situ* transient loss measurement (**Fig. 13a**), the following procedure is followed:

1) The temperature rise of the capacitor $T(t)$ is recorded with a high frame rate thermal camera (if the DUT is not accessible with a thermal camera, a temperature sensor can be used) for an operating point where the losses are known across temperature. Here, we use the 100 Hz excitation of **Fig. 12a**, but any previously-recorded low-frequency excitation is a good candidate.
2) With the equivalent thermal circuit of **Fig. 13b**, and assuming $R_{th,int}$ is negligible, the equivalent thermal resistance R_{th} and thermal capacitance C_{th} are extracted from the temperature curve as:

$$P(t) = C_{th} \cdot dT(t)/dt + \frac{T(t) - T_{amb}}{R_{th}}. \qquad (14)$$

For the measurement results in **Fig. 12a** and the Sawyer-Tower setup of **Fig. 13a**, the thermal resistance and capacitance are fitted as $R_{th} = 34.96\,°C/W$ and $C_{th} = 0.325\,Ws/°C$. **Fig. 13c.i** shows the recorded temperature curve from **Fig. 12a** for $f = 100$ Hz, and in **Fig. 13c.ii**, we see that the calculated capacitor losses with (14) and the measured $T(t)$ are in good agreement with the electrically-measured (using the Sawyer-Tower circuit) losses in **Fig. 12b**.

Note that both R_{th} and C_{th} are determined by the particular physical environment in which the capacitor is installed, and must be determined on a setup-by-setup basis. We show the application of this transient prediction method in **Section V**.

E. HF Excitation

Finally, as a filter component in a switched-mode converter like **Fig. 1,** the CCs will necessarily see switching

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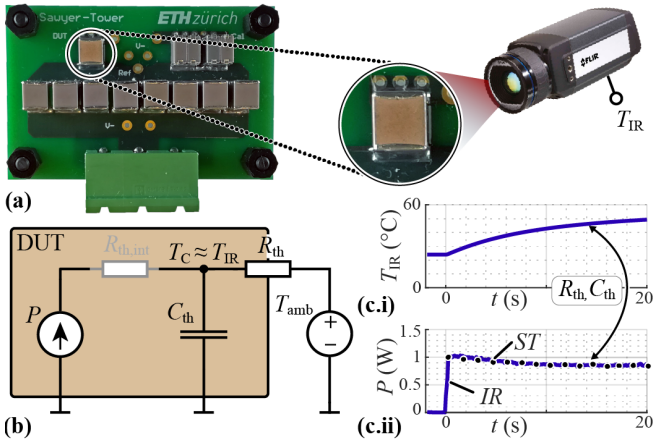

Fig. 13. Illustration of an *in situ* transient calorimetric capacitor loss measurement approach: **(a)** Sawyer-Tower circuit with highlighted DUT CC and FLIR A655sc thermal camera, **(b)** simplified thermal equivalent circuit of the DUT where the internal thermal resistance $R_{\mathrm{th,int}}$ is assumed to be negligible, **(c.i)** recorded temperature curve from **Fig. 12a** ($f = 100\,\mathrm{Hz}$) and **(c.ii)** calculated capacitor losses with $R_{\mathrm{th}} = 34.96\,^{\circ}\mathrm{C/W}$ and $C_{\mathrm{th}} = 0.325\,\mathrm{Ws/^{\circ}C}$.

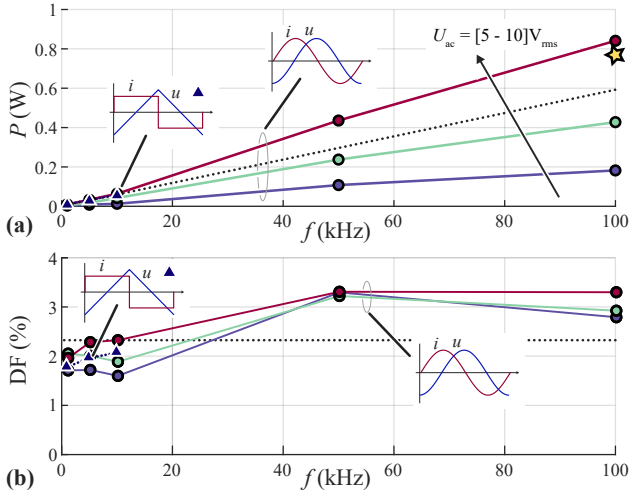

Fig. 14. Measured losses at high-frequency in the CCs DUT from $1\,\mathrm{kHz} - 100\,\mathrm{kHz}$ with an excitation voltage of 5, 7.5 and $10\,\mathrm{V_{rms}}$. Losses are identical between triangular (measurement indicated with triangular scatter points) and sinusoidal (indicated with round scatter points) excitations with the same peak voltage, as expected by the SE fitting of $\alpha = 1$. Triangular waveform measurements are limited by the power amplifier bandwidth to $10\,\mathrm{kHz}$. **(a)** Measured losses and **(b)** dissipation factor DF. Star scatter point shows thermally-measured losses using (14), which validates the high-frequency Sawyer-Tower measurements.

frequency harmonics. The losses from this high-frequency waveform component must be understood as well, and we seek to characterize the losses in the DUT from $1\,\mathrm{kHz} - 100\,\mathrm{kHz}$.

Methodology: Measuring these high-frequency losses across the large capacitances studied here introduces additional difficulties and a minor reconsideration and recalibration of the measurement setup (note that prior high-frequency Sawyer-Tower measurements measured capacitances of the, at most, nF order, not the $100\,\mathrm{nF}$ order studied here [25,26]). From **Fig. 2a**, we see that the DUT impedance is now in the range of Ω, and, according to the DF measurement of **Fig. 2c**, this places the ESR in the range of $10\,\mathrm{m\Omega}$ which is of the same order as the contact resistance of the solder joints and connection paths. Further, the current, which increases linearly with frequency, is several orders of magnitude higher than in **Section IV-A**, making the control of the resistive losses critical.

If the reference capacitor and calibration capacitor are considered lossless and $C_{\mathrm{ref}} \approx 10 \cdot C_{\mathrm{cal}}$, as in **Section IV-A**, equal contact resistance for both capacitors causes the apparent loss tangent of the reference capacitor to be ten times larger than that of C_{cal}, giving a *negative* loss reading for the calibration and also deteriorating the measurement with the DUT. Minimizing the return path impedance is therefore crucial and has to be verified with a calibration measurement. For the high-frequency measurements, it is preferred to have similar capacitance magnitudes between C_{ref} and the DUT to overcome this issue and to allow a calibration measurement with close to identical currents as in the DUT evaluation, and C_{cal} is implemented with one $0.2\,\mu\mathrm{F}$ (TDK, CAA572C0G2J204J640LH) and two $0.15\,\mu\mathrm{F}$ (TDK, C5750C0G2A154J230KE) C0G capacitors, yielding a total capacitance of $500\,\mathrm{nF}$, which is equal to the DUT under small-signal conditions. (Note that one alternative is measuring a capacitor with the same dielectric but less capacitance, which simultaneously increases the impedance and ESR and can be selected to again make the ESR much greater than the contact resistances. This approach was not selected here because the exact realization of the dielectric is not known with commercial devices.)

Excitations of 5, 7.5 and $10\,\mathrm{V_{rms}}$ are applied to the DUT, with the magnitude limited by the total losses, which scale with frequency. A sinusoidal excitation is applied with a high-frequency power amplifier up to $100\,\mathrm{kHz}$, and, to validate that $\alpha = 1$ holds at high-frequency, a triangular voltage (rectangular currents) excitation of $10\,\mathrm{V_{rms}}$ is also applied. The triangular waveform is limited to $10\,\mathrm{kHz}$ by the bandwidth of the high-frequency power amplifier.

Measurement results: **Fig. 14** shows the measured high-frequency losses under the triangular and sinusoidal voltage excitations. The dissipation factor DF for $10\,\mathrm{V_{rms}}$ is relatively flat (above $2\,\%$) up to $10\,\mathrm{kHz}$ and increases to $3.3\,\%$ at $100\,\mathrm{kHz}$ for losses of $860\,\mathrm{mW}$. As expected with $\alpha = 1$, the losses for triangular voltages and sinusoidal voltages with the same peak AC voltage are identical, as shown in **Fig. 14a**. A transient thermal measurement is performed to validate the high-frequency Sawyer-Tower measurements, where using (14) and the previously-derived R_{th} and C_{th} values, we find losses of $787\,\mathrm{mW}$ at $100\,\mathrm{kHz}$ (represented by the star scatter point in **Fig. 14a**).

These measurements provide a loss estimation for the high-frequency component in the filter capacitors. The measured DF does not change substantially when moving to the kHz range, with a small increase for higher excitation amplitudes. The effect of DC bias on the high-frequency losses was not considered, although recent research indicates a bias dependence for ceramic capacitor losses above $75\,\mathrm{kHz}$ [37]. Even under the assumption of constant SE parameters at high-frequency, there is excellent matching between the calculated and calorimetrically-measured losses in a practical application, as we show in the following section. In this

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section, we combine the high-frequency and low-frequency loss modelling approaches to provide guidelines to estimate CC losses in a switched-mode converter application.

V. Guidelines for Converter Loss Estimation

We again return to the analogy of ferro*magnetics* to highlight the challenges unique to ferroelectric CCs. In a converter like **Fig. 1**, the inductive components are subject to both low-frequency (typically sinusoidal and near line-frequency) current imposed by the control system and a high-frequency current ripple due to the PWM operation of the power semiconductors. Because these two frequencies are separated by multiple orders of magnitude, the loss contributions are typically considered separately and in most practical applications, the low-frequency core losses are small [38]. The high-frequency magnetic flux is determined easily by integrating the applied voltage-time area, but the losses for a given excitation are DC-bias dependent and SPGs are required to calculate the high-frequency core losses [35]. As gapped inductors are designed with sufficient margin to the saturation flux density of the core (to avoid a sudden roll-off of the inductance value), they feature an almost constant inductance value throughout the eligible current range and hence the premagnetization can easily be calculated [39]. In summary: with known SE parameters and SPGs, the assessment of core losses is relatively straightforward.

As previously presented, the capacitors of the sine-wave filter in the converter of **Fig. 1** also face a low-frequency voltage excitation and a high-frequency voltage ripple due to the PWM operation of the power semiconductors. To use the presented iGSE-C approach with ferroelectric capacitors, the charge excitation must be known, which for the high-frequency excitation can be obtained directly by integrating the high-frequency inductor current ripple. Assuming the Steinmetz parameters are independent of DC bias (shown in **Section IV-C** for low frequencies up to 250 Hz) for high frequencies as well, the high-frequency losses are straightforward to assess and are relatively minor in sine-wave filters with a large fundamental voltage swing and low high-frequency voltage ripple. In contrast to magnetic materials, however, the fundamental frequency losses in the CCs are substantial, as shown in this work. For a given voltage, the charge excitation depends on the non-linear relative permittivity (or differential capacitance), and with the SE and iGSE-C modelling dependent on the peak charge stored, the correct estimation of this charge is critical to obtain an accurate loss calculation. According to **Fig. 2d**, the differential capacitance of the DUT reduces by approximately 70 % for a DC bias of 400 V, and the nominal operating regime includes, essentially, substantial saturation which further complicates the charge estimation. This charge estimation is the focus of the following sub-section.

A. Evaluation of the Charge Excitation

For a given capacitor voltage excitation $U(t)$, the charge is defined by the differential capacitance C_d as:

$$Q(t) = \int C_\mathrm{d}(U) \cdot \frac{dU(t)}{dt} dt = \int C_\mathrm{d}(U) dU. \qquad (15)$$

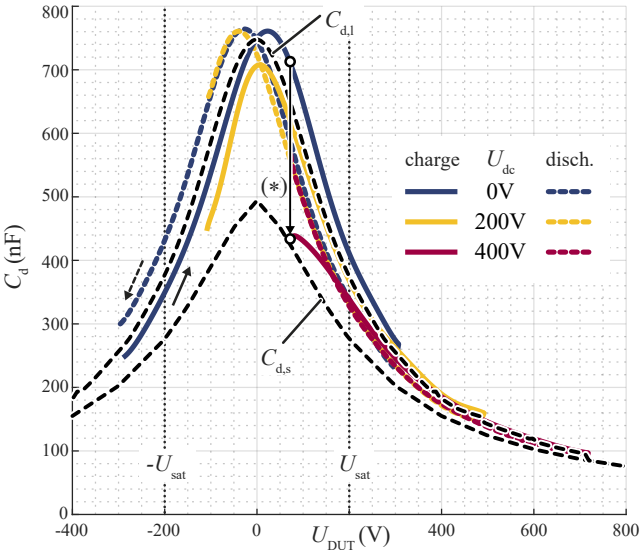

Fig. 15. Differential capacitance over voltage derived according to (6) for the measured hysteresis curves shown in **Fig. 10b** with 250 $\mathrm{V_{rms}}$ AC excitation and increasing DC bias of 0 V, 200 V, and 400 V. The differential capacitance is shown for the charging (solid) and discharging (dotted) portions of the voltage excitation. For a given voltage, C_d depends greatly on the overall hysteresis waveform, including the AC magnitude, DC bias, and direction of the excitation (see $(*)$, which highlights the variability near 0 V). The small-signal $C_\mathrm{d,s}$ and large-signal $C_\mathrm{d,l}$ differential capacitance curves can be used to estimate the charge excitation for small or large AC voltage excitations, respectively.

With the highly non-linear C_d found in **Section IV-A**, the small-signal C_d curve in **Fig. 2d** is only true under small-signal excitation conditions. Otherwise, $C_\mathrm{d}(U)$ must be back-calculated using (6) under the large-signal excitations. From **Fig. 10** and the discussion around those results, we can already see that multiple $C_\mathrm{d}(U)$ functions must exist that depend on the excitation magnitude and the DC bias. The extracted $C_\mathrm{d}(U)$ from the excitations in **Fig. 10b** are plotted in **Fig. 15** for $U_\mathrm{ac} = 250\,\mathrm{V_{rms}}$ and DC bias voltages of 0 V, 200 V, and 400 V (in the plot, we exclude regions where dQ/dt or dV/dt are close to zero to avoid poor signal-to-noise ratios).

First, we see a large dependence of differential capacitance both with DC bias U_dc and with the direction of the excitation (charging or discharging) in **Fig. 15**. The $(*)$ highlights that the C_d close to the zero-voltage crossing greatly depends on both the DC bias and the overall path of the hysteresis loop. In contrast, if the charging signal exceeds U_sat, the associated discharging C_d is, for the most part, largely independent of DC bias and AC magnitude. (The same holds true if the discharging curve exceeds $-U_\mathrm{sat}$, with identical charging curves.) For the $U_\mathrm{dc} = 400\,\mathrm{V}$ excitation, the capacitor voltage never changes sign, and the large-signal polarization is not fully relaxed when the minimum voltage is approached. The ensuing "non-switching transition" [40] (where the voltage polarity never reverses) results in a low differential capacitance C_d.

The non-linearity of the capacitance around the zero-voltage crossing, then, complicates the prediction of the stored charge for a given voltage waveform, as the integration in (15) is not straightforward. For large AC excitation

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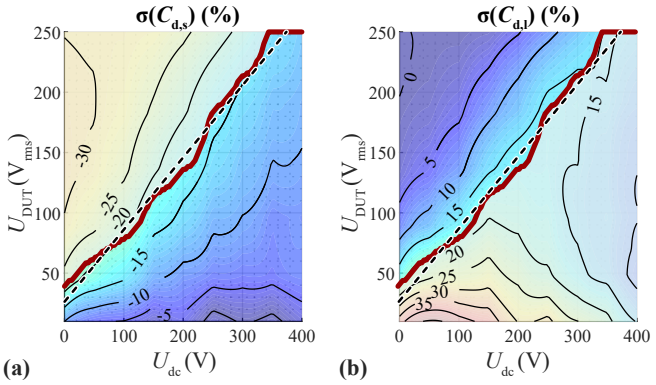

Fig. 16. Relative error σ of the calculated charge-equivalent capacitance $C_{\mathrm{Q,calc}}$ using (15) for sinusoidal AC excitation and DC bias relative to the measured C_{Q} of **Fig. 10d** with **(a)** the small-signal $C_{\mathrm{d,s}}$ and **(b)** the large-signal differential capacitance $C_{\mathrm{d,l}}$ (cf. **Fig. 15**) models. The red line indicates the boundary between the regions where the small- and large-signal approximations are respectively preferred to minimize the charge approximation error.

magnitudes, Q can instead be conservatively approximated with the large-signal capacitance as the average of C_{d} during the rising and falling voltage excitations, as shown in **Fig. 15** with the $C_{\mathrm{d,l}}$ dashed line. This curve is a good approximation when the AC swing exceeds $|U_{\mathrm{sat}}|$ on both the negative and positive voltage swings. $C_{\mathrm{d,s}}$ remains a valid prediction of charge storage under small-signal excitations.

For an arbitrary waveform, including those with the 3^{rd} harmonic injections of **Fig. 9a**, the charge in a given loop can be calculated with either $C_{\mathrm{d,s}}$ or $C_{\mathrm{d,l}}$, which respectively yield the lower and upper bounds on hysteretic losses, as shown in **Fig. 9d** and **Fig. 9e**. Neither prediction method of charge from a given voltage waveform, however, is perfect, and there remains the question of exactly what voltage magnitude constitutes a small- or large-signal excitation.

A comparison of the resulting charge approximation error (σ) using $C_{\mathrm{d,s}}$ and $C_{\mathrm{d,l}}$ for the measured charge in **Fig. 10d** is shown in **Fig. 16**. As expected, the small-signal charge prediction $C_{\mathrm{d,s}}$ is a good approximation when the AC magnitude is small absolutely or relative to the DC bias (cf. **Fig. 16a**), while the opposite holds true for the prediction given by $C_{\mathrm{d,l}}$ (cf. **Fig. 16b**).

The regions where the small- and large-signal approximation respectively yield the minimal absolute charge error $|\sigma|$ are separated by the red line U_{bound} in **Fig. 16**, which can be simplified as (the dashed lined in **Fig. 16**):

$$U_{\mathrm{bound}} = 0.60 \cdot U_{\mathrm{dc}} + 26.35\,\mathrm{V}. \tag{16}$$

For a minimal charge approximation error at a given DC bias U_{dc}, C_{d} is selected as:

$$C_{\mathrm{d}} = \begin{cases} C_{\mathrm{d,s}}, & U_{\mathrm{DUT,rms}} \leq U_{\mathrm{bound}} \\ C_{\mathrm{d,l}}, & U_{\mathrm{DUT,rms}} > U_{\mathrm{bound}}, \end{cases} \tag{17}$$

yielding a maximal charge approximation error of $|\sigma_{\mathrm{max}}| = 20\,\%$ across the full DC bias and AC magnitude sweep. With minor loops for non-sinusoidal excitations, (16) should be employed for each loop separately, as shown in **Fig. 9e**.

This charge estimation approach – necessitated by the non-linear ferroelectric characteristics, and especially by the large-signal polarization near 0 V – could be avoided by designers with two potential alternatives. Once the SE parameters have been derived for a given DUT, the losses can be calculated based solely on a charge measurement (e.g. using a current probe and integrating charge) when the device is excited with the desired fundamental frequency waveform. (Note that this method is difficult to use to *determine* the SE parameters, as discussed in **Section III**.) Alternatively, manufacturers could provide (in addition to SE parameters) online tools for hysteresis modeling based on their physical knowledge of polarization effects in commercial dielectrics.

B. Design Example

Finally, we employ the tools and measured losses here to calculate the total losses of CCs in a single-phase DC/AC converter with a split 800 V DC-link and a 50 Hz, 250 $\mathrm{V_{rms}}$ AC voltage (shown in **Fig. 17a.i**). The switching frequency is selected at $f_{\mathrm{s}} = 100\,\mathrm{kHz}$ and a two-stage filter (comprised of two identical filters, *S1* and *S2*, with a crossover frequency $f_{\mathrm{c}} = 10\,\mathrm{kHz}$) provides an attenuation of approximately 80 dB at the switching frequency. Each filter is constructed with an inductor of $L = 85\,\mu\mathrm{H}$ and 6 paralleled DUT capacitors ($C = 2.8\,\mu\mathrm{F}$). A load of $380\,\Omega$ is used at the output.

The filter stages have a nearly-identical fundamental-frequency voltage excitation (**Fig. 17a.ii**), with the fundamental-frequency voltage drop across the inductor of *S1* safely neglected. The peak high-frequency current ripple $\hat{i}_{\mathrm{L,HF}}$ of the inductor in *S1* can be calculated from the time varying duty cycle $d(t) = \frac{u_{\mathrm{ac}}(t)}{\frac{1}{2}U_{\mathrm{dc}}}$ pattern as:

$$\hat{i}_{\mathrm{L}}(t) = \frac{1}{8}\frac{U_{\mathrm{dc}}(1-d)(d+1)}{L f_{\mathrm{s}}}, \tag{18}$$

and reaches up to 12 A in this application. In *S2*, the high-frequency current ripple is attenuated by an additional 40 dB and is therefore negligible (**Fig. 17a.iii**), yielding an opportunity to break apart the relative loss contributions from the low-frequency and high-frequency components.

According to (17), the low-frequency charge is best calculated using $C_{\mathrm{d,l}}$, with $\hat{Q}_{\mathrm{LF}} = 159\,\mu\mathrm{C}$ as the result. To validate this prediction, the filter capacitor of *S2* was replaced with the ST setup, where a low-frequency peak excitation of $\hat{Q}_{\mathrm{LF}} = 156\,\mu\mathrm{C}$ was directly measured (cf. **Fig. 17b.i**).

The high-frequency charge excitation in *S1* can be obtained by integrating the high-frequency inductor current of *S1* and dividing the current by the 6 paralleled capacitors, giving a maximum per-device charge of $\hat{Q}_{\mathrm{HF,max}} = 2.5\,\mu\mathrm{C}$ (dotted line in cf. **Fig. 17b.i**). The measured switching-frequency charge ripple amplitude nicely follows this theoretical prediction.

Using the SE parameters from **Section IV-A** ($k = 1.06 \cdot 10^6, \alpha = 1, \beta = 2.12$), the low- and high-frequency losses for *S1* and *S2* can be calculated from the charge predictions above. In *S1* and *S2*, the calculated line-frequency losses are 450 mW, and the time-varying high-frequency losses in *S1* peak at 173 mW with an average value $\bar{P}_{\mathrm{HF}}$ of 64 mW (**Fig. 17b.ii**). The transient calorimetric measurement approach of **Section IV-D** is used to measure the losses

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(which cannot be accurately measured with the Sawyer-Tower circuit with the low- *and* high-frequency excitations, as discussed in **Section IV-E**).

Fig. 17c.i shows the temperature rise of the capacitors, which is translated into instantaneous power loss (**Fig. 17c.ii**) with (14) and the thermal equivalent circuit parameters from **Section IV-D**. The measured losses in *S2* are 459 mW, predicted with an error under 2 %. The high-frequency losses are indeed negligible in this stage. For the capacitor of *S1*, the measured losses increase by 122 mW over the losses in *S2* due to the high-frequency ripple. While the prediction of $\bar{P}_{\mathrm{HF}}$ is off by approximately a factor of two (64 mW predicted losses), the prediction error of total losses in *S1* is only 12 %, and the high-frequency error can be partially explained by the reported increase of DF by 30 % at high-frequency (**Fig. 14b**). Non-ideal current sharing among the capacitors is also a potential error source.

Nonetheless, the high-frequency losses of 122 mW are only 20 % of the overall losses, and clearly the low-frequency loss component dominates in CCs for the considered sine-wave filter with a small high-frequency voltage ripple compared to the fundamental voltage waveform. For motor drives with fundamental frequencies up to 200 Hz-300 Hz, this ratio may be even more tilted towards the low-frequency losses, The total loss approximation error for *S1* is under 12 %, validating the measurements, the iGSE-C model, and the charge estimation approaches in this work.

VI. Conclusion

Ferroelectric Class II Ceramic Capacitors (CCs) promise large volume reductions in inverter and rectifier sine-wave filters, and are expected to gain importance in future applications demanding exceptional power density. While prior work has found non-linear and large losses in these components, no extensible loss model is available in the literature that accurately describes these hysteretic losses.

In this work, a Steinmetz-based loss modeling approach – called the Improved Generalized Steinmetz Equation for ceramic Capacitors, or iGSE-C – is proposed and verified for a commercially-available X7R CC. We measure the ferroelectric hysteresis losses across AC excitation magnitude, DC bias, frequency, temperature, and harmonic injection using the Sawyer-Tower circuit.

Losses are shown to scale according to a power law with peak charge, with the Steinmetz coefficients constant over DC bias. By analogy with well-developed methods for ferro*magnetic* components in power electronics applications, the iGSE-C accurately predicts losses under non-sinusoidal voltage excitations, as long as the charge is accurately characterized or measured.

Finally, a procedure is given and validated for predicting total losses – the sum of low-frequency and high-frequency losses – in a sine-wave filter, with the low-frequency losses dominating the total power dissipation in the CCs.

Appendix A
Calorimetric Measurement Methods

A. Steady-State Calorimetric Measurement

A steady-state calorimetric measurement has the advantage that the fundamentally large ratio of reactive to active power has no impact on the measurement accuracy or precision, and these measurements were conducted with film capacitors for traction applications in [32]. With the strong temperature dependence of X7R CCs previously known [14], this technique is not possible here.

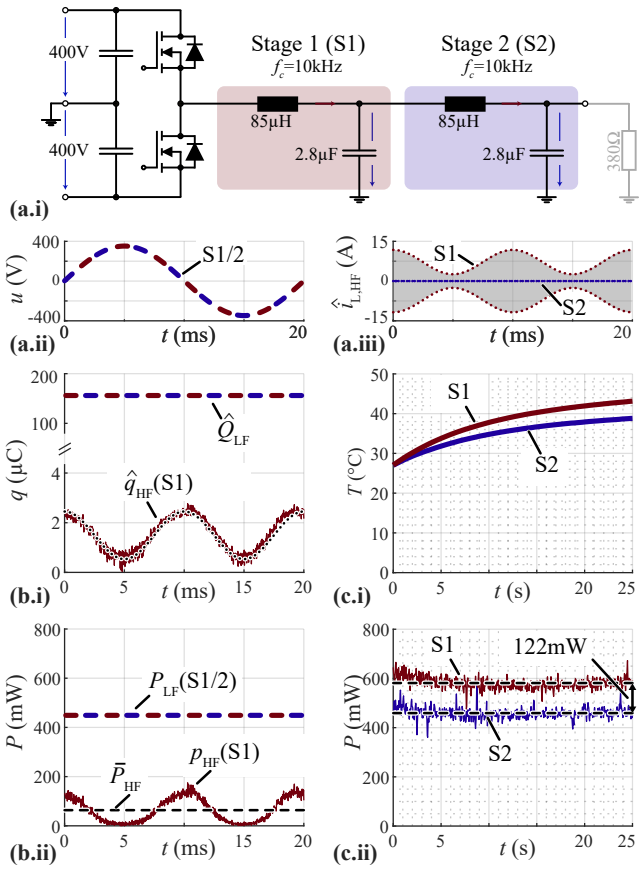

Fig. 17. (a.i) Example of single-phase DC/AC converter with a split 800 V DC-link and a 50 Hz, 250 V_{rms} AC voltage. The output sine-wave filter consists of two identical filter stages, where only the first filter stage *S1* is subject to a substantial high-frequency excitation. Calculated **(a.ii)** low-frequency AC voltage waveforms of the capacitors in *S1* and *S2* and **(a.iii)** calculated high-frequency envelope of the *S1* inductor current. **(b.i)** Measured (solid line) and calculated (dashed line) low-frequency charge excitation of *S1* and *S2* as well as the time-varying high-frequency charge waveforms of *S1*. **(b.ii)** Calculated low-frequency and high-frequency capacitor losses using the measured charge excitation and the SE parameters from **Section IV-A**. **(c.i)** Measured capacitor transient temperature curves of *S1* and *S2* during converter operation. **(c.ii)** Calculated capacitor losses (average values represented as dashed lines) from the transient thermal measurements of **(c.i)** with (14) and the thermal equivalent circuit parameters from **Section IV-D**.

B. Indirect Transient Calorimetric Measurement

An indirect measurement uses the temperature increase of something *other than the DUT* to estimate the losses in the DUT. These losses are typically recorded under quasi-steady-state conditions. In Ref. [33], the dielectric losses of insulation materials were evaluated by measuring the increase in temperature of a thermally-isolated test chamber (with a calibration resistor in an equal package). In [15], a similar approach was used, with the DUT located in an oil bath and the temperature increase measured. In [41] and

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[42], wide-bandgap-semiconductor switching losses were measured with the temperature increase of a brass block after a DC current calibration (the steep $\mathrm{d}v/\mathrm{d}t$-transients jeopardize any electrical measurement). While this measurement technique produces valid, accurate results, it is much slower than the implemented electrically-based technique.

C. Direct Transient Calorimetric Measurement

In order to rapidly evaluate semiconductor hard and soft switching losses, recently a new method was introduced where the temperature of the semiconductor case is measured directly (again after a DC current calibration step), reducing the measurement time to the range of seconds [36]. The same method was employed in [43] to characterize the losses of magnetic materials under large-signal excitations with frequencies up to $50\,\mathrm{MHz}$. The calibration losses are generated by impressing a DC current upon the magnetic core samples.

The DC calibration (or any other known loss calibration) is not possible for capacitors, and therefore this method is not directly applicable here. Based on existing capacitor loss data, however, this method can be employed for an *in situ* measurement in a hardware prototype, as discussed in **Section IV-D** and demonstrated in **Section V-B**.

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