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Novel Three-Phase Two-Third-Modulated Buck-Boost Current Source Inverter System Employing Dual-Gate Monolithic Bidirectional GaN e-FETs

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***Abstract*— The unprecedented characteristics of dual-gate (2G) monolithic bidirectional (MB) gallium nitride (GaN) enhancement-mode field-effect transistors (e-FETs) enable a potential performance breakthrough of current DC-link inverters, e.g. in terms of power conversion efficiency, power density, cost and complexity. In fact, a single 2G MB GaN e-FET can conveniently replace and outperform two anti-series connected conventional power semiconductors to realize the *four-quadrant* (AC) switch required in this circuit topology. Furthermore, a variable DC-link current control strategy can be applied to a three-phase (3-Φ) buck-boost (bB) current source inverter (CSI) system comprising a DC-link current impressing buck-type DC/DC input stage and a subsequent boost-type 3-Φ current DC-link inverter output stage to significantly reduce the occurring losses. The proposed strategy is denominated *Two-Third Modulation*, since by properly shaping the DC-link current with the input stage by means of a *Synergetic Control* structure, it allows to generate the desired 3-Φ sinusoidal load currents by switching only two out of the three phases of the output stage. Circuit simulations of the 3-Φ bB CSI system support the explanation of the analyzed concept and confirm the associated reduction of losses, for which analytical expressions are as well derived. Finally, the operation of new 2G MB GaN e-FET research samples is verified in a hardware prototype, taking the first step towards the practical realization of the described power converter.**

***Index Terms*— Dual-Gate Monolithic Bidirectional Gallium Nitride Enhancement-Mode Field-Effect Transistor, Three-Phase Buck-Boost Current Source Inverter System, Variable DC-Link Current Control.**

I. Introduction

THE three-phase (3-Φ) voltage DC-link inverter is the industry preferred solution to perform compact and efficient DC/AC energy conversion in variable speed drive (VSD) applications, which accounts for almost half of all global electricity consumption [1]. On-board of electric vehicles (EVs), the 3-Φ inverter is typically preceded by a boost-type DC/DC converter input stage [2] compensating for the dependency of the traction battery voltage (DC-link voltage) on the load and on the state of charge of the battery itself. This two-stage converter forms a 3-Φ boost-buck (Bb) voltage source inverter (VSI) system, which is also employed for high-speed compressor drives, fuel cell powered EVs and general battery powered VSDs.

The alternative quasi-dual approach is the 3-Φ buck-boost (bB) current source inverter (CSI) system [3] shown in **Fig. 1**, which comprises a DC-link current impressing buck-type DC/DC input stage and a subsequent boost-type 3-Φ current DC-link inverter output stage [4]. This solution is rarely adopted, mainly because of the higher count of power devices. In fact, a 3-Φ voltage DC-link inverter only requires six power semiconductors with unidirectional voltage blocking capability allowing bidirectional current flow, such as MOSFETs or IGBTs (eventually with external anti-parallel diodes), which are the most widely used power devices. Consequently, VSI systems are often preferred and, especially when wide band-gap (WBG), i.e. gallium nitride (GaN) and silicon carbide (SiC), power semiconductors are considered, high power conversion efficiencies and extreme power densities can be achieved at any power level [2], [5].

In contrast, a 3-Φ current DC-link inverter (shown in black in **Fig. 1**) requires six power semiconductors with bidirectional voltage blocking capability allowing unidirectional current flow, such as, e.g. symmetric GTOs. However, when design constraints demand switching frequencies in the 10-100 kHz range, these switches are preferably realized by anti-series connecting two discrete components, e.g. two transistors or a transistor and a diode. This ultimately causes an increase of chip area, cost, driving complexity and conduction losses which disfavor CSI systems in comparison with VSI systems.

Recent development in the power semiconductor industry culminated in the realization of monolithic bidirectional [6] (MB) GaN enhancement-mode field-effect transistor (e-FET) research prototypes [7]–[10] which feature bidirectional voltage blocking capability and allow current flow in both directions, i.e. excellently fitting the requirements of current DC-link inverters. In particular, ±600 V 26 mΩ research samples of a dual-gate (2G) MB GaN e-FET [11] are available from a major manufacturer of power semiconductors. Preliminary tests on these devices are performed in [12], however, their potential in a 3-Φ bB CSI system remains unclear and thus additionally motivates this work.

Beside the new components, other intrinsic characteristics of 3-Φ bB CSI systems triggered the interest of the authors in this circuit topology:

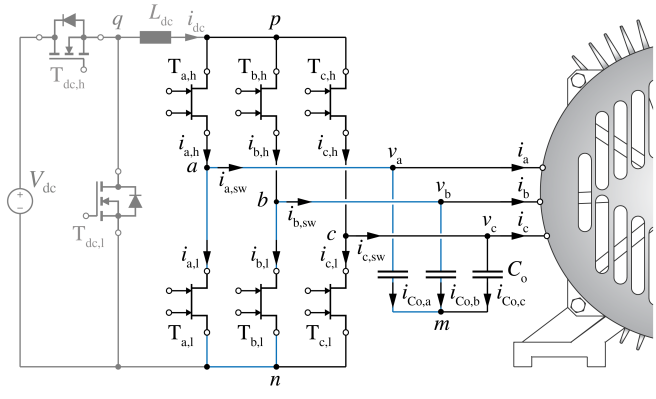

Fig. 1: Schematic of the 3-Φ bB CSI system. The boost-type 3-Φ current DC-link inverter output stage (black) is formed by six 2G MB GaN e-FETs and connected to the electric machine. The buck-type DC/DC converter input stage (shaded), connected to a supplying DC input voltage V_{dc}, introduces the bB functionality and allows to control and shape the DC-link current i_{dc}.

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- Current DC-link inverters generate continuous output voltage waveforms, whereas voltage DC-link inverters generate switched output voltage waveforms. Hence, external output filters, eventually compromising the power density, are often necessary in the latter case to mitigate EMI emissions [13] and, in case of VSDs, to avoid excessive insulation stress (e.g. caused by high switching speeds in combination with long motor cables) and losses in motors, as well as bearing wear-out [5].
- While voltage DC-link inverters switch a constant voltage and a variable current, the opposite is true for current DC-link inverters. Since the switching losses are typically stronger influenced by the switched voltage than by the switched current [14], lower switching losses might occur in the current DC-link approach for the same processed power [15], eventually resulting in higher efficiencies [16].
- Although capacitors (voltage DC-links) have a high energy storage density, a lower boundary for their volume is given by their current rating [17]. Differently, higher switching frequencies, i.e. WBG semiconductors, always enable the downsizing of magnetic components (current DC-links). Additionally, different cost, operating temperature range, critical environmental conditions, failure modes and failure rates are associated to capacitors and inductors. Hence, current DC-link inverters potentially show advantages over voltage DC-link inverters in certain applications.

In this paper, first, the mentioned 2G MB GaN e-FET research prototypes are presented in **Section II** and compared to the state-of-the-art. The operating principle of the selected 3-Φ bB CSI system is then introduced at the beginning of **Section III**. Afterwards, simulation results support the explanation of a variable DC-link current control strategy denominated *Two-Third Modulation* (TTM) [18]. Analytic calculations, performed in **Section IV**, highlight the performance improvement of the 3-Φ current DC-link inverter enabled by this concept. In **Section V**, the experimental hardware, designed to evaluate the switching performance of the 2G MB GaN e-FETs, is described and measured switching waveforms are discussed. Finally, **Section VI** provides an outlook for future work and **Section VII** concludes the paper.

II. Dual-Gate Monolithic Bidirectional GaN e-FET

The power device selected for the realization of the 3-Φ current DC-link inverter introduced in **Fig. 1** is a $\pm 600\,\mathrm{V}$ $26\,\mathrm{m\Omega}$ 2G MB GaN e-FET [12]. The main characteristics of this research prototype are compared in **Table I** with the ones of the best-in-the-market conventional GaN transistor in the same voltage class, i.e. a $650\,\mathrm{V}$ $25\,\mathrm{m\Omega}$ GaN e-FET [19]. To extend the operation of the commercial solution to *four-quadrants* while maintaining the same overall on-state resistance $R_{\mathrm{ss,on}}$, two anti-series and two parallel devices must be connected as shown in **Fig. 2(a)**, massively increasing costs and, as highlighted by **Fig. 2(b)**, the required PCB area with respect to the MB solution. Additionally, due to the increased parasitic output capacitance C_{oss}, the figure of merit (FoM) [5] of the so obtained AC-switch becomes almost three times worse than the one of the MB device. To summarize, the considered 2G MB GaN e-FET is expected to cause a performance breakthrough of 3-Φ bB CSI systems, and potentially of all circuit topologies requiring AC-switches as, e.g., matrix converters.

In order to simultaneously control the bidirectional voltage blocking and current flow capabilities, two gate voltages $v_{\mathrm{gs,n}}$ and $v_{\mathrm{gs,p}}$ must be separately applied to the 2G structure of the MB GaN e-FET as indicated in **Fig. 2(b)**, defining its operating state according to **Fig. 3(a)**. Alternatively, if only one gate is controlled, only unidirectional current flow is possible. The gate voltages $v_{\mathrm{gs,n}}$ and

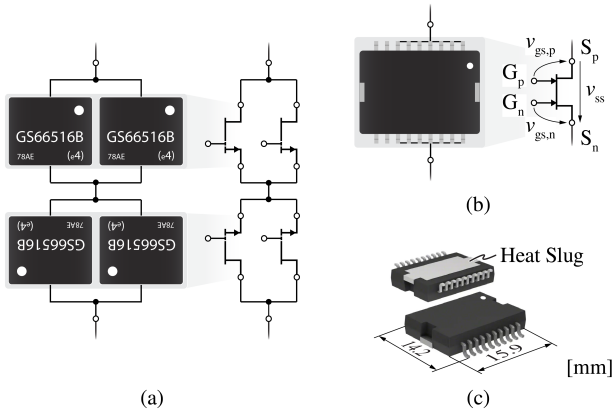


Fig. 2: Conventional realization of a *four-quadrant* (AC) switch with **(a)** two anti-series/two parallel $650\,\mathrm{V}$ $25\,\mathrm{m\Omega}$ GaN e-FETs [19] compared with **(b)** a single $\pm 600\,\mathrm{V}$ $26\,\mathrm{m\Omega}$ 2G MB GaN e-FET [12] (geometric proportions of the packages are preserved). Both solutions **(a)** and **(b)** achieve approximately the same voltage blocking capability and overall $R_{\mathrm{ss,on}}$, however **(b)** enables a massive saving in terms of package size. **(c)** Perspective view of the 20-pin package of the 2G MB GaN e-FET.

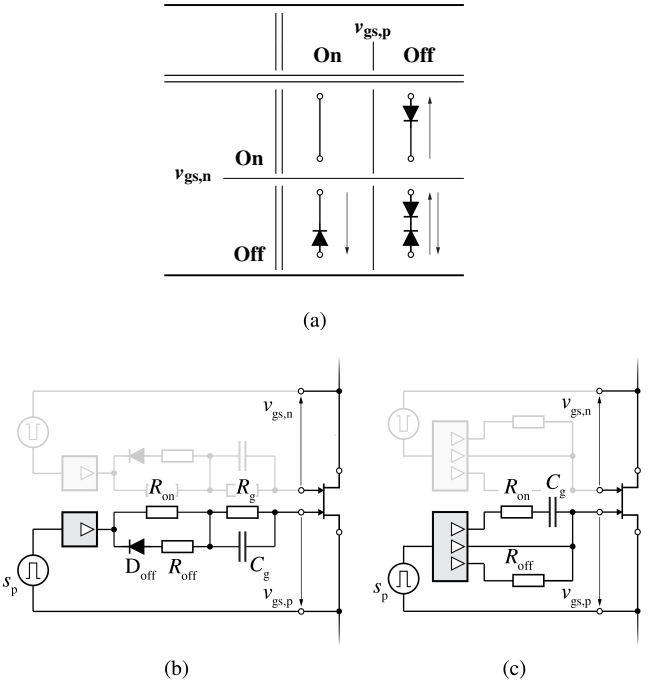


Fig. 3: (a) Equivalent circuit of the 2G MB GaN e-FET depending on the applied gate voltages $v_{\mathrm{gs,n}}$ and $v_{\mathrm{gs,p}}$. **(b)** Conventional gate driver circuit adapted to GITs [21] based on a commercial IC and **(c)** gate driver circuit for GITs based on a specialized IC [22].

$v_{\mathrm{gs,p}}$ must be isolated from each other because of the common-drain structure which, based on a single drift layer, yields to lower values of $R_{\mathrm{ss,on}}$ compared with the alternative common-source structure [9]. Since the device is of the *Gate Injection Transistor* (GIT) type [20], a constant current in the mA-range must flow through each gate to modulate the conductivity of the two-dimensional electron gas (2DEG) channel during on-state. As visible in **Fig. 3(b)**, conventional gate driver circuits can be modified to include this feature [21]; alternatively, an *ad hoc* integrated circuit (IC) [22] can be used. Adopting the latter approach, the compact gate driver design illustrated in **Fig. 3(c)**, requiring only three discrete components between the IC and the gate terminal, can be realized.

TABLE I: Main characteristics of the selected 2G MB GaN e-FET compared to the best-in-the-market conventional GaN transistor in the same voltage class as a single device (1x) and in the two anti-series/two parallel configuration (4x).

Power Semiconductor			$V_{ss,MAX}$	$I_{ss,MAX}$ @ 25 °C	$R_{ss,on}$ @ 25 − 150 °C	$C_{oss,Q}$ @ 400 V	$C_{rss,Q}$	FoM = $(R_{ss,on}Q_{oss})^{-1}$ @ 25 °C − 400 V	Package Size
Panasonic Co.	EDLS06SMD		±600 V	92 A	26 − 43 mΩ	190 pF	40 pF	506 MHz/V	2.3 cm²
GaN Systems Inc.	GS66516	(1x)	650 V	60 A	25 − 65 mΩ	281 pF	8 pF	355 MHz/V	1.0 cm²
		(4x)	±650 V	120 A		562 pF	16 pF	178 MHz/V	4.0 cm²

III. Three-Phase Two-Third-Modulated Buck-Boost Current Source Inverter System

The operating principle of the selected 3-Φ bB CSI system is described in this section. Afterwards, the proposed *Two-Third Modulation* (TTM) and associated *Synergetic Control* structure are explained with the support of simulation results.

A. Operating Principle

The 3-Φ bB CSI system illustrated in **Fig. 1** is herein simplified to the circuit shown in **Fig. 4** (cf. **Fig. 13** in [23]) to explain its basic functioning in motor operation, i.e. with power flowing from the DC-source to the electric machine. For this purpose, the buck converter and the DC-link inductor L_{dc} are replaced by the current source $i_{dc} > 0$, whereas the 3-Φ inverter is represented by the two *three-position* switches T_h and T_l.

The two output terminals tapped by the two switches define the one state of the 3-Φ inverter among overall nine (3^2) possibilities; e.g., in **Fig. 4**, a transition from state [ab] to [ac] is illustrated. The three shoot-through states [aa], [bb] and [cc] are denominated *zero states* in contrast to the remaining six states denominated *active states*. In the *zero states*, the 3-Φ inverter short circuits the DC-link terminals p and n whereas, in the *active states*, it connects the load L_o-R_o between them. Consequently, depending on the selected state, the DC-link voltage v_{pn} varies between 0 V (*zero states*) and the six line-to-line voltages $\pm v_{ab}$, $\pm v_{bc}$ and $\pm v_{ca}$ (*active states*), while the switching stage output currents $i_{a,sw}$, $i_{b,sw}$ and $i_{c,sw}$ can either assume the value of 0 A (*zero states*) or $\pm i_{dc}$ (*active states*). Hence, by appropriately switching T_h and T_l, and output filtering (through the output capacitors C_o), i_{dc} can be modulated and transformed into the continuous load currents i_a, i_b and i_c flowing through L_o-R_o.

B. Conventional Pulse-Width Modulation (PWM)

In a typical 3-Φ bB CSI system, the buck converter controls i_{dc} to a constant value I_{dc}, while the 3-Φ inverter is responsible for generating the sinusoidal load currents i_a, i_b and i_c with peak value $\hat{i}_{out} \leq I_{dc}$ ($m_{dc/ac} = \hat{i}_{out}/I_{dc}$). In **Fig. 6(a)**, **7(a)** and **8(a)**, the most significant waveforms of the 3-Φ inverter are summarized for the operating point specified in **Table II**. In these figures, the encircled numbers define the six symmetric sectors forming the overall output period $1/f_{out}$.

TABLE II: Circuit specifications considered in the simulations of the 3-Φ bB CSI system shown in **Fig. 6**, **7**, **8** and **10**.

	Description	Value	Figure
I_{dc}	DC-link current	20 A	**6(a)**
$\hat{i}_{out}$	peak load current	18.5 A	**6** and **10**
$\hat{v}_{out}$	peak output voltage	270 V	**10**
f_{out}	output frequency	50 Hz	
$\cos(\phi)$	power factor	~ 1	**6**, **7** and **8**
		0.707	**10**
P_{out}	output power	7.5 kW	**6**, **7** and **8**
		5.3 kW	**10**

In each interval of **Fig. 6(a)**, three of the six 2G MB GaN e-FETs forming the 3-Φ inverter are operated with PWM, i.e. are switched with switching frequency f_{sw}. For example in sector ①, characterized by $i_a > |i_b|$ and $i_a > |i_c|$, $T_{a,h}$ is permanently ON while $T_{b,h}$ and $T_{c,h}$ are permanently OFF, and all three low-side switches $T_{i,l}$ are alternately switched within a switching period $1/f_{sw}$. In other words, the states [aa], [ab] and [ac] are alternately applied since, as visible in the space vector diagram of **Fig. 5(a)**, these are (in this sector) the closest neighbors of the phasor of the reference load current $\vec{i}^*$, having $|\vec{i}^*| = m_{dc/ac} I_{dc} = \hat{i}_{out}$. Hence, $\vec{i}^*$ can be expressed as

$$\frac{\vec{i}^*}{I_{dc}} = \delta_{[aa]} \cdot [aa] + \delta_{[ab]} \cdot [ab] + \delta_{[ac]} \cdot [ac], \tag{1}$$

where $\delta_{[xy]}$ indicates the duty-cycle of the state [xy].

In **Fig. 6**, the gate control signal of each 2G MB GaN e-FET $T_{i,j}$, i.e. $s_{Ti,j}$, and its average within $1/f_{sw}$, i.e. $\bar{s}_{Ti,j}$, are additionally shown. The conversion from $\delta_{[xy]}$ to $\bar{s}_{Ti,j}$ is immediately deduced from **Fig. 4**

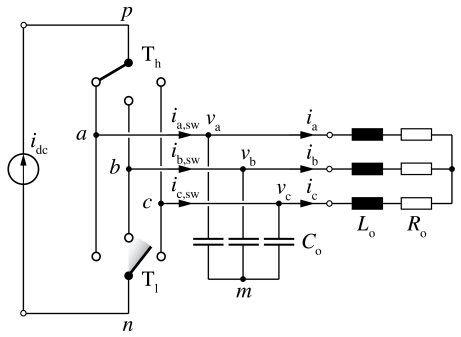


Fig. 4: Simplified representation of the 3-Φ bB CSI system of **Fig. 1**. The two *three-position* switches T_h and T_l, modulating $i_{dc} > 0$ by alternately connecting the output terminals a, b and c to the DC-link terminals p and n, model the operation of the 3-Φ inverter in a VSD application.

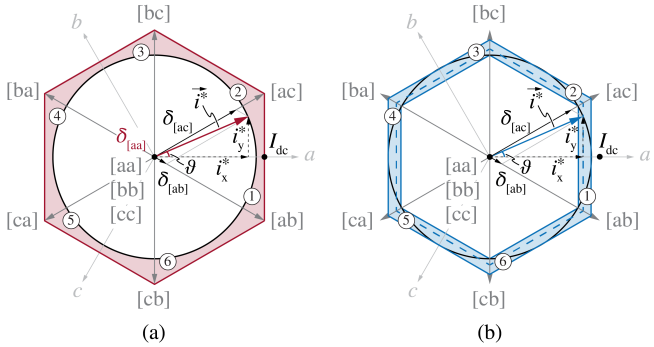


Fig. 5: Space vector diagram highlighting the nine states of the 3-Φ inverter and the phasor of the reference load current $\vec{i}^*$, where **(a)** represents the case of conventional PWM with the apothem of the hexagon fixed to I_{dc}, while in **(b)** the size of the hexagon is scaled according to *Two-Third Modulation*.

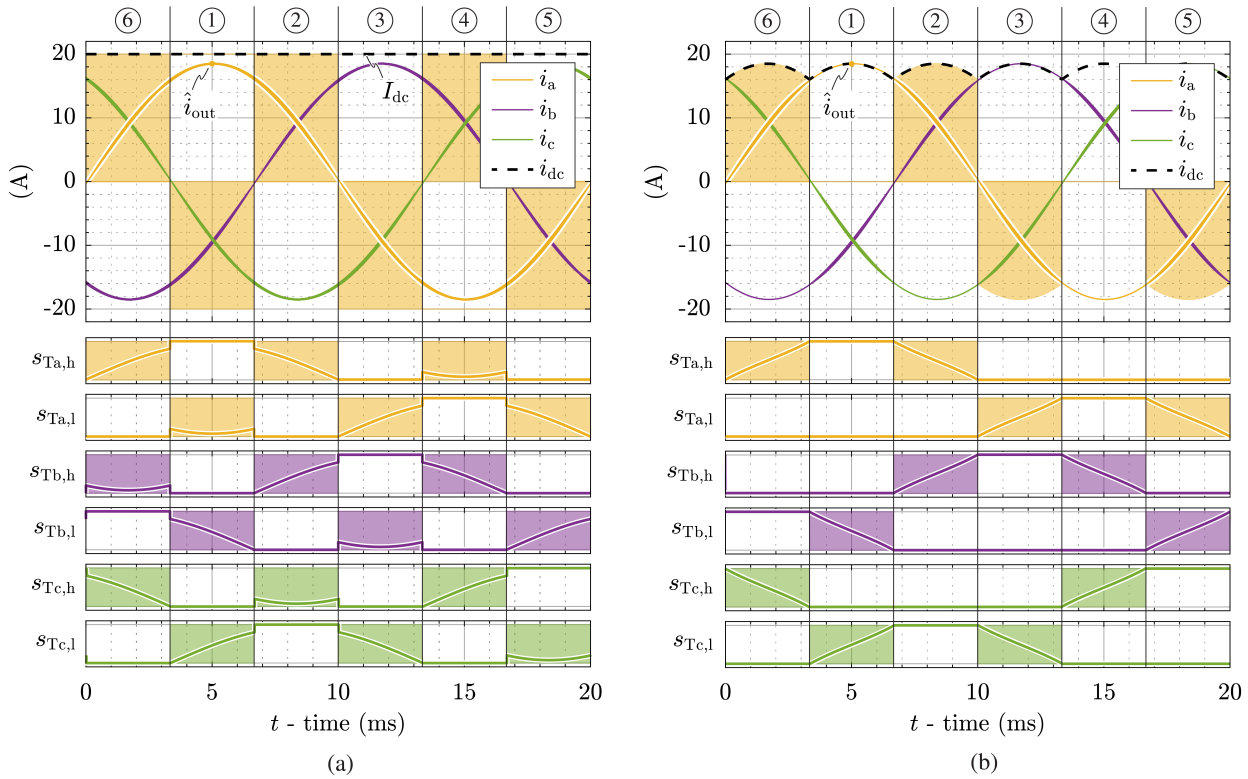


Fig. 6: DC-link current i_{dc}, sinusoidal load currents i_a, i_b and i_c with peak value $\hat{i}_{out}$ and gate control signals $s_{Ti,j}$ within one output period $1/f_{out}$ in case **(a)** conventional PWM is applied ($i_{dc} = I_{dc}$) and **(b)** *Two-Third Modulation* is applied ($i_{dc} = \max\{|i_a|, |i_b|, |i_c|\}$, neglecting the currents flowing in the output capacitors C_o) for the operating point specified in **Table II**. The encircled numbers define the six symmetric intervals of the output period. The colored lines in the graphs of $s_{Ti,j}$ correspond to their average $\bar{s}_{Ti,j}$ in a switching period $1/f_{sw}$. Further details are shown in **Fig. 7** and **8**.

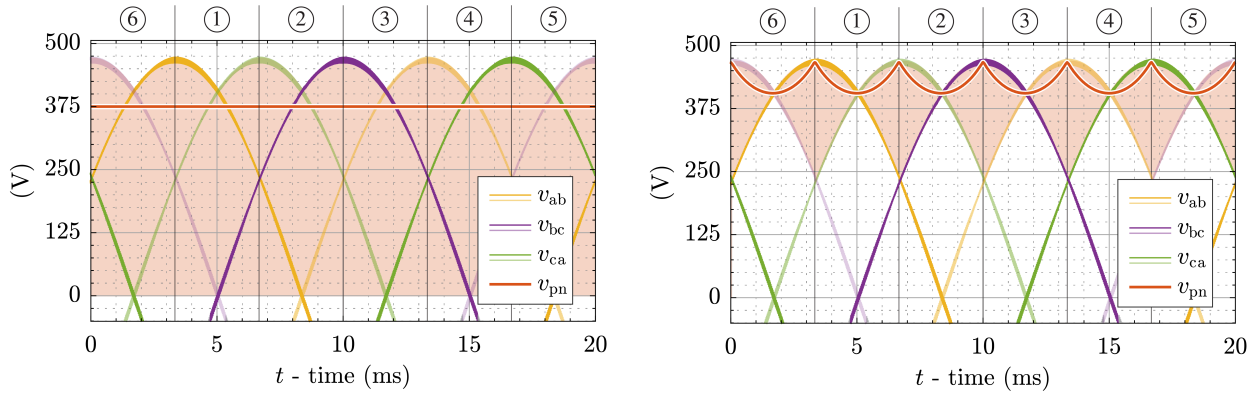


Fig. 7: Sinusoidal line-to-line voltages $\pm v_{ab}$, $\pm v_{bc}$ and $\pm v_{ca}$, and DC-link voltage v_{pn} within one output period $1/f_{out}$ in case **(a)** conventional PWM is applied and **(b)** *Two-Third Modulation* is applied for the operating point specified in **Table II**. The red lines correspond to the average DC-link voltage $\bar{v}_{pn}$ in a switching period $1/f_{sw}$. Further details are shown in **Fig. 6** and **8**.

and can be expressed as

$$\bar{s}_{Ti,h} = \sum_{y = a,\,b,\,c} \delta_{[iy]}, \qquad \bar{s}_{Ti,l} = \sum_{x = a,\,b,\,c} \delta_{[xi]} \qquad (i = a,\, b,\, c) \tag{2}$$

Furthermore, from **Fig. 5(a)**, the duty-cycles of the *active states* $\delta_{[ab]}$ and $\delta_{[ac]}$ can be derived from the projections of $\vec{i}^*$ according to

$$\frac{|\vec{i}^*|}{I_{dc}} \begin{bmatrix} \cos\vartheta \\ \sin\vartheta \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} \delta_{[ac]} \\ \delta_{[ab]} \end{bmatrix} \qquad (-\pi/6 < \vartheta < \pi/6). \tag{3}$$

The remaining fraction of the switching period is accounted for the *zero state*, whose duty-cycle $\delta_{[aa]}$ is calculated as

$$\delta_{[aa]} = 1 - (\delta_{[ac]} + \delta_{[ab]}) = 1 - m_{dc/ac} \cos\vartheta \geq 1 - \cos\vartheta \geq 0. \tag{4}$$

It should be noticed in (4) that even if $|\vec{i}^*| = I_{dc}$, $\delta_{[aa]}$ is always larger than zero (except for the point in time in the middle of ①, i.e. for $\vartheta = 0$, where $\delta_{[aa]} = 0$). Hence, a free-wheeling interval, i.e. an interval during which I_{dc} bypasses the load flowing through $T_{a,h}$ and $T_{a,l}$, is present during every switching period forming ①. Finally, since (3) and (4) can be extended for symmetry of the phases

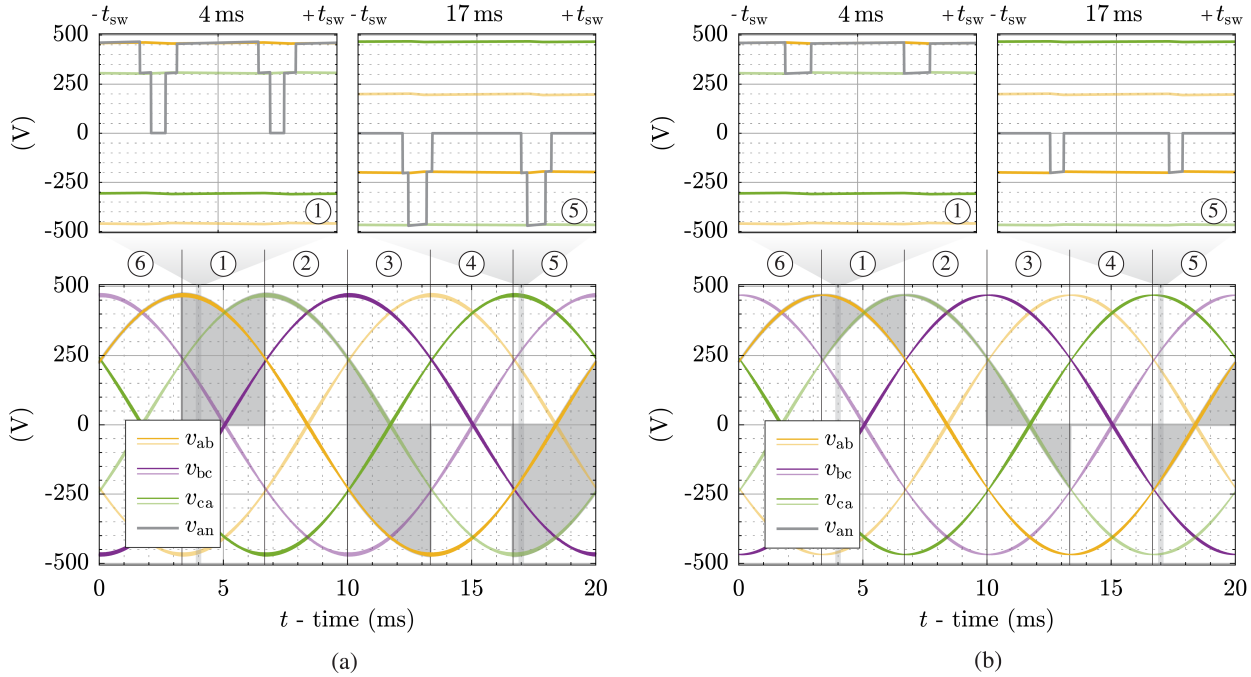


Fig. 8: Sinusoidal line-to-line voltages $\pm v_{ab}$, $\pm v_{bc}$ and $\pm v_{ca}$, and source-source voltage of $T_{a,l}$, i.e. v_{an}, within one output period $1/f_{out}$ in case **(a)** conventional PWM is applied and **(b)** *Two-Third Modulation* is applied for the operating point specified in **Table II**. The graphs in the upper part offer a zoomed view of v_{an} during a switching period $1/f_{sw}$. Further details are shown in **Fig. 6** and **7**.

to the other five sectors (from ② to ⑥), it can be concluded that *zero states* are always necessary with conventional PWM, i.e. the *zero state* and the two *active states* contribute to each switching period.

C. Two-Third Modulation and Synergetic Control [24]

1) Two-Third Modulation: According to **Section III-B**, a *zero state* free modulation should be preferred to maximize the efficiency of the 3-Φ bB CSI system. In fact, the transitions to (and from) the *zero states* cause additional switching losses and, during the *zero states* themselves, conduction losses occur even though no power is transferred to the load. Additionally, *zero states* are responsible for generating the highest common-mode voltage [25]. Hence, rewriting (4) for $\delta_{[aa]} = 0$,

$$i_{dc} = \hat{i}_{out} \cos\vartheta = i_a \qquad (-\pi/6 < \vartheta < \pi/6) \tag{5}$$

is obtained. For symmetry, (5) can be generalized to

$$i_{dc} = \max\{|i_a|, |i_b|, |i_c|\}, \tag{6}$$

which is valid for the entire output period, neglecting the currents flowing in C_o. In other words, if the buck converter controls and shapes i_{dc} to be equal to the instantaneous largest load current absolute value, e.g. to i_a during ①, the free-wheeling interval is avoided (since, e.g. again during ①, $i_{dc} - i_a = 0$).
Following this approach, only the two *active states* [ab] and [ac] (instead of all three states) are applied within one switching period; consequently, $T_{a,l}$ is permanently OFF and only two ($T_{b,l}$ and $T_{c,l}$) instead of three 2G MB GaN e-FETs are alternately switched, as illustrated in **Fig. 6(b)**. Accordingly, this concept is named *Two-Third Modulation* (TTM) and, as already speculated and further discussed in **Section IV-C**, it enables a significant reduction of switching losses. As a consequence of (6), the average DC-link voltage $\bar{v}_{pn}$ in **Fig. 7(b)** is not constant as in **Fig. 7(a)** but still guarantees a constant power $\bar{v}_{pn} i_{dc}$ at the input of the 3-Φ inverter. Moreover, since the *zero states* are avoided, the DC-link voltage v_{pn} never assumes the value 0 V.

In **Fig. 8** the voltage v_{an} across $T_{a,l}$ is indicated for completeness. During ① in **Fig. 8(b)**, generated applying TTM, v_{an} varies between v_{ab} and $-v_{ca}$, while in **Fig. 8(a)**, where conventional PWM is considered, it also reaches 0 V. The same reasoning can be extended to ⑤, where the three closest neighboring states are [ca], [cb] and [cc] (see **Fig. 5**), yielding to v_{an} not assuming the value of $-v_{ca}$ in **Fig. 8(b)**.
Finally, the effect of TTM in the space vector plane is highlighted in **Fig. 5(b)**. Adjusting i_{dc} as described translates into continuously scaling the dimensions of the hexagon such that its perimeter matches the trajectory defined by $\vec{i}^*$, resulting in $\delta_{[ac]} + \delta_{[ab]} = 1$, i.e. $\delta_{[aa]} = 0$.

2) Synergetic Control: A key requirement for TTM is a precise control and shaping of i_{dc}. For this purpose, the control structure illustrated in **Fig. 9** is proposed and described in the following.
The first part (**Fig. 9(a)**), shown only for phase a for the sake of brevity, consists of a *Proportional-Integral* (PI) output current controller with an inner PI output voltage controller. The reference load current i_a^* and output voltage v_a^* are compared with their measured counterparts i_a and v_a to generate the reference filter capacitor current $i^*_{Co,a}$. Feed-forwarding i_a^*, the reference switching stage output current $i^*_{a,sw}$ is finally obtained.
The second part (lower branch of **Fig. 9(b)**) calculates the nine $\delta_{[xy]}$ from the three $i^*_{i,sw}$ according to the procedure described in (3) and converts them in the six $\bar{s}_{Ti,j}$ as given in (2). Hence, it combines the six $\bar{s}_{Ti,j}$ with the measured v_a, v_b and v_c to calculate

$$\bar{v}_{pn} = \sum_{i\,=\,a,\,b,\,c} (\bar{s}_{Ti,h} - \bar{s}_{Ti,l}) v_i. \tag{7}$$

The third and last part (upper branch of **Fig. 9(b)**) transforms $i^*_{i,sw}$ in the reference DC-link current i^*_{dc} as defined in (6) and, with a conventional PI current controller, calculates the duty-cycle $\bar{s}_{Tdc,h}$ for the buck converter.
To conclude this section, the output waveforms of the 3-Φ bB CSI system, obtained implementing the described TTM and *Synergetic*

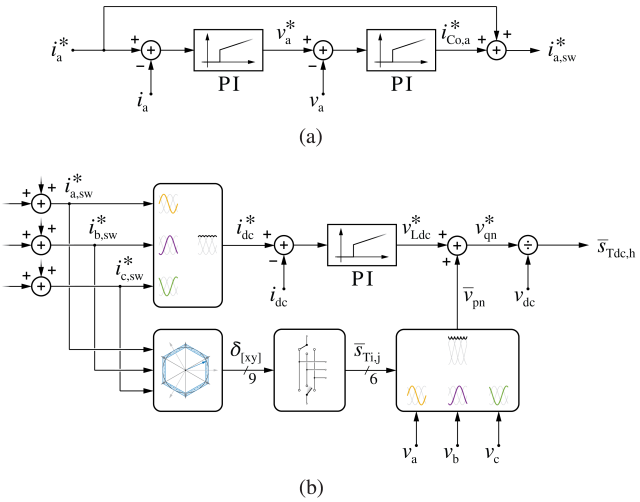


Fig. 9: Structure of the *Synergetic Control* combining the regulation and shaping of the DC-link current i_{dc} with *Two-Third Modulation*, where **(a)** generates the reference bridge-leg output current $i^*_{a,sw}$, while **(b)** calculates the duty-cycles of the buck converter $\bar{s}_{Tdc,h}$ and of the 3-Φ inverter $\bar{s}_{Ti,j}$.

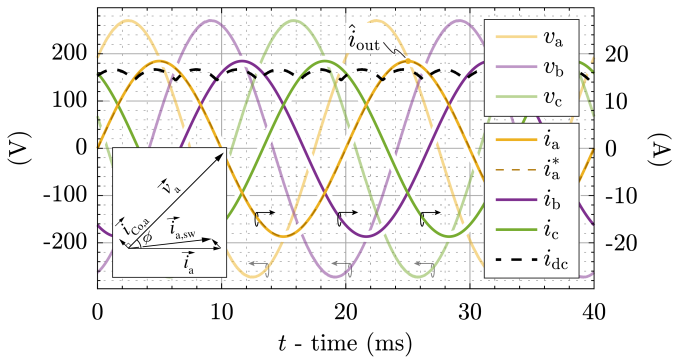


Fig. 10: DC-link current i_{dc}, sinusoidal load currents i_a, i_b and i_c with peak value $\hat{i}_{out}$, sinusoidal reference load current of phase a i^*_a and sinusoidal output voltages v_a, v_b and v_c obtained implementing *Two-Third Modulation* and the associated *Synergetic Control* structure in a circuit simulation environment for the operating point specified in **Table II**. The phasor diagram highlights the difference $i_{Co,a}$ between $i_{a,sw}$ and i_a.

Control structure in a circuit simulation environment, are shown in **Fig. 10** for the operating point specified in **Table II**. Differently from the ideal case considered in **Fig. 6(b)**, **7(b)** and **8(b)**, the discrepancy between $\hat{i}_{out}$ and i_{dc} due to $i_{Co,i}$ is evident in **Fig. 10**. Nevertheless, the reference i^*_a is perfectly tracked by i_a.

IV. Analysis of the Two-Third Modulation

With the basic understanding of TTM applied to the selected 3-Φ bB CSI system provided in **Section III**, advanced considerations, focused on the enabled reduction of switching losses, are briefly described in the following.

A. Range of Applicability

In case conventional PWM is considered, the relation between the modulation index $m_{dc/ac}$ of the 3-Φ inverter and the duty-cycle $\bar{s}_{Tdc,h}$ of the buck converter can be deduced from the power balance of the 3-Φ inverter which, neglecting the losses, can be expressed as

$$P_{out} = \frac{3}{2}\hat{v}_{out}\hat{i}_{out}\cos(\phi) = \bar{s}_{Tdc,h}V_{dc}I_{dc}. \tag{8}$$

Solving (8) for $m_{dc/ac}$,

$$\frac{\hat{i}_{out}}{I_{dc}} = m_{dc/ac} = \bar{s}_{Tdc,h}\frac{V_{dc}}{\hat{v}_{out}}\frac{2}{3}\frac{1}{\cos(\phi)} \tag{9}$$

is obtained. Since the ratio $m_{dc/ac}/\bar{s}_{Tdc,h}$ is proportional to the input/output voltage ratio $V_{dc}/\hat{v}_{out}$, different combinations of $m_{dc/ac}$ and $\bar{s}_{Tdc,h}$ result in the same voltage gain. In other words, the bucking and boosting efforts can be freely distributed between the input and output stages.

Differently, in case TTM is considered, $I_{dc} = \hat{i}_{out}\cos(\vartheta)$ must be inserted in (9) and

$$\bar{s}_{Tdc,h} = \frac{\hat{v}_{out}}{V_{dc}}\frac{3}{2}\frac{\cos(\phi)}{\cos(\vartheta)} = \frac{\hat{v}_{out,ll}}{V_{dc}}\frac{\sqrt{3}}{2}\frac{\cos(\phi)}{\cos(\vartheta)} \tag{10}$$

results after solving for $\bar{s}_{Tdc,h}$ and introducing the peak line-to-line output voltage $\hat{v}_{out,ll} = \sqrt{3}\,\hat{v}_{out}$. Comparing (9) with (10), it can be observed how the degree of freedom given by $m_{dc/ac}$ is lost in the second case. Furthermore, since $\bar{s}_{Tdc,h} \leq 1$, TTM can be applied only if (cf. (10)),

$$V_{dc} \geq \hat{v}_{out,ll}, \tag{11}$$

where the maximum value of $\cos(\phi)$, i.e. 1, and the minimum value of $\cos(\vartheta)$ during ①, i.e. $\sqrt{3}/2$, are considered.

When (11) holds, the 3-Φ bB CSI system is operated in buck-mode, i.e. the 3-Φ inverter only modulates i_{dc} according to TTM. If $V_{dc} < \hat{v}_{out,ll}$, instead, the buck converter can no longer control i_{dc}, since $\bar{v}_{pn}$ exceeds V_{dc}; consequently, $m_{dc/ac} < 1$ is necessary to reduce $\bar{v}_{pn}$ and conventional PWM must be used. In practice, the range of applicability of TTM should be defined in the design phase of the 3-Φ bB CSI system, opportunely selecting $\hat{v}_{out}$ and V_{dc}.

B. Conduction Losses

Since i_{dc} continuously flows through L_{dc} and always two MB GaN e-FETs, the conduction losses occurring in the 3-Φ inverter are proportional to the *Root-Mean-Square* (RMS) value of i_{dc}, i.e. $i_{dc,RMS}$. Considering i_{dc} given by (6),

$$i_{dc,RMS} = \sqrt{\frac{1}{\pi/3}\int_{-\pi/6}^{+\pi/6}\hat{i}^2_{out}\cos^2(\vartheta)\,d\vartheta} = 0.96\cdot\hat{i}_{out} \tag{12}$$

results. Consequently, for a given operating point, the conduction losses, which are quadratically dependent on $i_{dc,RMS}$, reduce by at least 8 % in case TTM is applied. Similarly, the average value of i_{dc} given by (6) can be calculated, obtaining $i_{dc,avg} = 3/\pi\ \hat{i}_{out} = 0.95\cdot\hat{i}_{out}$.

C. Switching Losses

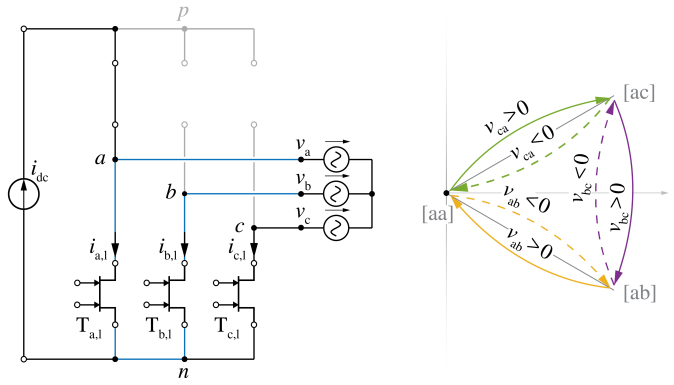
The missing piece to complete the structure of the *Synergetic Control* shown in **Fig. 9** is the transformation of the nine $\delta_{[xy]}$ (or of the equivalent six $\bar{s}_{Ti,j}$) into the actual gate signals $s_{Ti,j}$. Hence, the switching sequence according to which apply the three neighboring states within $1/f_{sw}$ must be defined. Each sequence differently influences several performance indexes of the 3-Φ bB CSI system [18], but only the switching losses are considered in the following.

For determining this sequence, a simplified representation of the 3-Φ inverter, valid during ①, is introduced in **Fig. 11(a)**. Only the three low-side switches $T_{i,l}$ are considered, since the switching state of the three high-side switches $T_{i,h}$ is fixed, i.e. $T_{a,h}$ is permanently ON while $T_{b,h}$ and $T_{c,h}$ are permanently OFF. It can be recognized that the three line-to-line voltages v_{xy} are applied across each pair of low-side switches $T_{x,l}$ and $T_{y,l}$, and that one of them in turn conducts i_{dc}. Therefore, the series connection of $T_{x,l}$ and $T_{y,l}$ can be considered as a bridge-leg configuration supplied from v_{xy} and having the negative DC-link terminal n as switch node, sinking i_{dc}. Consequently, the switching transition between two states, e.g. from [ab] to [ac], is

nothing else than the commutation of the bridge-leg formed by $T_{b,l}$ and $T_{c,l}$, supplied by v_{bc}. Assuming $i_{dc} > 0$ and practically constant, on the one hand the sign of v_{xy} determines whether a switching transition is soft or hard, while on the other hand the actual value of v_{xy} determines the occurring switching losses.

Fig. 11(b) and **Fig. 12** summarize the above mentioned statements. In particular in **Fig. 11(b)**, the three states considered in ① are indicated and connected by arrows whose directions highlight under which condition of v_{xy} (solid line for $v_{xy} > 0$ and dashed line for $v_{xy} < 0$), the indicated state transition causes a hard commutation. Soft commutations, occurring in the opposite direction, are considered loss-less and therefore neglected herein.

As already mentioned, the amplitude of the switched voltage defines the amount of losses generated in a hard transition. However, the three v_{xy} are not constant, but function of ϕ and of the instantaneous phase ϑ, once $\hat{v}_{out}$ is fixed. Accordingly, **Fig. 12** shows the average line-to-line voltages $\langle v_{xy} \rangle$ as a function of ϕ and normalized with respect to $\hat{v}_{out}$. Angular brackets $\langle \cdot \rangle$ are used to indicate the averaging over ①, i.e. over the $\pi/3$-wide output period interval having $-\pi/6 < \vartheta < \pi/6$. For convenience, positive and negative v_{xy} are averaged separately, obtaining $\langle v_{xy}^{+} \rangle$ (continuous lines) and $\langle v_{xy}^{-} \rangle$ (dashed lines), such that each line in **Fig. 12** directly relates to one arrow in **Fig. 11(b)**.



(a) (b)

Fig. 11: (a) Simplified representation of the 3-Φ inverter shown in **Fig. 1**. **(b)** Zoom of **Fig. 5** with arrows whose directions highlight under which condition of the output line-to-line voltage v_{xy} (solid line for $v_{xy} > 0$ and dashed line for $v_{xy} < 0$), the indicated transition causes a hard commutation of the corresponding bridge-leg shown in **(a)**.

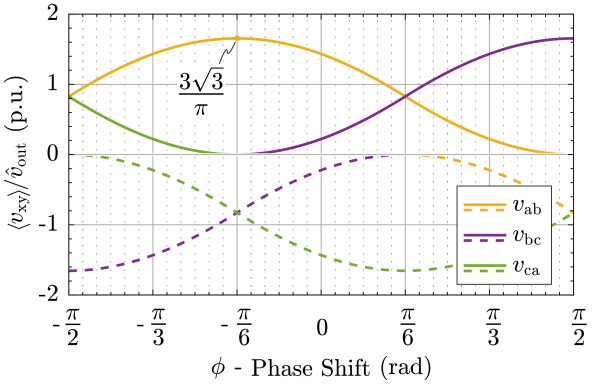


Fig. 12: Normalized average line-to-line voltages $\langle v_{xy} \rangle$ as function of the phase shift ϕ. Positive and negative line-to-line voltages v_{xy} are averaged separately, obtaining $\langle v_{xy}^{+} \rangle$ (continuous lines) and $\langle v_{xy}^{-} \rangle$ (dashed lines). When v_{xy} is always positive (negative), the dashed (continuous) line of corresponding color is 0.

E.g. at $\phi = -\pi/6$, $\langle v_{ab}^{+} \rangle = 3\sqrt{3}/\pi \ \hat{v}_{out}$ features a maximum while $\langle v_{ab}^{-} \rangle = 0$, since $v_{ab} > 0$; hence, the state transition from [ab] to [aa] (continuous yellow line) corresponds to a hard commutation with maximum switching losses, while the transition in the opposite direction (from [aa] to [ab], dashed yellow line) is loss-less. For the same ϕ, the two state transitions from [ab] to [ac] and from [ac] to [aa] (dashed purple and green lines respectively) result as well in hard commutations, however, since $\langle v_{bc}^{-} \rangle = \langle v_{ca}^{-} \rangle = -3\sqrt{3}/2\pi \ \hat{v}_{out}$, much lower switching losses occur. The state transitions in the opposite directions (continuous purple and green lines) are again loss-less, since $\langle v_{bc}^{+} \rangle = \langle v_{ca}^{+} \rangle = 0$.

In a complete switching period, a closed path along the graph of **Fig. 11(b)** must be walked. However, depending on ϕ and ϑ, the sequence of state transitions must be carefully selected, since different sequences correspond to switching different v_{xy} (and accordingly $\langle v_{xy} \rangle$), i.e. to different switching losses.

When conventional PWM is applied, all states must be included in the switching sequence, which can be achieved with three or four transitions (in the simplest cases). The two (clockwise and counter-clockwise) sequences formed by three transitions are asymmetric concerning the generated v_{pn} in a switching period and can result in one or two hard-switching transitions, depending on the sign of each v_{xy}. The three sequences formed by four transitions, instead, showing a symmetry with respect to one state, result in symmetric v_{pn} and always in two hard-switching transitions. When TTM is applied, instead, only the two *active states* have to be passed through; hence, this switching sequence requires only two transitions, only one of which is hard. The six switching sequences discussed above are summarized in **Table III**.

Two different sequences can be observed comparing the zoom on v_{an} during ① and ⑤ on top of **Fig. 8(a)** and **(b)**. The latter is obtained applying TTM whereas the first one applying the [ac]-symmetric sequence of conventional PWM .

After determining each $\langle v_{xy} \rangle$ as function of ϕ (see **Fig. 12**), the losses originated from each state transition, i.e. from each hard-switching transition, can be calculated and summed according to the selected state sequence (see **Table III**) to analytically approximate the switching losses $P_{sw} = E_{sw} f_{sw}$ occurring in the 3-Φ inverter. For each sequence, the cumulative switching energy

$$E_{sw} = \sum_{xy \ \in \ path} C_{oss,Q} \langle v_{xy} \rangle^2 + \frac{|\langle v_{xy} \rangle| i_{dc,avg}}{2} \left(\frac{|\langle v_{xy} \rangle|}{dv/dt} + \frac{i_{dc,avg}}{di/dt} \right) \quad (13)$$

is obtained if the conventional VI-overlap switching loss model is considered [5].

The results of this calculation repeated for all the state sequences listed in **Table III** are summarized in **Fig. 13**. It can be observed that TTM outperforms PWM, as already speculated, especially for low values of ϕ. The introduced approach allows to quantify this advantage and to more deeply understand its origin. In fact, TTM not only requires only one hard transition, but, as well, the switched voltages $\langle v_{bc}^{+} \rangle$ and $|\langle v_{bc}^{-} \rangle|$ are the smallest among all $|\langle v_{xy} \rangle|$ for low values of ϕ, further increasing the advantage. Only for $|\phi| > \pi/3$, $\langle v_{bc}^{+} \rangle$ and $|\langle v_{bc}^{-} \rangle|$ feature a maximum; hence, all sequences avoiding the transitions from [ab] to [ac] and viceversa result in lower switching losses.

In order to obtain the overall optimum state sequence, also two or more sequences can be combined, not only depending on ϕ, but eventually also on ϑ [26]. E.g., the anti-clockwise asymmetric sequence should be preferred to TTM for $\phi > +\pi/3$. However, TTM can nevertheless be applied if $\delta_{[aa]} = 0$, i.e. if [aa] is used only as a transitory state between [ac] and [ab] to avoid the most lossy switching transition associated to the direct commutation form [ac] to [ab].

TABLE III: Five state sequences connecting all the three states indicated in the graph of **Fig. 11(b)** as required for conventional PWM and sixth state sequence enabled by *Two-Third Modulation* (TTM) avoiding the *zero state* and requiring only two transitions.

Modulation	State Sequence	Note
PWM	... [ab], [aa] [ac] [ab], [aa] ...	cw-asym
	... [ac], [aa] [ab] [ac], [aa] ...	ccw-asym
	... [ac], [ac] [aa] [ab] [aa] [ac], [ac] ... ... [ab], [ab] [aa] [ac] [aa] [ab], [ab] ...	[aa]-sym
	... [aa], [aa] [ab] [ac] [ab] [aa], [aa] ... ... [ac], [ac] [ab] [aa] [ab] [ac], [ac] ...	[ab]-sym
	... [aa], [aa] [ac] [ab] [ac] [aa], [aa] ... ... [ab], [ab] [ac] [aa] [ac] [ab], [ab] ...	[ac]-sym
TTM	... [ac], [ab] [ac], [ab] ...	

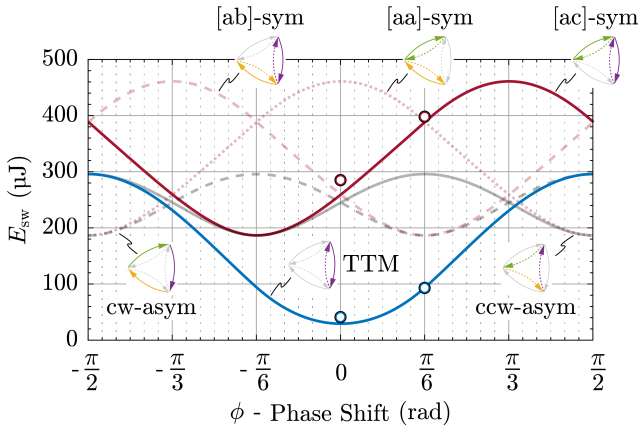


Fig. 13: Cumulative switching energy E_{sw} in a switching period $1/f_{sw}$ of the 3-Φ inverter shown in **Fig. 1** for the operating point specified in **Table II** as function of the phase shift ϕ and of the selected state sequence (see **Table III**). The thicker lines highlight E_{sw} associated to the [ac]-symmetric sequence of conventional PWM (red, **Fig. 8(a)**) and to *Two-Third Modulation* (blue, **Fig. 8(b)**) while the dots, resulting from the corresponding calculation in the simulation environment, prove the goodness of the developed analytic procedure.

To prove the correctness of the developed analytic procedure, the occurring switching losses are calculated in the simulation environment for the two operating points specified in **Table II**. The results for the case of the [ac]-symmetric sequence of conventional PWM (**Fig. 8(a)**) and of TTM (**Fig. 8(b)**) are indicated with dots in **Fig. 13**, confirming the accuracy of the method. The small discrepancy between analytic calculation and simulation is attributed to the considered hypotheses, e.g. averaging of v_{xy}, constant i_{dc} and loss-less soft-switching transitions.

In summary it should be pointed out that, in particular for $\phi \approx 0$, which is typical for VSDs employing synchronous machines or for grid connected inverters, the reduction of switching losses enabled by TTM amounts to 86 %, i.e.

$$\frac{E_{sw,TTM}}{E_{sw,PWM}} = 0.14. \tag{14}$$

V. Experimental Results

A test bench for the 2G MB GaN e-FETs introduced in **Section II** is realized as illustrated in **Fig. 14(a)**, **(b)** and **(c)**. It mainly consists of the three switches forming one side (e.g. the low-side) of the 3-Φ inverter presented in **Fig. 1**, since, as clarified in **Section IV-C**, this is sufficient, due to symmetry properties, to quantify the losses occurring in the entire 3-Φ structure. In addition to the three $T_{i,l}$, the realized PCB includes their respective gate drivers [22] (see **Fig. 3(b)**) with isolated signal transmission and isolated power supply, and a fraction of the overall C_o [27].

In particular, the bridge-leg formed by $T_{a,l}$ and $T_{b,l}$, highlighted in **Fig. 14 (d)**, is considered in the following. This bridge-leg is operated connecting a DC-voltage source V_{ba} between the terminals b and a, and a resistive-inductive load at the switching node terminal n to sink the output current i_{dc}. Measured waveforms of the switch node voltage v_{na} and of i_{dc} are recorded and plotted in **Fig. 15(a)** for $V_{ba} = 400\,\text{V}$ and $i_{dc,avg} = 5\,\text{A}$ (blue) and $0\,\text{A}$ (red). No significant over voltage and oscillation phenomena are observed on v_{na}, while a soft transition, a zero current transition and a hard transition are performed at switching speeds $^{dv}/_{dt}$ of about $15\,^{\text{V}}/_{\text{ns}}$. The voltage slope occurring for the soft transition confirms the expected $C_{oss,Q}$ value according to $2\,C_{oss,Q} = {}^{i_{dc}}/_{dv/dt}$ (cf. **Table I**).

For 2G MB GaN e-FETs (and AC-switches in general), particular care must be taken during the switching transition, such that always a path for the switched current is provided while one of the two switches blocks the bipolar switched voltage (see **Fig. 3(a)**). Hence, in this setup, the four gate signals $s_{Ti,lp}$ and $s_{Ti,ln}$ are generated according to the current driven multi-step commutation strategy [12], as illustrated in the lower part of **Fig. 15(b)** and **(c)** for the case of $i_{dc} > 0$. Additionally, the zoomed view of the measured v_{na} is overlapped with the equivalent circuits of the bridge-leg (I, II and III) determined by $s_{Ti,lp}$ and $s_{Ti,ln}$ (see **Fig. 3(a)**). These plots highlight how, depending on the type of switching transition, i.e. soft, zero current or hard, the commutation takes place at different instants of the multi-step sequence.

VI. Circuit Topology Variants and Future Research

Although only the 3-Φ bB CSI system shown in **Fig. 1** is discussed in the previous sections, several circuit topology variants are subject of ongoing research. Two examples, featuring additionally common-mode filter inductors, are indicated in **Fig. 16**. In particular, **Fig. 16(a)** illustrates an extension of the approach presented in **Fig. 1** where the DC-link inductor and the buck converter are split to form a symmetric multi-level buck-type DC/DC converter input stage [28]. **Fig. 16(b)**, instead, depicts a back-to-back approach capable of 3-Φ AC/AC conversion obtained by replicating and transforming the 3-Φ inverter into a 3-Φ buck-type current DC-link rectifier front-end [29], [30].

Both 3-Φ bB CSI systems can benefit from the advantages enabled by TTM, however, a significant difference between them should be noticed. In the solutions proposed in **Fig. 1** and **Fig. 16(a)**, in fact, the direction of power flow can be inverted only by inverting the direction of the DC-link current, while in the concept proposed in **Fig. 16(b)**, also a negative DC-link voltage is feasible. The latter option enables a simplified control structure and higher control dynamics concerning the inversion of power flow.

Furthermore, the possibility of replacing the normally-off 2G MB GaN e-FETs with a normally-on equivalent (shown blue in **Fig. 16**) in at least one of the bridge-legs forming the 3-Φ inverters and rectifiers is under investigation [31]. This approach makes the 3-Φ bB CSI systems robust with respect to an unexpected loss of gate voltage supply, since the normally-on devices would still provide a path allowing to safely discharge the DC-link inductors.

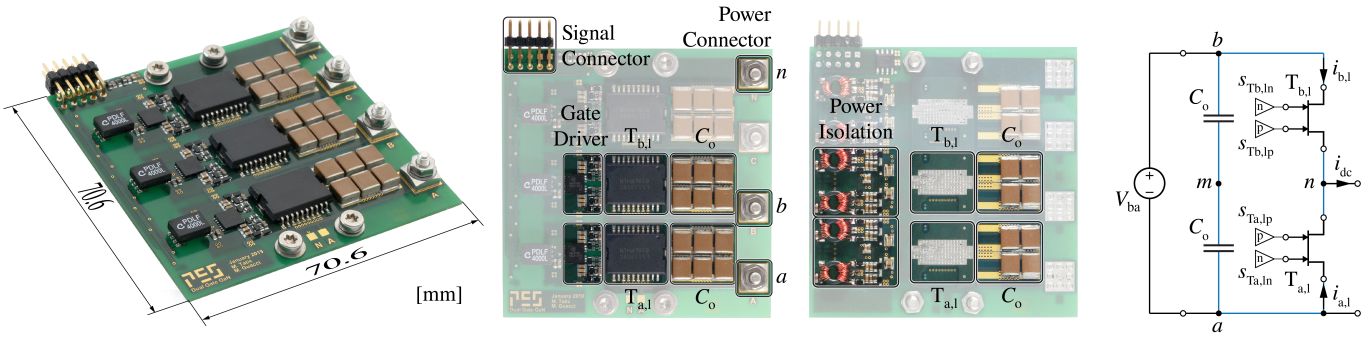


Fig. 14: **(a)** Perspective view, **(b)** top view and **(c)** mirrored bottom view of the test bench PCB including the three 2G MB GaN e-FETs $T_{i,l}$ forming the low-side of the 3-Φ inverter topology presented in **Fig. 1**, their respective gate drivers [22] with isolated signal transmission and isolated power supply, and a fraction of the overall output capacitors C_o [27], in addition to robust power and signal connectors. **(d)** Bridge-leg formed by $T_{a,l}$ and $T_{b,l}$ on which the waveforms shown in **Fig. 15** are measured. The blue line helps to recognize this bridge-leg structure in **Fig. 1** and **Fig. 11(a)**.

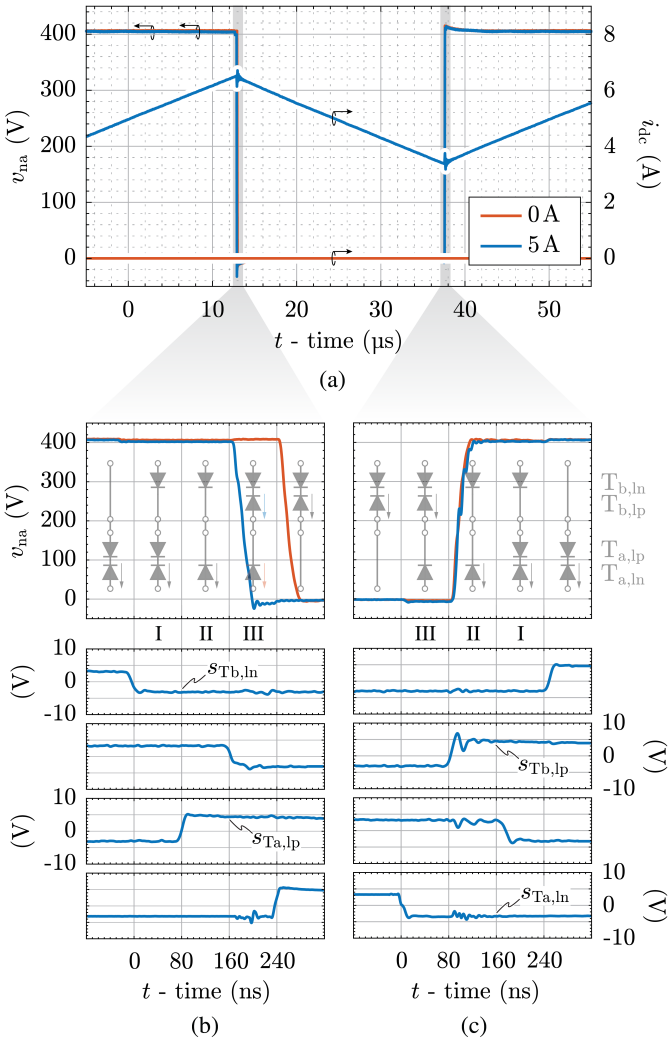


Fig. 15: **(a)** Measured waveforms of the switch node voltage v_{na} and of the output current i_{dc} during continuous operation of the bridge-leg shown in **Fig. 14 (d)** for $V_{ba} = 400\,\mathrm{V}$ and $i_{dc,avg} = 5\,\mathrm{A}$ (blue) and $0\,\mathrm{A}$ (red). **(b)-(c)** Zoomed view of v_{na} during a soft (blue in **(b)**), zero current (red in **(b)** and in **(c)**), and hard (blue in **(c)**) switching transition, associated gate signals $s_{Ti,lp}$ and $s_{Ti,ln}$ determined according to the current driven multi-step commutation strategy, and equivalent circuit of the bridge-leg.

VII. Conclusion

A 3-Φ bB CSI system employing a variable DC-link current control strategy denominated *Two-Third Modulation* (TTM) and 2G MB GaN e-FETs in its boost-type 3-Φ current DC-link inverter output stage is analyzed in this paper. The operation of these devices, which are suitable for any topology requiring AC-switches, is verified in a hardware prototype, where voltages up $400\,\mathrm{V}$ and currents up to $10\,\mathrm{A}$ are continuously switched applying the current driven multi-step commutation strategy. Furthermore, circuit simulations are performed to verify the operation of TTM and of the associated *Synergetic Control* structure, while analytic calculations quantify the enabled loss reduction, i.e. a $8\,\%$ reduction of conduction losses and a $86\,\%$ reduction of switching losses in case of unitary power factor, in comparison with conventional PWM concepts. Accordingly, 2G MB GaN e-FETs, in combination with TTM, have the potential to significantly enhance the performance of 3-Φ bB CSI systems, ultimately favoring their usage in place of 3-Φ Bb VSI systems.

References

[1] R. A. Torres, H. Dai, W. Lee, T. M. Jahns, and B. Sarlioglu, "Current-Source Inverters for Integrated Motor Drives using Wide-Bandgap Power Switches," in *Proc. of the IEEE Transportation Electrification Conference and Expo (ITEC)*, Long Beach, CA, USA, 2018.

[2] M. Antivachis, D. Bortis, D. Menzi, and J. W. Kolar, "Comparative Evaluation of Y-Inverter against Three-Phase Two-Stage Buck-Boost DC-AC Converter Systems," in *Proc. of the International Power Electronics Conference (IPEC-Niigata - ECCE Asia)*, Niigata, Japan, 2018.

[3] K. D. T. Ngo, "Topology and Analysis in PWM Inversion, Rectification and Cycloconversion," Ph.D. dissertation, California Institute of Technology, Pasadena, CA, USA, 1984.

[4] K. P. Phillips, "Current-Source Converter for AC Motor Drives," *IEEE Transactions on Industry Applications*, vol. 8, no. 6, pp. 679–683, 1972.

[5] M. Guacci, D. Bortis, and J. W. Kolar, "High-Efficiency Weight-Optimized Fault-Tolerant Modular Multi-Cell Three-Phase GaN Inverter for Next Generation Aerospace Applications," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Portland, OR, USA, 2018.

[6] F. Heinke and R. Sittig, "The Monolithic Bidirectional Switch (MBS)," in *Proc. of the 12th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Toulouse, France, 2000.

[7] T. Morita, M. Yanagihara, H. Ishida, M. Hikita, K. Kaibara, H. Matsuo, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "650 V 3.1 mΩ cm^2 GaN-Based Monolithic Bidirectional Switch Using Normally-Off Gate Injection Transistor," in *Proc. of the IEEE International Electron Devices Meeting (IEDM)*, Washington, DC, USA, 2007.

[8] J. Waldron and T. P. Chow, "Physics-Based Analytical Model for High-Voltage Bidirectional GaN Transistors Using Lateral GaN Power HEMT," in *Proc. of the 25th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, Kanazawa, Japan, 2013.

[9] D. Bergogne, O. Ladhari, L. Sterna, C. Gillot, R. Escoffier, and W. Vandendaele, "The Single Reference Bi-Directional GaN HEMT AC Switch," in *Proc. of the 17th European Conference on Power Electronics and Applications (EPE - ECCE Europe)*, Geneva, Switzerland, 2015.

[10] C. Kuring, O. Hilt, J. Böcker, M. Wolf, S. Dieckerhoff, and J. Würfl, "Novel Monolithically Integrated Bidirectional GaN HEMT," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Portland, OR, USA, 2018.

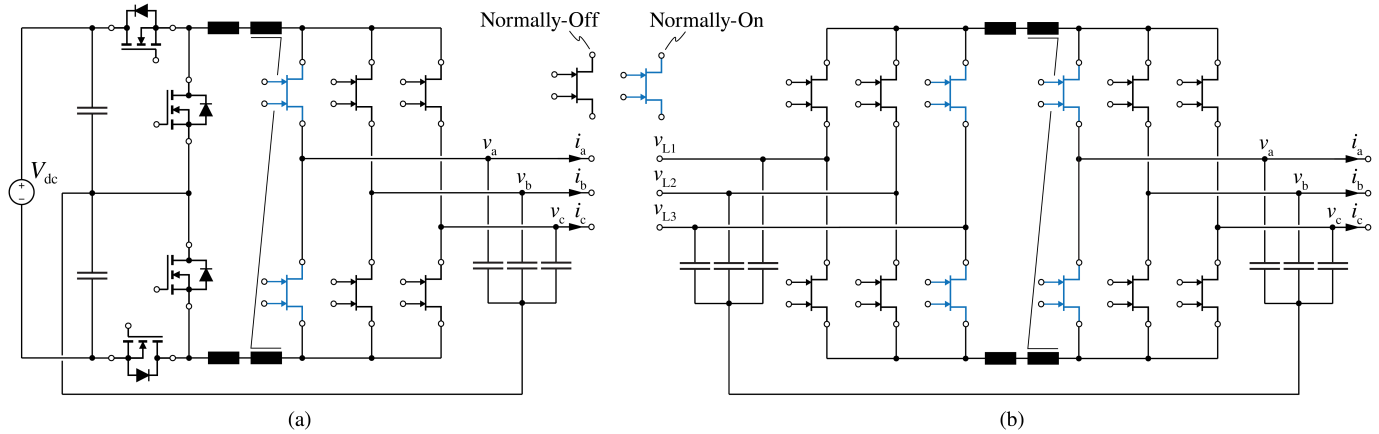


Fig. 16: Circuit topology variants for the realization of a 3-Φ bB CSI system featuring a common-mode filter inductor and bridge-legs with normally-on 2G MB GaN e-FETs (blue). **(a)** 3-Φ inverter with symmetric multi-level buck-type DC/DC converter input stage and **(b)** 3-Φ inverter with 3-Φ buck-type current DC-link rectifier front-end.

[11] S. Nagai, Y. Yamada, M. Hiraiwa, H. Ueno, S. Choe, Y. Kawai, O. Tabata, G. Yamada, N. Negoro, and M. Ishida, "A Compact GaN Bi-Directional Switching Diode with a GaN Bi-Directional Power Switch and an Isolated Gate Driver," in *Proc. of the 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Prague, Czech Republic, 2016.

[12] H. Uemeda, Y. Yamada, K. Asanuma, F. Kusama, Y. Kinoshita, H. Ueno, H. Ishida, T. Hatsuda, and T. Ueda, "High Power 3-Phase to 3-Phase Matrix Converter Using Dual-Gate GaN Bidirectional Switches," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, USA, 2018.

[13] H. Dai, T. M. Jahns, R. A. Torres, D. Han, and B. Sarlioglu, "Comparative Evaluation of Conducted Common-Mode EMI in Voltage-Source and Current-Source Inverters using Wide-Bandgap Switches," in *Proc. of the IEEE Transportation Electrification Conference and Expo (ITEC)*, Long Beach, CA, USA, 2018.

[14] J. Azurza Anderson, L. Schrittwieser, C. Gammeter, G. Deboy, and J. W. Kolar, "Relating the Figure of Merit of Power MOSFETs to the Maximally Achievable Efficiency of Converters," *to be published*, 2019.

[15] B. Sahan, S. V. Arajo, C. Nding, and P. Zacharias, "Comparative Evaluation of Three-Phase Current Source Inverters for Grid Interfacing of Distributed and Renewable Energy Systems," *IEEE Transactions on Power Electronics*, vol. 26, no. 8, pp. 2304–2318, 2011.

[16] G. J. Su and P. Ning, "Loss Modeling and Comparison of VSI and RB-IGBT Based CSI in Traction Drive Applications," in *Proc. of the IEEE Transportation Electrification Conference and Expo (ITEC)*, Detroit, MI, USA, 2013.

[17] J. W. Kolar and S. D. Round, "Analytical Calculation of the RMS Current Stress on the DC-Link Capacitor of Voltage-PWM Converter Systems," *IEE Proceedings - Electric Power Applications*, vol. 153, no. 4, pp. 535–542, 2006.

[18] Q. Lei, B. Wang, and F. Zheng Peng, "Unified Space Vector PWM Control for Current Source Inverter," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Raleigh, NC, USA, 2012.

[19] *GS66516B, GaN Systems Inc.*, Aug. 2018, Datasheet.

[20] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagi, T. Ueda, T. Tanaka, and D. Ueda, "Gate Injection Transistor (GIT) - A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3393–3399, 2007.

[21] D. Bortis, D. Neumayr, and J. W. Kolar, "$\eta\rho$-Pareto Optimization and Comparative Evaluation of Inverter Concepts Considered for the GOOGLE Little Box Challenge," in *Proc. of the IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Trondheim, Norway, 2016.

[22] *AN34092B, Panasonic Co.*, Jan. 2017, Datasheet.

[23] J. W. Kolar, T. Friedli, J. Rodriguez, and P. Wheeler, "Review of Three-Phase PWM AC-AC Converter Topologies," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 11, pp. 4988–5006, 2011.

[24] J. W. Kolar, M. Guacci, and D. Bortis, "Verfahren zum Regeln eines Dreiphasen-Pulsgleichrichtersystems mit Stromzwischenkreis," Jan. 2019, Patent Application P4688 CH.

[25] N. Zhu, B. Wu, D. Xu, N. R. Zargari, and M. Kazerani, "Common-Mode Voltage Reduction Methods for Medium-Voltage Current Source Inverter-Fed Drives," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Phoenix, AZ, USA, 2011.

[26] T. Halkosaari and H. Tuusa, "Optimal Vector Modulation of a PWM Current Source Converter According to Minimal Switching Losses," in *Proc. of the IEEE 31st Annual Power Electronics Specialists Conference (PESC)*, Galway, Ireland, 2000.

[27] *C5750X6S2W225K250KA, TDK Co.*, Jan. 2016, Datasheet.

[28] R. Naik and N. Mohan, "A Novel Grid Interface for Photovoltaic, Wind-Electric, and Fuel-Cell Systems with a Controllable Power Factor of Operation," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Dallas, TX, USA, 1995.

[29] J. C. Callaway, Y. Wang, R. Burgos, T. P. Chow, F. Wang, and D. Boroyevich, "Evaluation of SiC JFETs for a Three-Phase Current-Source Rectifier with High Switching Frequency," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2007.

[30] T. Friedli, S. D. Round, D. Hassler, and J. W. Kolar, "Design and Performance of a 200 kHz All-SiC JFET Current DC-Link Back-to-Back Converter," *IEEE Transactions on Industry Applications*, vol. 45, no. 5, pp. 1868–1878, 2009.

[31] G. Deboy, J. W. Kolar, M. Kasper, D. Bortis, and M. Guacci, "Current Source Converter Using Normally-On and Normally-Off Switches," Apr. 2019, Patent Application.