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***Abstract*—This paper details efficiency optimized operation and design of a bi-directional and isolated five-level Dual Active Bridge (5LDAB) converter for an application that requires ultra-wide voltage and power ranges. The rated power of the considered converter is $7.5\,\mathrm{kW}$, the specified input voltage range is $150\,\mathrm{V} \leq \mathbf{V_{dc1}} \leq 800\,\mathrm{V}$ and the output voltage is constant, $V_{\mathbf{dc2}} = 700\,\mathrm{V}$. In order to achieve high efficiency levels in a wide operating range, a modulation scheme is proposed to minimize the transformer rms current. Results of transformer rms currents and of efficiencies are presented for the 5LDAB and compared with the results obtained for an efficiency optimized conventional Dual Active Bridge (DAB) converter. Compared with the DAB topology, the 5LDAB converter can achieve an overall reduction of transformer rms currents and of conduction losses in the higher voltage regime of the operating range.**

***Index Terms*—DC/DC, Dual active bridge, DAB, Multilevel, Wide voltage range, Efficiency.**

I. Introduction

This paper investigates the design and the optimization of a high efficiency isolated and bidirectional DC–DC converter. The rated power of the considered converter is $7.5\,\mathrm{kW}$, the specified input voltage range is $150\,\mathrm{V} \leq V_{\mathrm{dc1}} \leq 800\,\mathrm{V}$ and the output voltage is constant, $V_{\mathrm{dc2}} = 700\,\mathrm{V}$. For this application the conventional Dual Active Bridge (DAB) converter may appear most viable after an initial evaluation of suitable converter topologies, due to the low number of components and the soft-switching capabilities enabling high efficiency operation. The DAB converter, however, is operated most efficiently if the ratio of input to output voltage ($V_{\mathrm{dc1}}/V_{\mathrm{dc2}}$) is close to the transformer turns ratio n [1], [2]. Thus, multilevel DAB realizations are considered to be strong competitors to the DAB converter. A DAB converter with a five-level input-side full bridge (denoted as 5LDAB converter on the following and shown in **Fig. 1**), for example, cannot only apply $v_{\mathrm{ac1}} = \pm V_{\mathrm{dc1}}$ or $v_{\mathrm{ac1}} = 0$ to the transformer but also $v_{\mathrm{ac1}} = \pm V_{\mathrm{dc1}}/2$, which is expected to extend the port voltage range where the DAB converter can be operated with high efficiency.

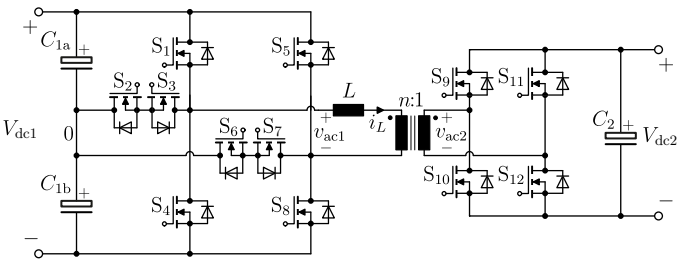

Fig. 1: Bi-directional 5LDAB converter considered for medium power ultra-wide input voltage range applications. The rated power of the considered converter is $7.5\,\mathrm{kW}$, the specified input voltage range is $150\,\mathrm{V} \leq V_{\mathrm{dc1}} \leq 800\,\mathrm{V}$ and the output voltage is constant, $V_{\mathrm{dc2}} = 700\,\mathrm{V}$.

The operating principle of the 5LDAB is presented in [3]–[6] for a multilevel DAB converter realized with Neutral-Point-Clamped (NPC) half-bridge circuits. NPC half-bridge circuits, however, require the freewheeling interval to be active for a minimum duration (in order to avoid excessive blocking voltage being applied to some of the power semiconductors [7]), which is in contradiction to the requirements of the optimized modulation scheme presented in [8] and would lead to increased losses at certain operating points. For this reason, the 5LDAB converter considered in this work employs T-type half-bridge circuits that allow the bridge output voltage $v_{\mathrm{ac1}}(t)$ to directly swing from the positive rail to the negative or vice versa without the need for a minimum retention time in the freewheeling state.

In this work, the optimized operation and design of the 5LDAB converter is detailed and the results with respect to rms transformer current and converter efficiency are compared to those obtained with an efficiency-optimized DAB. In the course of this investigation, the characteristics of the selected power semiconductors are summarized in **Section II**. Converter operation and design, including the derivations of analytical closed-form solutions for the control parameters of a new optimized 5LDAB converter modulation scheme, are outlined in **Section III** and **Section IV**, and the results are discussed in **Section V**. The obtained results demonstrate that the 5LDAB converter achieves high efficiency operation in a wide input voltage range. Moreover, the dependency of the calculated efficiency on the port voltages is less pronounced compared to that of a conventional DAB converter.

II. Employed semiconductors

The dominant criteria for the semiconductor selection are high efficiency (low conduction and switching losses) and the

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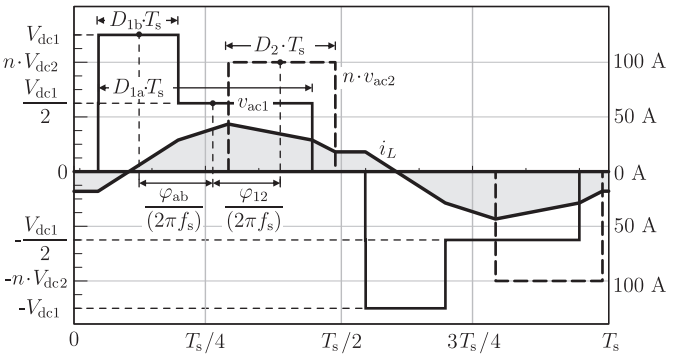


Fig. 2: General waveforms of v_{ac1}, v_{ac2} and i_L for the 5LDAB converter. The waveforms were obtained for $V_{dc1} = 500\,\mathrm{V}$, $n \cdot V_{dc2} = 400\,\mathrm{V}$, $D_{1a} = 0.4$, $D_{1b} = 0.15$, $D_2 = 0.2$, $\varphi_{ab} = -45°$, $\varphi_{12} = 52°$, $f_s = 100\,\mathrm{kHz}$, and $L = 16\,\mu\mathrm{H}$. The phase-shift angles are defined in the style of [8]. The high voltage levels of v_{ac1} applied at the beginning of each half-cycle is necessary to obtain minimum values of rms transformer current [8].

suitability of the selected power semiconductor switches with respect to reliable operation in a half-bridge configuration. For the switches S_1, S_4, S_5, S_8, S_9, S_{10}, S_{11}, and S_{12}, depicted in Fig. 1, SiC MOSFETs (C2M0080120D manufactured by CREE) with a blocking capability of 1200 V and an on-state channel resistance of $R_{DS,on} = 0.113\,\Omega$ at a junction temperature of 100°C are selected. For the remaining power switches S_2, S_3, S_6, and S_7 the Si MOSFET IPW65R041CFD (manufactured by Infineon) with a blocking capability of 650 V and an on-state channel resistance of $R_{DS,on}(100°C) = 66\,\mathrm{m}\Omega$ is considered.[1]

These selections were made in order to evaluate the performance expected with semiconductor devices that are directly available. Both considered power semiconductors are delivered in a TO-247 package and, thus, require the same footprint area.

III. Optimized modulation scheme

The power flow of the 5LDAB converter is controlled by appropriately adjusting five control parameters, i.e. the duty cycles D_{1a}, D_{1b}, and D_2 and the two phase-shift angles φ_{ab} and φ_{12}. **Fig. 2**, which depicts general waveforms of v_{ac1}, v_{ac2}, and i_L, defines these five control parameters (the phase-shift angles are defined in the style of [8]). Due to the high number of control parameters, the 5LDAB converter not only allows for power flow control but also enables the optimization, i.e. shaping, of the transformer current in order to maximize the efficiency. The modulation scheme used in the course of this work is an extended version of the modulation scheme presented in [8] and enables minimum or close-to-minimum transformer rms currents. Accordingly, also a low rms value of the current on the power semiconductors is ensured.

A. Normalization

All voltages and currents used in this chapter are normalized according to [8] in order to make the presented modulation scheme independent of the actual specifications:

V_{ref}	$= n\,V_{dc2}$	reference voltage,
Z_{ref}	$= 2\pi f_s L$	reference impedance,
I_{ref}	$= V_{ref}/Z_{ref}$	reference current,
P_{ref}	$= V_{ref}^2/Z_{ref}$	reference power,
T_{ref}	$= 1/f_s$	reference time,
$\overline{V}_{dc1}$	$= V_{dc1}/V_{ref}$	normalized dc voltage V_{dc1},
$\overline{V}_{dc2}$	$= n\,V_{dc2}/V_{ref} = 1$	normalized dc voltage V_{dc2},
$\overline{I}_L$	$= I_L/I_{ref}$	normalized inductor rms current,
$\overline{P}$	$= P/P_{ref}$	normalized converter power level,
D	$= T/T_{ref}$	normalized durations, duty cycles.

It is important to note, that, according to these definitions, $\overline{V}_{dc2} = 1$ always applies. Moreover, since the normalized maximum power of the DAB is equal to [8]

$$\overline{P}_{max} = \frac{4}{\pi}\overline{V}_{dc1}\overline{V}_{dc2} = \frac{4}{\pi}\overline{V}_{dc1}, \tag{1}$$

the normalized maximum dc current at port 1 is constant:

$$\overline{I}_{1,max} = \frac{\overline{P}_{max}}{\overline{V}_{dc1}} = \frac{4}{\pi}. \tag{2}$$

B. Approach for developing the new modulation scheme

The optimization problem leading to the desired modulation strategy can be stated according to:

$$\overline{I}_{L,min} = \min\ \overline{I}_L(\overline{V}_{dc1}, \overline{P}, D_{1a}, D_{1b}, D_2, \varphi_{ab}, \varphi_{12}), \tag{3}$$
$$0 \le D_{1a} \le 0.5, \quad D_{1b} - D_{1a} \le \varphi_{ab}/\pi \le D_{1a} - D_{1b},$$
$$0 \le D_{1b} \le D_{1a}, \quad -1 \le \varphi_{12}/\pi \le 1,$$
$$0 \le D_2 \le 0.5,$$

i.e. for a given operating point $\{\overline{V}_{dc1}, \overline{V}_{dc2} = 1, \overline{P}\}$ the available control parameters $\{D_{1a}, D_{1b}, D_2, \varphi_{ab}, \varphi_{12}\}$ are chosen within the given constraints so as to minimize the transformer rms current $\overline{I}_L$.

Similar to a conventional DAB converter, the conduction losses of the 5LDAB converter are closely related to the rms value of the transformer current, too. Therefore, analytical expressions for control parameters which feature minimum or close-to-minimum transformer rms currents can be used to establish straight-forward optimized operation of the 5LDAB converter. Due to the multivariable and non-linear nature of the extremum problem described with (3), however, no solutions have been obtained by directly solving (3). Instead, a two-step approach similar to [8] is chosen: in a first step, (3) is computed for a high number of different operating points using a numerical minimum search. In a second step, the computed waveforms of $\overline{v}_{ac1}$, $\overline{v}_{ac2}$, and $\overline{i}_L$ are inspected with respect to characteristic patterns, e.g. triangular transformer current waveforms, to synthesize a modulation scheme which features minimum or close-to-minimum transformer rms currents.

C. Optimized modulation scheme

Based on the results obtained by means of numerical optimization, eight different control modes have been identified. These eight modes together form the modulation scheme proposed in this paper. The control modes depend on the operating point $\{\overline{V}_{dc1}, \overline{V}_{dc2} = 1, \overline{P}\}$ as illustrated in Fig. 3.

[1] If switching losses would be of a concern, the GaN MOSFET RFJS3006F [manufactured by RF Micro Devices; blocking voltage: 650 V, $R_{DS,on}(100°C) = 62\,\mathrm{m}\Omega$] could be used, instead. However, in this work, low switching losses are expected due to the employed modulation scheme, cf. Section III-C.

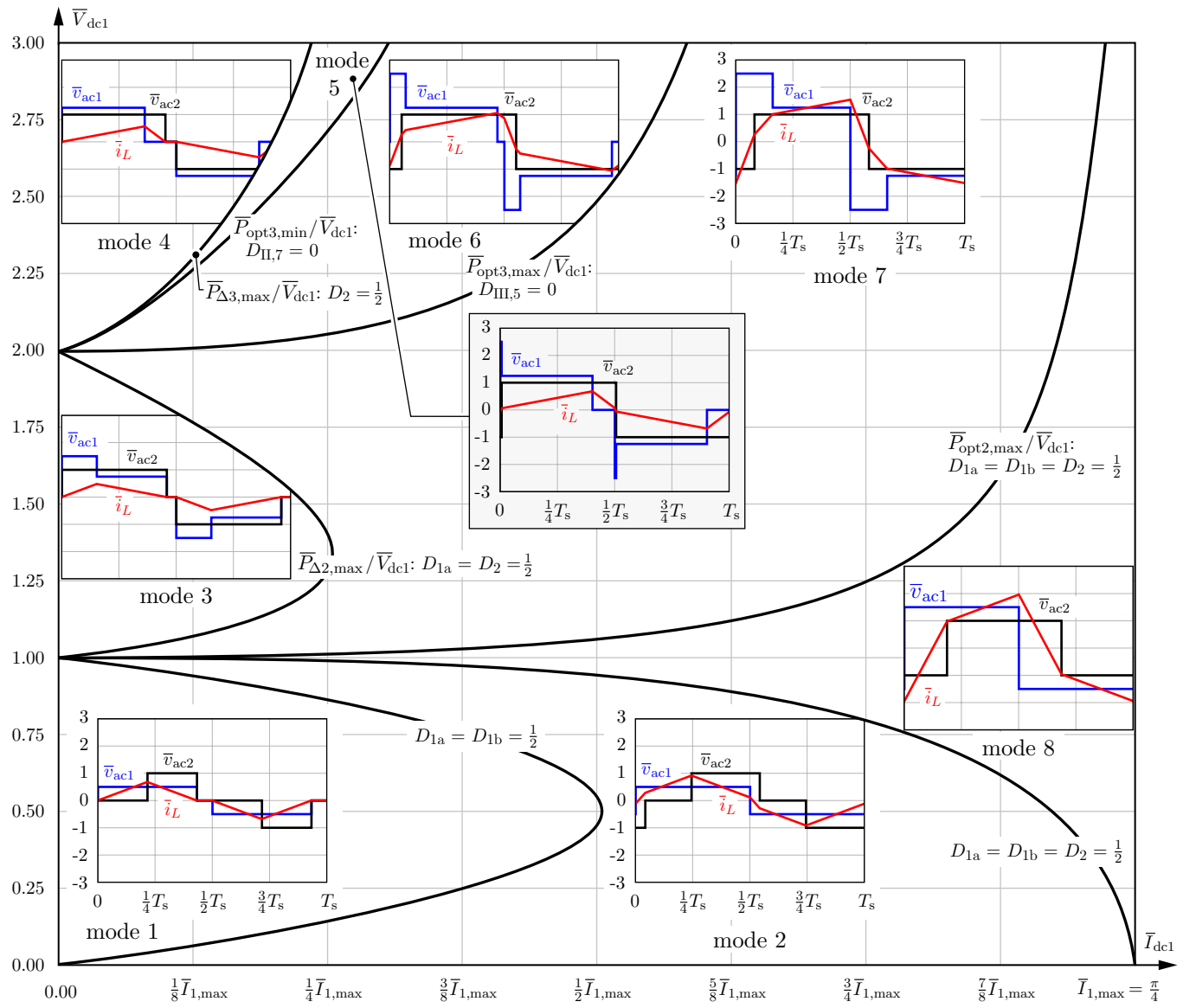


Fig. 3: Overview of the different control modes that are employed for the proposed optimized modulation scheme detailed in Section III-C. Typical steady-state waveforms of $\overline{v}_{\mathrm{ac1}}$, $\overline{v}_{\mathrm{ac2}}$, and $\overline{i}_L$ during one switching period $0 \leq t \leq T_{\mathrm{s}}$ are shown for each mode. This Figure is mirrored with respect to the $\overline{V}_{\mathrm{dc1}}$-axis in case of reverse operation, i.e. if $\overline{I}_{\mathrm{dc1}} < 0$ applies. The normalized durations $D_{\mathrm{II},6}$ and $D_{\mathrm{IV},6}$, used at the boundaries between modes 5/6 and 6/7, respectively, are defined in (17), (18), and (19). The operating points selected for the depicted waveforms are: *mode 1*: $\overline{I}_{\mathrm{dc1}} = 0.37\overline{I}_{1,\mathrm{max}}$, $\overline{V}_{\mathrm{dc1}} = 0.5$; *mode 2*: $\overline{I}_{\mathrm{dc1}} = 0.65\overline{I}_{1,\mathrm{max}}$, $\overline{V}_{\mathrm{dc1}} = 0.5$; *mode 3*: $\overline{I}_{\mathrm{dc1}} = 0.19\overline{I}_{1,\mathrm{max}}$, $\overline{V}_{\mathrm{dc1}} = 1.5$; *mode 4*: $\overline{I}_{\mathrm{dc1}} = 0.13\overline{I}_{1,\mathrm{max}}$, $\overline{V}_{\mathrm{dc1}} = 2.5$; *mode 5*: $\overline{I}_{\mathrm{dc1}} = 0.19\overline{I}_{1,\mathrm{max}}$, $\overline{V}_{\mathrm{dc1}} = 2.5$; *mode 6*: $\overline{I}_{\mathrm{dc1}} = 0.36\overline{I}_{1,\mathrm{max}}$, $\overline{V}_{\mathrm{dc1}} = 2.5$; *mode 7*: $\overline{I}_{\mathrm{dc1}} = 0.54\overline{I}_{1,\mathrm{max}}$, $\overline{V}_{\mathrm{dc1}} = 2.5$; and *mode 8*: $\overline{I}_{\mathrm{dc1}} = 0.93\overline{I}_{1,\mathrm{max}}$, $\overline{V}_{\mathrm{dc1}} = 1.5$.

In the following subsections, the control modes are discussed and analytical expressions for the respective control parameters are presented.

1) Low input voltage, $\overline{V}_{\mathrm{dc1}} < 1$ (modes 1, 2, and 8 in Fig. 3): the numerical results reveal that the additional degrees of freedom offered by the 5LDAB are not required, i.e. minimum rms currents can be achieved if the 5LDAB is operated as a conventional DAB according to [8]. Due to the low relative input voltage $\overline{V}_{\mathrm{dc1}}$, applying $\overline{v}_{\mathrm{ac1}} = \pm\overline{V}_{\mathrm{dc1}}/2$ is not exploited and thus,

$$D_{1\mathrm{a}} = D_{1\mathrm{b}} = D_1, \tag{4}$$

$$\varphi_{\mathrm{ab}} = 0 \tag{5}$$

applies. The remaining control parameters $\{D_1, D_2, \varphi_{12}\}$ are calculated with the expressions given in [8].[2]

2) Medium to high voltages and low power (modes 3 and 4 in Fig. 3): inspection of the numerically obtained results indicate that triangular current mode (TCM) modulation schemes are optimal. While TCM modulation is also optimal in case of mode 1 (low voltages), modes 3 and 4 differ with respect to mode 1 mainly in terms of the applied voltages $\overline{v}_{\mathrm{ac1}}$.

In *mode 3*, where medium relative input voltages $1 < \overline{V}_{\mathrm{dc1}} < 2$ apply, all of the 5 possible voltage levels for v_{ac1} are used. As illustrated in Fig. 3, TCM is achieved by means

[2]In [8] the modes 1, 2, and 8 are denoted TCM (Triangular Current Node), OTM (Optimal Transition Mode), and CPM (Conventional Phase Shift Modulation), respectively.

of equal durations of the active states of the primary and secondary side and the fact that $\overline{V}_{\text{dc1}}/2 < \overline{V}_{\text{dc2}} < \overline{V}_{\text{dc1}}$.

In *mode 4*, i.e. for high voltages $\overline{V}_{\text{dc1}} \geq 2$, only $\overline{v}_{\text{ac1}} = \pm\overline{V}_{\text{dc1}}/2$ and $\overline{v}_{\text{ac1}} = 0$ are used.

Modifying the solutions for TCM (e.g. found in [8]) accordingly leads to expressions for the control parameters in mode 3:

$$\left.\begin{aligned} D_{1\text{b}} &= \sqrt{\overline{P}\cdot\frac{2\overline{V}_{\text{dc2}}-\overline{V}_{\text{dc1}}}{2\pi\overline{V}_{\text{dc1}}\overline{V}_{\text{dc2}}(\overline{V}_{\text{dc1}}-\overline{V}_{\text{dc2}})}} \\ D_2 &= D_{1\text{a}} = D_{1\text{b}}\cdot\frac{\overline{V}_{\text{dc1}}}{2\overline{V}_{\text{dc2}}-\overline{V}_{\text{dc1}}} \\ \varphi_{12} &= 0 \\ \varphi_{\text{ab}} &= \text{sgn}(\overline{P})\,2\pi\,(D_{1\text{b}}/2 - D_{1\text{a}}/2) \end{aligned}\right\} \forall|\overline{P}| < \overline{P}_{\Delta 2,\text{max}}, \tag{6}$$

with

$$\overline{P}_{\Delta 2,\text{max}} = \frac{\pi\,(\overline{V}_{\text{dc1}}-2\overline{V}_{\text{dc2}})(\overline{V}_{\text{dc1}}-\overline{V}_{\text{dc2}})\,\overline{V}_{\text{dc2}}}{2\,\overline{V}_{\text{dc1}}}, \tag{7}$$

and mode 4:

$$\left.\begin{aligned} \varphi_{12} &= \text{sgn}(\overline{P})\pi\sqrt{\frac{\overline{V}_{\text{dc1}}/2-\overline{V}_{\text{dc2}}}{2\overline{V}_{\text{dc2}}^2\,\overline{V}_{\text{dc1}}/2}\cdot\frac{|\overline{P}|}{\pi}} \\ D_{1\text{a}} &= \frac{|\varphi_{12}|}{\pi}\cdot\frac{\overline{V}_{\text{dc2}}}{\overline{V}_{\text{dc1}}/2-\overline{V}_{\text{dc2}}} \\ D_2 &= D_{1\text{a}} + \frac{|\varphi_{12}|}{\pi} \\ \varphi_{\text{ab}} &= D_{1\text{b}} = 0 \end{aligned}\right\} \forall|\overline{P}| < \overline{P}_{\Delta 3,\text{max}}, \tag{8}$$

with

$$\overline{P}_{\Delta 3,\text{max}} = \frac{\pi\,(\overline{V}_{\text{dc1}}/2-\overline{V}_{\text{dc2}})\,\overline{V}_{\text{dc2}}^2}{\overline{V}_{\text{dc1}}}. \tag{9}$$

3) Medium to high voltages and medium power (modes 5, 6, and 7 in Fig. 3): we start our discussion with the observation of the power limit $\overline{P}_{\Delta 2,\text{max}}$ of mode 3, which occurs for $D_{1\text{a}} = D_2 \to 0.5$. At this point, the power can be further increased by using non-zero phase shifts $\varphi_{12} > 0$, making a seamless transition into *mode 7* feasible. Converter operation with mode 7, moreover, is optimal with respect to minimal transformer rms currents in a wide voltage and power range as confirmed by the preceding numerical investigation of the optimization problem (3). Analytical expressions of the respective control parameters are obtained by solving the following set of equations,

$$\begin{aligned} \bar{i}_1 &= \bar{i}_0 + 2\pi\,D_{\text{I},7}\,(\overline{V}_{\text{dc1}}+\overline{V}_{\text{dc2}}) && \text{(I)} \\ \bar{i}_2 &= \bar{i}_1 + 2\pi\,D_{\text{II},7}\,(\overline{V}_{\text{dc1}}-\overline{V}_{\text{dc2}}) && \text{(II)} \\ -\bar{i}_0 &= \bar{i}_2 + 2\pi\,D_{\text{III},7}\,(\overline{V}_{\text{dc1}}/2-\overline{V}_{\text{dc2}}) && \text{(III)} \\ \tfrac{1}{2} &= D_{\text{I},7} + D_{\text{II},7} + D_{\text{III},7} && \text{(IV)} \\ \overline{P} &= \overline{V}_{\text{dc2}}\big(-D_{\text{I},7}(\bar{i}_0+\bar{i}_1)+ \\ &\qquad D_{\text{II},7}(\bar{i}_1+\bar{i}_2)+D_{\text{III},7}(\bar{i}_2-\bar{i}_0)\big) && \text{(V)} \\ \overline{I}_L &= 2\Bigg(D_{\text{I},7}\frac{\bar{i}_0^2+\bar{i}_0\bar{i}_1+\bar{i}_1^2}{3}+ \\ &\qquad D_{\text{II},7}\frac{\bar{i}_1^2+\bar{i}_1\bar{i}_2+\bar{i}_2^2}{3}+D_{\text{III},7}\frac{\bar{i}_2^2-\bar{i}_2\bar{i}_0+\bar{i}_0^2}{3}\Bigg), && \text{(VI)} \end{aligned} \tag{10}$$

i.e. in mode 7, three (normalized) time intervals, $D_{\text{I},7}$, $D_{\text{II},7}$, and $D_{\text{III},7}$, can be distinguished during one half switching period, $T_\text{s}/2$, where different voltage conditions apply (cf. Fig. 3). The currents $\bar{i}_1$, $\bar{i}_2$ and $-\bar{i}_0$ apply at the end of the corresponding time intervals as expressed in (10)-(I-III). In steady-state, the current at the end of the third time interval is equal to the negative value of the initial current $\bar{i}_0$, cf. (10)-(III). The sum of all intervals is equal to half a switching period (10)-(IV), the expressions for power and transformer rms current are given in (10)-(V) and (10)-(VI), respectively. Solving the equation system (10) with respect to $D_{\text{I},7}$, $D_{\text{II},7}$, $\bar{i}_0$, $\bar{i}_1$, $\bar{i}_2$, and $\overline{I}_L$ leads to an expression for the transformer current $\overline{I}_L$ which only dependents on the operating point $\{\overline{V}_{\text{dc1}}, \overline{V}_{\text{dc2}} = 1, \overline{P}\}$ and $D_{\text{III},7}$. Since the desired modulation strategy should minimize $\overline{I}_L$, we can find the remaining unknown time interval $D_{\text{III},7}$ by solving

$$\frac{\partial\,\overline{I}_L(\overline{V}_{\text{dc1}},\overline{V}_{\text{dc2}},\overline{P},D_{\text{III},7})}{\partial\,D_{\text{III},7}} = 0, \tag{11}$$

for $D_{\text{III},7}$. Finally, the control parameters can be calculated with

$$\left.\begin{aligned} D_{1\text{a}} &= 0.5 \\ D_{1\text{b}} &= D_{\text{I},7} + D_{\text{II},7} \\ D_2 &= 0.5 \\ \varphi_{12} &= \text{sgn}(\overline{P})\,\pi\,(2D_{\text{I},7} + D_2 - D_{1\text{a}}) \\ \varphi_{\text{ab}} &= \text{sgn}(\overline{P})\,\pi\,(D_{1\text{b}} - D_{1\text{a}}) \end{aligned}\right\}$$

$$\begin{aligned} \forall\,\big((\overline{P}_{\Delta 2,\text{max}} \leq |\overline{P}| < \overline{P}_{\text{opt2,max}}) \wedge (1 < \overline{V}_{\text{dc1}} < 2)\big) \\ \vee\,\big((\overline{P}_{\text{opt3,max}} \leq |\overline{P}| < \overline{P}_{\text{opt2,max}}) \wedge (\overline{V}_{\text{dc1}} \geq 2)\big)\,. \end{aligned} \tag{12}$$

Due to space limitations, the intermediate results and the analytical results for $D_{\text{I},7}$, $D_{\text{II},7}$ and $D_{\text{III},7}$ are not shown here. However, the above described calculation steps can be performed with a software tool, such as Mathematica or Maple. No closed form solutions were found for the power levels $\overline{P}_{\text{opt2,max}}$ and $\overline{P}_{\text{opt3,max}}$ required for the boundary conditions. Instead, a numerical solver is used to solve

$$\overline{P}_{\text{opt2,max}} \;:\; D_{\text{III},7}(\overline{P}_{\text{opt2,max}}) = 0\,, \tag{13}$$

to determine $\overline{P}_{\text{opt2,max}}$, whereas conditions to find $\overline{P}_{\text{opt3,max}}$ are given below.

Different boundary conditions result at high input voltages, $\overline{V}_{\text{dc1}} \geq 2$, if $\overline{P} > \overline{P}_{\Delta 3,\text{max}}$ applies (cf. Fig. 3): at the

boundary between mode 4 and *mode 5*, we can observe that $\overline{P} = \overline{P}_{\Delta 3,\max}$ in mode 4 is achieved for $D_2 \to 0.5$. For increasing power, minimal transformer rms current is obtained if an additional time interval is introduced at the beginning of each half switching period, where the maximum possible voltage $V_{\text{dc1}} + n\,V_{\text{dc2}}$ is applied to the inductor L to achieve the required change of the transformer current, including a change of the sign of i_L, within the shortest possible duration, $D_{\text{I},5}$ (cf. mode 5 in Fig. 3). Equation (14) can be solved for the unknown variables $D_{\text{I},5}$, $D_{\text{II},5}$, $\bar{i}_0$, $\bar{i}_1$, $\bar{i}_2$ and $\overline{I}_L$.

$$
\begin{aligned}
\bar{i}_1 &= \bar{i}_0 + 2\pi\, D_{\text{I},5}\,(\overline{V}_{\text{dc1}} + \overline{V}_{\text{dc2}}) && \text{(I)}\\
\bar{i}_2 &= \bar{i}_1 + 2\pi\, D_{\text{II},5}\,(\overline{V}_{\text{dc1}}/2 - \overline{V}_{\text{dc2}}) && \text{(II)}\\
-\bar{i}_0 &= \bar{i}_2 - 2\pi\, D_{\text{III},5}\,\overline{V}_{\text{dc2}} && \text{(III)}\\
\tfrac{1}{2} &= D_{\text{I},5} + D_{\text{II},5} + D_{\text{III},5} && \text{(IV)}\\
\overline{P} &= \overline{V}_{\text{dc2}}\big(-D_{\text{I},5}(\bar{i}_0+\bar{i}_1)+ \\
&\qquad D_{\text{II},5}(\bar{i}_1+\bar{i}_2) + D_{\text{III},5}(\bar{i}_2-\bar{i}_0)\big) && \text{(V)}\\
\overline{I}_L &= 2\Bigg(D_{\text{I},5}\frac{\bar{i}_0^2+\bar{i}_0\bar{i}_1+\bar{i}_1^2}{3}+ \\
&\qquad D_{\text{II},5}\frac{\bar{i}_1^2+\bar{i}_1\bar{i}_2+\bar{i}_2^2}{3} + D_{\text{III},5}\frac{\bar{i}_2^2-\bar{i}_2\bar{i}_0+\bar{i}_0^2}{3}\Bigg). && \text{(VI)}
\end{aligned}
\tag{14}
$$

The remaining unknown time interval $D_{\text{III},5}$ can be found by means of solving

$$
\frac{\partial\, \overline{I}_L(\overline{V}_{\text{dc1}}, \overline{V}_{\text{dc2}}, \overline{P}, D_{\text{III},5})}{\partial\, D_{\text{III},5}} = 0, \tag{15}
$$

for $D_{\text{III},5}$. The control parameters are then obtained from

$$
\left.
\begin{aligned}
D_{1\text{a}} &= D_{\text{I},5} + D_{\text{II},5}\\
D_{1\text{b}} &= D_{\text{I},5}\\
D_2 &= 0.5\\
\varphi_{12} &= \text{sgn}(\overline{P})\pi(2D_{\text{I},5} + D_2 - D_{1\text{a}})\\
\varphi_{\text{ab}} &= \text{sgn}(\overline{P})\pi(D_{1\text{b}} - D_{1\text{a}})
\end{aligned}
\right\}
$$

$$
\forall\, \overline{P}_{\Delta 3,\max} \le |\overline{P}| < \overline{P}_{\text{opt3,min}}. \tag{16}
$$

The calculation of $\overline{P}_{\text{opt3,min}}$ is defined below, with (24).

We conclude the discussion of the modulation schemes with *mode 6*. The numerical solutions of (3) for this mode feature four instead of only three distinct time intervals with different voltage conditions as for all other modes discussed here (Fig. 3). Due to the increased degree of freedom, no closed-form analytical expressions have been found for the optimal control parameters. Therefore, a simplified, alternative approach is presented here which features close-to-minimal transformer rms currents. Inspection of Fig. 3 and of the equation systems (10) and (14) reveal that the voltage condition $\overline{v}_{\text{ac1}} = 0$, $\overline{v}_{\text{ac2}} = \overline{V}_{\text{dc2}}$ during $D_{\text{III},5}$ is unique to mode 5 and the voltage condition $\overline{v}_{\text{ac1}} = \overline{V}_{\text{dc1}}$, $\overline{v}_{\text{ac2}} = \overline{V}_{\text{dc2}}$ is unique to mode 7. Based on this observation it is proposed to perform an interpolation of those time intervals in mode 6,

$$
D_{\text{II},6} = D_{\text{II},7}\,\frac{\overline{P} - \overline{P}_{\text{opt3,min}}}{\overline{P}_{\text{opt3,max}} - \overline{P}_{\text{opt3,min}}}, \tag{17}
$$

$$
D_{\text{IV},6} = D_{\text{III},5}\,\frac{\overline{P}_{\text{opt3,max}} - \overline{P}}{\overline{P}_{\text{opt3,max}} - \overline{P}_{\text{opt3,min}}}. \tag{18}
$$

The other two time intervals $D_{\text{I},6}$ and $D_{\text{III},6}$ can then be calculated based on a set of equations describing mode 6,

$$
\begin{aligned}
\bar{i}_1 &= \bar{i}_0 + 2\pi\, D_{\text{I},6}\,(\overline{V}_{\text{dc1}} + \overline{V}_{\text{dc2}}) && \text{(I)}\\
\bar{i}_2 &= \bar{i}_1 + 2\pi\, D_{\text{II},6}\,(\overline{V}_{\text{dc1}} - \overline{V}_{\text{dc2}}) && \text{(II)}\\
\bar{i}_3 &= \bar{i}_2 + 2\pi\, D_{\text{III},6}\,(\overline{V}_{\text{dc1}}/2 - \overline{V}_{\text{dc2}}) && \text{(II)}\\
-\bar{i}_0 &= \bar{i}_3 - 2\pi\, D_{\text{IV},6}\,\overline{V}_{\text{dc2}} && \text{(III)}\\
\tfrac{1}{2} &= D_{\text{I},6} + D_{\text{II},6} + D_{\text{III},6} + D_{\text{IV},6} && \text{(IV)}\\
\overline{P} &= \overline{V}_{\text{dc2}}\big(-D_{\text{I},6}(\bar{i}_0+\bar{i}_1) + D_{\text{II},6}(\bar{i}_1+\bar{i}_2)+ \\
&\qquad D_{\text{III},6}(\bar{i}_2+\bar{i}_3) + D_{\text{IV},6}(\bar{i}_3-\bar{i}_0)\big) && \text{(V)}\\
\overline{I}_L &= 2\Bigg(D_{\text{I},6}\frac{\bar{i}_0^2+\bar{i}_0\bar{i}_1+\bar{i}_1^2}{3} + D_{\text{II},6}\frac{\bar{i}_1^2+\bar{i}_1\bar{i}_2+\bar{i}_2^2}{3}+ \\
&\qquad D_{\text{III},6}\frac{\bar{i}_2^2+\bar{i}_2\bar{i}_3+\bar{i}_3^2}{3} + D_{\text{IV},6}\frac{\bar{i}_3^2-\bar{i}_3\bar{i}_0+\bar{i}_0^2}{3}\Bigg), && \text{(VI)}
\end{aligned}
\tag{19}
$$

yielding

$$
D_{\text{I},6} = \frac{3 - 4D_{\text{IV},6} - \sqrt{e}}{12}, \tag{20}
$$

$$
D_{\text{III},6} = \frac{3 - 12D_{\text{II},6} - 8D_{\text{IV},6} + \sqrt{e}}{12}, \tag{21}
$$

with

$$
e = \left(9 + 24D_{\text{II},6} - 48D_{\text{II},6}^2 - 32D_{\text{IV},6}^2\right) - 48\overline{P}. \tag{22}
$$

Finally, the control parameters can be calculated with

$$
\left.
\begin{aligned}
D_{1\text{a}} &= D_{\text{I},6} + D_{\text{II},6} + D_{\text{III},6}\\
D_{1\text{b}} &= D_{\text{I},6} + D_{\text{II},6}\\
D_2 &= 0.5\\
\varphi_{12} &= \text{sgn}(\overline{P})\pi(2D_{\text{I},6} + D_2 - D_{1\text{a}})\\
\varphi_{\text{ab}} &= \text{sgn}(\overline{P})\pi(D_{1\text{b}} - D_{1\text{a}})
\end{aligned}
\right\}
$$

$$
\forall\, \overline{P}_{\text{opt3,min}} \le |\overline{P}| < \overline{P}_{\text{opt3,max}}. \tag{23}
$$

Again, a software tool is needed to perform the above calculation steps in order to obtain the respective closed-form expressions. The boundary power levels $\overline{P}_{\text{opt3,min}}$ and $\overline{P}_{\text{opt3,max}}$ can be numerically obtained by solving

$$
\overline{P}_{\text{opt3,min}} \;:\; D_{\text{II},7}(\overline{P}_{\text{opt3,min}}) = 0, \tag{24}
$$

and

$$
\overline{P}_{\text{opt3,max}} \;:\; D_{\text{III},5}(\overline{P}_{\text{opt3,max}}) = 0. \tag{25}
$$

IV. Design of the 5LDAB converter

The main design parameters of the 5LDAB converter are the transformer turns ratio, $n = N_1/N_2$, and the series inductance, L. These two parameters, however, cannot be directly calculated and are rather determined by means of an optimization procedure, e.g. by maximizing the average efficiency according to [1]. Thus, in order to conduct the corresponding efficiency optimization, the operating range, the objective function, and the considered modulation scheme need to be defined.

Figure 4 presents the specified operating range. A variable voltage, $150\,\text{V} \le V_{\text{dc1}} \le 800\,\text{V}$, applies to the input side, the output side voltage is constant and equal to 700 V. The

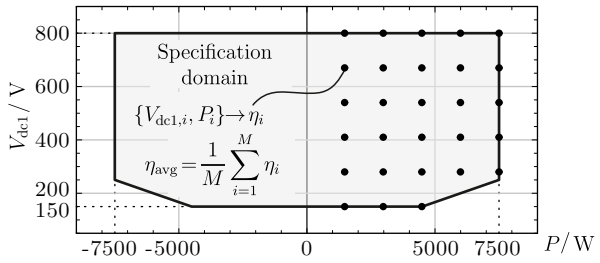


Fig. 4: Specification of operating ranges and average efficiency η_{avg}. The η_{avg} parameter denotes the average of the converter efficiency over a specified set of operating points $\{V_{\mathrm{dc1},i}, P_i\}$, with $i \in \{1, 2...M\}$ and $M = 28$. The losses are considered to be symmetric and independent of the power flow direction. Therefore, only operating points with positive power flow direction are considered. For efficiency calculation, the semiconductor conduction losses are considered the main source of losses [8] and, due to the presence of ZVS, serve for approximating the total efficiency. The efficiency of each operating point is calculated by $\eta_i = (P_i - P_{\mathrm{loss},i})/P_i$, where $P_{\mathrm{loss},i}$ is the semiconductor conduction losses for each operating point.

maximum power is 7.5 kW and the converter is required to provide the same maximum power in a bi-directional manner. The objective function considered for optimization is the average efficiency, η_{avg}, (defined in Fig. 4) which is calculated by averaging the efficiencies of each of the 28 discrete operating points depicted in Fig. 4, according to Section IV-A.

The employed modulation scheme features close-to-minimum transformer and switch rms currents and low switching losses in order to achieve high efficiency. With defined operating ranges, objective function, and modulation scheme, the most suitable values of n and L can be determined, cf. Section IV-B.

A. Loss model, efficiency calculation

It is assumed that mainly the power semiconductors generate losses and the total converter efficiency is calculated solely with the conduction losses of the power semiconductors [8]. The switching losses are expected to be comparably low, due to the employed modulation scheme, which enables switching at zero transformer current or ZVS. The contributions of copper and core losses of the magnetic components on the total losses strongly depend on the respective component volumes. Converter volumes are not further considered in this paper, however, are finally necessary to calculate reasonable losses of the magnetic components. Moreover, magnetic components are often cooled by means of natural convection, giving an allowable power dissipation that is typically considerably lower than the semiconductor losses that are dissipated via an active cooling system.

The MOSFETs' conduction losses are calculated based on the respective rms drain currents and the channel on-state resistances. The values of the channel on-state resistances are obtained from data sheets at an assumed junction temperature of 100°C and at the drain currents each MOSFET is rated for. The respective values are given in the previous Section II.

B. Efficiency-optimized 5LDAB converter design

With the modulation scheme and the loss model being defined, the efficiency at each specified operating point can be calculated (and, thus, η_{avg} can be determined) for given values of n and L. It is to be noted that, theoretically, any turns ratio can be selected, the specified power, however, limits the maximum allowable converter inductance according to [8]:

$$L < L_{\max} = \min\left[\frac{n\ V_{\mathrm{dc1}} V_{\mathrm{dc2}}}{2 f_{\mathrm{s}} P_{\max}(V_{\mathrm{dc1}})/\eta_{\mathrm{exp}}}\right] \frac{\varphi_{\max}}{\pi}\left(1 - \frac{\varphi_{\max}}{\pi}\right); \tag{26}$$

$P_{\max}$ depends on V_{dc1} due to the limited terminal current at port 1, cf. Fig. 4; $\varphi_{\max} = 60°$ is used to avoid excessive losses in case of low dc voltages being present at port 1; η_{exp} is set to 94%.

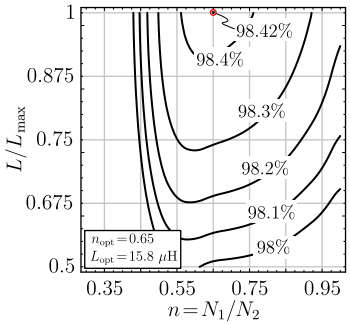


Fig. 5: Average efficiencies, $\eta_{\mathrm{avg}}(n, L)$ of the 5LDAB converter, calculated for different turns ratio and inductance values. Maximum average efficiency is achieved for $n_{\mathrm{opt}} = 0.65$ and $L_{\mathrm{opt}} = L_{\max} = 15.8\,\mu\mathrm{H}$.

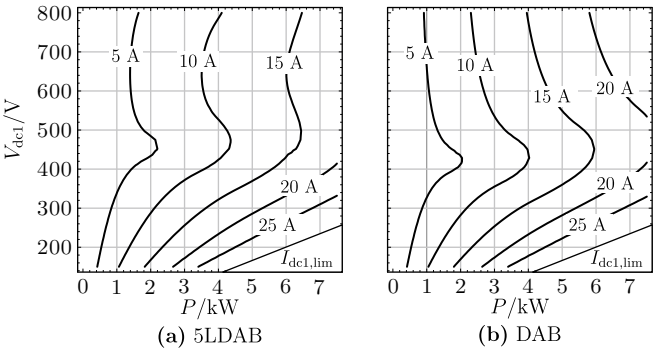
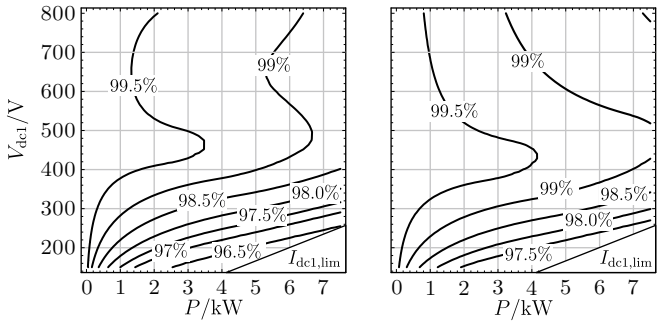


Fig. 6: Transformer rms currents calculated for the operating range specified in Fig. 4 and for $f_{\mathrm{s}} = 100\,\mathrm{kHz}$: (a) 5LDAB with $n_{\mathrm{opt}} = 0.65$ and $L_{\mathrm{opt}} = 15.8\,\mu\mathrm{H}$; (b) conventional DAB with $n_{\mathrm{opt}} = 0.6$ and $L_{\mathrm{opt}} = 14.6\,\mu\mathrm{H}$. For most operating points, the 5LDAB features lower transformer rms currents than the conventional DAB. Moreover, the distribution of the transformer rms current is more uniform for the 5LDAB than for the DAB, due to the capability of the 5LDAB to generate $v_{\mathrm{ac1}} = 0$, $\pm V_{\mathrm{dc1}}/2$, or $\pm V_{\mathrm{dc1}}$.

Figure 5 depicts the values for η_{avg} that are calculated for $0.3 \leq n \leq 1$ (step width is $\Delta n = 0.05$) and $0.5 \leq L/L_{\max} \leq 1.0$ (step width is $\Delta(L/L_{\max}) = 0.025$). According to this Figure, the turns ratio and the 5LDAB converter inductance at maximum average efficiencies are 0.65 and 15.8 µH, respectively. Further, L is equal to $L_{\max}$; this outcome is directly related to the operating points, selected in Fig. 4, that are used to calculate η_{avg} and the properties of the 5LDAB converter when operated in a wide voltage and power range.

V. Loss analysis and efficiency comparisons

The transformer rms currents calculated for the optimized 5LDAB converter, considering the operating range specified in Fig. 4, and $f_{\mathrm{s}} = 100\,\mathrm{kHz}$ are shown in **Fig. 6(a)**. For comparison reasons, **Fig. 6(b)** depicts the transformer rms currents that are calculated for an optimized conventional DAB converter, which employs full bridge circuits, realized with



(a) 5LDAB (b) DAB

Fig. 7: (a) Efficiencies calculated for the 5LDAB with $n_{\text{opt}} = 0.65$, $L_{\text{opt}} = 15.8\,\mu\text{H}$, and $f_{\text{s}} = 100\,\text{kHz}$; (b) efficiencies calculated for the conventional DAB with $n_{\text{opt}} = 0.6$, $L_{\text{opt}} = 14.6\,\mu\text{H}$, and $f_{\text{s}} = 100\,\text{kHz}$. In order to achieve a fair comparison, each switch of the conventional DAB's primary side full bridge is composed of two SiC MOSFETs being connected in parallel in order to keep the total number of TO-247 packages the same for both, the 5LDAB and the DAB converter topologies. The 5LDAB shows higher efficiency than the DAB at high port voltages V_{dc1}. At low port voltages, however, the efficiency of the conventional DAB is higher than that of the 5LDAB, by reason of nearly equal transformer rms currents for 5LDAB and DAB converters at low port voltages, cf. Fig. 6, and half the effective on-state resistances of the switches of the DAB's primary side full bridge.

C2M0080120 SiC MOSFETs, on the primary and secondary sides ($n_{\text{opt}} = 0.6$ and $L_{\text{opt}} = 14.6\,\mu\text{H}$). The 5LDAB converter features lower or equal transformer currents than the conventional DAB converter at most operating points, in particular for $V_{\text{dc1}} > 450\,\text{V}$. Furthermore, the distribution of the transformer rms current is more uniform, due to the capability of the 5LDAB converter to generate bridge output voltages of 0, $\pm V_{\text{dc1}}/2$, or $\pm V_{\text{dc1}}$.

Figures 7(a) and **(b)** present the efficiencies calculated for both converter topologies. In order to achieve a fair comparison, each switch of the primary side full bridge of the DAB converter is composed of two SiC MOSFETs that are connected in parallel, which reduces the effective on-state resistances of these switches to $R_{\text{DS,on,eff}} = R_{\text{DS,on}}/2 = 56\,\text{m}\Omega$ (due to $n = N_1/N_2 = 0.6$, the primary side currents are higher than the secondary side currents). With this, the 5LDAB and the DAB converters use the same total number of TO-247 packages. According to the results shown in Fig. 7, the 5LDAB converter shows higher efficiency at high port voltages V_{dc1}. At low port voltages, however, the efficiency of the conventional DAB converter is higher, by reason of nearly equal transformer rms currents for 5LDAB and DAB converters at low port voltages, cf. Fig. 6, and due to the reduced effective on-state resistances of the switches used for the DAB's primary side full bridge. **Figure 8** presents this result in more detail and explicitly focuses on the differences between the conduction losses calculated for the 5LDAB and the DAB converters. In Fig. 8, negative power values denote operating points where the 5LDAB converter achieves higher efficiency than the DAB converter and vice versa: the conventional DAB generates less losses at input voltages less than $400\,\text{V}$ and the 5LDAB is more efficient at high input voltages higher than $500\,\text{V} \ldots 600\,\text{V}$ (depending on the actual converter operating power level).

VI. Conclusion

This paper investigates the efficiency optimized operation and the efficiency optimized design of a $7.5\,\text{kW}$ bi-directional

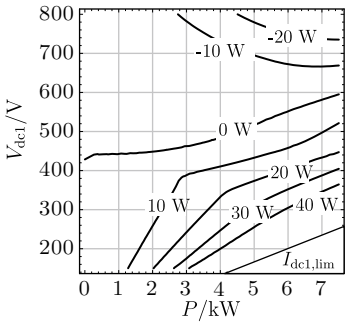


Fig. 8: Differences between the conduction losses calculated for the 5LDAB converter with $n_{\text{opt}} = 0.65$ and $L_{\text{opt}} = 15.8\,\mu\text{H}$ and the conventional DAB converter with $n_{\text{opt}} = 0.6$ and $L_{\text{opt}} = 14.6\,\mu\text{H}$; $f_{\text{s}} = 100\,\text{kHz}$. Negative values indicate regions where the 5LDAB converter generates less conduction losses than the DAB converter. Thus, improved efficiency is achieved for the 5LDAB converter for high port voltages. For low port voltages, however, less conduction losses are calculated for the conventional DAB converter, cf. Fig. 7.

and isolated five-level DAB converter for an application that requires ultra-wide operating voltage and power range. The considered converter topology, denoted as 5LDAB converter, employs a five-level full bridge circuit capable of generating five voltage level, i.e. 0, $\pm V_{\text{dc1}}/2$, and $\pm V_{\text{dc1}}$, on the primary side and a conventional full bridge circuit on the secondary side. An optimized modulation scheme is derived, which employs all five control parameters of the the 5LDAB converter in order to realize the required output power and simultaneously shape the transformer current such that minimum or close-to-minimum rms transformer current results. Closed-form solutions for the expressions used to calculate the corresponding control parameters can be derived, but are omitted for the sake of brevity.

The comparison of the conduction losses calculated for the 5LDAB and the conventional DAB converter reveals that an overall reduction of the rms transformer current is achieved with the 5LDAB converter. In the course of a fair comparison, which considers the same number of TO-247 packages for both, the 5LDAB and the DAB converters, lower conduction losses are calculated for the DAB converter at low port voltages, $V_{\text{dc1}} < 400\,\text{V}$. Reduced conduction losses are achieved in the higher voltage regime, i.e. for V_{dc1} higher than $500\,\text{V} \ldots 600\,\text{V}$ (depending on the actual converter operating power).

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