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***Abstract*—A semi-analytical modulation scheme to operate a single-phase, single-stage dual active bridge (DAB) AC–DC converter under full-operating-range zero voltage switching (ZVS) is proposed. The converter topology consists of a DAB DC–DC converter, receiving a rectified AC line voltage via a synchronous rectifier. ZVS modulation strategies previously proposed in literature are either based on current-based (CB) or energy-based (EB) ZVS analyses. The combined phase-shift, duty-cycle, and switching frequency modulation proposed in this paper relies on a novel, current-dependent charge-based (CDCB) ZVS analysis, taking into account the commutation charge of the (parasitic) switch capacitances as well as the time dependency of the commutation currents. Thereby, commutation inductance is shown to be an essential element in achieving full-operating-range ZVS. Experimental results obtained from a 3.7 kW bidirectional electric vehicle battery charger which interfaces a 400 V DC-bus with the 230 Vac, 50 Hz utility grid are given to validate the analysis and practical feasibility of the proposed strategy.**

***Index Terms*—AC–DC power conversion, battery charger, dual active bridge, modulation schemes, zero voltage switching.**

I. Introduction

An important application area for single-phase, utility interfaced, isolated AC–DC converters is the charging of plug-in hybrid electrical vehicles (PHEVs) and battery electric vehicles (BEVs) [1]. Bidirectional conversion capability is a key feature in the development of a smart interactive power network in which the energy systems play an active role in providing different types of support to the grid [2] (e.g. vehicle-to-grid (V2G) concepts [3]).

The soft-switching dual active bridge (DAB) converter, consisting of two active bridges interfaced by a high-frequency (HF) transformer and optional series inductor, was originally introduced in [4] for realizing high-efficiency, high-power-density, isolated DC–DC conversions with the capability of buck-boost operation and bidirectional power flow. By combining the DAB DC–DC converter with a synchronous rectifier (SR), it was shown in [5] that a single-phase, isolated, bidirectional, unity power factor AC–DC conversion can be effectively realized within a single conversion stage (1-S). No DC-link storage in the form of failure prone bulky electrolytic capacitors is required and compliance with AC power line EMC standards is possible [6], [7].

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Various strategies have been proposed in literature to modulate the bridges of the DAB converter. Whether the DAB is used in an DC–DC or a 1-S AC–DC configuration, they mainly focus on minimizing a (mostly loss related) cost function, without exceeding the boundaries of zero voltage switching (ZVS). However, regardless their objective, all ZVS modulation schemes so far presented are based on 'theoretical' current-based (CB) [6], [8]–[11] or energy-based (EB) [7], [12], [13] ZVS analyses (explanation of CB and EB ZVS: see last paragraph of Section II-B). When considering CB ZVS, substantial parts of the ZVS regions involve incomplete bridge commutations due to the presence of (parasitic) switch capacitances [14], leading to reduced efficiency and in the worst case destruction of the semiconductors switching devices. On the other hand, the EB ZVS analyses are more accurate but still involve difficulties, in particular concerning implementability and accuracy (see last paragraph of Section II-B).

CB ZVS schemes: Simple modulation schemes for achieving full-operating-range CB ZVS are given in [6], [8]. A modulation scheme with minimum reactive inductor power is presented in [9] while in [10] an optimal scheme with respect to minimum inductor rms currents is proposed.

EB ZVS schemes: A modulation scheme based on simplified EB ZVS constraints is presented in [7]. However, EB ZVS could not be fully achieved for the low power mode. Moreover, the transition between the low and high power modes encompasses highly undesirable discontinuous steps in the modulation variables. Also in [13] simplifications were made, yielding a simple full-operating-range EB ZVS modulation scheme which again involves a discontinuous mode transition.

To avoid the deficiencies of the CB and EB ZVS analyses, this paper introduces a current-dependent charge-based (CDCB) ZVS analysis, taking into account the commutation charge of the (parasitic) switch capacitances as well as the time dependency of the commutation currents. Subsequently, a simple, semi-analytical modulation scheme for obtaining full-operating-range CDCB ZVS as well as continuous modulation parameter trajectories is proposed, combining phase-shift, duty-cycle, and frequency modulation. The concept of commutation inductance is essential in this approach. The

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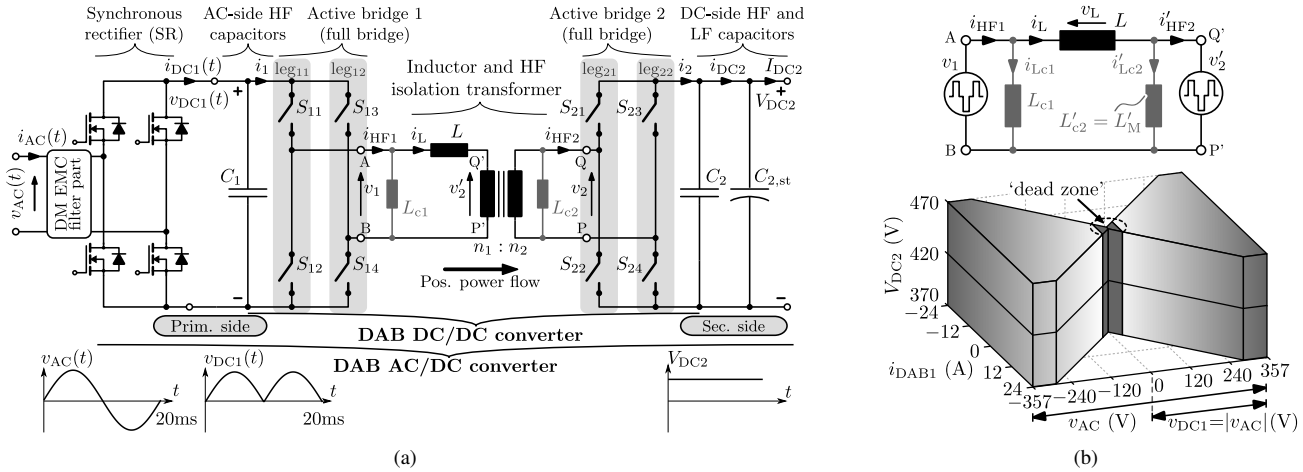


Fig. 1: (a) Circuit schematic of the single-phase, single-stage, bidirectional and isolated DAB AC–DC converter topology. (b) Top inset: simplified (lossless) electrical model of the DAB. Bottom inset: complete operating range of the investigated DAB converter.

TABLE I: Converter Specifications and Requirements

Property		*Value*
AC-side	V_{AC} ($\mathrm{V_{rms}}$)	230 (nominal) $207 \leqslant V_{\mathrm{AC}} \leqslant 253$
	$I_{\mathrm{AC,P,nom}}$ ($\mathrm{A_{rms}}$)	16 (nominal)
	f_{L} (Hz)	50
DC-side	V_{DC2} (V)	$370 \leqslant V_{\mathrm{DC2}} \leqslant 470$
EMC compliance		CISPR 22 Class B
PF		> 0.9 (at $I_{\mathrm{AC,P}} \geqslant 0.1 \cdot I_{\mathrm{AC,P,nom}}$)

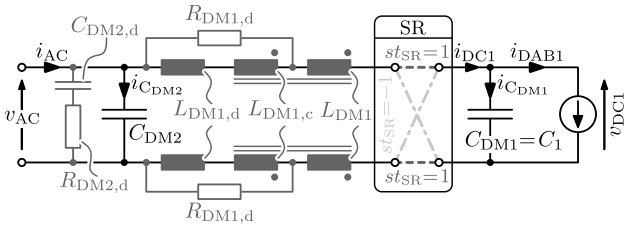


Fig. 2: Equivalent circuit of the converter's AC input side, with controllable current source, synchronous rectifier (SR), and 2-stage DM EMC filter.

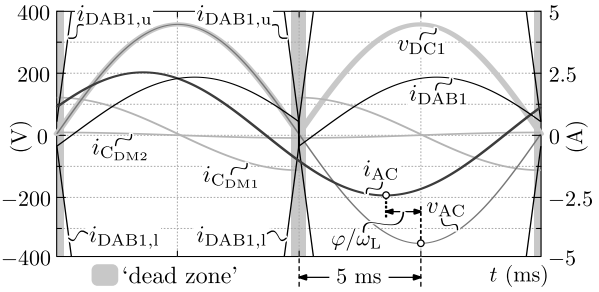


Fig. 3: Ideal input-side quantities for the worst case PF condition: $\hat{I}^{*}_{\mathrm{AC,P}} = \sqrt{2} \cdot 0.1 \cdot I_{\mathrm{AC,P,nom}} = 2.26$ A; $\hat{V}_{\mathrm{AC}} = \hat{V}_{\mathrm{AC,max}} = 357.8$ V; PF $= 0.9$.

analysis is applied to the single-phase, single-stage AC–DC converter (full bridge - full bridge DAB) shown in Fig. 1(a).

The specifications (Table I) of the investigated DAB AC–DC converter shown in Fig. 1(a) are based on the requirements for future electric vehicle on-board battery chargers, interfacing a 400 V DC-bus with the single-phase 230 $\mathrm{V_{rms}}$ / 50 Hz mains. The ability to use residential power sockets dictates a nominal (active) AC input current of $I_{\mathrm{AC,P}} = 16$ $\mathrm{A_{rms}}$ and a nominal power of $P_{\mathrm{nom}} = 3.7$ kW. The voltage ranges are further listed in Table I. The 400 $\mathrm{V_{nom}}$ DC-bus voltage was chosen based on the examples given in [1]. Bidirectional power flow enables vehicle-to-grid functionality, while galvanic isolation ensures safety. Other requirements are a high conversion efficiency, a high power density, EMC compliance to the CISPR 22 Class B standard, a high power factor (PF), and a low total harmonic distortion (THD) of the AC input current.

II. Analysis of the DAB Model

Referring to the schematic in Fig. 1(a), the rectified AC line voltage $v_{\mathrm{DC1}}(t) = |v_{\mathrm{AC}}(t)| = |\hat{V}_{\mathrm{AC}} \sin(\omega_{\mathrm{L}} t)|$, coming from the SR, is directly fed to the DAB DC–DC converter, with only a small HF filter capacitor C_1 in between. The DAB comprises HF transformer-coupled (with series inductor L) primary and secondary side full bridges, performing the regulation of DC voltage V_{DC2} while maintaining unity power factor at the AC side. Therefore they produce phase-shifted edge resonant square wave voltages v_1 and v_2 at the terminals of the HF AC-link, resulting in an inductor current i_{L}. AC currents i_{HF1} and i_{HF2} are rectified by the active bridges, resulting in net DC currents i_1 and i_2 at the respective sides. Filter capacitors C_1 and C_2 bypass the HF components of i_1 and i_2. Averaging $i_1(t)$ over one switching period $T_{\mathrm{s}} = 1/f_{\mathrm{s}}$ yields the DAB DC input current i_{DAB1}, e.g. at instant k:

$$i_{\mathrm{DAB1,k}} = i_{1,\mathrm{avg,k}} = \frac{1}{T_{\mathrm{s}}} \int_{kT_{\mathrm{s}}}^{(k+1)T_{\mathrm{s}}} i_1(t)\mathrm{d}t. \qquad (1)$$

Towards the converter's AC input side the DAB can be represented by a variable current source i_{DAB1} connected in parallel with the EMC input filter and the SR (Fig. 2). In order to realize the PFC requirement (Table I) the reactive power drawn by the EMC filter capacitors C_{DM1} and C_{DM2}

(Table IV) needs to be compensated by the DAB, requiring a limited reactive power transfer capability. For a given amplitude of the (active) AC input current $\hat{I}^*_{\mathrm{AC,P}}$ and PF ($=\cos(\varphi)$; see Fig. 3), i_{DAB1} can be calculated with:

$$i_{\mathrm{DAB1}} = st_{\mathrm{SR}} \Big[dir \cdot (\hat{I}^*_{\mathrm{AC,P}}/\mathrm{PF}) \sin(\omega_{\mathrm{L}} t + dir \cdot \arccos(\mathrm{PF})) - \omega_{\mathrm{L}}(C_{\mathrm{DM1}} + C_{\mathrm{DM2}}) \hat{V}_{\mathrm{AC}} \sin(\omega_{\mathrm{L}} t + \pi/2) \Big], \quad (2)$$

where ω_{L} is the 50 Hz AC line frequency, $\hat{V}_{\mathrm{AC}}$ the amplitude of the AC input voltage, st_{SR} the state of the SR, and 'dir' the power flow direction:

$$st_{\mathrm{SR}} = \begin{cases} 1 & \text{if } v_{\mathrm{AC}}(t) > 0, \\ -1 & \text{if } v_{\mathrm{AC}}(t) < 0, \end{cases} \quad (3)$$

$$dir = \begin{cases} 1 & \text{if } p(t) > 0 : \text{prim.} \rightarrow \text{sec. side}, \\ -1 & \text{if } p(t) < 0 : \text{sec.} \rightarrow \text{prim. side}. \end{cases} \quad (4)$$

The ideal converter's input-side quantities for the worst case PF condition (Table I; $\hat{I}^*_{\mathrm{AC,P}} = \sqrt{2} \cdot 0.1 \cdot I_{\mathrm{AC,P,nom}} = 2.26$ A; $\hat{V}_{\mathrm{AC}} = \hat{V}_{\mathrm{AC,max}} = 357.8$ V; PF $= 0.9$) are depicted in Fig. 3. For meeting the PFC requirements, and leaving some margin for dynamic controllability, the DAB input current limit $i_{\mathrm{DAB1,u}}(v_{\mathrm{DC1}}) = -i_{\mathrm{DAB1,l}}(v_{\mathrm{DC1}})$ (Fig. 3) is determined as:

$$i_{\mathrm{DAB1,u}}(v_{\mathrm{DC1}}) = \min \left(\frac{24 \cdot v_{\mathrm{DC1}}}{\hat{V}_{\mathrm{AC,min}}} + 0.5, 24 \text{ A} \right), \quad (5)$$

yielding the complete converter's operating range[1] shown in Fig. 1(b) (bottom inset). On the assumption of ideal components and by referring the model to the primary side of the transformer, a simplified electrical representation of the DAB is obtained (Fig. 1(b) (top inset)), where v'_2 is given by $v'_2 = v_2 \cdot n_1/n_2$. i_{DAB1} is controlled by applying a phase shift angle[2] ϕ between v_1 and v'_2 and additionally controlling the respective pulse width modulation angles τ_1 and τ_2 ($\tau_1, \tau_2 \leqslant 50$ %; Fig. 4). A last parameter that can be freely controlled (within a reasonable range) is the switching frequency f_{s}, resulting is four modulation parameters: $\mathbf{x} = (\phi, \tau_1, \tau_2, f_{\mathrm{s}})$.

A. Switching Modes and Commutation Inductance(s)

Depending on the sequence in time of the falling and rising edges of voltages v_1 and v'_2, twelve different switching modes can be distinguished [10]. Similar to [10], the final modulation scheme presented in this paper relies on two out of the twelve possible modes, which are the only ones feasible for efficient ZVS operation of the DAB. Mode 1 (high power mode) can be subdivided into a submode for positive power flow (i.e. mode 1^+; Fig. 4(a)) and a similar submode for negative power flow (i.e. mode 1^-; not shown). Mode 2 (low power mode; Fig. 4(b)) can be used for both positive and negative power flow. The given analysis is limited to mode 1^+ and mode 2 only (mode 1^- is similar to mode 1^+), being sufficient to derive the final modulation scheme. The modulation parameter relations for achieving the respective voltage patterns are:

$$\text{mode } 1^+ : \quad -\tau_1 + \pi \leqslant \phi \leqslant \tau_2, \quad (6)$$

$$\text{mode } 2 : \quad \tau_2 - \tau_1 \leqslant \phi \leqslant 0. \quad (7)$$

The modulation scheme presented in Section III relies on the inclusion of inductances which are placed in parallel with active bridge 1 (i.e L_{c1}) and with active bridge 2 (i.e. L_{c2}), as shown in Figs. 1(a) and 1(b) (top inset). They are further referred to as *'commutation inductances'* and always benefit the ZVS conditions due to the injection of a small reactive current in the respective bridge (i.e. i_{Lc1} resp. i_{Lc2}, Fig. 4). This effect is essential for achieving full-operating-range CDCB ZVS (cf. Section II-B) and for obtaining smooth mode transitions. According to Fig. 1(b) (top inset) and neglecting the transformer leakage inductances, the dynamics of the currents $i_{\mathrm{L}}(t)$, $i_{\mathrm{Lc1}}(t)$, and $i'_{\mathrm{Lc2}}(t)$ can be expressed as:

$$\frac{\mathrm{d}i_{\mathrm{L}}(t)}{\mathrm{d}t} = \frac{v_{\mathrm{L}}(t)}{L}, \quad \frac{\mathrm{d}i_{\mathrm{Lc1}}(t)}{\mathrm{d}t} = \frac{v_1(t)}{L_{\mathrm{c1}}}, \quad \text{and} \quad \frac{\mathrm{d}i'_{\mathrm{Lc2}}(t)}{\mathrm{d}t} = \frac{v'_2(t)}{L'_{\mathrm{c2}}},$$

with $v_{\mathrm{L}}(t) = v_1(t) - v'_2(t)$. The bridge currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ are calculated using:

$$i_{\mathrm{HF1}}(t) = i_{\mathrm{L}}(t) + i_{\mathrm{Lc1}}(t), \quad (8)$$

$$i_{\mathrm{HF2}}(t) = i'_{\mathrm{HF2}}(t) \frac{n_1}{n_2} = \Big(i_{\mathrm{L}}(t) - i'_{\mathrm{Lc2}}(t) \Big) \frac{n_1}{n_2}. \quad (9)$$

Solving these equations in each interval within half the switching period $T_{\mathrm{s}}/2$, as defined in Fig. 4, under the assumption of steady state operation (i.e. $i_{\mathrm{L}}(t) = -i_{\mathrm{L}}(t+T_{\mathrm{s}}/2)$; $i_{\mathrm{Lc1}}(t) = -i_{\mathrm{Lc1}}(t+T_{\mathrm{s}}/2)$; and $i'_{\mathrm{Lc2}}(t) = -i'_{\mathrm{Lc2}}(t+T_{\mathrm{s}}/2)$), and evaluating the resulting systems of equations yields the expressions in Table II for the HF AC-link currents at the different switching instances $\theta_{\mathrm{i}} = \{\alpha, \beta, \gamma, \text{and } \delta\}$[3], where $\theta = \omega_{\mathrm{s}} t$, with $\omega_{\mathrm{s}} = 2\pi f_{\mathrm{s}}$. V'_{DC2} is the primary side referred DC output voltage and d the primary side referred voltage conversion ratio: $d = V'_{\mathrm{DC2}}/v_{\mathrm{DC1}}$. Currents i_1 and i_2 are derived from respectively i_{HF1} and i_{HF2} by analyzing the conduction states[4] of the switches S_{xx}. Applying (1) for mode 1^+ and mode 2 and solving the resulting equations to ϕ yields the expressions for the phase shift angles[5] in order to achieve a certain DAB input current i_{DAB1}:

$$\phi_{\mathrm{m1^+}} = \frac{-\tau_1 + \tau_2 + \pi}{2} - \sqrt{\frac{-(\tau_2 - \pi)^2 + \tau_1(2\pi - \tau_1)}{4} - \frac{i_{\mathrm{DAB1}} \omega_{\mathrm{s}} L \pi}{V'_{\mathrm{DC2}}}}, \quad (10)$$

$$\phi_{\mathrm{m2}} = \frac{\tau_2 - \tau_1}{2} + \frac{i_{\mathrm{DAB1}} \omega_{\mathrm{s}} L \pi}{\tau_2 V'_{\mathrm{DC2}}}. \quad (11)$$

L_{c1} and L_{c2} do not contribute to the power transfer and are thus not present in the equations for i_{DAB1} and ϕ.

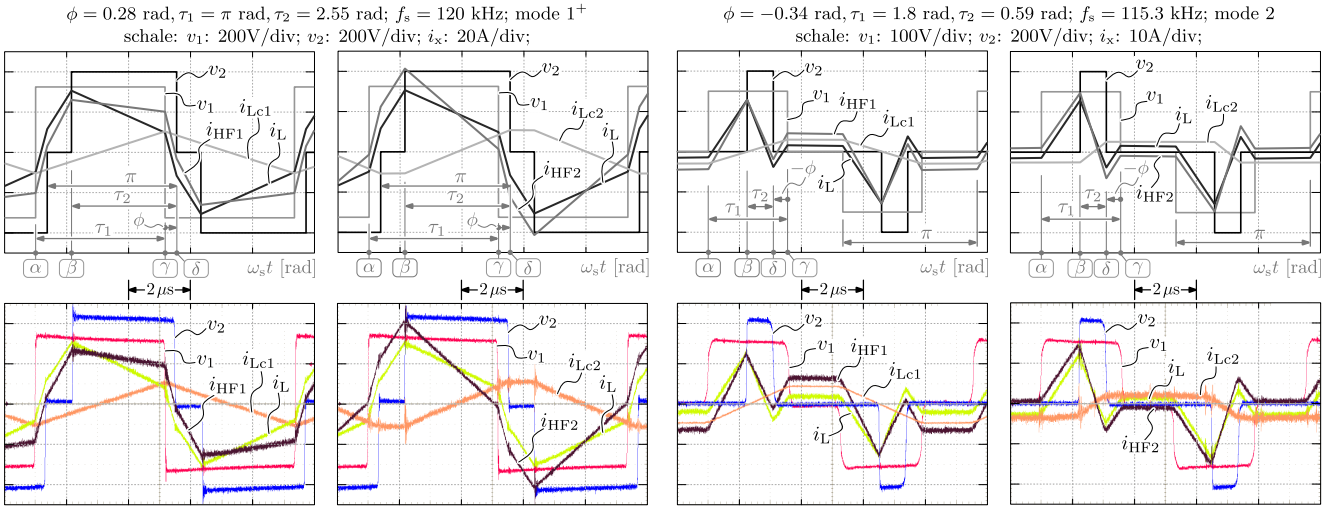
[1] Within -30 V$\leqslant v_{\mathrm{AC}} \leqslant 30$ V, the bridges of the DAB are inactive ('dead zone') as ZVS is quasi impossible in this voltage interval (see also Section III).

[2] The phase shift angle ϕ is defined as the angle between the first falling edge of v_1 and the first falling edge of v'_2 (see Fig. 4).

[3] α and β correspond with the positive rising edge of respectively v_1 and v'_2 while γ and δ correspond with the respective positive falling edges.

[4] The conduction states can be found in [6], Fig. 4.

[5] For mode 1^+ a second solution for ϕ exists (i.e. involving '$+\sqrt{\ldots}$'). This solution results in high HF AC-link rms currents and should not be considered.



(a) Mode 1^+; with prim. side commutation current (left column); with sec. side commutation current (right column). Top inset: simulation, bottom inset: measurement. Conditions: $v_{DC1} = 325$ V; $V_{DC2} = 400$ V; $i_{DAB1} = 18.4$ A.

(b) Mode 2; with prim. side commutation current (left column); with sec. side commutation current (right column). Top inset: simulation, bottom inset: measurement. Conditions: $v_{DC1} = 150$ V; $V_{DC2} = 400$ V; $i_{DAB1} = 2.12$ A.

Fig. 4: Voltage and current waveforms for (a) mode 1^+, (b) mode 2. The waveforms are obtained using: $L = 13$ μH, $L_{c1} = L_{c2} = 62.1$ μH, $n_1/n_2 = 1$.

TABLE II: HF AC-Link Currents i_L, i_{Lc1}, and i'_{Lc2} for Mode 1^+ and Mode 2

Mode 1 → Mode 1^+	i_L	i_{Lc1}	i'_{Lc2}
α	$\frac{v_{DC1}\left(d(-\tau_1+\tau_2/2-\phi+\pi)-\tau_1/2\right)}{\omega_s L}$	$\frac{-v_{DC1}\tau_1/2}{\omega_s L_{c1}}$	$\frac{V'_{DC2}\left(\tau_1-\tau_2/2+\phi-\pi\right)}{\omega_s L'_{c2}}$
β	$\frac{v_{DC1}\left(d\tau_2/2+\tau_1/2-\tau_2+\phi\right)}{\omega_s L}$	$\frac{v_{DC1}\left(\tau_1/2-\tau_2+\phi\right)}{\omega_s L_{c1}}$	$\frac{-V'_{DC2}\tau_2/2}{\omega_s L'_{c2}}$
γ	$\frac{v_{DC1}\left(d(-\tau_2/2+\phi)+\tau_1/2\right)}{\omega_s L}$	$\frac{v_{DC1}\tau_1/2}{\omega_s L_{c1}}$	$\frac{V'_{DC2}\left(\tau_2/2-\phi\right)}{\omega_s L'_{c2}}$
δ	$\frac{v_{DC1}\left(-d\tau_2/2-\tau_1/2-\phi+\pi\right)}{\omega_s L}$	$\frac{v_{DC1}\left(-\tau_1/2-\phi+\pi\right)}{\omega_s L_{c1}}$	$\frac{V'_{DC2}\tau_2/2}{\omega_s L'_{c2}}$
Mode 2	i_L	i_{Lc1}	i'_{Lc2}
α	$\frac{v_{DC1}\left(d\tau_2/2-\tau_1/2\right)}{\omega_s L}$	$\frac{-v_{DC1}\tau_1/2}{\omega_s L_{c1}}$	$\frac{-V'_{DC2}\tau_2/2}{\omega_s L'_{c2}}$
β	$\frac{v_{DC1}\left(d\tau_2/2+\tau_1/2-\tau_2+\phi\right)}{\omega_s L}$	$\frac{v_{DC1}\left(\tau_1/2-\tau_2+\phi\right)}{\omega_s L_{c1}}$	$\frac{-V'_{DC2}\tau_2/2}{\omega_s L'_{c2}}$
γ	$\frac{v_{DC1}\left(-d\tau_2/2+\tau_1/2\right)}{\omega_s L}$	$\frac{v_{DC1}\tau_1/2}{\omega_s L_{c1}}$	$\frac{V'_{DC2}\tau_2/2}{\omega_s L'_{c2}}$
δ	$\frac{v_{DC1}\left(-d\tau_2/2+\tau_1+\phi\right)}{\omega_s L}$	$\frac{v_{DC1}\left(\tau_1/2+\phi\right)}{\omega_s L_{c1}}$	$\frac{V'_{DC2}\tau_2/2}{\omega_s L'_{c2}}$

B. Current-Dependent Charge-Based (CDCB) ZVS Analysis

The zero voltage switching (ZVS) principle is explained using Figs. 5(a) and 5(b), considering the commutation of current $i_{leg_{11}} = -i_{HF1}$ from the bottom switch S_{12} to the top switch S_{11} of bridge leg$_{11}$ ($i_{leg_{11}}$ is positive at the switching instant t_{sw}; i_{HF1} is negative; Fig. 5(b)). As shown in Fig. 5(c) (top inset), each switch[6] S_{xx} consists of a power transistor T_{xx}, a diode D_{xx}, and a nonlinear parasitic capacitance C_{xx} (i.e. $C_{oss}(V_{DS})$; Fig. 5(c), bottom inset). The total parasitic leg capacitance to be considered for the commutation is highly nonlinear and can be calculated with:

$$C_{leg_{11}} = C_{12}(v_{DS,S_{12}}) + C_{11}(v_{DS,S_{11}}). \tag{12}$$

Quasi lossless ZVS turn-off of switch S_{12} is achieved if the drain-source channel of T_{12} is fully opened before $i_{leg_{11}}$ has provided enough charge to $C_{leg_{11}}$ for causing a significant rise of drain-to-source voltage $v_{DS,S_{12}}$ (quasi zero-voltage turn-off of switch S_{12}). This can be seen in Fig. 5(b) where at time instant t_3 the gate of S_{12} is completely off while $v_{DS,S_{12}}$ is still low. This is a result of the nonlinear parasitic switch capacitances C_{xx} which have a high value at low voltages (during t_2–t_3; Fig. 5(c)), keeping $v_{DS,S_{12}}$ low at turn-off.

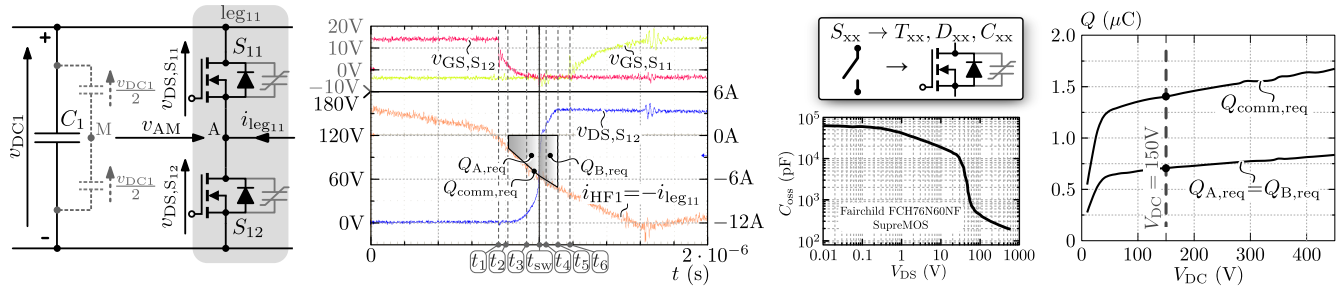
Quasi lossless ZVS turn-on of switch S_{11} is achieved if T_{11} can be turned on when its anti-parallel diode D_{11} is conducting (time instant t_6, Fig. 5(b)). This requires the resonance which occurs between $C_{leg_{11}}$ and the HF AC-link inductances, and during which $C_{leg_{11}}$ is charged by $i_{leg_{11}}$ ($= -i_{HF1}$) (t_3–t_5) to complete before turn-on of T_{11}.

The CDCB ZVS criterium proposed in this paper is based on above considerations where the commutation of bridge leg$_{11}$ is driven by the current $i_{leg_{11}}$ which flows into the leg and charges $C_{leg_{11}}$. The total charge needed to complete the commutation, $Q_{comm,req}(V_{DC})$, can be subdivided into charges $Q_{A,req}(V_{DC})$ and $Q_{B,req}(V_{DC})$, each required to achieve a voltage change of half the DC-bus voltage ($V_{DC}/2$):

$$Q_{A,req}(V_{DC}) = Q_{B,req}(V_{DC}) = \frac{Q_{comm,req}(V_{DC})}{2}. \tag{13}$$

$Q_{comm,req}(V_{DC})$, $Q_{A,req}(V_{DC})$, and $Q_{B,req}(V_{DC})$ for the used MOSFETs are shown in Fig. 5(d) which was obtained using circuit simulator GeckoCIRCUITS^{TM} [15], where a nonlinear capacitor $C(u)$ that is based on small-signal measurements (such as in Fig. 5(c), bottom inset) can be directly employed [16]. $Q_{comm,req}$, $Q_{A,req}$, and $Q_{B,req}$ do not only depend on

[6] In this work Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are considered only. The FAIRCHILD FCH76N60NF SupreMOS super-junction MOSFETs are used for the DAB active bridges due to their excellent soft-switching performance (inter alia the nonlinear output capacitance) and low on-resistance.



(a) (b) (c) (d)

Fig. 5: (a) Bridge leg of the DAB converter. (b) Example of a commutation of current $i_{\mathrm{leg}_{11}} = -i_{\mathrm{HF}1}$ from the bottom switch S_{12} to the top switch S_{11} of bridge leg S_{11}–S_{12}. The DC-bus voltage of the bridge leg, $v_{\mathrm{DC}1}$, is 150 V for this example. (c) Top inset: representation of the HF high voltage switches S_{xx} (MOSFETs) of the DAB active bridges. Bottom inset: parasitic output capacitance $C_{\mathrm{oss}}(V_{\mathrm{DS}})$ of the used MOSFETs. (d) Charges required to achieve a voltage change of the full DC-bus voltage (V_{DC}) and of half the DC-bus voltage ($V_{\mathrm{DC}}/2$) during commutation of a bridge leg (i.e. charging/discharging of the parasitic leg capacitance C_{leg}). The 150 V line corresponds with the example in Fig. 5(b).

V_{DC} but also slightly on the leg current. Therefore they are derived using an average $i_{\mathrm{leg,AVG}}$, applying a margin (0.05 and 0.1 μC) for component variances and circuit imperfections.

ZVS commutation of a bridge leg (switching instant θ_{i}) occurs when the charges $Q_{\mathrm{A,av}}$ and $Q_{\mathrm{B,av}}$ that are available in the leg-current before (i.e. $Q_{\mathrm{A,av}}$) and after (i.e. $Q_{\mathrm{B,av}}$) instant θ_{i} are at least equal to resp. $Q_{\mathrm{A,req}}(V_{\mathrm{DC}})$ and $Q_{\mathrm{B,req}}(V_{\mathrm{DC}})$. $Q_{\mathrm{A,av}}$ and $Q_{\mathrm{B,av}}$ are calculated using resp. a backward and a forward integration of the leg current, starting at θ_{i}:

$$Q_{\mathrm{A,av}} = s^{\pm} \cdot \left[\left(\sum_{j=1}^{n_{\mathrm{B}}} \int_{\theta_{i-j+1}}^{\theta_{i-j}} \frac{i_{\mathrm{HF}}}{\omega_{\mathrm{s}}} \mathrm{d}\theta \right) + \int_{\theta_{i-n_{\mathrm{B}}}}^{\theta_x} \frac{i_{\mathrm{HF}}}{\omega_{\mathrm{s}}} \mathrm{d}\theta \right] \geqslant Q_{\mathrm{A,req}}, \tag{14}$$

$$Q_{\mathrm{B,av}} = s^{\pm} \cdot \left[\left(\sum_{j=1}^{m_{\mathrm{F}}} \int_{\theta_{i+j-1}}^{\theta_{i+j}} \frac{-i_{\mathrm{HF}}}{\omega_{\mathrm{s}}} \mathrm{d}\theta \right) + \int_{\theta_{i+m_{\mathrm{F}}}}^{\theta_y} \frac{-i_{\mathrm{HF}}}{\omega_{\mathrm{s}}} \mathrm{d}\theta \right] \geqslant Q_{\mathrm{B,req}}, \tag{15}$$

- θ_{x}: first instant prior to θ_{i} where i_{HF} crosses zero;
- θ_{y}: first instant after θ_{i} where i_{HF} crosses zero;
- $\theta_{\mathrm{i-j}}$ and $\theta_{\mathrm{i+j}}$: switching instances of the three remaining bridges;
- n_{B}: number of switching instances between θ_{x} and θ_{i};
- m_{F}: number of switching instances between θ_{i} and θ_{y};
- $s^{\pm} = -1$ for $\theta_{\mathrm{i}} = \{\alpha, \delta\}$, $s^{\pm} = 1$ for $\theta_{\mathrm{i}} = \{\beta, \gamma\}$;
- $i_{\mathrm{HF}} = i_{\mathrm{HF}1}$ for $\theta_{\mathrm{i}} = \{\alpha, \gamma\}$, $i_{\mathrm{HF}} = i_{\mathrm{HF}2}$ for $\theta_{\mathrm{i}} = \{\beta, \delta\}$

In order for a given set of input parameters ($V_{\mathrm{DC}2}$, $v_{\mathrm{DC}1}$, τ_1, τ_2, ϕ, L, $L_{\mathrm{c}1}$, $L_{\mathrm{c}2}$, n_1/n_2 and f_{s}) to ascertain whether quasi lossless ZVS commutation is achieved in all DAB bridges, these *current-dependent charge-based constraints* need to be met at each switching instant $\theta_{\mathrm{i}} = \{\alpha, \beta, \gamma, \text{and } \delta\}$.

In order to achieve switching at the predicted moment, the switching delay $t_{\mathrm{sw,del}}$ ($= t_{\mathrm{sw}} - t_2$, Fig. 5(b)) has to be dynamically compensated in the controller. Moreover, a dynamic dead-time (t_{dead}) adaptation is required for each bridge leg, avoiding back commutation. At each switching instant θ_{i}, $t_{\mathrm{sw,del}}$ and t_{dead} are respectively calculated with:

$$t_{\mathrm{sw,del}} = \frac{\theta_i - \theta_A}{\omega_{\mathrm{s}}}, \tag{16}$$

$$t_{\mathrm{dead}} = \frac{\theta_B - \theta_A}{\omega_{\mathrm{s}}}, \tag{17}$$

where θ_{A} and θ_{B} are the instances where the backward and forward integration (eqns. (14) and (15); starting point θ_{i}) of the corresponding leg current equals the charge needed to achieve a voltage change of half the DC-bus voltage ($V_{\mathrm{DC}}/2$). θ_{A} and θ_{B} are found by respectively solving:

$$s^{\pm} \cdot \int_{\theta_i}^{\theta_A} \frac{i_{\mathrm{HF}}}{\omega_{\mathrm{s}}} \mathrm{d}\theta = Q_{\mathrm{A,req}}, \tag{18}$$

$$s^{\pm} \cdot \int_{\theta_i}^{\theta_B} \frac{-i_{\mathrm{HF}}}{\omega_{\mathrm{s}}} \mathrm{d}\theta = Q_{\mathrm{B,req}}. \tag{19}$$

Lastly it is verified if $t_{\mathrm{sw,del}}$ and $(t_{\mathrm{dead}} - t_{\mathrm{sw,del}})$ are smaller than an upper limit, avoiding too long commutation delays. This yields a set of *time-based constraints*[7]:

$$t_{\mathrm{sw,del}} \leqslant t_{\mathrm{sw,del,max}}, \tag{20}$$

$$t_{\mathrm{dead}} - t_{\mathrm{sw,del}} \leqslant (t_{\mathrm{dead}} - t_{\mathrm{sw,del}})_{\mathrm{max}}. \tag{21}$$

The CDCB ZVS analysis deals with deficiencies of ZVS analyses previously used in literature, where the current-based (CB) ZVS descriptions do not include the (parasitic) switch capacitances and assume that ZVS of a bridge leg is achieved when the drain-to-source current of the switch which initiates the commutation (turn-off) is positive at the switching instant. The influence of the switch capacitances is described in inter alia [7], [12], [13] by evaluating the energy balance between the switch capacitances and the HF AC-link inductances (energy-based (EB) ZVS analyses). However, in [7] the state of the one active bridge is not taken into account in the ZVS verification of the other, and in [12], [13] a (quasi) simultaneous state change within the one and/or together with the other active bridge is not allowed. Moreover the EB ZVS analyses are based on energy equivalent switch capacitances, resulting in significant errors as explained in [16]. In this paper the error due to the linear approximation of the HF AC-link currents is small as, due to the strong non-linearity of the leg capacitances, the energy transfer to and from the capacitances during commutation is almost fully concentrated in time intervals t_2–t_3 and t_4–t_5 (Fig. 5(b)). In these intervals $v_{\mathrm{DS,S}_{12}}$ remains approximately constant, and the expressions in Table II are still valid.

[7] A reasonable value for these limits is 500 ns (for the used MOSFETs).

III. CDCB ZVS Modulation Scheme

The derivation of the CDCB ZVS modulation scheme is illustrated using the prototype system parameters listed in Table IV. A transformer turns ratio of $n_1/n_2 = 1$ is chosen such that $V'_{\mathrm{DC2,min}} > (\hat{v}_{\mathrm{DC1,max}} + 10\ V$ margin) is always satisfied[8]. The switching frequency range of 75 kHz $\leqslant f_{\mathrm{s}} \leqslant$ 120 kHz assures a compact converter design without causing excessive switching frequency related losses (upper limit $f_{\mathrm{s,max}} = 120$ kHz) while leaving enough margin for the EMC DM input filter to attenuate the lower HF harmonics of the input current (lower limit[9] $f_{\mathrm{s,min}} = 75$ kHz). The main inductance value, $L = 13\ \mu$H, is the result of an iteration performed during the converter's design phase and is chosen in the range of $L \approx (0.75\ \ldots\ 0.85) \cdot L_{\max}$, where $L_{\max}$ is determined by the maximum achievable DAB input current (acc. to eqn. (14) in [10]):

$$\frac{V'_{\mathrm{DC2,min}}}{8 f_{\mathrm{s,max}} L_{\max}} \geqslant (i_{\mathrm{DAB1,max}} = 24\ \mathrm{A}). \tag{22}$$

Below it is explained in three steps how the final semi-analytical full-operating-range CDCB ZVS modulation scheme is obtained. In **step 1** analytical equations are presented which allow to calculate ϕ τ_1, and τ_2 in order to facilitate current-based (CB) ZVS. Assuming a non-zero positive commutation current and using $L_{\mathrm{c1}} = L_{\mathrm{c2}} = \infty$ (traditional DAB), it is shown that the CB ZVS constraints (and thus also the CDCB ZVS constraints proposed in Section II-B), cannot be met in the entire 50 Hz AC input voltage interval. In **step 2** the calculation of ϕ, τ_1, and τ_2, as well as the resulting values are the same as in **step 1**. By now applying finite values for commutation inductances L_{c1} and L_{c2}, the CB ZVS constraints are satisfied during the entire 50 Hz interval. However, although the CDCB ZVS area is substantially enlarged, full-operating-range CDCB ZVS is still not achieved. In **step 3** (also using finite values for L_{c1} and L_{c2}) the expressions from step 1 and step 2 are combined with a simple numerical iteration loop, yielding full-operating-range CDCB ZVS.

Step 1, $L_{\mathrm{c1}} = L_{\mathrm{c2}} = \infty$, CB ZVS constraints, analytical solution: It is assumed that CB ZVS is achieved when at each switching instant $\theta_{\mathrm{i}} = \{\alpha,\ \beta,\ \gamma,$ and $\delta\}$ the drain-to-source current of the switch which initiates the commutation (turn-off) has a non-zero positive value (i.e. $i_{\mathrm{p,comm}}$ for the primary side bridge and $i_{\mathrm{s,comm}}$ for the secondary side bridge). For $L_{\mathrm{c1}} = L_{\mathrm{c2}} = \infty$, $i_{\mathrm{Lc1}}(t) = i_{\mathrm{Lc2}}(t) = 0$, $i_{\mathrm{HF1}}(t) = i_{\mathrm{L}}(t)$ acc. to (8), and $i_{\mathrm{HF2}}(t) = i_{\mathrm{L}}(t) \cdot n_1/n_2$ acc. to (9). Referring $i_{\mathrm{s,comm}}$ to the transformer's primary side, $i'_{\mathrm{s,comm}} = n_2/n_1 \cdot i_{\mathrm{s,comm}}$, this yields the following CB ZVS constraints:

$$s^{\pm} \cdot i_{\mathrm{L}}(\alpha) \geqslant i_{\mathrm{p,comm}}, \tag{23}$$
$$s^{\pm} \cdot i_{\mathrm{L}}(\gamma) \geqslant i_{\mathrm{p,comm}}, \tag{24}$$
$$s^{\pm} \cdot i_{\mathrm{L}}(\beta) \geqslant i'_{\mathrm{s,comm}}, \tag{25}$$
$$s^{\pm} \cdot i_{\mathrm{L}}(\delta) \geqslant i'_{\mathrm{s,comm}}, \tag{26}$$

[8]Other setting would imply conditions where d is close or equal to 1. Here ZVS is hard to obtain as the inductor volt-seconds product needed to achieve the required current crossing in interval $\beta - \delta$ (Fig. 4(b); mode 2) is too small.

[9]f_{s}, which is doubled towards the DAB input port, is only decreased below 120 kHz for the low v_{DC1} interval in order to facilitate CDCB ZVS (see further). During this interval the harmonic content of the input current is low.

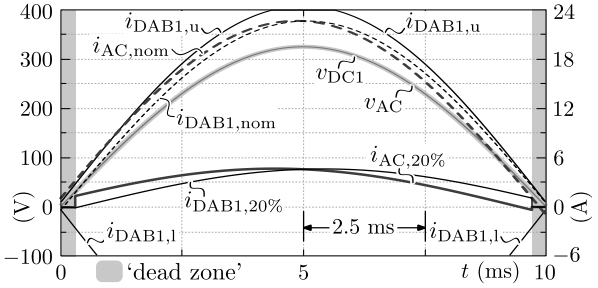


Fig. 6: DAB input currents i_{DAB1}, required to achieve $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$; PF = 0.999 resp. $I_{\mathrm{AC,P}} = 0.2 \cdot I_{\mathrm{AC,P,nom}} = 3.2\ \mathrm{A_{rms}}$; PF = 0.983. Here, $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$ (nom. AC input voltage).

with $s^{\pm} = -1$ for $\theta_{\mathrm{i}} = \{\alpha, \delta\}$, $s^{\pm} = 1$ for $\theta_{\mathrm{i}} = \{\beta, \gamma\}$. We showed in Section IV of [6] how eqns. (23)-(26), eqns. (10)-(11) and the equations in Table II for $i_{\mathrm{L}}(\theta_{\mathrm{i}})$ can be combined in order to meet these conditions in quasi the entire operating range. For a point of operation $[v_{\mathrm{DC1}}, V'_{\mathrm{DC2}}, i_{\mathrm{DAB1}}]$, for given $[L,\ n_1/n_2,\ f_{\mathrm{s}}]$, for defined set values $[i^*_{\mathrm{p,comm}},\ i'^*_{\mathrm{s,comm}}]$, and for $i_{\mathrm{DAB1}} \geqslant 0$ (positive power flow), modulation angles ϕ, τ_1, and τ_2 can be calculated using the following steps:

1) Calculate ϕ, τ_1, τ_2 using Table III, mode 2, column 2a;
2) If the result for τ_1 is $\geqslant \pi$: calculate ϕ, τ_1, τ_2 using Table III, mode 2, column 2b;
3) If the result for ϕ is $\geqslant 0$: calculate ϕ, τ_1, τ_2 using Table III, mode 1^+.

For $i_{\mathrm{DAB1}} < 0$, one can calculate ϕ, τ_1, and τ_2 following the same steps and using $|i_{\mathrm{DAB1}}|$ in the equations of Table III. The resulting phase shift angle ϕ needs to be recalculated with:

$$\forall\ i_{\mathrm{DAB1}} < 0 : \phi = (\tau_2 - \tau_1 - \phi)|_{i_{\mathrm{DAB1}} = |i_{\mathrm{DAB1}}|}. \tag{27}$$

The procedure is illustrated for a first run through a half cycle of the nominal AC input voltage ($V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$) at $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$, and PF = 0.999 (acc. to Fig. 6). Other settings are: $V_{\mathrm{DC2}} = 370$ V, $f_{\mathrm{s}} = 120$ kHz (fixed). Remind that $L_{\mathrm{c1}} = L_{\mathrm{c2}} = \infty$. The limits $i_{\mathrm{p,comm}}$ and $i_{\mathrm{s,comm}}$ are arbitrarily chosen to be 2 A, determining the set values $i^*_{\mathrm{p,comm}} = i'^*_{\mathrm{s,comm}} = 2$ A. The resulting AC trajectories are shown in Fig. 7 (solid lines[10]). In Fig. 7(c) it can be seen that $s^{\pm} \cdot i_{\mathrm{L}}(\alpha)$ and $s^{\pm} \cdot i_{\mathrm{L}}(\gamma)$ satisfy (23)-(24). However, (26) is violated during certain intervals of the 50 Hz half period, as can be seen in Fig. 7(d). This is in particular the case along the boundary between mode 1^+ and mode 2 at which (24) and (26) cannot be simultaneously met. The situation is even worse for the commutation charges[11] $Q_{\mathrm{A,av}}$ and $Q_{\mathrm{B,av}}$ which do not reach the CDCB ZVS limit (Section II-B, eqns. (14), (15)), as shown in Figs. 7(e) and 7(f).

Step 2, finite L_{c1} and L_{c2}, CB ZVS constraints, analytical solution: A second run (Fig. 7; dot dashed lines) is performed using the same conditions as in the first run, with the difference that now finite values for L_{c1} and L_{c2} are applied, being:

[10]The graphs are not fully symmetric due to the PF correction.

[11]For convenience only $Q_{\mathrm{A,av}}$ and $Q_{\mathrm{B,av}}$ for commutation instances $\theta_{\mathrm{i}} = \{\alpha$ and $\delta\}$ are shown, being the most critical for ZVS operation.

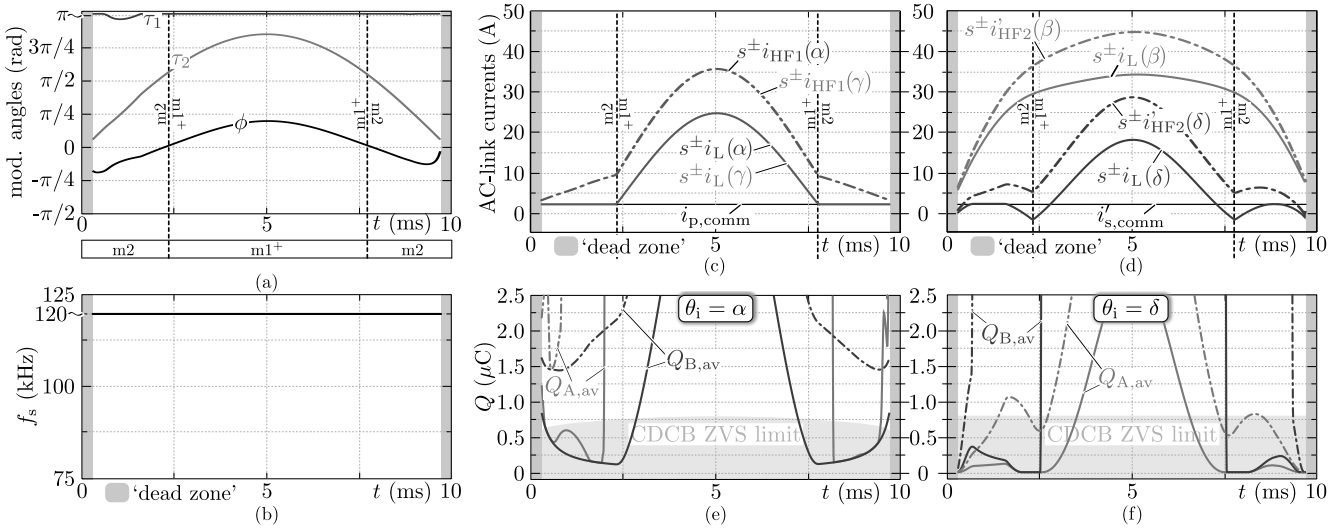


Fig. 7: AC trajectories for $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16$ A$_{\mathrm{rms}}$, PF $= 0.999$, and $V_{\mathrm{DC2}} = 370$ V (half cycle of $V_{\mathrm{AC}} = 230$ V$_{\mathrm{rms}}$; acc. to Fig. 6). Moreover, $f_{\mathrm{s}} = 120$ kHz (fixed) and $i^{*}_{\mathrm{p,comm}} = i'^{*}_{\mathrm{s,comm}} = 2$ A. Solid lines: $L_{\mathrm{c1}} = L_{\mathrm{c2}} = \infty$, dot dashed lines: $L_{\mathrm{c1}} = L_{\mathrm{c2}} = 62.1$ μH.

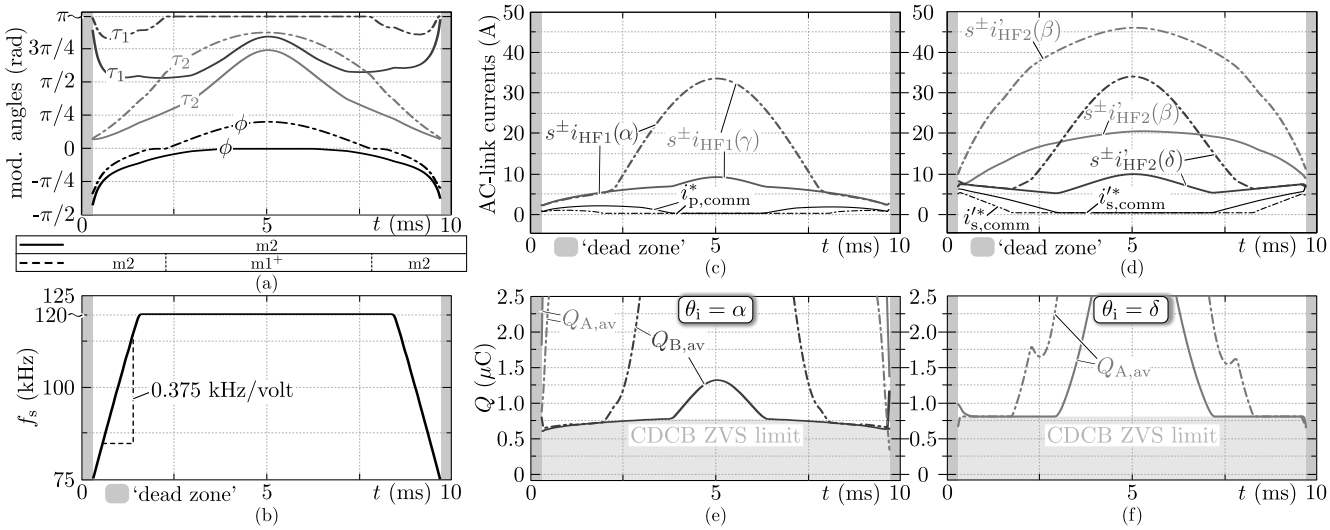


Fig. 8: AC trajectories for $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16$ A$_{\mathrm{rms}}$, PF $= 0.999$ (dot dashed lines), and $I_{\mathrm{AC,P}} = 0.2 \cdot I_{\mathrm{AC,P,nom}} = 3.2$ A$_{\mathrm{rms}}$, PF $= 0.983$ (solid lines), at $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370$ V (half cycle of $V_{\mathrm{AC}} = 230$ V$_{\mathrm{rms}}$; acc. to Fig. 6). $L_{\mathrm{c1}} = L_{\mathrm{c2}} = 62.1$ μH.

$L_{\mathrm{c1}} = L_{\mathrm{c2}} = 62.1$ μH (Table IV; the values for L_{c1} and L_{c2} are detailed in the next paragraph). The calculation of ϕ, τ_1, and τ_1, as well as their respective values are the same as in step 1 (Fig. 7(a)). In Figs. 7(c) and 7(d) it can be seen that L_{c1} and L_{c2} always benefit the commutation currents (i.e. $s^{\pm} \cdot i_{\mathrm{HF1}} > s^{\pm} \cdot i_{\mathrm{L}}$ for $\theta_{\mathrm{i}} = \{\alpha, \gamma\}$ and $s^{\pm} \cdot i'_{\mathrm{HF2}} > s^{\pm} \cdot i_{\mathrm{L}}$ for $\theta_{\mathrm{i}} = \{\beta, \delta\}$). As a result, the curves for $s^{\pm} \cdot i_{\mathrm{HF1}}$ and $s^{\pm} \cdot i'_{\mathrm{HF2}}$ are now all above the limits $i_{\mathrm{p,comm}}$ and $i'_{\mathrm{s,comm}}$ during the entire 50 Hz half cycle. However, $Q_{\mathrm{A,av}}$ and $Q_{\mathrm{B,av}}$ at $\theta_{\mathrm{i}} = \delta$ are still below the CDCB ZVS limit during certain intervals.

Step 3, finite L_{c1} and L_{c2}, CDCB ZVS constraints, semi-analytical solution: In a third run, again applying $L_{\mathrm{c1}} = L_{\mathrm{c2}} = 62.1$ μH, for each calculation of [ϕ, τ_1, τ_2] (i.e. for each operating point [v_{DC1}, V'_{DC2}, i_{DAB1}]) an iteration of $i^{*}_{\mathrm{p,comm}}$ and $i'^{*}_{\mathrm{s,comm}}$ is performed until $Q_{\mathrm{A,av}}$ and $Q_{\mathrm{B,av}}$ are above the CDCB ZVS limit. This yields the final semi-analytical CDCB ZVS modulation strategy which is summarized in Fig. 9. For each operating point [v_{DC1}, V'_{DC2}, i_{DAB1}]$_{(i,j,k)}$ of the converter's operating range the modulation angles ϕ, τ_1, and τ_2 are calculated according the procedure explained step 1 (i.e. using Table III). Thereby, a simple optimizer performs the iteration of $i^{*}_{\mathrm{p,comm}}$ and $i'^{*}_{\mathrm{s,comm}}$ until the CDCB ZVS constraints (Section II-B) are satisfied. Additionally the optimizer minimizes the arbitrarily defined cost function[12] $f_{\mathrm{cost}} = I^2_{\mathrm{HF1}} + I^2_{\mathrm{HF2}}$. After the calculation is finished for the entire DAB operating range according to Fig. 1(b) (bottom inset), it is checked if full-operating-range CDCB ZVS is achieved. If this is not the case, then L_{c1} and/or L_{c2} are

[12]As the same MOSFETs are used in both DAB bridge, f_{cost} is proportional to the DAB's condition losses.

TABLE III: Expressions for Calculating the Modulation Angles τ_1, τ_2, and ϕ acc. to [6].

	mode 2		mode 1^+
	2a	*2b*	
τ_1	$\omega_s L\left(\frac{2i^*_{p,comm}}{v_{DC1}} - \frac{di'^*_{s,comm}}{v_{DC1}-V'_{DC2}}\right) - \sqrt{\frac{d\omega_s L}{v_{DC1}-V'_{DC2}}\left(\frac{d(i'^*_{s,comm})^2\omega_s L}{v_{DC1}-V'_{DC2}} - dir\cdot 2i_{DAB1}\pi\right)}$	π	π
τ_2	$\frac{-i'^*_{s,comm}\omega_s L}{v_{DC1}-V'_{DC2}} - \sqrt{\frac{\omega_s L}{v_{DC1}V'_{DC2}}\left(\frac{(i'^*_{s,comm})^2\omega_s L}{v_{DC1}-V'_{DC2}} - dir\cdot\frac{2}{d}i_{DAB1}\pi\right)}$	$\frac{\tau_1}{d} - \frac{2\omega_s L i^*_{p,comm}}{V'_{DC2}}$	$\frac{\tau_1}{d} - \frac{2\omega_s L i^*_{p,comm}}{V'_{DC2}}$
ϕ	$\frac{-\omega_s L(i^*_{p,comm}+i'^*_{s,comm})}{v_{DC1}}$	eqn. (11)	eqn. (10)

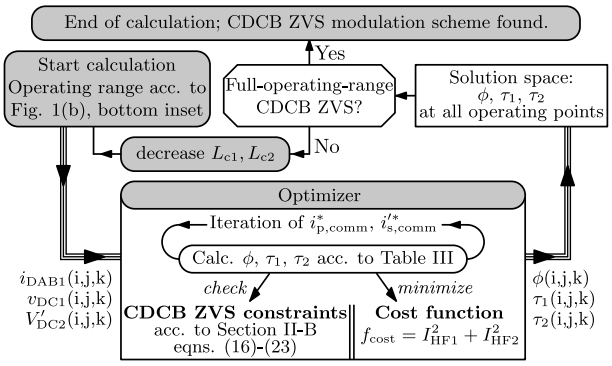


Fig. 9: Calculation procedure in order to determine a full-operating-range CDCB ZVS modulation scheme.

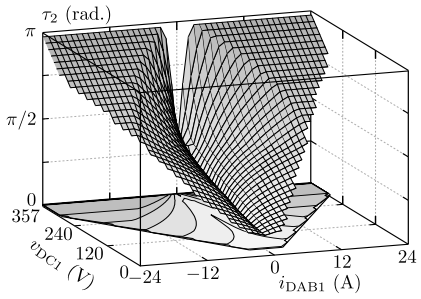


Fig. 10: Calculation result for τ_2 in the entire range (i_{DAB1}-range and v_{DC1}-range) at the, for ZVS, worst case output voltage $V_{DC2} = V_{DC2,min} = 370$ V. The simulation is performed according to step 3, including prim. and sec. side commutation inductances ($Lc1 = Lc2 = 62.1$ μH).

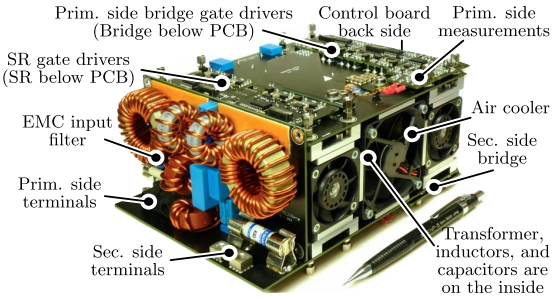


Fig. 11: 3.7 kW, single-phase, single-stage, bidirectional and isolated DAB AC–DC converter prototype (177 mm x 130 mm x 72 mm).

decreased. This process is repeated until CDCB ZVS is obtained in the full operating range. For the investigated DAB AC-DC converter[13], this yields $L_{c1} = L_{c2} = 62.1$ μH.

The results of the third run are shown in Fig. 8 (dot dashed lines) where is can be seen that CDCB ZVS is achieved during the entire 50 Hz half cycle ($Q_{A,av}$ and $Q_{B,av}$ are above the CDCB ZVS limit; Figs. 8(e) and 8(f)). The solid lines correspond with the trajectories for $I_{AC,P} = 0.2 \cdot I_{AC,P,nom} = 3.2$ A_{rms}, and PF $= 0.983$. Also here, CDCB ZVS is achieved during the entire 50 Hz half cycle. Moreover, the resulting modulation parameter trajectories as well as the mode transitions are continuous Fig. 8(a). Remarkable is the fact that in order to achieve CDCB ZVS (i.e. enough charge needs to be available in the leg current before and after the commutation instant), currents $s^{\pm}\cdot i_{HF1}(\theta_i)$ and $s^{\pm}\cdot i'_{HF2}(\theta_i)$ are often higher than 5-10 A as can be seen in Figs. 8(c) and 8(d). Important to note is also that for the low v_{DC1} intervals a variable frequency modulation is applied as can be seen in Fig. 8(b). This is necessary to achieve CDCB ZVS during the intervals where $v_{DC1} << V'_{DC2}$. Fig. 10 shows the calculation result for τ_2 in the entire range (i_{DAB1}-range and v_{DC1}-range) at the, for ZVS, worst case output voltage $V_{DC2} = V_{DC2,min} = 370$ V.

IV. Experimental Results

The experimental results are obtained from the DAB AC–DC prototype depicted in Fig. 11, which is designed according to the specifications given in Table I. The basic technical data of the system is given in Table IV. Furthermore, the transformer as well as inductors L and L_{c1} are implemented with planar EELP cores assemblies (N97 core material) and Litz wire. L_{c2} is implemented by the magnetizing inductance of the transformer (i.e. $L_{c2} = L_M = 62.1$ μH), avoiding increased volume and costs. The FCH76N60NF (SupreMOS™) and the STY112N65M5 (PowerMESH™) MOSFETs are chosen for respectively the DAB active bridges and the SR switches.

The control hardware consists of an on-board FPGA (Altera EP3C25) which is responsible for generating the PWM gate drive signals, for reading in the A/D converters, and for 'fast' overcurrent and overvoltage protection. The FPGA communicates over Ethernet with an off-board PC-based Real-Time Target (RTT) from Triphase [17][14] which can be programmed and operated through Matlab/Simulink™. Here, the PI current

[13] Although in this paper the DAB is implemented with $L_{c1} = L_{c2}$, also other scenarios can be considered, e.g. using $L_{c1} \neq L_{c2}$ or using only one commutation inductance. The latter yields more unbalanced AC-link currents.

[14] In a next phase the functions of the RTT can be implemented on the EP3C25 FPGA by means of an embedded CPU [17].

TABLE IV: Parameters of the Prototype System

Transformer turns ratio n_1/n_2	1
Switching frequency f_s	75 kHz…120 kHz
L, L_{c1}, $L_{c2} = L_M$	13 μH, 62.1 μH, 62.1 μH
C_1 (MKP), C_2 (MKP), $C_{2,st}$ (ELCO)	13.2 μF, 10.5 μF, 1.17 mF
$C_{DM1} = C_1$, C_{DM2}	13.2 μF, 1 μF
Prototype Power Density Values (at 3.7 kW Nominal Power)	
Total system, incl. EMC filter (DM & CM), incl. $C_{2,st} = 1170$ μF	2.2 kW/liter
Total system, incl. EMC filter (DM & CM), excl. $C_{2,st} = 1170$ μF	2.7 kW/liter
Total system, excl. EMC filter (DM & CM), excl. $C_{2,st} = 1170$ μF	3.2 kW/liter

and voltage controllers (i.e. control of resp. i_{DAB1} and V_{DC2}), the phase locked loop, the 'slow' protection, and the lookup tables for the control parameter generation and the delay and dead-time compensation are implemented.

A. Measurements

Below, the results from a DC–DC and AC–DC characterization of the prototype system at room temperature (T_A = 22 °C) are presented. Although the power source did not allow to sink energy, and therefore only positive power flow could be applied, the results for negative power flow would be similar as the DAB is completely symmetric.

1) DC–DC Operation: Fig. 4 depicts the HF AC-link currents and voltages for mode 1^+ and mode 2 operation, applying DC voltages at both the AC input and the DC output terminals. The measurements show very good agreement with the simulations, validating the CDCB ZVS analysis method and practical implementation of the strategy. Additionally CDCB ZVS operation was successfully verified by visual inspection of the waveforms, according to Section II-B. Very high efficiencies of more than 97 % were measured in DC–DC operation of the complete DAB AC-DC converter (positive power range), excluding auxiliary (i.e. gate drivers, fans, and control board) losses (Fig. 12). Note that these measurements also include the losses in the synchronous rectifier and the input EMC filter. Thus the efficiency of the DAB converter only is even higher.

2) AC–DC Operation: The nominal AC input voltage V_{AC} = 230 V_{rms} is provided to the input (AC-side) of the converter by an AC power source, while the output (DC-side) is connected to a 5.9 mF DC-bus and a load. Fig. 13 depicts

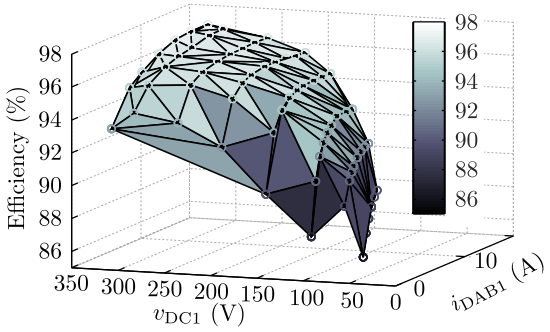


Fig. 12: Measured efficiency in DC–DC operation. The measurements are taken at the nominal DC output voltage V_{DC2} = 400 V, at different DAB input currents i_{DAB1} and input voltages v_{DC1}.

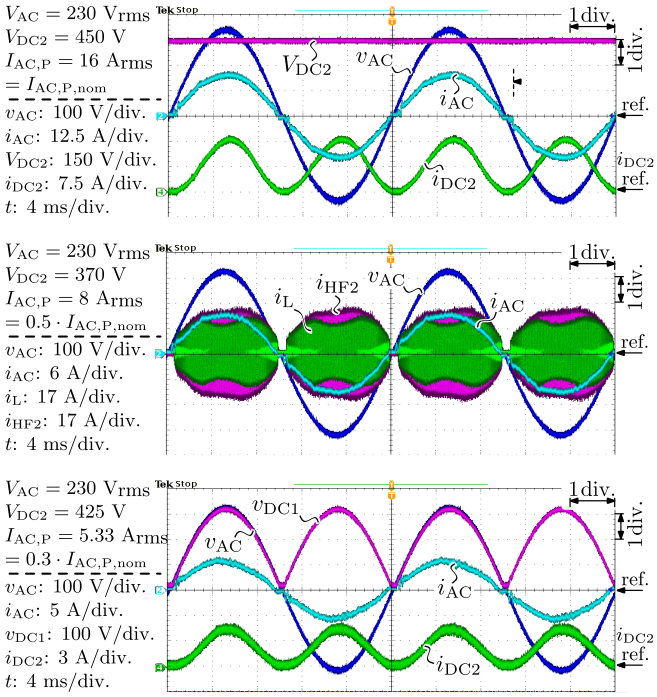


Fig. 13: Measured waveforms in AC–DC operation at different input currents and output voltages, and at the nominal AC input voltage V_{AC} = 230 V_{rms}.

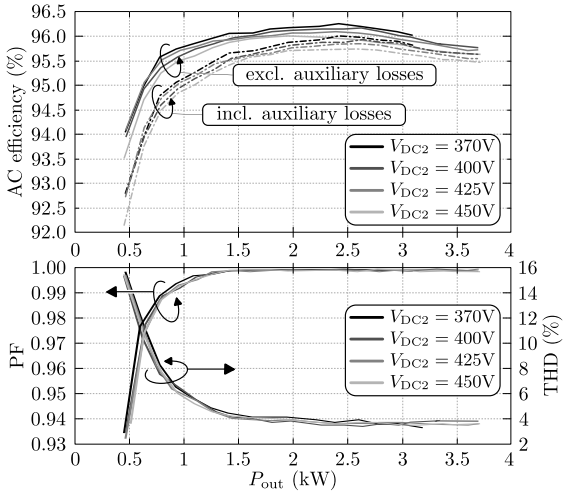


Fig. 14: Measured efficiency, THD, and PF in AC–DC operation. Measurements are taken at the nominal AC input voltage V_{AC} = 230 V_{rms}, in the entire power range and at different output voltages.

the measured waveforms at different input currents and output voltages. Note that the maximum output voltage that could be applied with the measurement setup is V_{DC2} = 450 V. The system was successfully tested in the full power range (up to an output power of 3.7 kW), showing waveforms with little distortion (Fig. 13 and Fig. 14 (bottom inset, THD)), a PF close to unity (Fig. 14 (bottom inset, PF)), and a high conversion efficiency in the entire power and output voltage range (Fig. 14 (top inset)). The latter is measured including and excluding auxiliary (i.e. gate drivers, fans, and control board) losses. Moreover, a very high power density is achieved

(Table IV). Further optimization of the AC-link components would yield even higher efficiencies and power densities.

V. Conclusion

A simple, semi-analytical modulation scheme to enable ZVS in the complete operating range of a single-phase, single-stage, bidirectional and isolated DAB AC–DC converter is presented. The conventional current-based ZVS considerations are extended towards a current-dependent charge-based (CDCB) ZVS analysis, taking into account the commutation charge of the (parasitic) switch capacitances as well as the time dependency of the commutation currents. It is shown that the CDCB ZVS constraints cannot be satisfied using the conventional implementation of the DAB converter. As a result, the use of 'commutation inductances' is considered essential. The proposed modulation scheme is successfully demonstrated on a 3,7 kW, bidirectional, and unity power factor electric vehicle battery charger which interfaces a 400 V DC-bus with the 230 Vac, 50 Hz utility grid. High conversion efficiencies (full load and low load; > 96 % peak efficiency), a high PF, a low total harmonic distortion, and a high power density are reported. This proves the practical value of the presented strategy and the feasibility of the single-stage DAB AC–DC converter for isolated, bidirectional AC–DC applications. Further optimization of the AC-link components would yield even higher efficiencies. A T-type HF AC-link and/or the use of the transformer's leakage inductances are the subject of further optimization.

References

[1] S. Haghbin, S. Lundmark, M. Alakula, and O. Carlson, "Grid-Connected Integrated Battery Chargers in Vehicle Applications: Review and New Solution," *IEEE Trans. on Ind. Electron.*, vol. 60, no. 2, pp. 459–473, Feb. 2013.

[2] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodriguez, "Control of Power Converters in AC Microgrids," *IEEE Trans. on Power Electron.*, vol. 27, no. 11, pp. 4734–4749, Nov. 2012.

[3] K. Clement-Nyns, E. Haesen, and J. Driesen, "The Impact of Vehicle-to-Grid on the Distribution Grid," *Electric Power Systems Research, Elsevier*, vol. 81, no. 1, pp. 185–192, Jan. 2011.

[4] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A Three-Phase Soft-Switched High Power Density DC/DC Converter for High Power Applications," in *IEEE Ind. Appl. Soc. Annual Meeting*, vol. 1, Oct. 1988, pp. 796–805.

[5] K. Vangen, T. Melaa, S. Bergsmark, and R. Nilsen, "Efficient High-Frequency Soft-Switched Power Converter with Signal Processor Control," in *IEEE 13th Int. Telecommun. Energy Conf. (INTELEC)*, Nov. 1991, pp. 631–639.

[6] J. Everts, J. Van den Keybus, F. Krismer, J. Driesen, and J. W. Kolar, "Switching Control Strategy for Full ZVS Soft-Switching Operation of a Dual Active Bridge AC/DC Converter," in *IEEE 27th Ann. Appl. Power Electron. Conf. and Expo. (APEC)*, Feb. 2012, pp. 1048–1055.

[7] F. Jauch and J. Biela, "Single-Phase Single-Stage Bidirectional Isolated ZVS AC-DC Converter with PFC," in *15th Int. Power Electron. and Motion Control Conf. (EPE/PEMC)*, Sept. 2012, pp. LS5d.1,1–8.

[8] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, "Transformer-Coupled Multiport ZVS Bidirectional DC–DC Converter With Wide Input Range," *IEEE Trans. on Power Electron.*, vol. 23, no. 2, pp. 771–781, March 2008.

[9] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Modulation Strategy to Operate the Dual Active Bridge DC-DC Converter Under Soft Switching in the Whole Operating Range," *IEEE Trans. on Power Electron.*, vol. 26, no. 4, pp. 1228–1236, April 2011.

[10] F. Krismer and J. W. Kolar, "Closed Form Solution for Minimum Conduction Loss Modulation of DAB Converters," *IEEE Trans. on Power Electron.*, vol. 27, no. 1, pp. 174–188, Jan. 2012.

[11] L. Xue, D. Diaz, Z. Shen, F. Luo, P. Mattavelli, and D. Boroyevich, "Dual Active Bridge Based Battery Charger for Plug-In Hybrid Electric Vehicle with Charging Current Containing Low Frequency Ripple," in *IEEE 28th Annual Applied Power Electronics Conference and Exposition (APEC 2013)*, March 2013, pp. 1920–1925.

[12] Z. Shen, R. Burgos, D. Boroyevich, and F. Wang, "Soft-Switching Capability Analysis of a Dual Active Bridge DC-DC Converter," in *IEEE Elec. Ship Techn. Symp. (ESTS)*, April 2009, pp. 334–339.

[13] G. Guidi, A. Kawamura, Y. Sasaki, and T. Imakubo, "Dual Active Bridge Modulation with Complete Zero Voltage Switching Taking Resonant Transitions Into Account," in *14th Europ. Conf. on Power Electron. and Appl. (EPE)*, Sept. 2011, pp. 1–10.

[14] M. H. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance Characterization of a High-Power Dual Active Bridge dc-to-dc Converter," *IEEE Trans. on Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Nov.-Dec. 1992.

[15] Gecko-Simulations AG - GeckoCIRCUITS. Free version available. [Online]. Available: www.gecko-simulations.com

[16] U. Drofenik, A. Musing, and J. W. Kolar, "Voltage-Dependent Capacitors in Power Electronic Multi-Domain Simulations," in *Int. Power Electron. Conf. (IPEC)*, June 2010, pp. 643–650.

[17] Triphase NV. 3PExpress^{TM}, Rapid System Development for Power Conversion Applications. [Online]. Available: www.triphase.com