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PV Panel-Integrated High Step-Up High Efficiency Isolated GaN DC-DC Boost Converter

M. Kasper,
M. Ritz,
D. Bortis,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

PV Panel-Integrated High Step-up High Efficiency Isolated GaN DC-DC Boost Converter

Matthias Kasper, Magdalena Ritz, Dominik Bortis and Johann W. Kolar
Power Electronic Systems Laboratory
ETH Zurich, Physikstrasse 3
Zurich, 8092, Switzerland
kasper@lem.ee.ethz.ch

***Abstract*—PV systems consisting of series connected PV panels suffer from reduced power output if the panels within a string receive unequal irradiance. One possible solution to this problem is to provide each panel with a high step-up DC-DC converter that allows to connect all converter outputs in parallel at the input of a central DC-AC converter feeding the PV power into the mains. In this paper, a classification of high step-up DC-DC converter concepts is presented. The isolated series resonant converter in half-cycle discontinuous conduction mode with an additional boost stage is selected as best suited concept and optimized by means of an efficiency/power density (η-ρ) Pareto optimization. This also includes an adpation of the modulation scheme for low output power in order to maximize the conversion efficiency. Based on the optimization results a converter prototype is presented and efficiency measurement results are shown.**

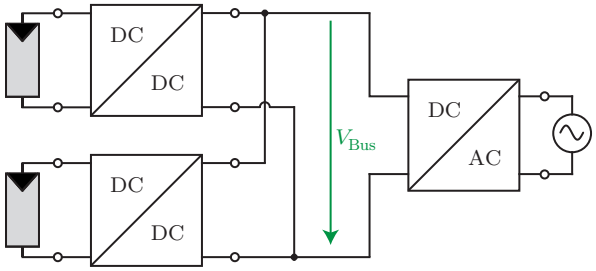

Fig. 1: Simplified PV system consisting of two PV panels with high step-up panel-integrated DC-DC converters and a central DC-AC inverter. Each PV panel output voltage is stepped-up to reach the level of the bus voltage V_{Bus} of the central DC-AC inverter.

I. Introduction

Photovoltaic (PV) systems usually comprise one or more parallel strings consisting of series connected PV panels. Due to the series connection the panel voltages, which are usually around 20 to 40 V depending on the temperature, are added up to reach a certain bus voltage. In Europe, at least around 380 V are required for the central (single-phase) DC-AC inverter to feed power into the grid. Moreover, this series connection of PV panels inherently implies that the output currents of all PV panels are equal. However, if the PV panels in a string receive unequal irradiance, the condition of equal current generation within a string is no longer fulfilled. As a result, the power which can be harvested from the string decreases below the theoretical available power. This is due to the fact that the shaded PV panels are bypassed if the string current is kept at the level of the unshaded panels. Alternatively, the string current could also be reduced by the central DC-AC inverter to match the (low) current level of the shaded panel. This would in turn lead to a sub-optimal operation of the unshaded panels and thus also to a power output of the string below the theoretical maximum.

As a solution to overcome this limitation, different DC-DC converter concepts [1] can be used on PV panel level which allow operating each panel in the Maximum Power Point (MPP). Among those DC-DC converters there are also concepts that no longer connect the PV panels in series but in parallel. Such a parallel connected full-power (cf. [1]) converter concept will be examined in this paper. With this approach, each PV panel is equipped with a DC-DC converter and the converter outputs are connected in parallel, i.e. to the DC-bus at the central DC-AC inverter input, as shown in **Fig. 1**. This requires the use of an appropriate converter topology with a high step-up ratio and, at the same time, also a high conversion efficiency. In Section II different topologies that meet these requirements are identified and evaluated and the most suitable concept is selected for an in-depth analysis and optimization. The η-ρ (efficiency/power density) Pareto optimization and the corresponding results are presented in Section III. Based on the optimization outcome, a prototype employing only GaN switches is assembled and the measurement results are shown in Section IV. Finally, conclusions are drawn in Section V.

II. Classification of High Step-Up Topologies

In this section an overview and a classification of suitable DC-DC converter topologies for high step-up voltage conversion is presented.

In literature, several converter topologies have been proposed with both high step-up ratios and high efficiency. Those topologies can be classified into two main categories: isolated and non-isolated concepts. Depending on the country where the PV system is installed, it might be necessary to have an isolation stage in the PV panel integrated DC-DC converters. However, the criteria for selecting the best suited concept for PV panel integration are common to both categories: high conversion efficiency both at full and part load, easy controllability, high power density and a low part count for reduced costs as well as a long system lifetime.

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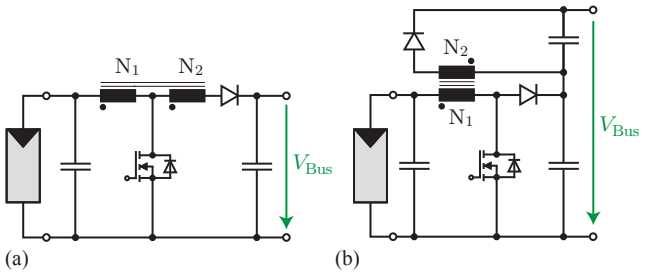

Fig. 2: Non-isolated high step-up converter topologies: (a) boost converter with tapped inductor and (b) boost-flyback topology.

A. Non-isolated Topologies

Non-isolated high step-up converters are usually either boost converters with coupled inductors (**Fig. 2(a)**) [2]–[5] or boost converters combined with a flyback converter [6]–[8] (**Fig. 2(b)**). A high conversion efficiency can be achieved with soft-switching if additional circuits are added to these basic concepts. The converters are auxiliary modifications of the conventional boost converter structure, in which large duty cycles would occur at such high conversion ratios. As a consequence, at high conversion ratios the conventional boost converter would suffer from low efficiency due to high switching losses resulting from hard switching at high voltage and from the reverse recovery effect of the diode. Additionally, since the conversion gain of the boost converter is a non-linear function of the duty cycle, large duty cycles would also have a negative effect on the control dynamics.
High conversion ratios can also be achieved with voltage multiplier topologies, such as e.g. switched capacitor converters like the flying capacitor converter [9], [10]. A drawback of these topologies is the limited controllability of the output voltage, which is usually an integral multiple of the input voltage and thus not continuously adjustable. This would only be given for a hybrid combination of a switched capacitor and an inductor-based converter [11].

B. Isolated Topologies

Isolated DC-DC converter topologies usually employ a high frequency transformer. A transformer is inherently well suited for the application in converters with a high voltage conversion requirement, as the step-up ratio can be set with the turns ratio. The topologies with a transformer can work with either unidirectional core excitation, as e.g. given for flyback or forward converter, or with bidirectional core excitation (push-pull, half-bridge or full-bridge converter). Since the former category exhibits phases within a switching period where no power is transferred to the load, their power density and efficiency are lower compared to the latter category and thus is not considered further. For reduced switching losses and component stresses either additional auxiliary circuits, e.g. snubber circuits, can be used or topologies with inherent ZVS/ZCS capability such as the resonant half-bridge and full-bridge converters can be selected [12]. The series resonant converter (SRC) is especially well suited for applications with high output voltage and high efficiency at part load operation

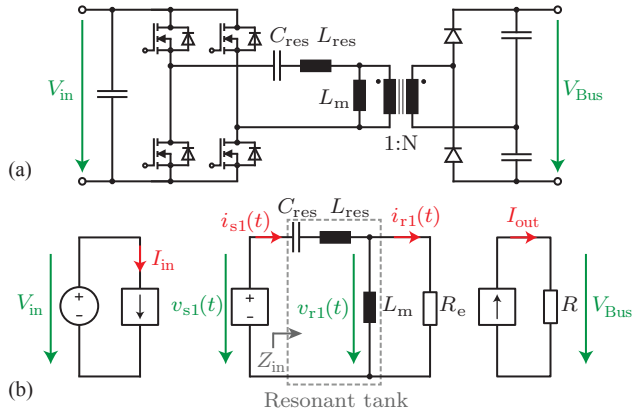

Fig. 3: (a) Series resonant converter topology and (b) equivalent circuit which models the fundamental frequency behavior.

[13] and is therefore selected for further consideration (cf. **Fig. 3(a)**). As the input voltage needs to be stepped up, the SRC is advantageously equipped with a full-bridge inverter and a voltage doubler as rectification circuit, in order to reach the highest voltage transfer ratio at a given transformer turns ratio. In combination with MOSFETs it is preferable to operate the SRC above resonance [14] as this allows utilizing the resonant current at the switching instant to achieve ZVS.

C. Selection of Topology

From the aforementioned classification of topologies, the SRC offers the advantages of high efficiency, as it can operate without switching losses due to ZVS, and a high power density because of its bidirectional core excitation. However, the switching frequency has to be adjusted in order to vary the voltage transfer ratio of the converter such that the varying PV panel voltage is stepped-up to a fixed output voltage level.
Based on the SRC circuit depicted in **Fig. 3(a)** the equivalent circuit for the fundamental harmonics analysis (FHA) can be derived, as visualized in **Fig. 3(b)**. The resonant network reacts mainly to the first harmonic of the square wave voltage produced by the full-bridge switch network, thus higher harmonics can be neglected in the analysis allowing the use of the FHA method [13]. Hence, the input voltage of the resonant tank $v_{s1}(t)$ equals the first harmonic of the square wave voltage, i.e.

$$v_{s1}(t) = \frac{4V_{in}}{\pi} \sin(\omega_s t) \ . \tag{1}$$

where ω_s is determined by the switching frequency $\omega_s = 2\pi f_s$. The average value of the input current I_{in} can be obtained by averaging the absolute value of the current $i_{s1}(t)$, which is drawn by the resonant tank, over half a switching period. This yields

$$I_{in} = \frac{2\hat{I}_{s1}}{\pi} \cos(\phi_s) \ , \tag{2}$$

where $\hat{I}_{s1}$ is the amplitude of the first harmonic of the sinusoidal resonant current $i_{s1}(t)$ and ϕ_s is the phase angle with respect to the voltage $v_{s1}(t)$.
The rectifier network can also be analyzed with the FHA

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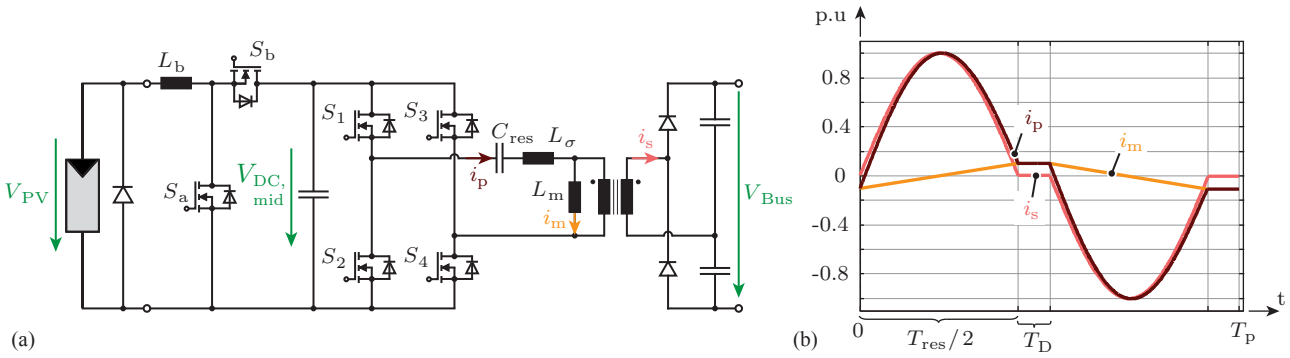

Fig. 4: Proposed converter topology: (a) two stage converter consisting of a boost converter and a SRC and (b) working principle of the SRC. The SRC is operated in the half-cycle discontinuous conduction mode which utilizes the magnetizing current i_m for ZVS during dead-time T_D and features a constant voltage transfer ratio.

method if it is again assumed that the resonant tank has a negligible response to higher harmonics. Thus, the voltage $v_{r1}(t)$ (on the primary side of the transformer) is the first harmonic of the square wave voltage that is impressed by the rectified current. This yields for a voltage doubler configuration

$$v_{r1}(t) = \frac{2V_{Bus}}{N\pi}\sin(\omega_s t - \phi_s)\ , \tag{3}$$

where N is the transformer turns ratio. The voltage $v_{r1}(t)$ is in phase with the resonant tank output current

$$i_{r1}(t) = \hat{I}_{r1}\sin(\omega_s t - \phi_s)\ , \tag{4}$$

where $\hat{I}_{r1}$ is the peak value of the sinusoidal current at fundamental frequency. Based on that, the value of the DC output current I_{out} can be obtained by averaging the rectified resonant tank output current $|i_{r1}(t)|$ over half a switching period, which results in

$$I_{out} = \frac{1}{N\pi}I_{r1}\ . \tag{5}$$

Furthermore, the equivalent load resistance R_e on the primary side of the transformer can be calculated as

$$R_e = \frac{v_{r1}(t)}{i_{r1}(t)} = R\frac{2}{N^2\pi^2}\ . \tag{6}$$

With the result for R_e the input impedance of the resonant tank can be derived as

$$Z_{in}(s) = sL_{res} + \frac{1}{sC_{res}} + (R_e||sL_m)\ . \tag{7}$$

Based on that, the voltage gain of the resonant tank can be derived as

$$G_{res}(s) = \left|\frac{(R_e||sL_m)}{Z_{in}(s)}\right|\ , \tag{8}$$

which varies with the switching frequency. The resonant tank exhibits two resonance frequencies given as

$$f_{res,1} = \frac{1}{2\pi\sqrt{L_{res}C_{res}}}\ ,\ f_{res,2} = \frac{1}{2\pi\sqrt{(L_{res}+L_m)C_{res}}}\ , \tag{9}$$

and the gain of the resonant tank equals one, if operated at $f_{res,1}$. If it is assumed that the leakage inductance of the transformer, which usually has a value below one or two percent of the value of the magnetizing inductance, is utilized as resonance inductance L_{res} then the frequencies $f_{res,1}$ and $f_{res,2}$ differ by a factor of around ten, according to eq. (9). The transfer ratio of V_{in} to V_{Bus} for $f_{sw} \neq f_{res,1}$ is not only depending on the switching frequency, but also on the power level. Thus, in order to cover the total PV panel voltage range ($V_{PV} = 15...45\,V$) at all power levels, the converter design becomes challenging. To account for that, in [15] the leakage inductance was chosen to be in the same order of magnitude as the magnetizing inductance, thus requiring a transformer design with dedicated windings for achieving a high leakage inductance. If, in contrast, the magnetizing inductance is reduced, e.g. by introducing an airgap in the main magnetic path, the magnetizing current will increase and cause higher conduction losses.

From the considerations above it can be seen that the voltage transfer ratio of V_{in} to V_{Bus} is only constant, if the SRC is operated at resonance frequency $f_{sw} = f_{res,1}$. At this operating point the transfer ratio is independent of the load current. Therefore, in this paper a two-stage topology is proposed, which consists of a boost converter and a SRC as shown in **Fig. 4(a)**. The boost converter steps the changing PV voltage V_{PV} to an intermediate constant voltage bus $V_{DC,mid}$. The SRC converter is operated at $f_{res,1}$ in half-cycle discontinuous conduction mode (HC-DCM) [16] as shown in **Fig. 4(b)**. This enables a very efficient voltage conversion by utilizing the transformer leakage inductance as resonance inductance and the magnetizing current in combination with the parasitic output capacitances of the full-bridge MOSFETs for ZVS switching. The duration of the square wave pulses of the full-bridge are equal to the time required for the resonant current to complete one half wave, i.e. $T_{res}/2$. Between the square wave pulses a dead-time T_D is introduced, during which the remaining magnetizing current charges and/or discharges the parasitic capacitances of the MOSFETs in such way that ZVS is achieved before the full-bridge switches turn on for the next half cycle. As only the magnetizing current is used for ZVS, the SRC can operate without switching losses independent of the transferred power.

The concept of applying two converter stages simplifies the design and the control of the system. The bridge legs of the SRC are operated at a fixed switching frequency with 50% duty cycle and 180 ° phase shift. Since the output voltage V_{Bus}

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Tab. I: Specifications of the PV panel integrated high-step up boost converter.

Parameter	Variable	Value
Max. converter power	P_{conv}	275 W
Max. input voltage	$V_{\text{PV,max}}$	45 V
Min. input voltage	$V_{\text{PV,min}}$	15 V
Max. input current	$I_{\text{PV,max}}$	10 A
Bus voltage	V_{Bus}	400 V
Min. ambient temperature	T_{min}	−20°C
Max. ambient temperature	T_{max}	80°C

is controlled by the central DC-AC inverter, the voltage of the intermediate DC bus $V_{\text{DC,mid}}$ is also constant. Thus, the boost stage can perform Maximum Power Point (MPP) tracking of the PV panel by proper variation of the duty cycle D_{boost} of switch S_{a}.

III. Converter Optimization

In this chapter the design and optimization of the boost converter and the SRC stage are presented. The full set of converter specifications is listed in **Tab. I**.
The degrees of freedom in the design of the converter are the level of the intermediate bus voltage $V_{\text{DC,mid}}$, the resonance frequency f_{res} of the SRC and the switching frequency $f_{\text{sw,boost}}$.

A. Choice of the Value of $V_{DC,mid}$

In contrast to the SRC stage operating in ZVS at all times, the boost stage creates switching losses since it operates in continuous conduction mode. The switching losses of the boost converter are influenced by the input current as well as by the voltage $V_{\text{DC,mid}}$ and increase with increasing values of both. As the input current is determined by the MPP of the PV panel and thus cannot be altered, it is preferable to select a value of $V_{\text{DC,mid}}$ which is as low as possible, i.e. slightly above the maximum converter input voltage to keep the duty cycle in a reasonable range with good controllability and efficiency. Based on this, an intermediate bus voltage level of $V_{\text{DC,mid}} = 50\,\text{V}$ is chosen. Thus, the duty cycle of the boost converter varies in the range of $D_{\text{boost}} = 0.1...0.7$ for input voltages in the range of $V_{\text{PV}} = 15...45\,\text{V}$.

B. Optimization Procedure of Boost Stage

The losses of the boost stage comprise inductor losses and semiconductor switching and conduction losses. Regarding the inductor L_{b}, different values for the peak-to-peak current ripple $\Delta I_{\text{L,max}} = [20\%...100\%]$ of the maximum average value of the inductor current $I_{\text{in,max}}$ have been used for the following optimization. Based on that, a value of $\Delta I_{\text{L,max}} = 60\%$ of $I_{\text{in,max}}$ has been selected. The maximum inductor current ripple occurs for $D_{\text{boost}} = 0.5$ which is given at $V_{\text{PV}} = 25\,\text{V}$. For the product of inductance and switching frequency this yields a value of

$$L_{\text{b}} f_{\text{sw}} = \frac{V_{\text{DC,mid}}}{4\Delta I_{\text{L,max}} I_{\text{in,max}}} \approx 2.1\,\text{H}\cdot\text{Hz}\ . \tag{10}$$

Furthermore, the maximum flux density in the core has to be kept well below the saturation flux density, i.e.

$$B_{\text{sat}} > B_{\text{max}} = \frac{L_{\text{b}} \hat{I}_{\text{L}}}{N_{\text{Ind}} \cdot A_{\text{c,min}}}\ , \tag{11}$$

with N_{ind} being the number of turns, $A_{\text{c,min}}$ the minimum core cross section and $\hat{I}_{\text{L}}$ the peak value of the inductor current.
The inductor losses comprise core losses and winding losses. The core losses can be calculated by using the improved Generalized Steinmetz Equation (iGSE), which yields as core losses per unit volume

$$P_{\text{V,core}} = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt\ , \tag{12}$$

with ΔB being the local peak-to-peak flux density and

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta}\ , \tag{13}$$

where α, β and k are material parameters that can be deduced from manufacturer's data sheets. According to [17], equations (12) and (13) can be simplified for the case of piecewise linear waveforms as present in the converter.
The winding losses are caused by the DC inductor current and by eddy current losses, which increase with increasing frequency. The eddy currents contribute to skin and proximity effect losses, which can be analytically approximated according to [18]. Harmonics up the 10th order are considered in the calculations.
For the boost and the synchronous rectification switch Gallium Nitrid (GaN) FETs by EPC (EPC2001) are selected, since they feature lower switching losses compared to Silicon MOSFETs at a given switching frequency. As the switching losses are strongly influenced by parasitic inductances of the circuit layout, a layout similar to the one already successfully tested in [1] has been taken as a reference and the losses have been validated with LTSpice simulations of the manufacturer's switch models. Furthermore, the on-state resistance $R_{\text{DS,on}}$ of the switches and the resistance of the PCB traces account for conduction losses.

C. Optimization Procedure of SRC

Since the SRC is operated with ZVS, the main loss contributors are transformer losses and conduction losses in both the switches and the PCB traces.
The transformer needs to be designed for a turns ratio of $N_{\text{sec}}/N_{\text{prim}} = 4$ because the voltage needs to be stepped up from $V_{\text{DC,mid}} = 50\,\text{V}$ to half the value of $V_{\text{Bus}} = 400\,\text{V}$ since a voltage doubler is used for the rectification. As a first approximation, disregarding the magnetizing current $i_{\text{m}}(t)$ and the dead-time T_{D}, the peak value of the primary current $\hat{I}_{\text{p}}$ can be calculated for a given PV panel power P_{PV} as

$$\hat{I}_{\text{p}} = \frac{\pi \cdot P_{\text{PV}}}{2 \cdot V_{\text{DC,mid}}}\ . \tag{14}$$

and the RMS value as

$$I_{\text{p,rms}} = \frac{\hat{I}_{\text{p}}}{\sqrt{2}} = \frac{\sqrt{2}\pi \cdot P_{\text{PV}}}{4 \cdot V_{\text{DC,mid}}}\ . \tag{15}$$

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As the current exhibits a sinusoidal waveform, the winding losses can be calculated by using only the fundamental frequency for the calculation of the AC resistance of the windings, taking proximity and skin effect into account.
The core losses can be assessed by first considering the flux linkage Ψ_p in the transformer, which exhibits in a first approximation a triangular waveform with a peak value of $\hat{\Psi}_\mathrm{p}$ on the primary side, i.e.

$$\hat{\Psi}_\mathrm{p} = \frac{V_\mathrm{DC,mid}}{4 \cdot f_\mathrm{sw}} \ . \tag{16}$$

Depending on the flux linkage, the flux density in the core can be calculated as

$$B = \frac{\Psi_\mathrm{p}}{N_\mathrm{p} \cdot A_\mathrm{c,min}} \ , \tag{17}$$

with a peak value that has to be well below the saturation flux density

$$B_\mathrm{sat} > B_\mathrm{max} = \frac{\hat{\Psi}_\mathrm{p}}{N_\mathrm{p} \cdot A_\mathrm{c,min}} \ . \tag{18}$$

For the switches of full-bridge stage also GaN FETs by EPC (EPC2001) are selected due to a lower capacitance $C_\mathrm{OSS}(V_\mathrm{DS})$ compared to Si MOSFETs with similar voltage rating and on-state resistance $R_\mathrm{DS,on}$. This allows to minimize the dead-time T_D which is required to charge/discharge the capacitances $C_\mathrm{OSS}(V_\mathrm{DS})$ of all switches.

D. Optimization Results

For different core types (ETD and EFD cores) made of N87 Siferrite material and a selection of Rupalit litz wires the inductor and transformer losses have been calculated for an operating point of $P_\mathrm{PV} = 250\,\mathrm{W}$ and $V_\mathrm{PV} = 30\,\mathrm{V}$. As several combinations of inductor cores and transformer cores exist, an efficiency/power density (η-ρ) Pareto plot (**Fig. 5**) is created, which visualizes the achievable converter efficiency for all possible combinations at the selected operating point. For calculating the total converter volume, boxed volumes of the main components, i.e. the inductor, the transformer and PCB have been considered.

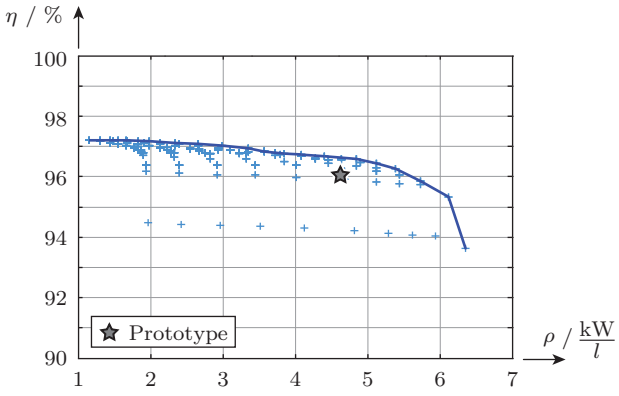

Fig. 5: Optimization results for an operating point of $P_\mathrm{PV} = 250\,\mathrm{W}$ and $V_\mathrm{PV} = 30\,\mathrm{V}$ visualized as efficiency/power density (η-ρ) Pareto plot. Each marker represents one combination of an inductor core size and transformer core size.

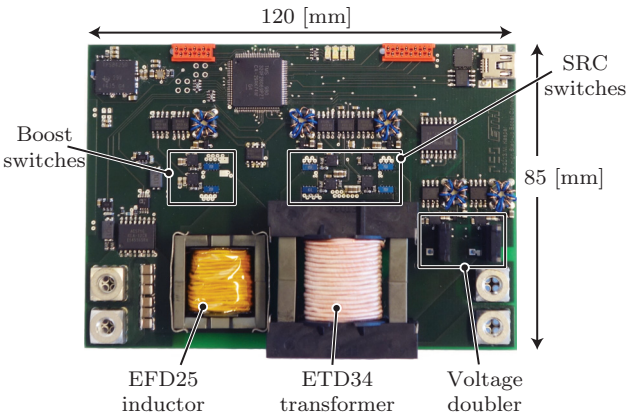

Fig. 6: Prototype of the high step-up boost converter comprising a boost stage, an isolated SRC stage and a voltage doubler rectifier.

IV. Prototype and Experimental Results

In this chapter a prototype of the two stage high-step up boost converter together with measurement results is presented.
Based on the optimization results a converter prototype has been assembled, shown in **Fig. 6**. The switching frequency of the boost stage is set to an optimized value of $f_\mathrm{sw,boost} = 210\,\mathrm{kHz}$ and the inductor consists of an EFD25 core with an inductance of $L_\mathrm{b} \approx 10\,\mu\mathrm{H}$ i.e. $N = 7$ turns (420 strands with $71\,\mu\mathrm{m}$ diameter) and an air gap of $l_\mathrm{gap} = 0.76\,\mathrm{mm}$.
The transformer of the SRC is composed of an ETD34 core with $N_\mathrm{p} = 9$ primary turns (420 strands with $71\,\mu\mathrm{m}$ diameter) and $N_\mathrm{s} = 36$ secondary turns (120 strands with $71\,\mu\mathrm{m}$ diameter) and is operated at a resonance frequency of $f_\mathrm{res} = 350\,\mathrm{kHz}$. In order to limit the influence of the dead time T_D on the RMS value of the transformer current, its value is limited to 10% of the resonance period. This requires a magnetizing inductance of $L_\mathrm{m} \approx 60\,\mu\mathrm{H}$ and thus a total air gap of $l_\mathrm{gap} = 0.1\,\mathrm{mm}$ in the transformer core. With a leakage inductance of $L_\sigma \approx 380\,\mathrm{nH}$ the resonance capacitance has to be $C_\mathrm{m} \approx 484\,\mathrm{nF}$ in order to tune the resonance circuit to the desired resonance frequency.

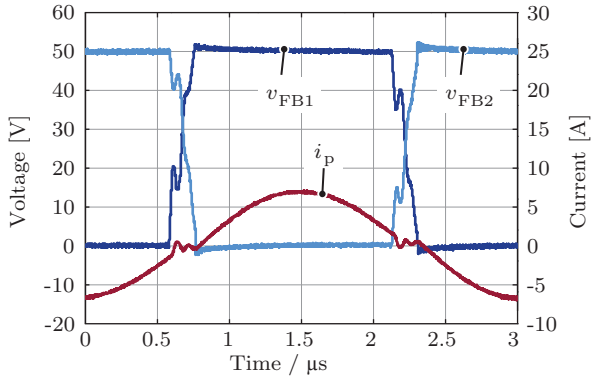

Fig. 7: Measured waveforms of the converter prototype showing the output voltage of both bridge-legs (v_FB1 and v_FB2) of the full bridge and the transformer current i_p on the primary side at an operating point of $P_\mathrm{PV} = 200\,\mathrm{W}$, $V_\mathrm{DC,mid} = 50\,\mathrm{V}$ and $V_\mathrm{Bus} = 400\,\mathrm{V}$.

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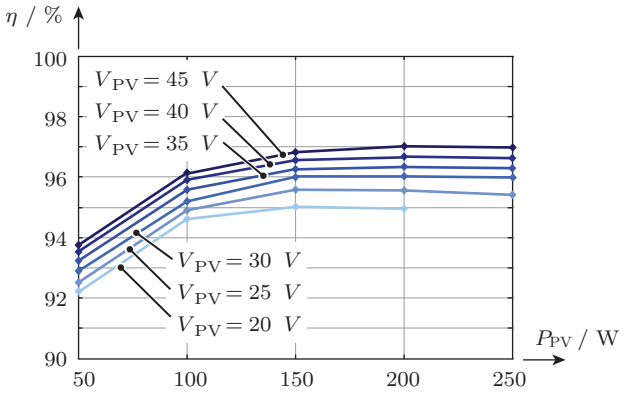

Fig. 8: Measured efficiency of the prototype for different levels of input voltage V_{PV} and different levels of converter input power P_{PV}.

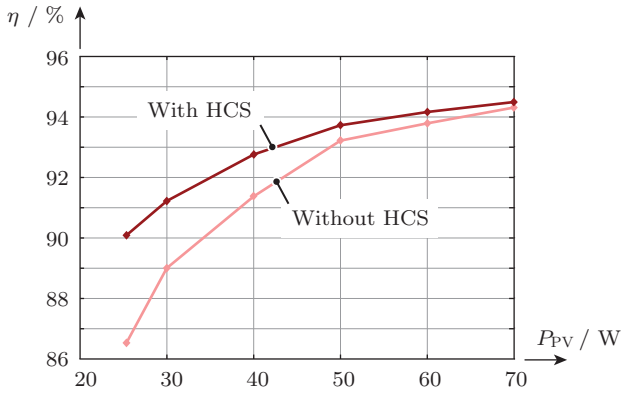

Fig. 10: Comparison between the measured efficiency of the prototype in half-cycle skipping (HCS) mode and in normal HC-DCM for an input voltage of $V_{PV} = 35\,\mathrm{V}$ at different levels of converter input power P_{PV}.

The voltage doubler rectifier circuit consists of Silicon Carbide (SiC) diodes by Cree (C3D02060E).

The measurement results shown in **Fig. 7** verify the operation of the SRC in half-cycle discontinuous conduction mode. After each resonant half-wave of the primary current i_p, the magnetizing current charges/discharges the parasitic capacitances of the GaN FETs in the full-bridge as can be seen with the bridge-leg voltages v_{FB1} and v_{FB2}. Thus, no switching losses are generated in the full-bridge switches of the SRC.

The converter efficiency has been measured for different input voltages V_{PV} at different levels of input power P_{PV} and the results are visualized in **Fig. 8**. The converter efficiency increases with increasing input voltage V_{PV} as the conduction and switching losses of the boost stage decrease with decreasing input current i.e. increasing input voltage at a given power level. A peak efficiency of around 97% is achieved at the operating point with an input voltage of $V_{PV} = 45\,\mathrm{V}$ and an input power of $P_{PV} = 200\,\mathrm{W}$.

A. Improving Part Load Efficiency

For operation of the SRC in HC-DCM the magnetizing flux causes core losses independent of the transferred power. At low levels of the input power P_{PV} these constant losses constitute a relatively large part of the total losses since other loss contributors, such as e.g. conduction losses and switching losses of the boost stage, decrease with decreasing input power. Hence, in order to improve the part load efficiency of the converter, the modulation scheme of the SRC can be slightly changed as shown in **Fig. 9** by introducing a free-wheeling state for the magnetizing current during time T_{FW}. This half-cycle skipping (HCS) mode reduces the frequency, at which resonant half wave pulses are processed by the SRC and thus also the frequency at which the magnetizing flux changes, which results in lower core losses. This principle of operation is comparable to the line cycle skipping (LCS) method of PFC boost converters which achieves an almost flat efficiency curve over the transferred power [19]. One disadvantage, however, are increased peak and RMS values of the resonant current, giving rise to higher winding losses in the transformer. Thus, an optimal free-wheeling time T_{FW} can be found for each power level with the lowest converter losses.

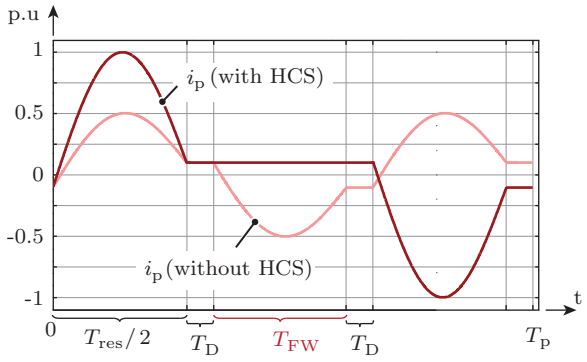

Fig. 9: Operating principle of the half-cycle skipping (HCS) mode. In comparison to the normal HC-DCM operation, a free-wheeling state for the magnetizing current during time T_{FW} is introduced.

The efficiency measurement results for the prototype at low power operation at an input voltage of $V_{PV} = 35\,\mathrm{V}$ are shown in **Fig. 10** for the case of HCS operation in comparison to normal HC-DCM operation.

V. Conclusion

The analysis and design of a high step-up DC-DC converter with high efficiency for PV panel integration has been presented. The converter employs a boost stage for the adaption of the temperature dependent PV panel output voltage of $V_{PV} = 15...45\,\mathrm{V}$ to an intermediate constant bus voltage of $V_{DC,mid} = 50\,\mathrm{V}$. The high step-up conversion to a converter output voltage of $V_{Bus} = 400\,\mathrm{V}$ is accomplished by a second isolated stage i.e. a series resonant converter (SRC) operated in half-cycle discontinuous mode (HC-DCM), where the magnetizing current of the transformer is utilized to achieve soft-switching. Based on the results of an efficiency/power density (η-ρ) Pareto optimization, a prototype has been assembled employing only wide band-gap semiconductor devices such as GaN FET switches and SiC diodes. Measurement results verify the operation of the SRC in HC-DCM and also show that a peak converter efficiency of slightly above 97% could be achieved at a power level of $P_{PV} = 200\,\mathrm{W}$ and an input

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voltage of $V_{\mathrm{PV}} = 35\,\mathrm{V}$. The efficiency at part load operation can be improved by operating the SRC in half-cycle skipping (HCS) mode which reduces the core losses of the transformer.

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