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SiC-Based Unidirectional Solid-State Transformer Concepts for Directly Interfacing 400V DC to Medium-Voltage AC Distribution Systems

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SiC-Based Unidirectional Solid-State Transformer Concepts for Directly Interfacing 400V DC to Medium-Voltage AC Distribution Systems

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***Abstract*—400 V DC distribution networks present a promising solution for supplying high-power DC loads such as information processing systems, transportation battery charging facilities and DC micro grids, among others. For these applications, high transmission efficiency, reliability and controllability are mandatory. With the current technology, these loads are fed from PWM rectifiers which are connected to the three-phase Low-Voltage (LV) distribution grid (400 V AC in Europe). The LV grid itself is supplied via Low-Frequency Transformers (LFT) from the Medium-Voltage (MV) grid, providing galvanic isolation and the required voltage step down.**

This paper presents three unidirectional AC/DC SiC-based Solid-State Transformer (SST) topologies with direct connection to the MV grid, which avoid the utilization of the aforementioned LFT by integrating a Medium-Frequency (MF) conversion stage, thus increasing the efficiency and power density of this supply system. The SST topologies are compared by means of a chip area-based comparative evaluation. Finally, the most suited among the presented topologies is Pareto-optimized, achieving a total MV AC to 400 V DC efficiency of 98.3 %. It is shown that the optimized SST features 40 % less overall losses compared to state-of-the-art solutions.

I. Introduction

The increasing energy consumption of high-power DC loads demands for highly efficient and compact power supply units in order to save energy, space and costs. In this context, 400 V DC presents a standard voltage level in applications such as information processing systems [1], [2], battery charging facilities for public transportation within DC micro grids [3] and industry automation, where several motor inverters are frequently sharing a common DC-link. In some cases, this 400 V DC voltage may be further step down in order to generate an e.g. 48 V DC level, as is the case of telecom applications [4]. Due to the high required power level, typically the power supplies in these applications are connected to a three-phase MV grid through a three-phase LFT (cf. Fig. 1 (a)), which transforms the MV voltage down to e.g. 400 V or 480 V AC while providing galvanic isolation. From there, several three-phase PWM rectifiers supply a particular load or a common 400 V DC bus, depending on the specific application.

In order to avoid the bulky LFT and to potentially increase efficiency, a power supply comprising SST technology with direct connection to a 6.6 kV MV grid as shown in Fig. 1 (b) is proposed in this paper. The basic structure of the proposed system consists of three independent 50 kW single-phase SSTs feeding a common 400 V DC bus, in contrast to [2] where an MV power distribution architecture with MF isolation transformer for data centers with a

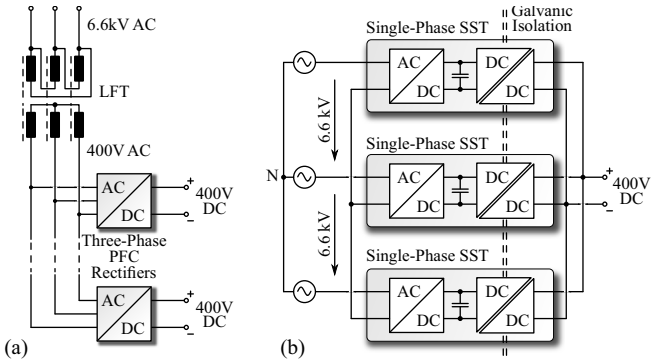


Fig. 1. State-of-the-art 400 V DC power supply with a Low-Frequency Transformer (LFT) and several three-phase PWM rectifiers (a); Proposed approach comprising three single-phase AC/DC SST units with direct connection to the 6.6 kV MV grid (b).

magnetically integrated MF AC-link has been described. Given the targeted power level, multiple of these single-phase SST units would be required in order to interface the three-phase MV grid.

As indicated in Fig. 1 (b), each of these single-phase AC/DC SSTs consists of a rectifier stage, an intermediate DC-link (in case a two-stage conversion strategy is adopted) and an isolated DC/DC stage. Given that the main targeted applications behave as a passive load, i.e. do not possess power regeneration capabilities, the considered SST structures in this paper are of the unidirectional type, allowing power to flow only from the MV AC grid to the 400 V DC bus and therefore reducing the complexity of the system. This unidirectional power transfer capability, however, maintains most of the key SST functionalities such as power-factor correction, available isolated DC-link and input/output side disturbance isolation.

In order to compare the proposed unidirectional SST topologies with respect to the state-of-the-art solution (cf. Fig. 1 (a)), the performance of LFTs and three-phase PWM rectifiers in the 1 MVA range (which is a typical power for the desired applications and corresponds to 20 of the presented single-phase units) is briefly shown in the following. For the three-phase rectifier, a full-load efficiency of $\eta_{\mathrm{REC}} = 98\,\%$ is assumed. This efficiency is based on datasheets of three-phase IGBT-based PWM inverters from [5] and [6], assuming that the efficiency of an equivalent rectifier is approximately the same as for these inverters. Concerning the LFT, an ultra-efficient 1 MVA dry-type transformer is considered [7], showing an efficiency

of $\eta_{\mathrm{LFT}} = 99.23\,\%$. The total state-of-the-art system would thus possess an efficiency of $\eta_{\mathrm{LFT\cdot REC}} = \eta_{\mathrm{LFT}} \cdot \eta_{\mathrm{REC}} = 97.25\,\%$, which will be compared with the selected and optimized unidirectional SST solution in the next sections.

The paper is structured as follows: Section II shows an overview of the considered SST concepts and describes the different topologies. In Section III, a chip area-based comparative evaluation of the SST topologies is presented in order to determine the most suitable topology for the desired application. In Section IV, this topology is Pareto-optimized considering efficiency and power density. Finally, a summary and a brief outlook is provided in Section V.

II. SST Topology Overview

Given that the AC side of the SST is directly connected to the 6.6 kV MV grid, the power electronic circuit must be rated for this rather high voltage level. i.e. either semiconductors with a blocking capability in the range of 10 kV or several series-connected converter cells with standard lower voltage semiconductors are required. From the various available SST structures proposed in literature [8], [9], the following single-phase SST topologies have been selected:

1) Five-Level AC/DC topology, cf. Fig. 2 (a_1).
2) Modular Multilevel Converter (MMLC) topology, cf. Fig. 2 (b_1).
3) Multi-Cell Boost (MCB) topology, cf. Fig. 2 (c_1).

In order to allow a consistent topology comparison, the MV side of the considered SSTs is based on 1.7 kV, 50 A SiC devices from Cree, namely the CPM2-1700-0040B SiC MOSFET ($R_{\mathrm{DS,on}} = 40\,\mathrm{m\Omega}$) and the CPW5-1700-Z050B SiC Schottky diode. The rectifier stages on the LV side of the transformer are diode rectifiers based on the CPW5-0650-Z050B SiC Schottky diode (650 V, 50 A) in order to reach a simple construction and therefore higher reliability. Since the considered SSTs are single-phase systems, it is necessary to filter the power fluctuation with two times mains frequency coming from the AC grid. The DC-link energy (and therefore the volume) is assumed to be equal for all topologies. Furthermore, the total DC-link voltage is fixed to $V_{\Sigma,\mathrm{DC}} = 7.5\,\mathrm{kV}$ and is distributed over eight semiconductors for all topologies, resulting in a blocking voltage of $7.5\,\mathrm{kV}/8 = 937.5\,\mathrm{V}$ per device. For the comparison of the topologies, the switching frequency f_{sw} of the MOSFETs and the transformer excitation frequency f_{TR} are set to $50\,\mathrm{kHz}$[1]. This way, the system specifications are defined as shown in Table I.

TABLE I
Specifications of the Unidirectional SST Topologies.

Parameter	Description	Value
V_{AC}	Phase-to-phase MV grid voltage	6.6 kV
V_{out}	DC output voltage	400 V
P_{SST}	Total system power	50 kW
$V_{\Sigma,\mathrm{DC}}$	Accumulated DC-link voltage	7.5 kV
V_{SiC}	SiC device blocking voltage	937.5 V
$\Delta V_{\mathrm{DC,rel}}$	Rel. DC-link voltage ripple	10 %
f_{TR}	Transformer excitation frequency	50 kHz
f_{sw}	MOSFET switching frequency	50 kHz

A. Five-Level AC/DC Topology

The five-level AC/DC topology which is shown in Fig. 2 (a_1) is based on the well-known multilevel Neutral Point Clamped (NPC) concept. It consists of an unidirectional five-level PWM rectifier stage, a 7.5 kV split DC-link and an independent isolated DC/DC converter. The special feature of this particular topology is that all switches and diodes on the MV side are based on MOSFET and diode strings as indicated in Fig. 2 (a_1). Although there are devices with higher voltage blocking capabilities available, this approach of series connection of 1.7 kV devices is chosen in order to consistently stay within the same semiconductor technology in all topologies for a comprehensive comparison in Section III. The rectifier stage is based on two three-level NPC bridge legs whereby the outer switches of each bridge leg are replaced by diodes, allowing only unidirectional power flow while reducing the complexity and the costs compared to bidirectional three-level bridge legs. The DC/DC stage consists of one three-level NPC bridge leg feeding a MF transformer which provides galvanic isolation and the desired voltage transfer ratio. Additionally, the DC/DC stage compensates the above mentioned low-frequency power fluctuation and controls the output voltage. Figs. 2 (a_2) and (a_3) show the generated AC voltage v_{AC} and current i_{AC} on the MV side and the transformer primary voltage v_{T} and current i_{T} for a DC/DC converter switching frequency of 50 kHz. The advantages of this topology are a low complexity, low control effort and the independence of the rectifier and the DC/DC stage.

B. MMLC Topology

The MMLC topology originally presented in [10] has received high attention for HVDC applications [11]–[13] and MV drive systems [14], [15] over the last years due to its modularity and scalability. A special type of the MMLC is the single-phase direct AC/AC converter [16] which is shown in Fig. 2 (b_1). This converter is able to generate two AC voltages with independent amplitudes and frequencies at its terminals A-B and C-D (cf. Fig. 2 (b_1)). The terminals A-B are connected to the MV grid via a filter inductor while terminals C-D feed an MF transformer which provides isolation and the required voltage transfer ratio. The secondary side of the transformer is connected to a diode rectifier with an output inductor. The voltages of the four converter arms are directly depending on the line and the transformer voltages:

$$v_{\mathrm{a1}} = v_{\mathrm{a4}} = \frac{v_{\mathrm{AC}} + v_{\mathrm{T}}}{2} \tag{1}$$

$$v_{\mathrm{a2}} = v_{\mathrm{a3}} = \frac{v_{\mathrm{AC}} - v_{\mathrm{T}}}{2}. \tag{2}$$

As the frequencies of v_{AC} and v_{T} are different, each converter arm must be able to generate peak voltages of $\pm|\hat{v}_{\mathrm{AC}} + \hat{v}_{\mathrm{T}}|/2$ which results in three important considerations:

1) According to the value for the DC-link voltage $V_{\Sigma,\mathrm{DC}}$ from Table I, each converter arm's accumulated DC-link voltage is fixed to 7.5 kV for $|\hat{v}_{\mathrm{AC}}| \leq 7.5\,\mathrm{kV}$ and $|\hat{v}_{\mathrm{T}}| \leq 7.5\,\mathrm{kV}$;
2) The submodules must be able to generate positive and negative voltages and thus consist of full-bridges;
3) According to the SiC device blocking voltage V_{SiC} from Table I, each converter arm consists of $N = 8$ submodules.

[1]This switching frequency constraint will be relaxed once the evaluation of the optimum switching frequency is studied in Section IV.

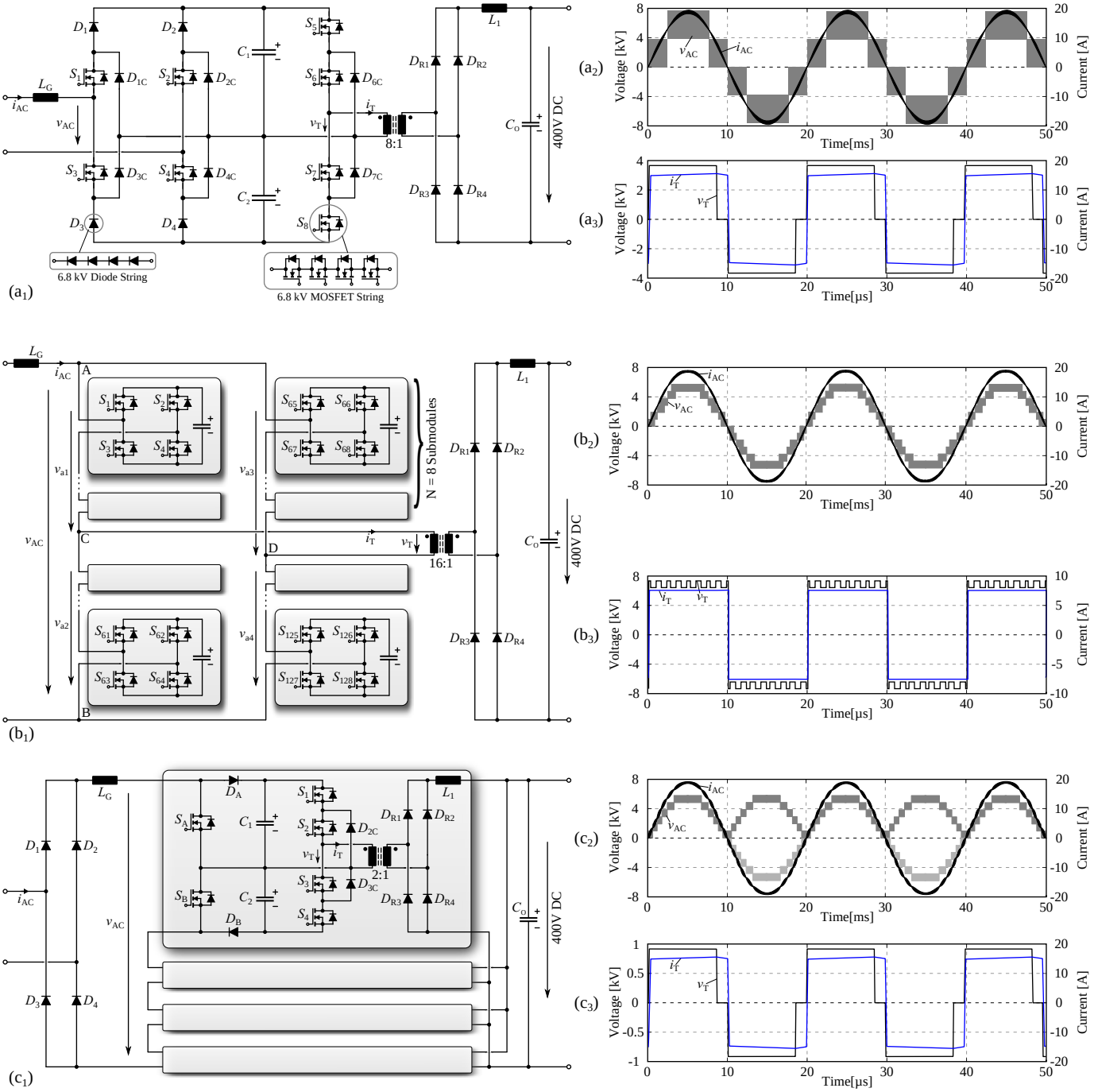


Fig. 2. (a_1) Five-level AC/DC topology with its AC input voltage and current waveforms (a_2), as well as its transformer primary voltage and primary current (a_3); (b_1) AC/AC MMLC with transformer and secondary side rectifier. (b_2) shows the generated input AC voltage and current waveforms and (b_3) the transformer primary voltage and primary current; (c_1) MCB Topology with four Input Series Output Parallel (ISOP)-connected converter stages; (c_2) shows the generated AC voltage and current waveforms and (c_3) the transformer primary voltage and primary current.

The submodule capacitors have to be designed such that the 2^{nd} harmonic power pulsation from the AC grid can be filtered, allowing a total DC-link voltage ripple of $10\,\%$. As the power pulsation is not depending on the converter topology, the total DC-link energy and volume will be approximately the same as for other topologies [16]. In addition, the controller has to ensure balanced submodule voltages which implies that each submodule requires a measurement and control of its DC-link voltage [17].

The gate signals for the individual MOSFETs are generated by means of phase-shifted PWM whereby the triangular carrier signals of the submodules in one converter arm are shifted by $360^\circ / (2N) = 22.5^\circ$ with respect to each other in order to achieve $2N+1$ modulation as described in [18]. Fig. 2 (b_2) shows the generated AC grid voltage v_{AC} and the current i_{AC} for nominal operation. The voltage waveform shows 13 levels for a modulation index of $m_1 = 0.85\%$ resulting in nominal transferred power, whereby the considered MMLC topology is able to generate a maximum of $2N + 1 = 17$ levels for a unity modulation index.

For the transformer excitation, a rectangular voltage waveform was chosen in order to achieve a high utilization of the transformer. Fig. 2 (b_3) shows the transformer primary voltage v_{T} and current i_{T} for an excitation frequency of $50\,\mathrm{kHz}$. While the transformer current is impressed by the output inductor L_1, the transformer voltage is formed out of the available voltage levels as can be seen in the figure. The controller must ensure equal positive and negative volts-time areas at the transformer's terminals in order to avoid magnetic saturation of the transformer core. The control of the output voltage is achieved by varying the amplitude of the transformer primary voltage.

As both, the transformer excitation frequency f_{TR} and the switching frequency f_{sw} have been fixed to $50\,\mathrm{kHz}$ for a consistent comparison with the other topologies, the required PWM carrier frequency f_{carrier} has to be calculated. Furthermore, for the calculation of the required AC line inductance, the achieved MV AC PWM frequency $f_{\mathrm{PWM,AC}}$ is derived in the following. The frequency of the output voltage of a single submodule is given by

$$f_{\mathrm{submodule}} = 2 \cdot f_{\mathrm{carrier}} + m \cdot f_{\mathrm{TR}} \tag{3}$$

where $m = |\hat{v}_{\mathrm{T}}|/V_{\Sigma,\mathrm{DC}}$ is the modulation index of the transformer voltage which is set to $m = 0.85$. The average switching frequency of the MOSFETs (fixed to $f_{\mathrm{sw}} = 50\,\mathrm{kHz}$) is given by [16]

$$f_{\mathrm{sw,MMLC-FET}} := f_{\mathrm{sw}} = f_{\mathrm{submodule}}/2. \tag{4}$$

Inserting equation (4) in (3) yields

$$f_{\mathrm{carrier}} = \frac{2f_{\mathrm{sw}} - m \cdot f_{\mathrm{TR}}}{2}. \tag{5}$$

For $f_{\mathrm{sw}} = f_{\mathrm{TR}} = 50\,\mathrm{kHz}$ and $m = 0.85$, the required carrier frequency is $f_{\mathrm{carrier}} = 28.75\,\mathrm{kHz}$ (additional switching cycles due to voltage balancing have been neglected). The effective PWM frequency at the MV AC terminals is given by $f_{\mathrm{PWM,AC}} = 2N \cdot f_{\mathrm{carrier}} = 460\,\mathrm{kHz}$.

C. MCB Topology

The MCB topology proposed in [9] is shown in Fig. 2 (c_1) and consists of a modular approach with a lower number of switches compared to the previously presented topologies. The AC grid is interfaced by a full-bridge diode rectifier followed by a common boost-inductor and four Input-Series Output-Parallel (ISOP)-connected converter modules. Each converter module consists of a three-level boost PFC rectifier stage, a split DC-link and a three-level NPC bridge-based isolated DC/DC stage which provides galvanic isolation and the required voltage step down. Since each of the three-level PFC rectifier stages has one redundant switching state, the split DC-link can easily be balanced if necessary, whereby ISOP converters are usually self-balancing [19], [20].

An important feature of this topology (regarding Fig. 2 (c_1)) is its modularity in both, power flow and MV side voltage direction [8]. By adjusting the number of cells, the system could be adapted to AC line voltages higher than the here specified $6.6\,\mathrm{kV}$. On the other hand, this topology can be split into three independent parts in the power flow direction, namely:

1) the input diode rectifier stage,
2) the boost PFC rectifier stage, and
3) the DC/DC stage,

all acting independently from each other and thus offering high design flexibility.

Since the input rectifier diodes $D_1 ... D_4$ (cf. Fig. 2 (c_1)) are operated at line frequency, SiC diodes (which are typically designed for fast switching) would no represent the optimum choice, given that a series connection of at least five of the $1.7\,\mathrm{kV}$, $50\,\mathrm{A}$ SiC diodes would be necessary in order to block the input voltage and would therefore show a considerably high forward voltage drop. In order to increase efficiency, the aforementioned flexibility is exploited by using low forward voltage drop silicon line frequency diodes for the input rectifier stage. In this case, the $D471N$ ($8.5\,\mathrm{kV}$, $565\,\mathrm{A}$) from Eupec was selected. It should be noted that the current rating of the selected diode is considerably higher than actually required for the desired power of the analyzed MCB topology. However, the current ratings of available low forward voltage drop diodes with blocking capabilities in the 8...10 kV range are typically higher than $500\,\mathrm{A}$ since their targeted applications (such as MV drive systems) are usually aimed for the MVA power range. For a more efficient utilization of the selected rectifier diodes, one of these bridge rectifiers could feed a whole SST group which is connected to one phase. For this reason in the following calculations, which deal with only one single-phase unit, the $8.5\,\mathrm{kV}$, $565\,\mathrm{A}$ diode has been scaled down to a $50\,\mathrm{A}$ version in order to be consistent with the $50\,\mathrm{A}$ SiC diode. The chip area scaling process is discussed separately in Section III-C.

In the PFC rectifier stage, it is important to note that the switching patterns of the $N_{\mathrm{PFC}} = 8$ PFC rectifier MOSFETs of the boost stages are all phase-shifted by $360^\circ / (N_{\mathrm{PFC}}) = 45^\circ$ with respect to each other. This effectively increases the frequency of the voltage waveform which is applied to the boost inductor L_{G} by a factor of N_{PFC}. Furthermore, the voltage steps which are applied to the inductor are decreased by a factor of N_{PFC} as well. As a result, the interleaving of the PFC rectifier MOSFET switching patterns reduces the required boost inductance by a factor of $N_{\mathrm{PFC}}^2 = 64$ for the

same maximum input current ripple compared to the non-interleaved modulation [21], or alternatively, the switching frequency can be reduced while keeping the inductance value constant. Finding the optimum trade-off between switching frequency and line inductor volume will be part of the optimization in Section IV.

Fig. 2 (c_2) shows the generated (rectified) line voltage v_{AC} and the line current i_{AC} for nominal operation. As can be seen, the voltage waveform shows 13 levels. For a fully utilized modulation index, the MCB topology is able to generate $2N_{\mathrm{PFC}} + 1 = 17$ voltage levels.

The topology of the DC/DC stage is the same as in the five-level AC/DC topology with the difference that the DC-link voltage of each cell is $V_{\Sigma,\mathrm{DC}}/4 = 1875\,\mathrm{V}$ and the switches are realized with single CPM2-1700-0040B devices. As the DC/DC stages are independent of the PFC rectifier stage, the switching patterns of the four DC/DC stages are also phase shifted (in this case by $90°$) in order to reduce the output capacitor's current ripple, achieving a lower capacitance value.

III. Chip Area-Based Comparative Evaluation of the SST Topologies

In this section, the SST topologies are compared to each other concerning required chip area, semiconductor losses as well as input inductor and transformer volume.

A. Component Load Factors

In a first step, the Component Load Factors (CLFs), namely the relative VA-rating and the relative RMS-rating of the semiconductors in the three SST topologies are calculated in order to compare the chip areas which the different topologies require. According to [22], the relative MOSFET and diode RMS ratings are defined as

$$\tau_{\mathrm{FET}} = \sum_{\mathrm{i}=1}^{n_{\mathrm{FET}}} \frac{I_{\mathrm{FET,rms,i}}}{I_0} \tag{6}$$

and

$$\tau_{\mathrm{D}} = \sum_{\mathrm{i}=1}^{n_{\mathrm{D}}} \frac{I_{\mathrm{D,rms,i}}}{I_0} \tag{7}$$

and are a measure for the conduction losses and for the required chip area. Thereby, n_{FET} and n_{D} denominate the total number of MOSFETs and diodes in the considered topology. $I_{\mathrm{FET,rms,i}}$ and $I_{\mathrm{D,rms,i}}$ describe the RMS current stresses of the i_{th} MOSFET and the i_{th} diode respectively. The average DC current $I_0 = P_{\mathrm{SST}}/V_{\Sigma,\mathrm{DC}} = 6.66\,\mathrm{A}$ is used as a reference which is common for all topologies.

The second considered CLF is the relative VA-rating which is defined as

$$\mu_{\mathrm{FET}} = \sum_{\mathrm{i}=1}^{n_{\mathrm{D}}} \frac{u_{\mathrm{FET,max,i}} \cdot i_{\mathrm{FET,max,i}}}{P_{\mathrm{SST}}} \tag{8}$$

and

$$\mu_{\mathrm{D}} = \sum_{\mathrm{i}=1}^{n_{\mathrm{D}}} \frac{u_{\mathrm{D,max,i}} \cdot i_{\mathrm{D,max,i}}}{P_{\mathrm{SST}}} \tag{9}$$

for MOSFETs and diodes, respectively [22]. The relative VA-rating is the total required (not installed) MOSFET/diode switching capacity in relation to the total system power. Table II shows the relative RMS and the relative VA ratings of the MOSFETs and diodes for the three SST topologies. As can be seen, the MMLC topology shows considerably uneven MOSFET and diode ratings given that the MV side of the MMLC consists of 128 SiC MOSFETs whereas the diode ratings are only resulting from the output rectifier. On the other hand, the MCB topology shows the lowest ratings in total due to its low number of semiconductors.

TABLE II
Relative RMS-Ratings (τ_{FET}, τ_{D}) and Relative VA-Ratings (μ_{FET} and μ_{D}) of the Considered SST Topologies.

Parameter	Five-Level	MMLC	MCB
τ_{FET} (RMS)	47.35	99.75	34.94
τ_{D} (RMS)	47.26	11.26	33.85
μ_{FET} (VA)	10.23	30.3	7.48
μ_{D} (VA)	18.14	4.7	17.82

The CLFs from Table II indicate a first trend towards which SST topology would show the lowest construction effort. However, the CLFs do not give enough information about the actual losses and the required chip area. Additionally, as the three topologies are all based on the same SiC devices, the current load capability of the MOSFETs would be utilized differently in the three topologies, increasing the complexity of the comparative evaluation.

In order to compare the topologies consistently, the chip areas of all semiconductors in the three topologies are individually scaled in the next step such that the maximum junction temperature of each chip reaches 125 °C. Therefore, the semiconductor losses as well as the characteristics of the thermal circuit from the chip to the ambient have to be modeled. For the devices which process the pulsating power of the single-phase AC input, the time dependency of their instantaneous losses, which lead to time dependent junction temperatures, has to be considered.

B. Modeling Approach

The utilized loss models of the semiconductors are based on the device datasheets and include conduction losses and switching losses. The thermal properties of the devices are considered in a transient thermal model.

1) Conduction Losses: The conduction losses of the semiconductors are calculated via the forward characteristic curves (in case of diodes) and the on-state resistance (in case of MOSFETs) from the device datasheets. As the conduction losses depend on the junction temperature of the device, which is not known in advance, an iterative method is used to calculate the correct temperature-dependent conduction losses. This is done by feeding the total (conduction and switching) losses into a (chip area dependent) thermal model, calculating the actual junction temperature, selecting the new operating point out of the forward characteristics and iterating until a defined temperature tolerance has been reached.

2) Switching Losses: The switching losses of the semiconductors are calculated via the effective charge- and energy-equivalent capacitances (in order to include the nonlinearity of the capacitances) of the switching MOSFET and its complementary devices (MOSFETs or diodes) according to [23]. The required charge- and energy-equivalent capacitances have been calculated based on the capacitance

curves given in the device datasheets. Zero Voltage Switching (ZVS) transitions are considered to cause negligible switching losses [24].

3) Thermal Model: As a basis for the thermal model, the ambient temperature is assumed to be $T_{\mathrm{A}} = 40\,^{\circ}\mathrm{C}$. Furthermore, it is assumed that the semiconductors are mounted on a heat sink with a constant temperature of $T_{\mathrm{HS}} = 80\,^{\circ}\mathrm{C}$. Between the heat sink and the semiconductor case (TO-247), an insulation pad with a thermal resistance of $R_{\mathrm{th,pad}} = 1\,\mathrm{K/W}$ is assumed. The thermal characteristics of the semiconductors are based on datasheet information. In order to enable the calculation of the time-dependent junction temperature of the devices that are stressed with the fluctuation resulting from the single-phase AC input, the transient thermal junction-to-case impedance $G(t)$ (which is effectively a thermal step response to a power loss step) has been extracted from the datasheets. From this, the thermal impulse response $G'(t)$ has been calculated by differentiating the transient thermal impedance,

$$G'(t) = \frac{\partial}{\partial t} G(t). \tag{10}$$

The time dependent junction temperature can then be obtained by convoluting the instantaneous losses $P_{\mathrm{loss}}(t)$ with the thermal impulse response

$$T_{\mathrm{j}}(t) = P_{\mathrm{loss}}(t) \star G'(t). \tag{11}$$

C. Chip Area Scaling

The scaling of the chip area has a direct impact on the conduction losses, the switching losses and the thermal properties of the devices. The relation between these properties and the chip area is explained for MOSFETs and diodes in the following:

- Conduction Losses:
  - For MOSFETs, the on-state-resistance is scaled inversely proportional with respect to the chip area: $R_{\mathrm{DS,scaled}} = R_{\mathrm{DS0}} \cdot A_0/A$ such that the conduction losses increase proportionally with decreasing chip area.
  - For diodes, the threshold voltage is kept constant while the slope of the forward characteristic (the differential conductance) is scaled proportionally to the chip area.
- Switching Losses:
  - As the switching losses of the devices on PFC rectifier side depend on the device capacitances, the charge- and energy-equivalent capacitances of both, MOSFET and diode chips, are scaled proportionally with the chip area. A decreased chip area leads thus to proportionally decreased capacitive switching losses. In the converters with a dedicated DC-DC converter stage, the switches are operated under ZVS[2] and therefore, assuming the capacitance remains always high enough in order to reach soft-switching transitions, negligible switching losses are assumed.
- Thermal Properties
  - When the chip area is scaled, the effective surface area of the thermal interfaces from junction to case and from case to the heat sink are also scaled, leading to linearly increased thermal resistances (including the transient thermal impedance) with decreasing chip area and therefore a thermally-limited load current capability of the devices.

As a consequence, a chip with a decreased area causes proportionally higher conduction losses and proportionally lower switching losses whereby it can dissipate proportionally less power as a result of the thermal restrictions.

Due to these rather complex inter-relations, the chip area scaling (with the aim of always fully reaching the chip's thermal limit in order to perform a consistent topology comparison) is done iteratively. The first iteration is performed with the original chip area and therefore also the original forward and thermal characteristics as well as an initial junction temperature which is set equal to the heat sink temperature of $80\,^{\circ}\mathrm{C}$. The chip area is then scaled stepwise whereby the resulting junction temperature is calculated in each step until its maximum value reaches $125\,^{\circ}\mathrm{C}$.

D. Comparative Evaluation

For a more detailed comparison of the three topologies and in order to also give an impression about the system costs, the relative chip price $\zeta_{\mathrm{chip}} = \zeta_{\mathrm{x,tot}}/\zeta_{\mathrm{MMLC,tot}}$ of the chip area-scaled semiconductors has been calculated with the help of information provided by the manufacturers. Thereby, the total chip price $\zeta_{\mathrm{MMLC,tot}}$ of the chip area-scaled MMLC is used as a reference. $\zeta_{\mathrm{x,tot}}$ depicts the total chip price of the considered chip area-scaled topology (x = five-level, MCB, MMLC).

Additionally, the required heat sink volume V_{HS} for the chip area scaled topologies as well as the transformer and the AC line inductor volumes V_{TR} and $V_{\mathrm{L,AC}}$ have been calculated. The heat sink volume is computed using a Cooling System Performance Index of $CSPI = 10\,\mathrm{W/Kdm^3}$ according to [25]. The resulting heat sink volume is

$$V_{\mathrm{HS}} = \frac{P_{\mathrm{S,tot}}}{(T_{\mathrm{A}} - T_{\mathrm{HS}}) \cdot CSPI}, \tag{12}$$

where $P_{\mathrm{S,tot}}$ stands for the total semiconductor losses.

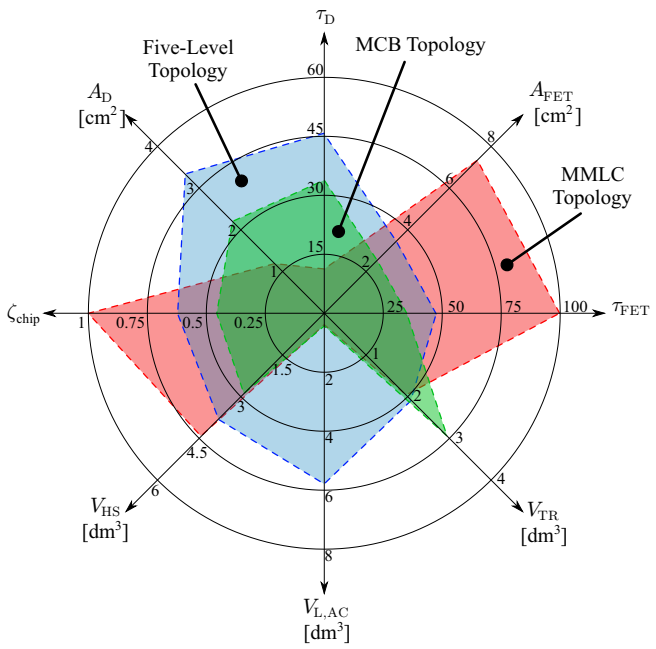
The calculation of the AC line inductor volume is based on the applied voltage-time area and a maximum allowed peak-to-peak input current ripple of $\Delta i_{\mathrm{AC}} = 10\,\%$. For each topology, an optimized input inductor has been designed with the method described in Section IV. The transformer volumes have also been calculated with the same method using a transformer excitation frequency of $f_{\mathrm{TR}} = 50\,\mathrm{kHz}$ for all three topologies. Table III gives an overview of the effective PWM frequencies at the MV terminals of the three topologies as well as the number of voltage levels, the required input inductance L_{G} for $\Delta i_{\mathrm{AC}} = 10\,\%$ and the input inductor volume $V_{\mathrm{L,AC}}$.

TABLE III
AC TERMINAL PWM FREQUENCY AS WELL AS INPUT INDUCTOR VOLUME AND INDUCTANCE.

SST	$f_{\mathrm{PWM,AC}}$	Levels	Inductance L_{G}	$V_{\mathrm{L,AC}}$
Five-Level	100 kHz	5	5.1 mH	5.80 dm^3
MMLC	460 kHz	17	275 µH	0.33 dm^3
MCB	400 kHz	17	316 µH	0.37 dm^3

Finally, Fig. 3 shows the described results of the comparative

[2]With the exception of the inner switches of the NPC-based DC-DC converters in Fig. 2 which are operated under reduced voltage switching [24].



τ_{FET}	Tot. MOSFET rel. RMS rating	ζ_{chip}	Rel. chip costs (total SST)
A_{FET}	Tot. MOSFET chip area	V_{HS}	Tot. heat sink volume
τ_D	Tot. Diode rel. RMS rating	$V_{L,AC}$	Line inductor volume
A_D	Tot. Diode chip area	V_{TR}	Tot. transformer volume

Fig. 3. Comparative evaluation of the different 50 kW SST topologies. The total area of one topology polygon is a measure for its performance: The smaller the area, the higher the performance. The figure shows that the MCB topology achieves the highest overall performance while it also exhibits the lowest chip areas and/or semiconductor costs among the topologies.

evaluation of the different SST topologies. It considers the relative RMS-ratings τ_{FET} and τ_D, the total MOSFET and diode chip area A_{FET} and A_D, the relative chip prices ζ_{chip}, the heat sink volume V_{HS} as well as the AC line inductor and the transformer volumes $V_{L,AC}$ and V_{TR}. It is visible that the MCB topology shows the best overall performance among the considered topologies. Its efficiency is the highest (as the smallest heat sink volume indicates) and the MCB topology would also be the lowest cost solution. The five-level topology suffers especially from its large input inductor whereas the MMLC is the most expensive option (gate drivers and auxiliary circuitry not considered) and shows the lowest efficiency.

Regarding the transformer volumes V_{TR} in Fig. 3, the transformers of the MMLC and the five-level AC/DC topology feature virtually equal volume whereas the total volume of the four MCB transformers is 40 % higher due to the transformer scaling laws and the same primary/secondary isolation layer thickness occupying a higher share of the winding window in a smaller transformer construction.

Comparing the relative RMS ratings τ_{FET} and τ_D to the required chip areas A_{FET} and A_D (which have been calculated with the chip area scaling approach), a good conformity can be recognized. This means that the relatively simple CLF analysis is a fast method for an initial topology comparison whereas the rather complex chip area scaling analysis provides absolute numbers for the required chip areas and considers further details such as switching losses and a transient thermal model of the semiconductors.

IV. MCB Topology Optimization

Based on the previous comparative evaluation, the MCB topology represents the best suited option among the considered unidirectional SST topologies. In order to explore its maximum performance, this topology is optimized considering power density and efficiency in the following. Thereby, the optimization is based on the real existing semiconductors instead of the chip area-scaled versions in order to obtain a design with real implementation potential, with the exception of the line frequency bridge rectifier diodes $D_1 \dots D_4$ in Fig. 2 (c_1) which are considered as a 50 A down-scaled version for the aforementioned reasons (cf. Section II-C). Additionally, the switching frequencies of the PFC rectifier stage ($f_{sw,PFC}$) and the DC/DC stage ($f_{sw,DCDC}$) will be free parameters throughout the optimization.

Due to the independence of the boost converter stage of the PFC rectifier and the DC/DC converter stage provided by the intermediate DC-link, the optimization is realized in two steps:

1) Optimization of the boost stage with $f_{sw,PFC}$, the line inductor current ripple Δi_{AC} and the particular design of the line inductor (cf. Section IV-A) as degrees of freedom;
2) Optimization of the DC/DC stage with $f_{sw,DCDC}$, the output inductor current ripple ΔI_{out} and the particular designs of the transformer and the output inductor as degrees of freedom.

A. Optimization of the Magnetic Components

The aforementioned magnetic components are optimized with the approach given in [26]. With this method, a magnetic and thermal model of the inductor and transformer is implemented. The components are based on available ferrite E-cores (with $N87$ core material) and the high-frequency losses in the conductors are considered as well as the non-sinusoidal excitation for the calculation of core losses. As input parameters, the core geometry, material, the maximum number of stacked cores, the considered frequency range and the desired conductor diameter and Litz-wire strand diameter range are considered. All these parameters are combined with each other, resulting in a large design space for the multi-objective optimization. For all possibilities, the volume and the losses (among other parameters such as the optimal number of Litz-wire strands and the costs of the magnetic component) are calculated. Thereby, a maximum core and winding temperature of 125 °C has been allowed.

B. PFC Rectifier Stage Optimization

For the optimization of the boost stage, a design space consisting of a PFC rectifier switching frequency range of $f_{sw,PFC} = 3...100$ kHz and a peak-to-peak input current ripple range of $\Delta i_{AC} = 5...25$ % has been generated. For each input inductor design (which is related to a specific switching frequency), the corresponding conduction and switching losses of the SiC devices and the required heat sink volume have been calculated, leading to overall losses and volume of the PFC rectifier stage. The DC-link volume has been calculated based on foil capacitors with an assumed constant energy density of 153 J/dm^3 (as given for this capacitor technology in the required voltage range [27]) and a maximum voltage ripple of $\Delta V_{DC,rel} = 10$ %. For the total volume of the PFC rectifier stage (and the DC/DC converter

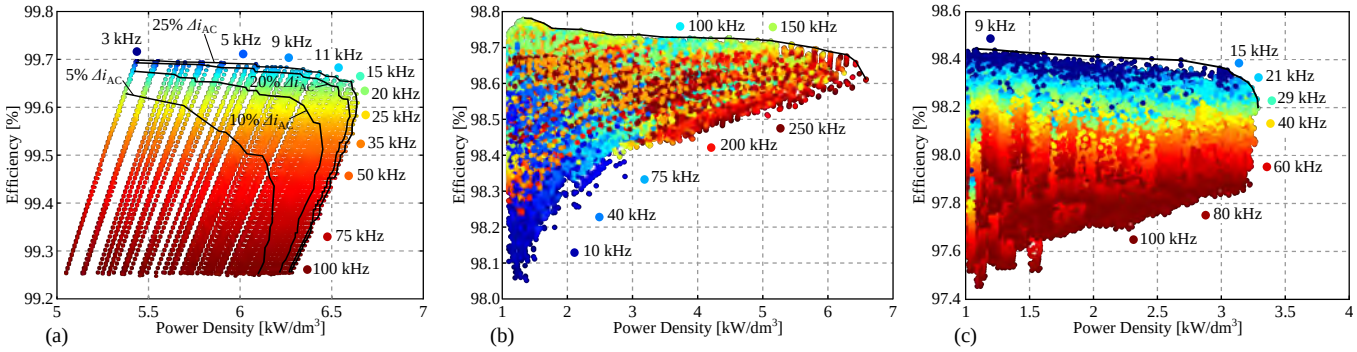


Fig. 4. $\eta - \rho$ Pareto optimization of (a) the boost stage of the PFC rectifier with color-coded switching frequency, (b) the DC/DC converter stage with color-coded DC/DC converter switching frequency and (c) the total system with color-coded boost stage switching frequency. The volume utilization factor k_{VOL} is already included in these $\eta - \rho$ planes.

stage as well), a volume utilization factor $k_{\mathrm{VOL}} = 0.75$ has been assumed in order to consider empty spaces in the practical assembly. The total volume of the system is thus

$$V_{\mathrm{tot}} = \frac{1}{k_{\mathrm{VOL}}} \cdot \sum_{\mathrm{i}=1}^{n} V_{\mathrm{component,i}}. \tag{13}$$

Fig. 4 (a) shows the Efficiency-Power Density ($\eta - \rho$) performance plane of the PFC rectifier stage (including the input rectifier stage $D_1 \ldots D_4$) and the Pareto-fronts for different input current ripples. The color indicates the switching frequency $f_{\mathrm{sw,PFC}}$ of the PFC rectifier stage. The figure shows that the efficiency is strongly depending on the switching frequency which is a result of the capacitive switching losses of the boost converters which are not operated under soft-switching conditions. Furthermore, it is visible that the demand for a small input current ripple reduces both, power density and efficiency. In order to reduce the MV side EMI filter requirements (which have been neglected in this analysis), only designs with an input peak-to-peak current ripple of $\Delta i_{\mathrm{AC}} = 10\,\%$ are considered for the further optimization. Under this constraint, the PFC rectifier stage reaches a maximum power density of $6.3\,\mathrm{kW/dm^3}$ at an efficiency of $99.6\,\%$ for a boost stage switching frequency of $25\,\mathrm{kHz}$.

C. DC/DC Converter Optimization

In a second step, the DC/DC converter has been optimized. Therefore, a switching frequency range of $f_{\mathrm{sw,DCDC}} = 10...250\,\mathrm{kHz}$ and a peak-to-peak output current ripple range of $\Delta I_{\mathrm{out}} = 1...20\,\%$ has been specified. Based on this, a large number of transformer and output inductor designs has been generated. Each combination of a transformer and output inductor (which have been designed for the same switching frequency) leads to one DC/DC converter design. For each design, the switching losses and the conduction losses of the SiC semiconductors have been calculated.

Fig. 4 (b) shows the $\eta - \rho$ performance plane for the DC/DC converter. The color indicates the switching frequency of the DC/DC converter stage. The figure shows that there is no pronounced dependency of the switching frequency on the efficiency and the power density but rather a tendency which indicates that designs with a low switching frequency show a lower efficiency and large volume whereas designs with a switching frequency of $150...250\,\mathrm{kHz}$ show the highest performance. This can be explained by the low switching losses of the MOSFETs due to ZVS and reduced voltage switching as explained in [24]. An efficiency of $98.6\,\%$ is reached at the maximum power density of $6.6\,\mathrm{kW/dm^3}$.

D. Total System Optimization

In order to obtain the overall $\eta - \rho$ performance limit, i.e. Pareto front, of the complete MCB topology, each PFC rectifier design has been combined with each DC/DC converter design. Fig. 4 (c) shows the $\eta - \rho$ Pareto front of the complete MCB topology. In this case the color indicates the PFC rectifier switching frequency $f_{\mathrm{sw,PFC}}$. The designs in the upper right corner of the Pareto front indicates efficiencies of $98.3\,\%$ at power densities of $3.2\,\mathrm{kW/dm^3}$ for the total system (including the volume utilization factor k_{VOL}).

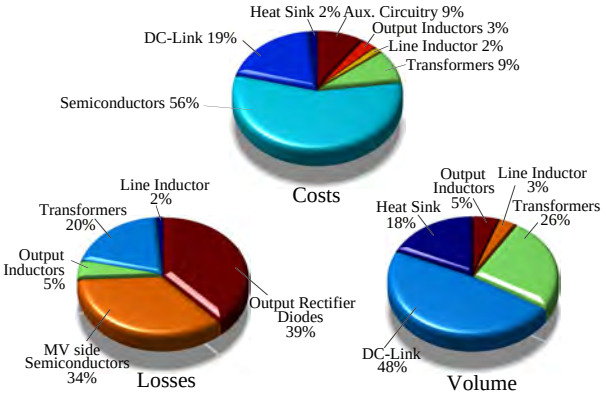


Fig. 5. Loss, volume and cost breakdown of the optimized MCB topology.

Comparing the power density and efficiency of the optimized SST to the state-of-the-art approach with an LFT and a three-phase PWM rectifier, the SST shows a ca. $1\,\%$ higher efficiency, as indicated in Table IV. Furthermore, a significant volume and weight reduction is expected due to the saving of the LFT.

In addition to the results in Fig. 4, Fig. 5 shows the breakdown of the system costs (which have been estimated according to [27]), the losses and the volume for the optimum design. It can be seen that the semiconductors (MV side devices and output rectifiers) are responsible for more than half of the costs and more than two thirds

TABLE IV
EFFICIENCY COMPARISON OF THE PROPOSED SST AND THE STATE-OF-THE-ART APPROACH.

System	Efficiency	Relative Losses
LFT and three-phase rectifier	97.25 %	100 %
SST	98.3 %	62 %

of the losses whereby the output diode rectifier has a considerably high impact. These losses could be reduced by applying synchronous rectification. Concerning volume, the DC-link accounts for half of the total volume due to the low-frequency input power pulsation from the single-phase MV AC connection.

V. CONCLUSION/OUTLOOK

In this paper, three different unidirectional SST topologies with direct connection to the MV AC grid and 400 V DC output are analyzed and compared regarding efficiency, power density and costs by means of a chip area-based comparative evaluation. The MCB topology which shows the best performance among the considered topologies has been optimized and exhibits highly attractive power density and efficiency figures for future 400 V DC distribution systems. Moreover, the modular structure of the MCB topology offers high reliability due to the low total number of switches and the ability to operate with redundant cells.

Compared to the state-of-the-art approach with LFT and three-phase PWM rectifiers, the AC/DC SST achieves 40 % lower losses while also providing full galvanic isolation and the characteristic increased functionalities provided in general by AC/DC SST technology. As a consequence, unidirectional SST structures are a promising solution for supplying high-power DC loads directly from the MV AC grid.

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