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***Abstract*— Battery chargers supplied from the three-phase mains are typically realized as two-stage systems consisting of a three-phase PFC boost-type rectifier with an output DC link capacitor followed by a DC/DC buck converter if boost and buck functionality is required. In this paper, a new modulation scheme for this topology is presented, where always only one out of three rectifier half-bridges is pulse width modulated, while the remaining two phases are clamped and therefore a higher efficiency is achieved. This modulation concept with a minimum number of active half-bridges, denoted as *1/3 rectifier*, becomes possible if in contrast to other modulation schemes the intermediate DC link voltage is varied in a six-pulse voltage fashion, while still sinusoidal grid currents in phase with their corresponding phase voltages and a constant battery output voltage are obtained. In this paper, a detailed description of the novel 1/3 rectifier's operating principle and the corresponding control structure are presented and the proper closed loop operation is verified by means of a circuit simulation. Finally, the performance gain of the 1/3 rectifier control scheme compared to conventional modulation schemes is evaluated by means of a virtual prototype system.**

I. Introduction

In order to allow a further proliferation of electric vehicles (EV), a widely distributed battery charging infrastructure is crucial [1]. Applications with power levels above several kW are typically powered by three-phase PFC rectifiers [2], which in certain cases allow for a bidirectional power flow and therefore also feature the option of using the EV batteries as a grid energy storage and consequently improve the grid stability by feeding power back to the mains [3]. Due to the wide variation of EV battery voltages, charging stations have to cover a wide range in DC output voltage U_o and according to the recently published *China Grid 2017 Electric Vehicle Charging Equipment Supplier Qualification Verification Standard* nominal output power has to be provided for a DC voltage range of $750\,\mathrm{V}$ down to $400\,\mathrm{V}$, which overlaps with the Chinese grid peak line-to-line voltage $\hat{U}_\mathrm{ll} = \sqrt{3}\cdot\sqrt{2}\cdot 220\,\mathrm{V} \simeq 540\,\mathrm{V}$ and therefore a charger with boost and buck functionality [4] is needed (cf. **Fig. 1(a)**). A prominent solution to comply with these specifications is to use a two-stage converter system consisting of a three-phase boost-type PFC rectifier followed by a DC/DC buck converter [5], [6] shown in **Fig. 1(b)**. There, the control of the two converter stages is typically decoupled, which means that the three-phase boost PFC rectifier draws sinusoidal grid currents i_a, i_b, i_c in phase with their respective phase voltages u_a, u_b, u_c while at the intermediate DC link capacitor C_pn a constant voltage u_pn, which has to be larger than $\hat{U}_\mathrm{ll}$, is generated [7]. This voltage u_pn is then stepped down to the required output and/or battery voltage U_o by the subsequent DC/DC converter with features an independent control structure. For battery chargers, especially in mobile applications, typically a compact and lightweight system realization is demanded. Therefore, high switching frequencies are required in order to downsize the passive components, which due to the increased switching losses on the other hand also reduce the converter efficiency. Therefore, for three-phase PFC rectifiers (as well as inverter systems) third harmonic injection techniques [8] or space vector modulation [9] are employed to reduce the component stresses and better utilize the DC link voltage. Advanced modulation techniques to reduce the switching losses have been introduced, e.g. Discontinuous Pulse Width Modulation (DPWM) where only two rectifier half-bridges are switched at a time and the remaining half-bridge connected to either the most positive ($\mathrm{DPWM}_\mathrm{max}$) or most negative ($\mathrm{DPWM}_\mathrm{min}$) [10], or the maximum absolute mains phase voltage (DPWM1 [11]) is clamped, thus reducing the switching losses by more than one third compared to normal PWM operation, while still sinusoidal input currents and a constant DC link voltage can be achieved. In single-stage converter systems clearly both requirements, i.e. sinusoidal input currents and constant DC link voltage have to be fulfilled. In two-stage systems as shown in **Fig. 1(b)**, however, there is no need to provide a constant intermediate DC link voltage u_pn to the subsequent DC/DC converter, since any low-frequency voltage fluctuation at C_pn can be compensated by the DC/DC converter, such that still a constant output voltage U_o is present at the battery terminals.

The novel modulation scheme proposed in this paper, actually uses this degree of freedom of a variable intermediate DC link voltage in such a way that only one rectifier half-bridge has to be switched and the other two half-bridges are clamped to either the positive (p) or negative (n) DC link voltage rail, accordingly the system is denominated as *1/3 rectifier*. Hence, the number of active half-bridges is reduced to a minimum, resulting in even lower overall switching losses than DPWM while still sinusoidal input currents and a constant output voltage U_o are obtained. In **Section II**, the proposed modulation scheme and the characteristic waveforms of the 1/3 rectifier are described. Afterwards, a cascaded control structure implementing the desired clamped rectifier operation is explained in **Section**

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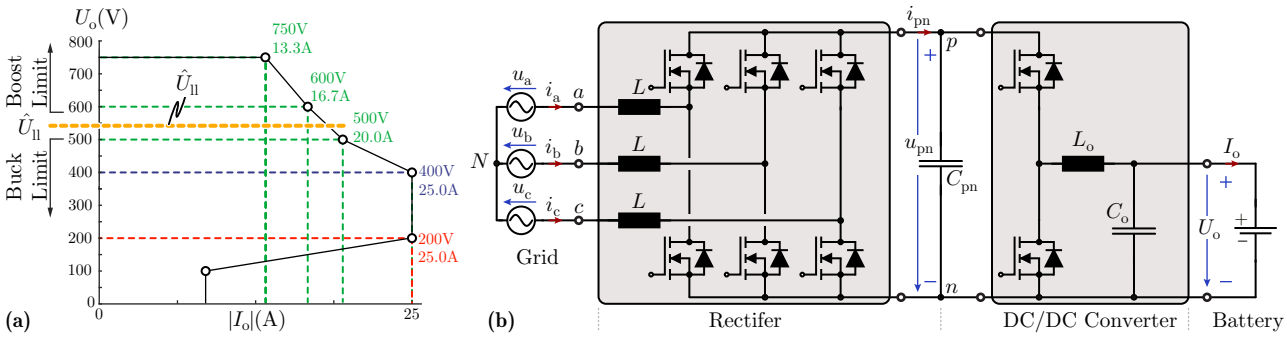

Fig. 1: **(a)** Battery voltage U_o and current range I_o for a 10 kW EV battery charger system corresponding to the *China Grid 2017 Electric Vehicle Charging Equipment Supplier Qualification Verification Standard*. The nominal output power has to be provided for a battery voltage range from 750 V down to 400 V, which means that for the highlighted grid peak line-to-line voltage $\hat{U}_{ll}$, the battery charging system has to feature boost and buck functionality. **(b)** Circuit diagram of a typically used two-stage converter system consisting of a three-phase PFC boost-type rectifier and a subsequent DC/DC buck converter to generate output voltages above and below $\hat{U}_{ll}$.

III, whereas the proper operation is verified in **Section IV** by means of a close loop circuit simulation. In a next step, the novel 1/3 rectifier and/or 1/3 modulation is compared to conventional modulation techniques for a 10 kW battery charger application in **Section V** and finally, in **Section VI** the findings of this publication are summarized.

II. Modulation Concept

In order to allow a better understanding of the proposed converter operating principle, the modulation scheme of the 1/3 rectifier is derived from another circuit topology, namely the Integrated Active Filter (IAF) buck-type PFC rectifier [12]–[14] illustrated in **Fig. 2(a)**. The IAF PFC rectifier consists of a passive three-phase diode rectifier, a current injection network (highlighted in light yellow) and a subsequent DC/DC buck converter stage. As can be noticed, since the input phase voltages are directly applied to the diode rectifier stage, the conduction state of the diode bridge-legs only depends on the actual mains voltages. In the following, the converter operation is explained for the first of six mains voltage sectors where $u_a > u_b > u_c$ (i.e. $\omega t \in [0°, 60°]$ highlighted in **Fig. 2(b)-(c)**). In *sector I*, the upper diode of the bridge-leg of phase a and the lower diode of the bridge-leg of phase c are conducting, which means that phase a is attached to the positive (p) and phase c to the negative (n) DC link voltage rail and therefore $u_{ac} = u_a - u_c$ determines the DC link voltage u_{pn}, which always equals the momentary largest line-to-line input voltage U_{ll} of the respective sector. Hence, within one mains period the DC link voltage u_{pn} exhibits a six-pulse voltage shape as shown in **Fig. 2(b)**. Consequently, if the current injection network is disabled, in *sector I* only the phases a and c are conducting the DC link current i_{pn}, which in case of a constant output power operation (i.e. $U_o \cdot I_o = u_{pn} \cdot i_{pn} = const.$ which means the buck stage employs a time varying duty cycle) results in quasi-square wave shaped grid currents i_a, i_b, i_c within one mains period. However, now the current injection network can be utilized to impress a current i_Y to the non-conducting middle phase, i.e. in *sector I* phase b is selected by the bidirectional phase selector switches and a current $i_Y = -i_b$ proportional to the phase voltage u_b is injected into phase b by proper pulse width modulation of the bridge-leg with midpoint Y. According to Kirchhoff's current law, at the neutral point N the phase currents sum up to zero and due to the constant output power operation, symmetric sinusoidal grid currents in phase with their respective phase voltages can be achieved for all three phases (cf. **Fig. 2(c)**), even though in the case of the IAF rectifier only one half-bridge is pulse width modulated [13].

The same modulation principle is now applied to the conventional three-phase boost-type PFC rectifier shown in **Fig. 2(d)**, whereas instead of a dedicated current injection network in each voltage sector always the bridge-leg connected to the minimum absolute phase voltage, i.e. the highlighted phase b in *sector I*, is high-frequency switched and a phase current proportional to the corresponding phase voltage is injected. In contrast to the IAF converter, the high-side switch of the bridge-leg a as well as the low-side switch of the bridge-leg c have to be actively turned-on within *sector I*, since the mains voltages are not directly applied, but are decoupled by the input inductors L. Hence, the voltage across each inductor of the two clamped bridge-legs is found by half of the difference between the momentary largest mains line-to-line voltage U_{ll} and the DC link voltage u_{pn}. This means that in steady state operation, the voltage u_{pn} has to closely follow the actual maximum line-to-line voltage U_{ll}, i.e. it has to show a six-pulse voltage shape again, and only a small voltage difference must be applied to the inductors in order to achieve sinusoidal input current waveforms. However, since the switches of the two absolute largest input phases are permanently clamped, the DC link voltage u_{pn} has to be controlled by the subsequent DC/DC buck converter, which in analogy to the IAF converter can be achieved if in steady state a constant power is drawn from the load or the intermediate DC link, respectively. In **Fig. 2(e)-(f)**, the corresponding duty cycles and switching states for the three-phase boost-type PFC rectifier and the DC/DC buck converter are shown. It can be noted that at any time in total only two bridge-legs, one of the rectifier and the one of the DC/DC stage, are switched, while the other bridge-legs are clamped to either the positive (p) or negative (n) DC link voltage rail. Consequently, in comparison to the DPWM operation principle, the rectifier stage switching losses can be further reduced by more than a factor of two, because in case of the 1/3 rectifier beneficially always only

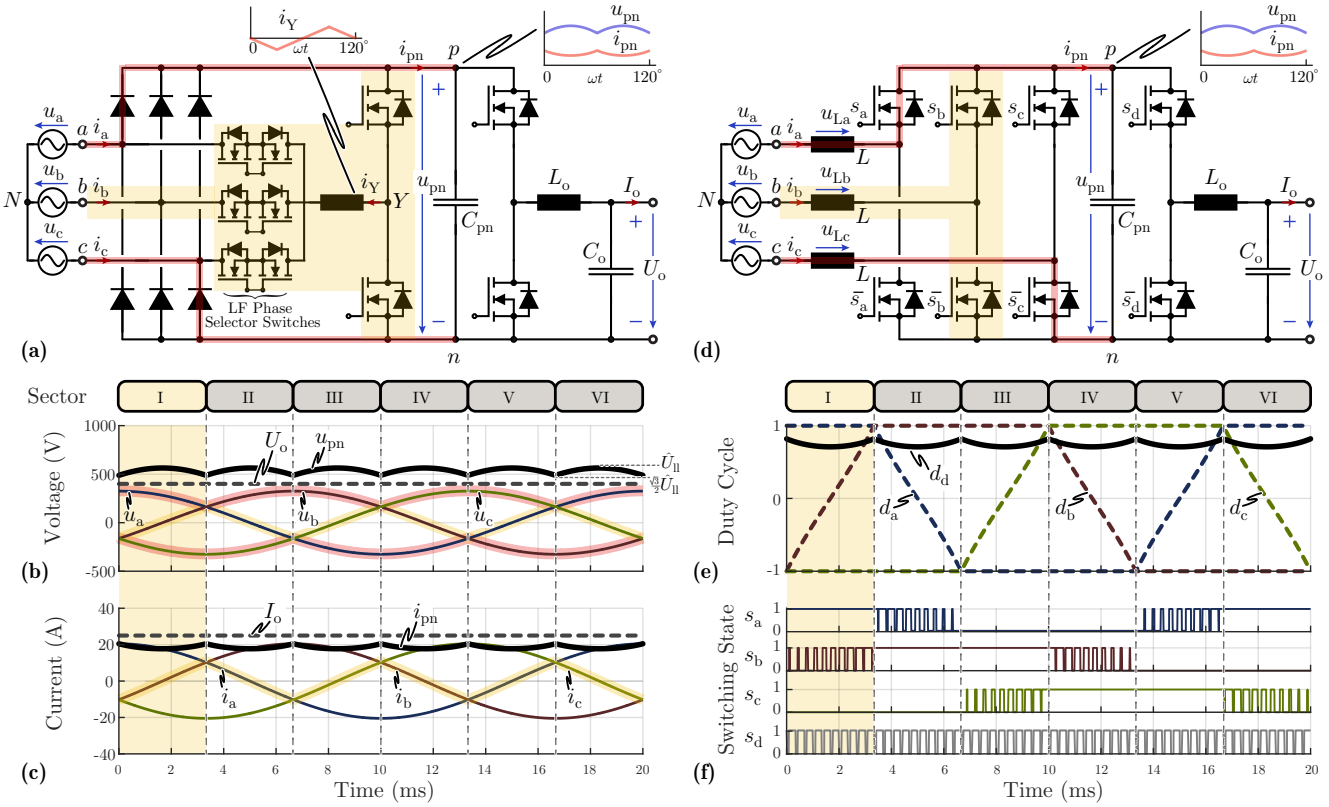

Fig. 2: **(a)** IAF buck-type PFC rectifier consisting of a three-phase diode rectifier, a current i_Y injection network (highlighted in light yellow) and a subsequent DC/DC buck converter, where the rectifier conduction state is highlighted for mains voltage *sector I*, where $\omega t \in [0°, 60°]$. **(b)** Input voltage waveforms u_a, u_b, u_c and resulting six-pulse shaped intermediate DC link voltage u_pn as well as the constant output DC voltage U_o within one grid fundamental period. **(c)** Phase currents i_a, i_b, i_c and resulting DC link current i_pn if the DC/DC buck converter is operated as a constant power load. The voltage and current waveforms are obtained with the IAF buck-type PFC rectifier as well as with the proposed 1/3 rectifier. **(d)** Circuit diagram of the 1/3 rectifier, where for *sector I* the highlighted phase b is switching and phases a and c are clamped to the positive (p) and negative (n) DC link voltage rail, respectively. **(e)** Duty cycles d_a, d_b, d_c of the 1/3 rectifier and d_d of the buck stage, where a value of +1 and -1 refers to clamped operation to p and n, respectively. **(f)** Schematic view of the 1/3 rectifier's switching signals s_a, s_b and s_c and the DC/DC buck converter with s_d which is continuously switched, such that in total always only two bridge-legs are pulse width modulated at a given time.

the rectifier bridge-leg carrying the lowest instantaneous grid current is switched. In addition, symmetric stresses result for the high- and low-side rectifier power semiconductors as can be observed by the half wave symmetry of the duty cycle waveforms in **Fig. 2(e)**.

It should be mentioned that in contrast to the IAF PFC rectifier, the 1/3 rectifier features boost and buck functionality, however, the proposed operation mode is only applicable as long as the system is operated in buck mode, where $U_\mathrm{o} < \frac{\sqrt{3}}{2}\hat{U}_\mathrm{ll}$. In cases where the output voltage exceeds the peak line-to-line voltage $\hat{U}_\mathrm{ll}$, the converter enters the boost mode and hence the bridge-leg of the DC/DC buck stage is clamped ($d_\mathrm{d} = 1$) and the intermediate DC link voltage u_pn is stepped up directly to the desired constant output voltage U_o by the boost-type rectifier. This can only be achieved if e.g. with DPWM a second rectifier bridge-leg is pulse width modulated. However, also in boost mode only a total of two bridge-legs are switched at a time. As will be shown in **Section IV**, the intermediate output voltage range $\frac{\sqrt{3}}{2}\hat{U}_\mathrm{ll} < U_\mathrm{o} \leq \hat{U}_\mathrm{ll}$, where buck and boost functionality is required, can also be covered by only switching two bridge-legs by means of a combined 1/3 and DPWM rectifier operation.

III. Control

The 1/3 rectifier control structure shown in **Fig. 3** is based on conventional PFC rectifier control with cascaded voltage and current PI regulators. Given unity power factor operation, the rectifier can be described from the grid's perspective by an equivalent symmetric three-phase star-connected ohmic load with conductance value G^*, which is set by the *output voltage control* depending on the control error of the DC output voltage and/or the output power demand P_o^*. Subsequently, in the *grid current control* block the grid current references i_a^*, i_b^* and i_c^* are calculated based on G^* and the respective measured phase voltages u_a, u_b and u_c such that the desired unity power factor operation is achieved, where each grid current is controlled individually by a current regulator Ri_grid. In a conventionally modulated system, the resulting rectifier half-bridge midpoint voltage references u_Ba^*, u_Bb^* and u_Bc^* would be directly translated into rectifier phase PWM duty cycles using e.g. Space Vector Modulation. Instead, according to **Section II** in the *phase selector* block the phases with the most positive and negative actual grid voltage are set to be clamped and formulate the reference value of the intermediate voltage $u_\mathrm{pn}^* = u_\mathrm{max}^* - u_\mathrm{min}^*$, while the PWM duty cycle of

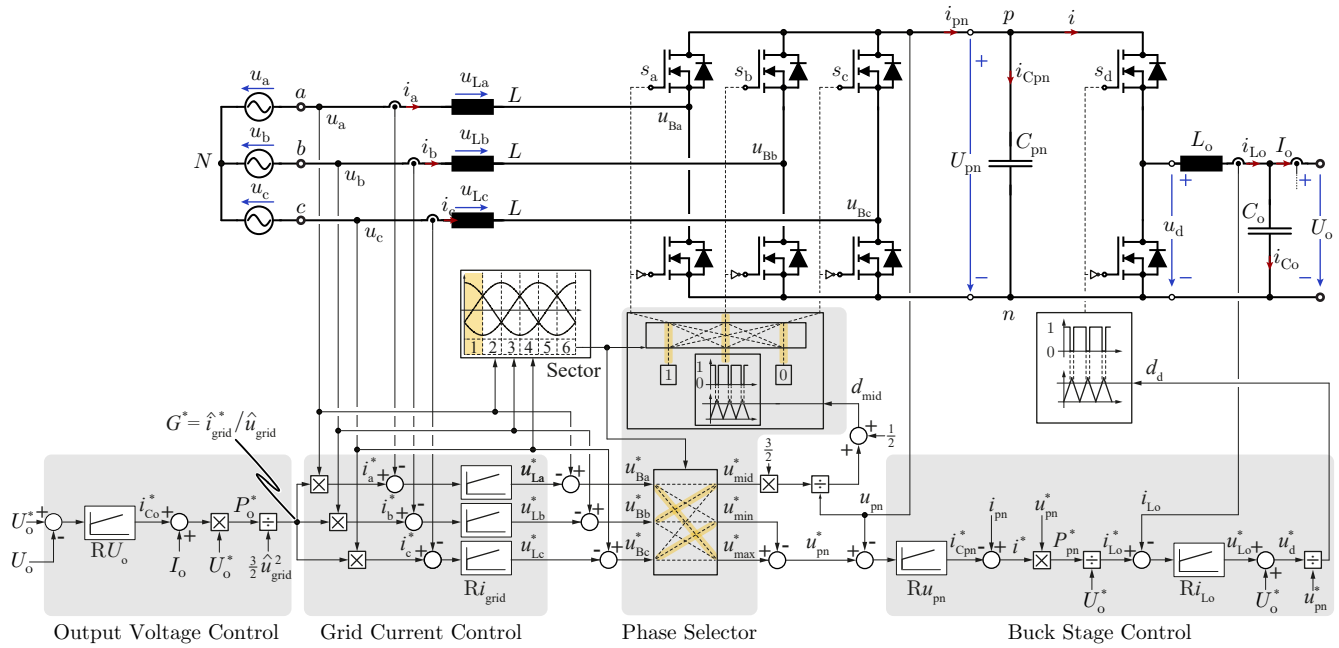

Fig. 3: Cascaded 1/3 rectifier output voltage control with the required measurements and indicated phase assignment for sector I.

the remaining rectifier half-bridge is directly calculated from the respective voltage reference u^*_{mid} and u_{pn}. Subsequently, in the *buck stage control* block again a cascaded voltage and current control structure for the DC/DC converter is present, where a time varying intermediate voltage u^*_{pn} and a constant output voltage reference U^*_{o} have to be tracked.
The very same control structure can be applied when feeding power from a DC source back to the grid in inverter operation (e.g. in case of PV power processing). There the phase currents are 180° phase shifted to their respective phase voltages or, a negative equivalent phase conductance value G^* is seen from the grid's perspective.

IV. Simulation

Given the multi-cascaded control structure shown in **Fig. 3**, each PI controller is to be tuned separately for the present reference tracking demand, where special attention is required on the overall performance of the system or, each regulator is to be designed sufficiently faster than its direct supervisory controller to prevent oscillations in transient operation.
The control concept of **Section III** is verified by means of a closed loop circuit simulation, where the controller signals are updated once in each switching period in order to minimize the dead time. The resulting voltage and current waveforms for different operating conditions can be observed in **Fig. 4**, where in all cases a switching frequency of 100 kHz, grid and DC inductance values of 100 µH are employed and a grid phase voltage of 220 Vrms is set. In **Fig. 4(a)** a total output power of 10 kW is converted into a DC output voltage of 400 V in 1/3 rectifier operation, while in **Fig. 4(b)** the same power is transferred with capacitive phase shifted currents ($\phi = \pi/4$), such that larger grid current amplitudes result. Then, in **Fig. 4(c)** a load step of 50 % is applied and finally in **Fig. 4(d)** an output voltage of 525 V is generated by a combined DPWM and 1/3 rectifier modulation scheme, where only two bridge-legs are pulse width modulated at any time.
In all considered operating points the control system is able to maintain a constant output voltage, while the grid currents are tracked closely to their reference values, confirming the unity power factor and phase shifted sinusoidal input current operation. Furthermore, sudden changes in load current or also a dynamic change of the modulation scheme can be adjusted without significant transient overvoltages or overcurrents. Due to the unconnected mains star point N the switching frequency operated phase in 1/3 modulation (i.e. the phase with the lowest absolute mains voltage) causes a switching frequency level common mode voltage $U_{\mathrm{cm,HF}} = 1/3 \cdot U_{\mathrm{B,mid}}$, where $U_{\mathrm{B,mid}}$ is the respective switched node potential, while the clamped phases mutually cancel out and contribute in sum no common mode voltage at all. Therefore, a current ripple results in all AC-side inductors, where the maximum current ripple can be observed always in the switching phase which is a factor of two higher compared to the current ripple of the clamped phases.

V. Comparative Evaluation

In order to evaluate the gained advantages of the novel 1/3 rectifier concept, three modulation schemes are compared with respect to the resulting efficiency for the operating range defined by the EV battery charger specifications shown in **Fig. 1(a)**, namely conventional PWM without any third harmonic injection and an intermediate voltage

$$u_{\mathrm{pn}}(U_{\mathrm{o}}) = \max\left(\frac{2}{\sqrt{3}}\hat{U}_{\mathrm{ll}}, U_{\mathrm{o}}\right), \tag{1}$$

DPWM where the phase with the lowest instantaneous grid voltage value is clamped and/or the harmonic injection allows a better intermediate voltage utilization

$$u_{\mathrm{pn}}(U_{\mathrm{o}}) = \max(\hat{U}_{\mathrm{ll}}, U_{\mathrm{o}}), \tag{2}$$

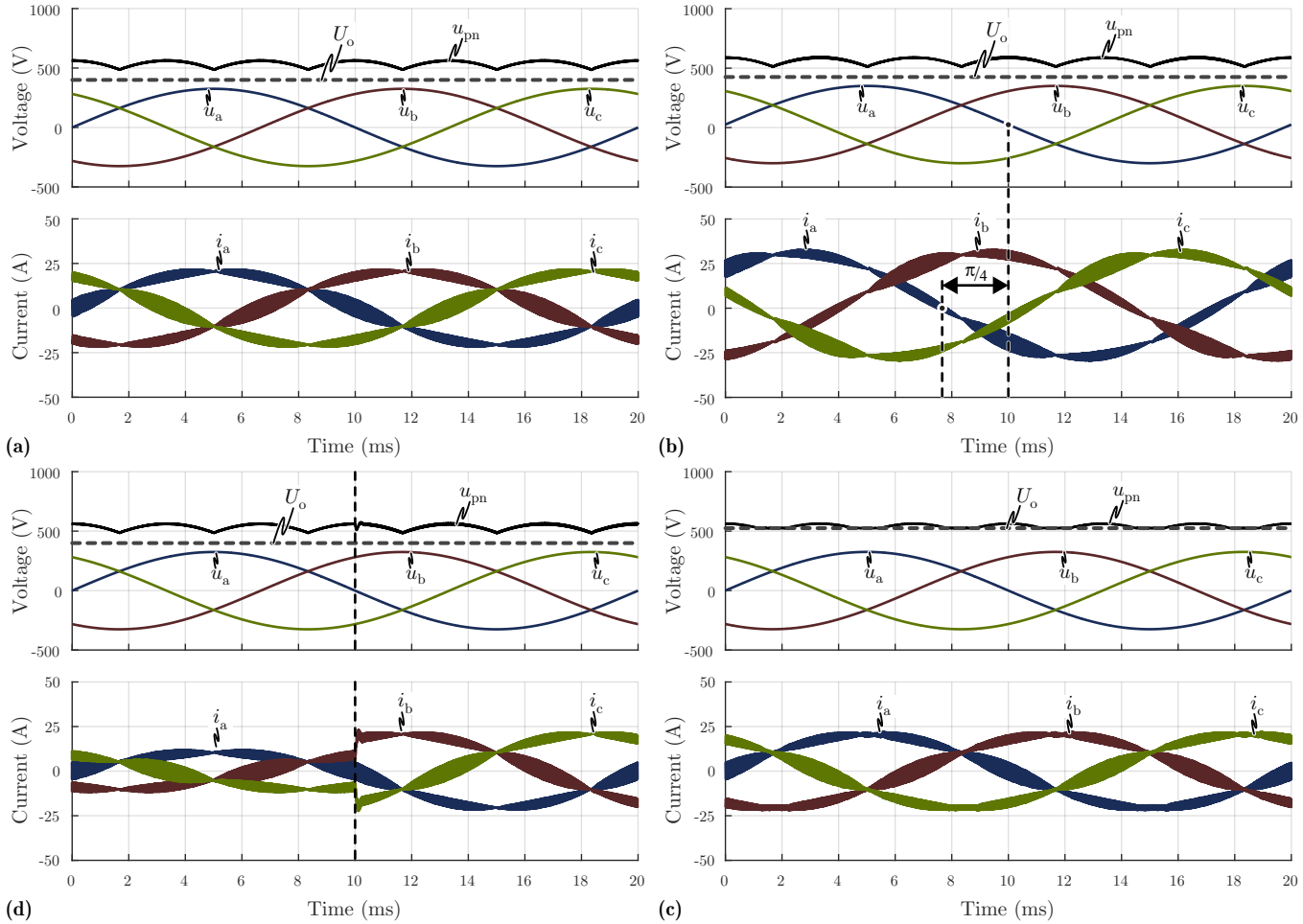

Fig. 4: Resulting closed loop circuit simulation current and voltage waveforms of a 10 kW rectifier for **(a)** $U_o = 400\,V$ and ohmic PFC operation, **(b)** $U_o = 400\,V$ and ohmic/capacitive operation ($\phi = \pi/4$), **(c)** $U_o = 400\,V$, where a load step of 50 % (i.e. from 5 kW to 10 kW) takes place after half of the fundamental period, **(d)** $U_o = 525\,V$ which is generated employing a combined modulation scheme with 1/3 rectifier and DPWM operation.

and the proposed 1/3 modulation scheme employing a time varying low intermediate voltage

$$u_{pn}(U_o) = \begin{cases} \in [\frac{\sqrt{3}}{2} \cdot \hat{U}_{ll}, \hat{U}_{ll}], & U_o \leq \hat{U}_{ll} \\ U_o, & U_o > \hat{U}_{ll} \end{cases} \tag{3}$$

The resulting semiconductor switching losses depend on both the hard switched voltage and current [15], where the voltage across all bridge-legs is defined by the intermediate voltage u_{pn} such that decreased switching losses can be expected when employing DPWM and 1/3 modulation compared to PWM. More importantly, given the discontinuous switching operation of the rectifier bridge-legs the switching losses can be expected to decrease by more than $1/3$ for DPWM and $2/3$ for the 1/3 modulation compared to PWM due to the reduced number of switching transitions within a grid fundamental period and especially because of the fact that with 1/3 modulation always the smallest grid current is switched in unity power factor operation. Then, employing symmetric bridge-legs the current is impressed by the inductor connected to the switched node and flows either through the high- or low-side switch, where the resulting conduction losses are independent of the bridge-leg switching state. Now, as all inductor currents are subject to closed loop control (cf. **Fig. 3**) while the occurring inductor current ripple has only minor influence on the respective RMS current value at nominal power, the semiconductor conduction stresses can be considered independent of the modulation scheme in a good approximation.

For this reason, a EV battery charger system which was dimensioned for the specifications in **Fig. 1(a)** and conventional PWM can also be operated with the other modulation schemes of interest, such that a comparison of the occurring losses for the operation concepts is possible for a given converter system. The corner points relevant for the component dimensioning with PWM are at the respective maximum output power and $u_{pn} = U_o = 750\,V$ for the rectifier bridge-legs and inductors, while $U_o = 400\,V$ yields the maximum stresses for the DC/DC converter switches and $U_o = u_{pn}/2 = 325\,V$ (i.e. duty cycle $d_d = 50\,\%$) for the DC-side inductor. The comparison amongst the modulation strategies is carried out in the following for a virtual 10 kW battery charger system employing switching frequencies $f_s = 48\,kHz$ and inductance values $L = 100\,\mu H$ in the AC/DC and DC/DC stage, where the component details are given in **Table I**. The resulting semiconductor hard- and

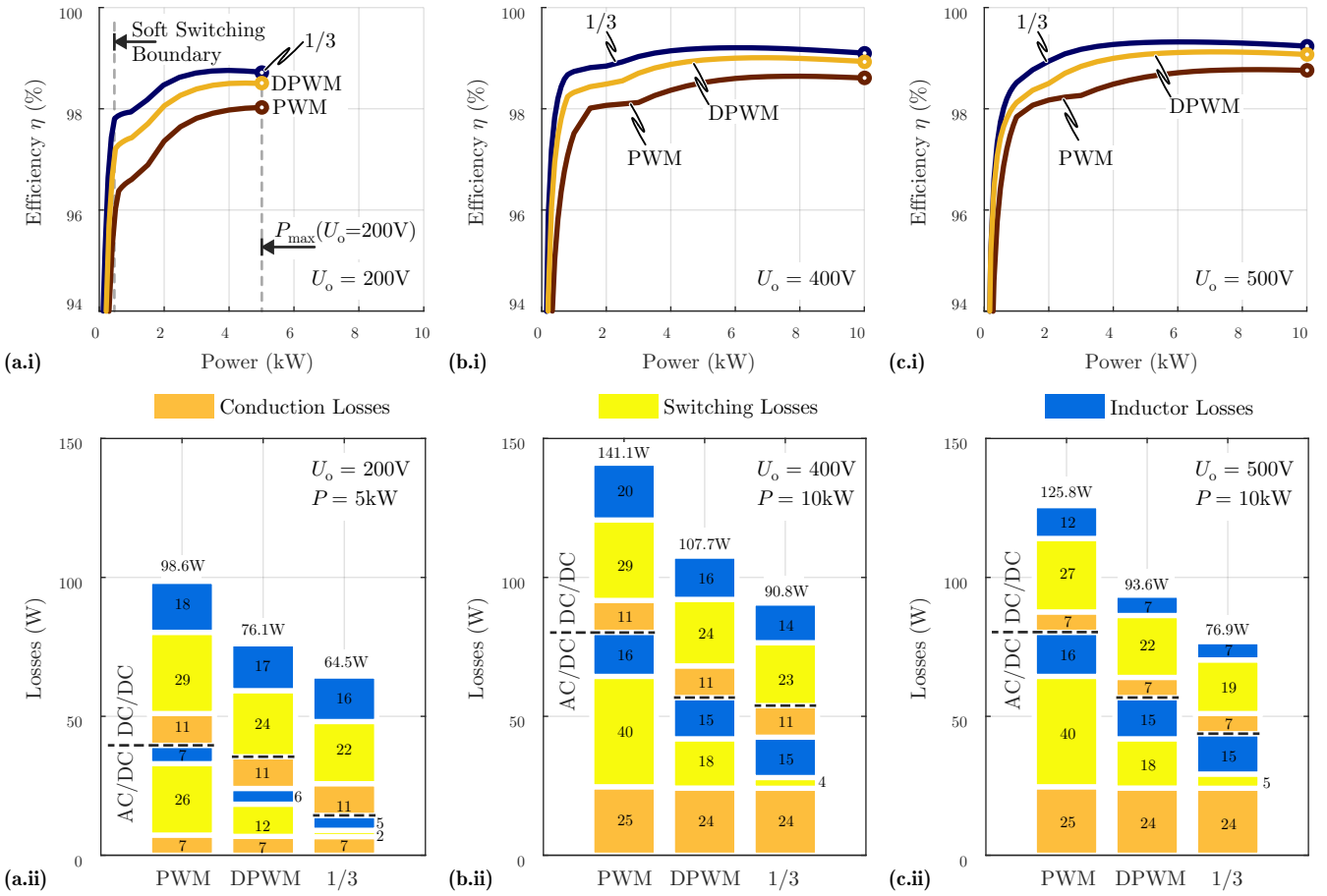

Fig. 5: **(a.i)-(c.i)** Efficiency depending on the output power P and **(a.ii)-(c.ii)** loss distribution for the respective maximum value of P of a virtual EV battery charger system according to **Table I** with PWM, DPWM and 1/3 rectifier modulation for an output voltage of **(a)** $U_o = 200\,\mathrm{V}$, **(b)** $U_o = 400\,\mathrm{V}$ and **(c)** $U_o = 500\,\mathrm{V}$.

soft-switching losses are derived using a lossmap, while the inductor iron as well as DC and/or low-frequency and high-frequency copper losses are calculated according to [16]. As film capacitors exhibit a very low ESR they are considered to be lossless in the efficiency calculation.

In **Fig. 5(a.i-c.i)** the resulting efficiency depending on the output power and modulation scheme is shown for several DC voltage levels U_o, where for $U_o < 400\,\mathrm{V}$ the power is restricted by the DC current limit (cf. **Fig. 1(a)**). At low power levels, a flattening or even a non-monotonically increasing efficiency can be observed for all modulation schemes and output voltage levels U_o, which results due to the DC/DC converter changing from soft- to hard-switching with increasing DC output current and leading locally to a significant change in the total converter losses. As the intermediate voltage u_{pn} is not equal for PWM, DPWM and 1/3 modulation, different DC current ripples result, and therefore the transition from soft- to hard-switched operation takes place for different values of P for each modulation approach and output voltage level U_o. Comparing the efficiencies for the different modulation schemes, e.g. for $U_o = 200\,\mathrm{V}$ (cf. **Fig. 5(a.i)**) the efficiency at $P = 5\,\mathrm{kW}$ can be increased from 98.1 % with PWM to 98.5 % with DPWM and to even 98.7 % employing 1/3 modulation. Very similar relations establish for a higher output voltage $U_o = 400\,\mathrm{V}$ (cf. **Fig. 5(b.i)**) and $U_o = 500\,\mathrm{V}$ (cf. **Fig. 5(c.i)**), where it can be noted, that the maximum efficiency for DPWM and 1/3 modulation does not occur for the maximum respective output power, but for part load operation. This results, as the system optimization and dimensioning was carried out for PWM and is by no means optimal for the discontinuous operation of the bridge-legs, which is especially accentuated for the 1/3 rectifier. Therefore, a further substantial efficiency gain could be enabled by a system redesign. **Fig. 5(a.ii-c.ii)** show the detailed loss distribution for the same output voltages at the

	(3x) AC/DC	(1x) DC/DC
MOSFET	1.2 kV SiC $R_{ds} = 25\,\mathrm{m\Omega}$ $C_{oss} = 220\,\mathrm{pF}$	1.2 kV SiC $R_{ds} = 25/2\,\mathrm{m\Omega}$ $C_{oss} = 2 \cdot 220\,\mathrm{pF}$
Inductor	4x E36/18/11 N87 $d_{litz} = 2.6\,\mathrm{mm}$ $d_{strand} = 200\,\mu\mathrm{m}$ $N_{wind} = 16$	4x E 42/21/20 N87 $d_{litz} = 3.4\,\mathrm{mm}$ $d_{strand} = 100\,\mu\mathrm{m}$ $N_{wind} = 14$

TABLE I: Virtual 10 kW EV batter charger component specifications for the bridge-legs and inductors, where switching frequencies $f_s = 48\,\mathrm{kHz}$ and inductance values $L = 100\,\mu\mathrm{H}$ are employed in the PFC rectifier (AC/DC) and the DC/DC stage.

respective maximum system power, where the semiconductor losses clearly dominate the converter performance. For all shown cases a reduction of the total system losses by approximately $25\,\%$ for DPWM and $35\,\%$ for 1/3 rectifier operation is possible compared to conventional PWM. When focusing on the rectifier semiconductor switching losses, one can observe that a loss reduction of a factor 2 is possible with DPWM as the phase showing the most negative phase voltage is clamped while carrying a large current, yielding an improved performance compared to PWM. Then, employing the proposed 1/3 modulation, the rectifier switching losses almost vanish and are now reduced by up to a factor of 12. This superior performance follows, as in unity power factor operation the rectifier bridge-legs are only switching in the vicinity of the AC current zero crossing, where also the maximum current ripple occurs, such that even for moderate current ripple values complete soft-switching results. In the switching losses of the DC/DC converter one can also observe the negative influence of the elevated intermediate voltage u_{pn} for PWM operation (cf. (1)-(3)), where the occurring losses depend both on the transferred power and the voltage difference $\Delta u = u_{\mathrm{pn}} - U_{\mathrm{o}}$ that has to be converted. Hence, by employing the DPMW and 1/3 modulation even the switching losses of the DC/DC converter can be reduced. Especially at $U_{\mathrm{o}} = 500\,\mathrm{V}$ (cf. **Fig. 5c.ii**), where the DC/DC converter bridge-leg is already temporarily clamped in 1/3 modulation, also the switching losses in the DC/DC converter are strongly reduced by $25\,\%$ compared to PWM. Furthermore, when investigating the losses in the inductive components, one can observe that the clamped operation of DPWM and 1/3 modulation combined with the reduced intermediate DC link voltage u_{pn} also allows to slightly decrease the high-frequency inductor losses for $U_{\mathrm{o}} = 200\,\mathrm{V}$ and $U_{\mathrm{o}} = 400\,\mathrm{V}$. When the DC/DC converter bridge-leg is clamped, only DC and/or low-frequency copper losses result and therefore for $U_{\mathrm{o}} = 500\,\mathrm{V}$ a decrease in inductor losses of more than $40\,\%$ results for 1/3 modulation with its partially clamped DC/DC converter bridge-leg compared to conventional modulation. Finally, the semiconductor conduction losses remain unaffected by the modulation scheme in a very good approximation as can be observed for the AC/DC and the DC/DC stage such that now for the 1/3 modulation the rectifier stage losses are clearly dominated by the conduction losses. Therefore, the converter efficiency could be significantly increased in that case by redesigning the converter, i.e. by employing more chip area in order to minimize the total semiconductor losses. In summary, in can be stated for **Fig. 5**, that for the given converter system, the efficiency can be increased significantly for the analyzed operating points by employing the novel 1/3 modulation instead of conventional PWM modulation, where the efficiency curves of 1/3 modulation and DPWM start converging once the output voltage approaches $\hat{U}_{\mathrm{ll}}$.
This is clearly shown in **Fig. 6(a)** where the influence of the DC output voltage on the efficiency (cf. **Fig. 6(a.i)**) and the losses (cf. **Fig. 6(a.ii)**) is further investigated, while again the maximum output power is considered in each operating point. According to **Fig. 1(a)** between $U_{\mathrm{o}} = 200\,\mathrm{V}$ and $U_{\mathrm{o}} = 400\,\mathrm{V}$, P linearly increases from $5\,\mathrm{kW}$ to $10\,\mathrm{kW}$ and is then kept constant as shown in **Fig. 6(a.iii)**. When

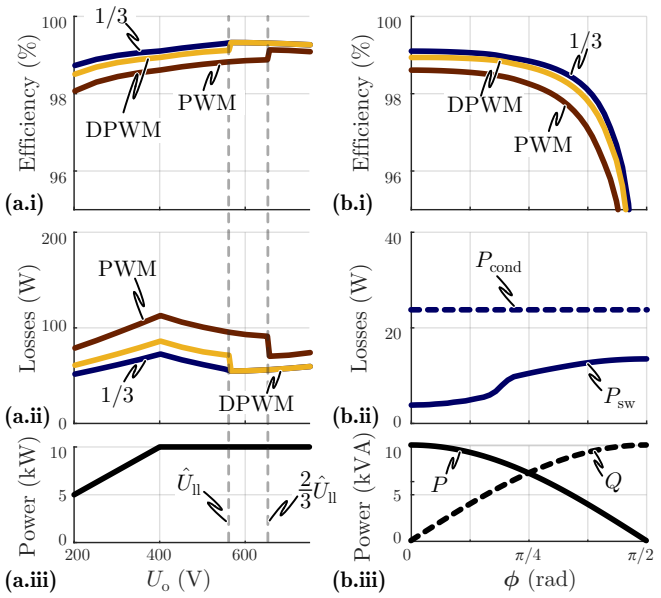

Fig. 6: Influence on the system performance of **(a)** the DC output voltage U_{o} for maximum output power and unity power factor, **(b)** the grid current-voltage phase shift angle ϕ for $U_{\mathrm{o}} = 400\,\mathrm{V}$ and an AC apparent power of $S = 10\,\mathrm{kVA}$, where only positive values of ϕ are shown as the performance penalty is identical for inductive and capacitive phase shift. In **(a.i)** the resulting efficiency and in **(a.ii)** the total losses of the battery charger system for PWM, DPWM and 1/3 modulation are given, while **(a.iii)** illustrates the resulting output power profile according to **Fig. 1(a)**. In **(b.i)** again the system efficiency for all modulation schemes and in **(b.ii)** the rectifier stage semiconductor switching losses (P_{sw}) and conduction losses (P_{cond}) for 1/3 modulation and in **(b.iii)** the active P and reactive power Q are presented, where for $\phi = 0$ (i.e. unity power factor operation) an active power of $P = 10\,\mathrm{kW}$ is transferred.

starting from low DC output voltages, the resulting losses increase with the system power up to $400\,\mathrm{V}$ where the maximum losses result, i.e. the worst case design point (as already mentioned) for the design of the converter. Then, when further increasing U_{o} the losses decay with decreasing buck effort since the power is held constant, which means that the DC current decreases. Once $U_{\mathrm{o}} = u_{\mathrm{pn}}$ is reached a step in the losses and the efficiency occurs for PWM and DPWM as the DC/DC converter bridge-leg is clamped such that only the DC semiconductor conduction losses remain, where the switching transition occurs at different voltage levels due to the different intermediate DC voltage u_{pn}. A difference in efficiency and losses between DPWM and PWM sustains, as with DPWM two and with PWM three rectifier bridge-legs are switched. In contrast, for the 1/3 modulation a smooth transition to DPWM operation takes place within $U_{\mathrm{o}} \in [\frac{\sqrt{3}}{2} \cdot \hat{U}_{\mathrm{ll}}, \hat{U}_{\mathrm{ll}}]$, where the DC/DC bridge-leg is temporarily clamped when the maximum instantaneous line-to-line voltage drops below U_{o}, while PFC control is maintained by switching two rectifier bridge-legs employing DPWM. For this reason 1/3 modulation and DPWM yield identical performance for higher values $U_{\mathrm{o}} > \hat{U}_{\mathrm{ll}}$. Most interestingly, the application of the 1/3 modulation allows to decrease the maximally occurring losses at $U_{\mathrm{o}} = 400\,\mathrm{V}$ such that the required heatsink volume could be decreased by more than $35\,\%$, which also clearly highlights that the

converter would have to be redesigned to either achieve an even higher efficiency, higher power density or lower costs (cf. **Fig. 6(a.ii)**). Finally, in **Fig. 6(b)** the influence of the reactive power consumption on the system performance (i.e. $\cos\phi < 1$) is highlighted for an apparent grid power of $S = 10\,\mathrm{kVA}$ and $U_\mathrm{o} = 400\,\mathrm{V}$. As the occurring losses are equal for inductive and capacitive grid currents, only positive grid current-voltage phase shift angles ϕ are shown. **Fig. 6(b.i)** shows again the system efficiency for the three modulation schemes of interest, where in any case the efficiency drops with the decreasing active P and increasing reactive power Q transfer (cf. **Fig. 6(b.iii)**). When studying the rectifier semiconductor losses for 1/3 modulation shown in **Fig. 6(b.ii)** in detail, one can observe that the conduction losses P_cond remain unaffected by ϕ due to the constant AC current amplitude and thus constant RMS current value. For low values of $\phi < \pi/8$ also the switching losses P_sw increase only slightly as despite the phase shift the switching frequency operated bridge-legs remain soft-switched. When ϕ is further increased, a sudden increase of P_sw takes place which again saturates once all switching transitions are hard-switched. Therefore the performance of the 1/3 rectifier is highly insensitive to small current-voltage phase shifts, and even for large values of ϕ a performance gain compared to DPWM and PWM sustains.

VI. Conclusion

A novel modulation scheme for a three-phase boost-type PFC rectifier system with a subsequent buck converter employing a variable intermediate DC link voltage in order to minimize the current control effort in the rectifier stage was introduced and the operating principle was derived from the *Integrated Active Filter PFC Rectifier* and discussed in detail. A cascaded control structure for sinusoidal input current shaping and output voltage/power control was presented and the two-phase clamped operation was subsequently verified by means of a closed loop circuit simulation for several stress profiles. For a virtual prototype EV battery charger designed for conventional PWM operation, a substantial gain in system efficiency, i.e. a $35\,\%$ loss reduction compared to a conventionally modulated system was achieved. This results, as even for moderate AC current ripples the 1/3 rectifier modulation yields a completely soft-switched rectifier stage, such that the switching losses could be reduced by more than a factor of 10.

As was pointed out, the two-phase-clamped and/or 1/3 modulation can be applied in any boost-type rectifier system with a subsequent buck converter without changes in hardware and has therefore a great potential also for existing systems, where 1/3 modulation could be enabled easily by a software update. Furthermore, a system optimized for 1/3 rectifer modulation could break through current power density and efficiency barriers and therefore is of high interest for industrial EV charger applications. A verification of the new approach by means of a prototype system will be conducted in a next step.

References

[1] P. Hertzke, N. Müller, S. Schenk, and T. Wu, "The global electric-vehicle market is amped up and on the rise," *McKinsey*, 2018.

[2] D. Aggeler, F. Canales, H. Zelaya, D. L. Parra, A. Coccia, N. Butcher, and O. Apeldoorn, "Ultra-fast dc-charge infrastructures for ev-mobility and future smart grids," in *Proc. of the IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT Europe)*, Oct. 2010, pp. 1–8.

[3] M. Falahi, H. M. Chou, M. Ehsani, L. Xie, and K. L. Butler-Purry, "Potential power quality benefits of electric vehicles," *IEEE Transactions on Sustainable Energy*, vol. 4, no. 4, pp. 1016–1023, Oct. 2013.

[4] J. W. Kolar and T. Friedli, "The essence of three-phase pfc rectifier systems," in *Proc. of the 33rd IEEE International Telecommunications Energy Conference (INTELEC)*, Oct. 2011, pp. 1–27.

[5] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2151–2169, May 2013.

[6] D. C. Erb, O. C. Onar, and A. Khaligh, "Bi-directional charging topologies for plug-in hybrid electric vehicles," in *Proc. of the 25th IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb. 2010, pp. 2066–2072.

[7] J. P. M. Figueiredo, F. L. Tofoli, and B. L. A. Silva, "A review of single-phase pfc topologies based on the boost converter," in *Proc. of the 9th IEEE/IAS International Conference on Industry Applications (INDUSCON)*, Nov. 2010, pp. 1–6.

[8] G. Buja and G. Indri, "Improvement of pulse width modulation techniques," *Archiv für Elektrotechnik*, vol. 57, no. 5, pp. 281–289, Sep. 1975.

[9] H. W. van der Broeck, H. Skudelny, and G. V. Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Transactions on Industry Applications*, vol. 24, no. 1, pp. 142–150, Jan. 1988.

[10] K. Taniguchi, Y. Ogino, and H. Irie, "Pwm technique for power mosfet inverter," *IEEE Transactions on Power Electronics*, vol. 3, no. 3, pp. 328–334, Jul. 1988.

[11] M. Depenbrock, "Pulse width control of a 3-phase inverter with non-sinusoidal phase voltages," in *Proc. of the IEEE/IAS International Semiconductor Power Converter Conference*, Mar. 1977, pp. 399–403.

[12] M. Jantsch and C. Verhoeve, "Inverters with three phase output and without electrolyte capacitor for improved lifetime, efficiency and costs of grid connected systems," in *Proc. of the 14th European Photovoltaic Solar Energy Conference (EU PVSEC)*, Jun. 1997.

[13] T. B. Soeiro, F. Vancu, and J. W. Kolar, "Hybrid active third-harmonic current injection mains interface concept for dc distribution systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 7–13, Jan. 2013.

[14] L. Schrittwieser, J. W. Kolar, and T. B. Soeiro, "99% efficient three-phase buck-type sic mosfet pfc rectifier minimizing life cycle cost in dc data centers," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 1, pp. 47–58, Mar. 2017.

[15] X. Li, L. Zhang, S. Guo, Y. Lei, A. Q. Huang, and B. Zhang, "Understanding switching losses in sic mosfets: toward lossless switching," in *Proc. of the 3rd IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov. 2015, pp. 257–262.

[16] P. Papamanolis, F. Krismer, and J. W. Kolar, "Minimum loss operation of high-frequency inductors," in *Proc. of the 33rd IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2018.