Power Electronic Systems
Laboratory

Proceedings of the 2nd IEEE International Power Electronics and Application Conference and Exposition (PEAC 2018), Shenzhen, China, November 4-7, 2018

A New Bidirectional Three-Phase Phase-Modular Boost-Buck AC/DC Converter

D. Menzi,
D. Bortis,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

A New Bidirectional Three-Phase Phase-Modular Boost-Buck AC/DC Converter

David Menzi, Dominik Bortis and Johann W. Kolar
Power Electronic Systems Laboratory
ETH Zurich, Switzerland
menzi@lem.ee.ethz.ch

***Abstract*—In this paper, a new phase-modular bidirectional three-phase boost-buck AC/DC converter topology is introduced. Each of its three phase modules is operated independently and consists of a boost-buck converter, allowing to directly convert an AC voltage into an arbitrary DC voltage by only modulating one of the two converter stages at a time, where the AC voltages are applied against a reference point common to all phases. Hence, single-stage high-frequency energy conversion is enabled, resulting in a highly compact and highly efficient converter system realization. In a first step, the basic structure of the phase-modular converter (PMC) is derived from the well known cascaded arrangement of a three-phase boost-type rectifier and a subsequent DC/DC buck converter, followed by a discussion of its operating principle and characteristic waveforms. Furthermore, the corresponding DC output voltage control scheme is presented which allows a seamless transition between buck and boost operation in each phase module. Finally, the phase-modular converter and the conventional two-stage system are compared by means of simple indices as well as a two-dimensional Pareto optimization concerning efficiency η and power density ρ.**

***Index Terms*—three-phase, AC/DC converter, PFC rectifier, inverter, boost, buck, dual-mode, phase-modular.**

I. Introduction

Bidirectional three-phase AC/DC converters find use in various areas and as power flow in both directions is possible, represent a very generic interface between arbitrary three-phase AC voltages (i.e. with peak phase-to-ground value $\hat{U}_{\rm ac}$) and a DC voltage $U_{\rm dc}$. Typical applications are electric vehicle (EV) battery chargers (cf. **Fig. 1(a)**), which for high power ratings (i.e. P>3 kW) are usually supplied from the three-phase AC grid to generate a DC output voltage according to the batteries rated voltage or charging state. Hence, $U_{\rm dc}$ needs to closely follow a defined profile [1] and power can also be fed back from the battery to the grid. In other applications, photo-voltaic (PV) inverters connect to three-phase AC voltages from a widely varying input DC voltage which depends e.g. on the temperature and the extracted current, or battery/fuel-cell fed variable speed motor drives (cf. **Fig. 1(b)**) need to generate AC voltages within a wide range, i.e. $\hat{U}_{\rm ac} \in [0, \hat{U}_{\rm ac,max}]$, while also the DC voltage is subject to large variations.

Hence, applications employing bidirectional three-phase AC/DC converters (e.g. as three-phase rectifiers are considered in the following) often demand the capability of covering a wide input and/or output voltage range. However, single-stage rectifier systems typically feature only either buck or boost capability [2], such that buck converters are limited to DC voltages $U_{\rm dc} \leq (1-\varepsilon)\cdot\frac{3}{2}\hat{U}_{\rm ac}$ and boost converters to DC voltages $U_{\rm dc} \geq (1+\varepsilon)\cdot\sqrt{3}\hat{U}_{\rm ac}$, where ε (with a typical value of e.g. $\varepsilon = 15\,\%$) constitutes a margin between the AC line-to-line peak voltage and the DC link voltage in order to maintain grid current and output voltage control capability under all operating conditions. In **Fig. 1(c)** the resulting gap in the DC voltage between the operating limits of the two converter types is highlighted for a low voltage (LV) mains with $U_{\rm ll} = \sqrt{3}/\sqrt{2}\cdot\hat{U}_{\rm ac} = 400\,{\rm Vrms}$. As can be seen clearly, the single-stage systems are not directly applicable

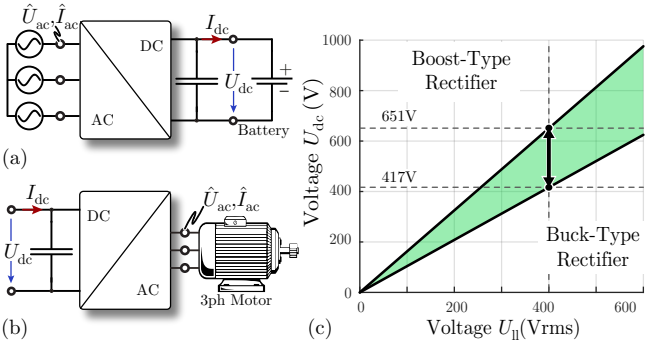

Fig. 1: Typical applications of bidirectional three-phase AC/DC converters with wide input and/or output voltage range, namely **(a)** three-phase mains rectification for e.g. a battery charging system and **(b)** DC voltage source (e.g. battery or fuel-cell) fed motor drive inverter, **(c)** DC output voltage $U_{\rm dc}$ limitations of single-stage buck-type and boost-type rectifiers depending on the AC line-to-line voltage $U_{\rm ll}$, where a margin of $\varepsilon = 15\,\%$ between AC line-to-line peak voltage and the DC link voltage is considered.

if the input and output voltage range is overlapping, i.e. when boost and buck functionality is required. In this case, the cascaded arrangement of a three-phase rectifier and a DC/DC converter is a standard solution, where either a three-phase buck-type rectifier is combined with a DC/DC boost converter or a three-phase boost-type rectifier is combined with a DC/DC buck converter, i.e. a buck-boost or boost-buck AC/DC converter structure is employed, yielding a two-stage energy conversion.

As in three-phase buck rectifier systems the grid currents cannot be controlled directly, the boost-buck AC/DC converter illustrated in **Fig. 2(a.ii)** and further denoted as *Phase-Integrated Converter* (PIC) is especially prominent in applications where a low input current Total Harmonic Distortion (THD) is a key requirement. **Fig. 2(a.i)** shows the mains phase voltages $u_{\rm an}$, $u_{\rm bn}$ and $u_{\rm cn}$ referenced to the negative DC voltage rail n of the rectifier, where an intermediate voltage $U_{\rm pn} \geq 2\cdot\hat{U}_{\rm ac}$ is generated in the simplest case when third harmonic injection techniques [3] are not considered. The DC/DC converter steps $U_{\rm pn}$ down to the desired DC voltage $U_{\rm dc} \in [U_{\rm min}, U_{\rm max}]$, which combined with the assumed constant power operation defines the DC current range (cf. **Fig. 2(a.iii)**). However, the major drawback of a cascaded topology approach, especially pronounced at low DC voltage $U_{\rm dc} = U_{\rm min}$ and high power levels where the intermediate DC link voltage $U_{\rm pn}$ must be stepped down substantially, is that the complete output power has to be converted twice at a time, i.e. the four half-bridges shown in **Fig. 2(a.ii)** are all switching the high intermediate DC link voltage resulting in a limited efficiency.

In the literature [4]–[9], for single-phase PV inverters consisting of a DC/DC boost converter and a grid-side buck-type full-bridge inverter, a dual-mode control concept, i.e. a combined control of the DC/DC and DC/AC converter was introduced, where the intermediate DC link voltage is

978-1-5386-6054-6/18/$31.00

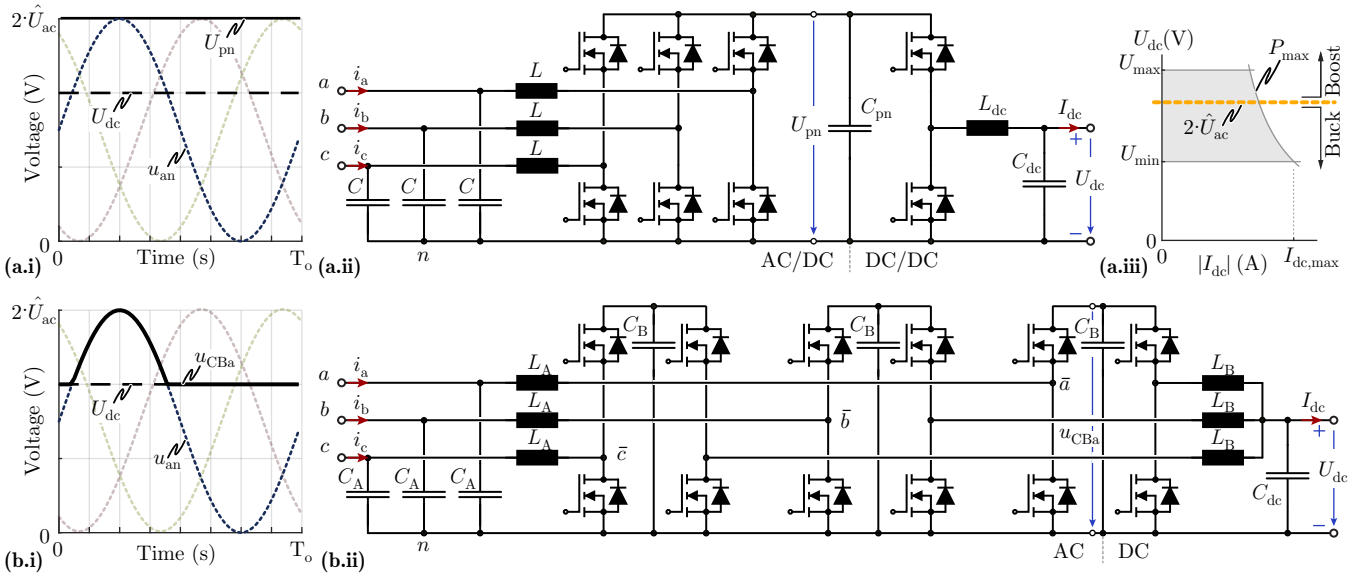

Fig. 2: **(a)** Combination of a three-phase boost-type rectifier and a DC/DC buck converter, i.e. a Phase-Integrated Converter (PIC), which can be arbitrarily operated within overlapping input and output voltage ranges. The intermediate DC link voltage U_{pn} must be controlled to be larger than $2 \cdot \hat{U}_{\mathrm{ac}}$, hence all four half-bridges are continuously switched at a voltage equal to U_{pn}. The grid phase voltage amplitude $\hat{U}_{\mathrm{ac}}$ is indicated in the DC output voltage range, clearly demanding boost-buck capability of the rectifier system. **(b)** Alternative proposed three-phase Phase-Modular Converter (PMC) employing three independently controlled boost-buck converter modules, which means that the three intermediate voltages across the capacitors C_{B} are varying over time and are controlled such that always only one of the two half-bridges is operated in each phase module.

no longer constant but varying over time. Depending on the instantaneous ratio of DC and AC voltage always only one of the two converter stages is pulse width modulated (PWM), while the other one is being clamped, such that a decrease in the total system losses could be verified in [6], [7], [9] due to the decreased number of switching transients per fundamental period.

For cascaded three-phase AC/DC converters a dual-mode control concept has not yet been investigated and the aim of this paper is to compare the performance of the PIC (cf. **Fig. 2(a.ii)**) approach with the one of a phase-modular arrangement, which results from splitting the inductor L_{DC} and the half-bridge of the DC/DC buck converter, as well as the DC link capacitor C_{pn} into three individual phase modules. The resulting *phase-modular* boost-buck structure is depicted in **Fig. 2(b.ii)** and the converter is denoted as *Phase-Modular Converter* (PMC), since it consists of three independent phase modules with dedicated intermediate DC link capacitors C_{B} instead of a common DC link capacitor C_{pn} but still keeps a common negative DC link voltage rail and/or AC output voltage reference point n (no connection of n to the mains neutral is required). Advantageously and in contrast to the single DC link voltage U_{pn} of the PIC system (cf. **Fig. 2(a.i)**), the intermediate voltages u_{CB} of the phases do not need to be controlled to a constant and equal value which always must stay above $2 \cdot \hat{U}_{\mathrm{ac}}$ or the maximum AC line-to-line voltage in case of third harmonic injection PWM, but can be shaped depending on the ratio between the needed DC output voltage and the corresponding phase input voltage (cf. **Fig. 2(b.i)**). This offers a further degree of freedom in the control of each phase module, which means that in any operating point only one, i.e. either the boost or the buck half-bridge, instead of both half-bridges has to be switched, while the other half-bridge is clamped, yielding a dual-mode operation and enabling a *single-stage high-frequency energy conversion* and thus a higher conversion efficiency.

In **Section II**, the operating principle of the PMC as well as the characteristic waveforms are introduced and discussed in detail based on a rectifier application. Subsequently, in **Section III**, a basic control scheme for one phase module is presented. In **Section IV** a comprehensive comparison between the PIC and the PMC approach by means of simple indices and a Pareto comparison of power density and efficiency based on actual component characteristics is conducted for a 10 kW bidirectional three-phase boost-buck rectifier system. In closing, the results of the analyses are summarized and an outlook to further research is given.

II. Converter Operating Principle

The PMC consisting of three identical phase modules is shown in **Fig. 2(b.ii)**, where the AC side mains voltages u_{an}, u_{bn} and u_{cn} are measured with respect to the negative DC voltage rail n, which means that these voltages are unipolar and strictly larger than zero. Hence, in order to generate sinusoidal voltages with an amplitude close to $\hat{U}_{\mathrm{ac}}$ at the bridge leg outputs $\bar{a}$, $\bar{b}$ and $\bar{c}$, an offset of $u_{\mathrm{off}} \geq \hat{U}_{\mathrm{ac}}$ has to be added to the actual sinusoidal grid phase voltages u_{a}, u_{b} and u_{c} in each phase. This offset represents a common-mode component and therefore cannot drive any current in an open star point arrangement, while the differential mode voltages can be controlled in such a way that *Power Factor Correction* (PFC) operation is enabled, i.e. a sinusoidal shape of the input and/or mains phase currents i_{a}, i_{b} and i_{c} results. Due to the phase-modular structure of the PMC, the operating principle is illustrated in detail in **Fig. 3(a)** for phase a only. The phase module consists of the two half-bridges B_{A} (**boost** stage) and B_{B} (**buck** stage) which are either stepping up or stepping down the grid input voltage u_{an}. The half-bridges are both connected to the intermediate capacitor C_{B}, which is also referenced to n, yielding a symmetric converter structure with a second-order LC-filter on the input and output side. Consequently, the half-bridges are located in the phase module's center and the generated switching noise is confined to the inner converter part. Furthermore, the voltage u_{CB} of C_{B} is controlled such that at any time only one half-bridge is switched at high frequency while the other half-bridge is continuously clamped. This mutually exclusive

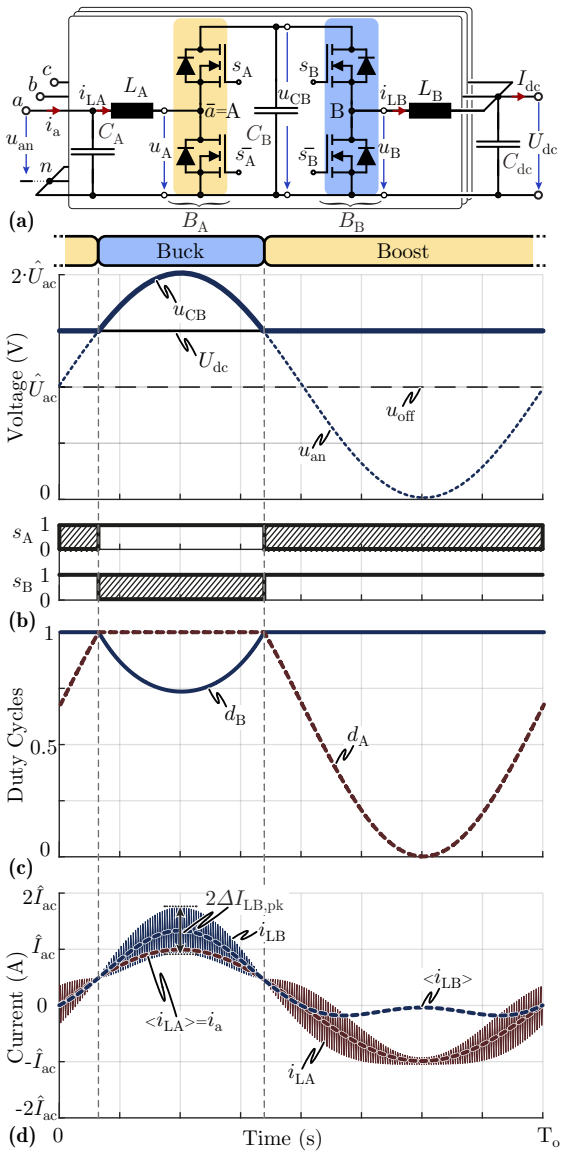

Fig. 3: **(a)** Circuit diagram of one PMC phase module, where the boost B_A and buck B_B half-bridge are highlighted. Corresponding waveforms **(b)** of the grid phase voltage u_an with offset voltage u_off and the intermediate DC link voltage u_CB with respect to the output DC voltage U_dc, as well as the gate signals s_A and s_B, **(c)** the duty cycles d_A and d_B, **(d)** the inductor currents i_LA and i_LB within one output period during boost ($U_\mathrm{dc} > u_\mathrm{an}$) and buck ($U_\mathrm{dc} \leq u_\mathrm{an}$) operation.

operation can be achieved by controlling the intermediate voltage to $u_\mathrm{CB}(t) = \max(u_\mathrm{an}(t), U_\mathrm{dc})$. This means that in cases where the instantaneous grid voltage u_an is smaller than the output voltage U_dc, i.e. in **boost operation**, the high-side switch of the buck half-bridge B_B is continuously turned-on (i.e. $u_\mathrm{CB} = U_\mathrm{dc}$) and only the boost half-bridge B_A is pulse width modulated such that the local average value $\langle u_\mathrm{A} \rangle$ is equal to the desired voltage u_an (neglecting the inductor voltage drop required for impressing a sinusoidal current i_LA). On the other hand, when $u_\mathrm{an} > U_\mathrm{dc}$, i.e. in **buck operation**, the boost half-bridge B_A high-side switch is continuously turned on (i.e. $u_\mathrm{CB} = u_\mathrm{an}$) and the buck half-bridge B_B is modulated (cf. **Fig. 3(b)**). Accordingly, the duty cycles d_A and d_B of the boost and buck stage can be derived directly from the input to output voltage ratio as

$$\left.\begin{aligned} d_\mathrm{A}(t) &= \min(1, m(t)) \\ d_\mathrm{B}(t) &= \min(1, m^{-1}(t)) \end{aligned}\right\} \in [0,1], \qquad (1)$$

with $m(t) = \frac{u_\mathrm{an}(t)}{U_\mathrm{dc}}$.

In **Fig. 3(c)** the time behavior of the duty cycles d_A and d_B within one output voltage period is shown and it reveals that the transition between boost and buck operation is completely seamless. The resulting current waveforms i_LA and i_LB of the filter inductors L_A and L_B are illustrated in **Fig. 3(d)**. As can be noticed, during **boost operation** when B_A is modulated, the switched voltage u_A is applied to the AC input filter, leading to an inductor current i_LA consisting of the fundamental grid current $\langle i_\mathrm{LA} \rangle = i_\mathrm{a}$ with a superimposed high-frequency (HF) current ripple $\Delta I_\mathrm{LA,pk} = \frac{1}{2}\frac{(1-d_\mathrm{A})u_\mathrm{an}}{f_\mathrm{A} L_\mathrm{A}}$. In contrast, at the output filter inductor L_B no HF voltage time area is generated by B_B since in this case the high-side switch of B_B is clamped and therefore only a low-frequency component, i.e. a fraction of the grid phase current, $i_\mathrm{LB} = d_\mathrm{A} \cdot i_\mathrm{a}$, is present. On the other hand, during **buck operation** when B_B is switched, the input inductor current $i_\mathrm{LA} = i_\mathrm{a}$ does not contain a switching frequency component. At the output side, however, i_LB consists of a local average current $\langle i_\mathrm{LB} \rangle = \frac{i_\mathrm{a}}{d_\mathrm{B}}$ strictly larger than the grid phase current combined with a HF current ripple $\Delta I_\mathrm{LB,pk} = \frac{1}{2}\frac{(1-d_\mathrm{B})U_\mathrm{dc}}{f_\mathrm{B} L_\mathrm{B}}$ due to the switching operation.

For the sake of completeness, it has to be mentioned, that the switching frequencies f_A and f_B of B_A and B_B do not necessarily need to be equal. This provides a further degree of freedom in selecting the current ripples $\Delta I_\mathrm{LA,pk}$ and $\Delta I_\mathrm{LB,pk}$ or for the dimensioning of the inductors L_A and L_B. Furthermore, the previously mentioned offset voltage does not have to be constant, but can be freely selected, as long as $u_\mathrm{an}(t) \geq 0, \forall t$ is fulfilled. Therefore harmonic injection techniques known from two-level rectifier and inverters can be implemented, such as 1/6 third harmonic injection [3] or Space Vector Modulation [10], [11] to mitigate component stresses or e.g. Discontinuous Pulse Width Modulation [12], where always the module with the lowest phase voltage is clamped to even further reduce the number of commutations and/or switching losses per grid fundamental period.

III. PMC Control Structure

Given the modular structure of the PMC, each phase can be controlled in the same way, therefore, the controller part specific to each phase is again only highlighted for module a, which is shown with the respective gate drive and measurement signals in **Fig. 4(c)**. The goal of the control system is to track the DC output voltage to its reference value, while maintaining sinusoidal AC currents in phase with the respective grid voltages. Thereby, the DC voltage control structure illustrated in **Fig. 4(a)** is based on the well known PFC rectifier control scheme, where the DC voltage controller $\mathrm{R}U_\mathrm{dc}$ translates the DC voltage error into the charging current demand of C_dc and from that calculates the needed output power P^* which has to be delivered from the three-phase mains input. Hence, based on this and the peak input voltage $\hat{U}_\mathrm{ac}$, the phase current references i_a^*, i_b^* and i_c^* proportional to the instantaneous mains phase voltages u_a, u_b and u_c can be deduced. Afterwards, the calculated phase current references and the mains phase voltages are fed to the PMC specific control part which is given for phase a in **Fig. 4(b)**. Under the assumption, that in a good approximation the input filter inductor current i_LA is equal to the grid current i_a (low-frequency component of the filter capacitor current neglected), the input current controller $\mathrm{R}i_\mathrm{LA}$ then processes the current control error Δi_LA into the inductor voltage reference u_LA^*, which together with the feedforward term u_an, i.e. the phase input voltage u_a including the offset voltage u_off present in all phases, yields the reference average

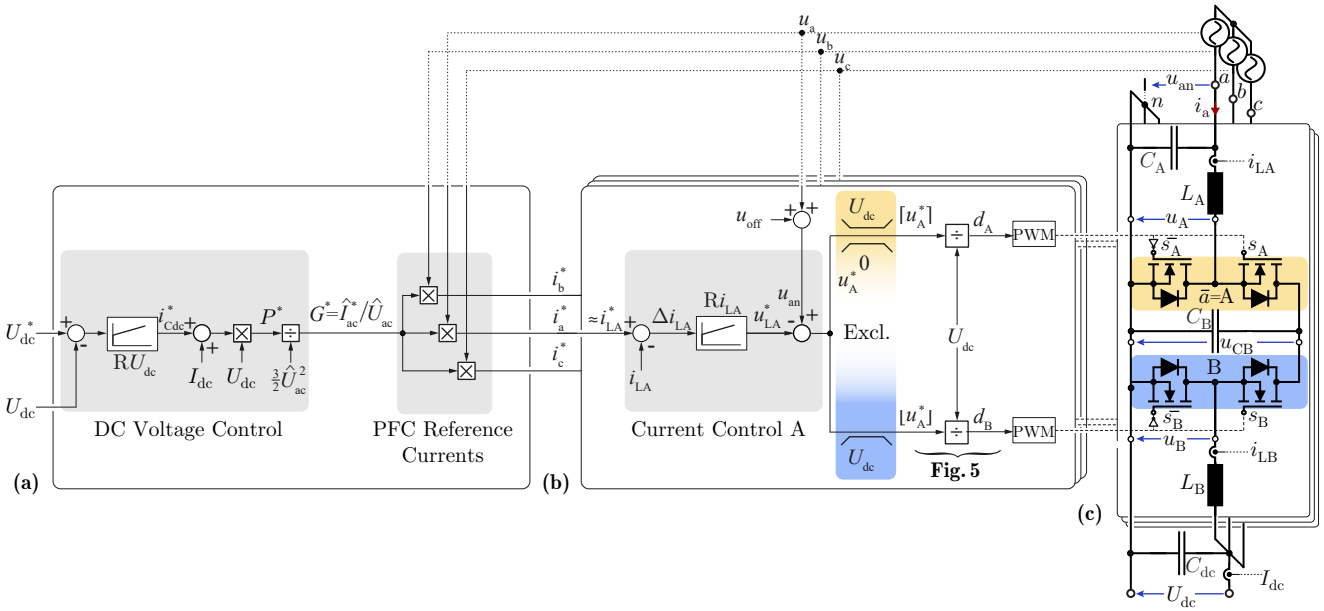

Fig. 4: Cascaded output voltage control structure of the PMC including **(a)** DC output voltage control and generation of (sinusoidal and/or mains phase voltage proportional) PFC phase current references, **(b)** mutually exclusive buck and boost control of phase a, where the duty cycles of stage A and B are calculated directly from the switched node voltage reference u_{A}^*, **(c)** converter power circuit diagram of phase a with gate signals and measurement points.

midpoint voltage u_{A}^* of the bridge-leg B_{A}.

Aiming for single-stage HF energy conversion, the instantaneous values of u_{A}^* (which is approximately equal to the phase voltage u_{an}) and the DC output voltage U_{dc} determine whether the phase module is operated in **boost** mode ($u_{\mathrm{A}}^* < U_{\mathrm{dc}}$ and high-side switch of B_{B} clamped while the grid input current is controlled by the switched node voltage u_{A}^*) or in **buck** mode ($u_{\mathrm{A}}^* \geq U_{\mathrm{dc}}$ and B_{A} clamped, while the grid side inductor current is controlled by means of the intermediate voltage u_{CB} regulated by B_{B}). In the simplest case, both duty cycles are calculated directly from the instantaneous values of u_{A}^* and U_{dc} to $d_{\mathrm{A}} = \lceil u_{\mathrm{A}}^* \rceil / U_{\mathrm{dc}}$ and $d_{\mathrm{B}} = U_{\mathrm{dc}} / \lfloor u_{\mathrm{A}}^* \rfloor$, where the two parallel limiters highlighted in **Fig. 4(b)** indicate the operation mode and assure that at any point in time one of the duty cycles is equal to one and the high-side switch of the respective half-bridge is clamped, yielding the mutually exclusive HF operation of the module half-bridges. In boost operation, this control strategy yields a very good reference tracking performance, as only one energy storage element is located between u_{an} and U_{dc} (as $u_{\mathrm{CB}} = U_{\mathrm{dc}}$), while with B_{B} clamped the remaining passive components act as a DC output filter. However, in buck operation, the additional energy storage elements (C_{B}, L_{B}) in between U_{dc} and u_{an} are not considered in the derivation of d_{B} and while in steady state the reference value can be tracked accurately, a reduced control performance in transient operation has to be accepted. If ultimate reference tracking performance is of interest, the derivation of the duty cycle d_{B} can be carried out employing a multi-cascaded structure with a dedicated control of the voltage u_{CB} of C_{B} and the current i_{LB} of L_{B} such that all energy storage elements of the converter module are considered in buck operation. Hence, the division used in Fig. 4(b) to derive d_{B} from u_{A}^* would be substituted by the control structure given in **Fig. 5**. However, as in boost operation B_{B} is clamped ($d_{\mathrm{B}} = 1$), with this control structure u_{CB} and i_{LB} cannot be controlled. If now a deviation of the reference values u_{CB}^* and i_{LB}^* establishes, the control error leads to an integration of the controller output and causes transient oscillations when entering buck mode again. To prevent this, the introduced buck mode controllers $\mathrm{R}u_{\mathrm{CB}}$ and $\mathrm{R}i_{\mathrm{LB}}$ are continuously reset in boost operation.

IV. COMPARATIVE EVALUATION

In the following, a detailed performance comparison of the PMC and PIC topology is conducted, where both systems feature the same terminal behavior but internally exhibit fundamentally different waveforms. As losses and volume of a power electronics system are typically determined by the semiconductor losses, and the heatsink as well as the inductor volume [13], a simplified comparison by means of indices based on the fundamental converter waveforms is conducted. Then, in a second step, a comprehensive multi-objective optimization comparison, where all relevant degrees of freedom and component characteristics are considered is presented. For both comparisons, a 10 kW rectifier application powered from the European three-phase LV mains ($\hat{U}_{\mathrm{ac}} = 325\,\mathrm{V}$) is assumed, where constant power has to be provided for a DC output voltage range of $U_{\mathrm{dc}} = [400, 600\,\mathrm{V}]$ which could not be covered by a single-stage boost- or buck-type system (cf. **Fig. 1(c)**).

A. Indices

The fundamental waveforms of a converter are independent from the selection of components and electric parameters (e.g. switching frequency, inductance values) and are resulting from the basic modulation scheme and yield some general requirements for the dimensioning of the components, as well as their volume and occurring losses. Therefore, indices for the inductor volume τ_{L} and the semiconductor losses are introduced, where due to the inherent trade-off between

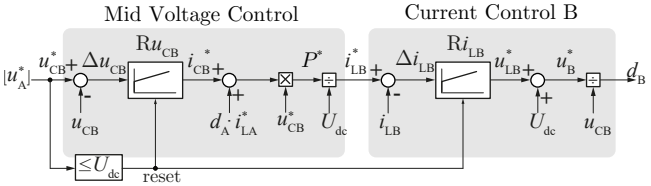

Fig. 5: Extended buck stage control circuit, where the passive elements C_{B} and L_{B} are also considered in the calculation of d_{B} in order to maximize the controller dynamics.

switching and conduction losses, the conduction loss τ_{C} and switching loss index τ_{S} are considered separately. Any voltage and current ripple due to the switched operation is neglected and for clarity only one phase module of the PMC is compared to a PIC single-phase equivalent converter (i.e. consisting of one AC phase and a DC/DC converter with $1/3$ rated power) and the occurring stresses in one fundamental period are summed up over the relevant components k (e.g. all half-bridges).

For a symmetric half-bridge, the inductor connected to the midpoint impresses an RMS current $\tilde{i}_{\mathrm{L}}$ that flows through either the high or low side switch and the total conduction losses are independent of the switching state and scale with the square of the inductor current, while in general the required semiconductor chip area and therefore the semiconductor cost also scale with τ_{C},

$$\tau_{\mathrm{C}} = \sum_{k} \tilde{i}^{2}_{\mathrm{L,k}}. \tag{2}$$

Neglecting the current ripple, there occurs one soft and one hard-switched transition in a PWM operated half-bridge during each switching period, where the latter clearly dominates the switching losses. As both the semiconductor voltage u_{T} and semiconductor current i_{T} influence the hard switching losses [14], the average value of the product $u_{\mathrm{T}} \cdot i_{\mathrm{T}}$ over a fundamental period T_{o} states a good measure to indicate switching losses. Obviously, clamped half-bridges do not contribute to the switching losses, as no switching transitions occur,

$$\tau_{\mathrm{S}} = \sum_{k} < u_{\mathrm{T,k}} i_{\mathrm{T,k}} >_{[\mathrm{T_o}]} . \tag{3}$$

The volume of an inductor can be estimated based on its area product [15] and scales for a given saturation flux and maximum conductor current density approximately with its inductance value L, as well as the RMS $\tilde{i}_{\mathrm{L}}$ and peak current $\hat{i}_{\mathrm{L}}$. Therefore the volume index τ_{L} is defined as

$$\tau_{\mathrm{L}} = \sum_{k} L_{\mathrm{k}} \hat{i}_{\mathrm{L,k}} \tilde{i}_{\mathrm{L,k}}. \tag{4}$$

While the relevant current values are considered to be independent of the switched operation, suitable inductance values have to be selected for each topology. A simple approach is to calculate L based on a worst case current ripple criterion. In this paper, for the calculation of L a switching frequency of $f_{\mathrm{s}} = 50\,\mathrm{kHz}$ and a maximum current ripple of $\Delta I = \pm 20\,\%$ relative to its peak fundamental value is selected. Furthermore, for the DC output side, the worst case current ripple occurs for both converters during maximum buck operation (i.e. $U_{\mathrm{dc}} = 400\,\mathrm{V}$) and at the AC input side for the PMC the maximum current ripple is obtained at maximum boost operation (i.e. $U_{\mathrm{dc}} = 600\,\mathrm{V}$), while for the PIC the AC-side current ripple remains unaffected by the DC output voltage due to the constant intermediate voltage U_{pn}. Hence, the following inductance values, $L_{\mathrm{DC}}(\mathrm{PIC}) = 307.7\,\mu\mathrm{H}$, $L_{\mathrm{AC}}(\mathrm{PIC}) = 396.1\,\mu\mathrm{H}$, $L_{\mathrm{DC}}(\mathrm{PMC}) = 230.8\,\mu\mathrm{H}$, and $L_{\mathrm{AC}}(\mathrm{PMC}) = 365.6\,\mu\mathrm{H}$ result.

The required filtering effort on the grid side can be compared for PIC and PMC by evaluating the emissions recorded by an EMI test receiver connected to a Line Impedance Stabilization Network (LISN), where for the given f_{s} and ΔI the first harmonic component above $150\,\mathrm{kHz}$ (according to *CISPR 11* [16], i.e. here the 4^{th} switching frequency carrier harmonic) and its side-bands within $\pm 4.5\,\mathrm{kHz}$ need to be considered for the worst case operating point (i.e. $U_{\mathrm{dc}} = 600\,\mathrm{V}$). According to [17] the filtering effort can be estimated based on the RMS $i_{\mathrm{eq,rms}}$ and peak $i_{\mathrm{eq,pk}}$

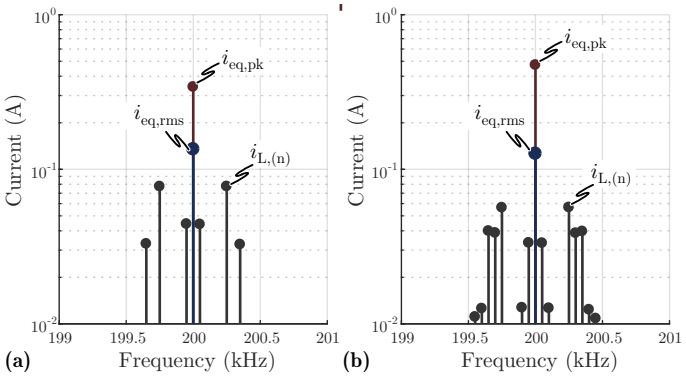

Fig. 6: Resulting spectrum around the first relevant harmonic component (i.e. 4^{th} carrier harmonic at $f_{\mathrm{s}} = 200\,\mathrm{kHz}$) as well as the equivalent currents for **(a)** PIC with $i_{\mathrm{eq,rms}} = 0.13\,\mathrm{Arms}$ and $i_{\mathrm{eq,pk}} = 0.34\,\mathrm{A}$, and **(b)** PMC with $i_{\mathrm{eq,rms}} = 0.13\,\mathrm{Arms}$ and $i_{\mathrm{eq,pk}} = 0.47\,\mathrm{A}$, where in both cases the sidebands decay by more than one order of magnitude within $\pm 1\,\mathrm{kHz}$.

equivalent currents defined as

$$i_{\mathrm{eq,rms}} = \sqrt{\sum_{f=195.5\,\mathrm{kHz}}^{204.5\,\mathrm{kHz}} i_{\mathrm{L}}(f)^2}, \quad i_{\mathrm{eq,pk}} = \sum_{f=195.5\,\mathrm{kHz}}^{204.5\,\mathrm{kHz}} i_{\mathrm{L}}(f). \tag{5}$$

The resulting spectrum around the first relevant carrier harmonic component at $200\,\mathrm{kHz}$ as well as the equivalent currents are shown for PIC and PMC in **Fig. 6(a)** and **(b)**, where in both cases the sidebands decay by more than an order of magnitude within $\pm 1\,\mathrm{kHz}$ and therefore the full EMI receiver measurement window of $\pm 4.5\,\mathrm{kHz}$ is not shown for conciseness. As for $U_{\mathrm{dc}} = 600\,\mathrm{V}$ the PMC is working mostly in boost operation, $i_{\mathrm{eq,rms}} = 0.13\,\mathrm{Arms}$ results for both PIC and PMC. The PIC spectrum consists of the expected odd fundamental harmonics around the even carrier multiple, while the partially discontinuous operation of the PMC causes additional sideband harmonics, such that an increased value of $i_{\mathrm{eq,pk}} = 0.47\,\mathrm{A}$ compared to $0.34\,\mathrm{A}$ for the PIC results in the linear summation. However, the difference in $i_{\mathrm{eq,pk}}$ is comparably small, as even a deviation by a factor of 2 would only require an additional attenuation of $-6\,\mathrm{dB}$ and would cause only a minor increase in the total filter volume, such that the simple inductor current ripple criterion can be considered suitable for a fair comparison amongst the two topologies.

Hence, the introduced indices allow to compare the fundamental differences of the PIC and the PMC, where for the sake of completeness also the *Y-Converter* (YC) [18], a second phase-modular approach with buck-boost instead of a boost-buck structure and a minimum number of three inductive components, is also included. The results of the indices based comparison are shown for the two extreme cases $U_{\mathrm{dc}} = 400\,\mathrm{V}$ and $U_{\mathrm{dc}} = 600\,\mathrm{V}$ for a separate analysis of DC-side and AC-side in **Fig. 7(a.i)** and **(b.i)**, where the points relevant for the inductor dimensioning are highlighted, as well as for the total converter system in **Fig. 7(a.ii)** and **(b.ii)**. The indices are normalized to the respective worst case value of the total PIC system occurring at $U_{\mathrm{dc}} = 400\,\mathrm{V}$ such that the PIC indices form a unity equilateral triangle in **Fig. 7(a.ii)**.

Focusing on the detailed analysis in **Fig. 7(a.i)** and **(b.i)** it can be noted in a first step that due to the constant high intermediate DC voltage U_{pn} of the cascaded PIC, its boost stage indices $\tau_{\mathrm{S,ac}}$, $\tau_{\mathrm{C,ac}}$ and $\tau_{\mathrm{L,ac}}$ are completely independent of U_{dc}, while the maximum stresses and index values on the for the buck stage occur for maximum buck operation (i.e. $U_{\mathrm{dc}} = 400\,\mathrm{V}$), especially due to the increased

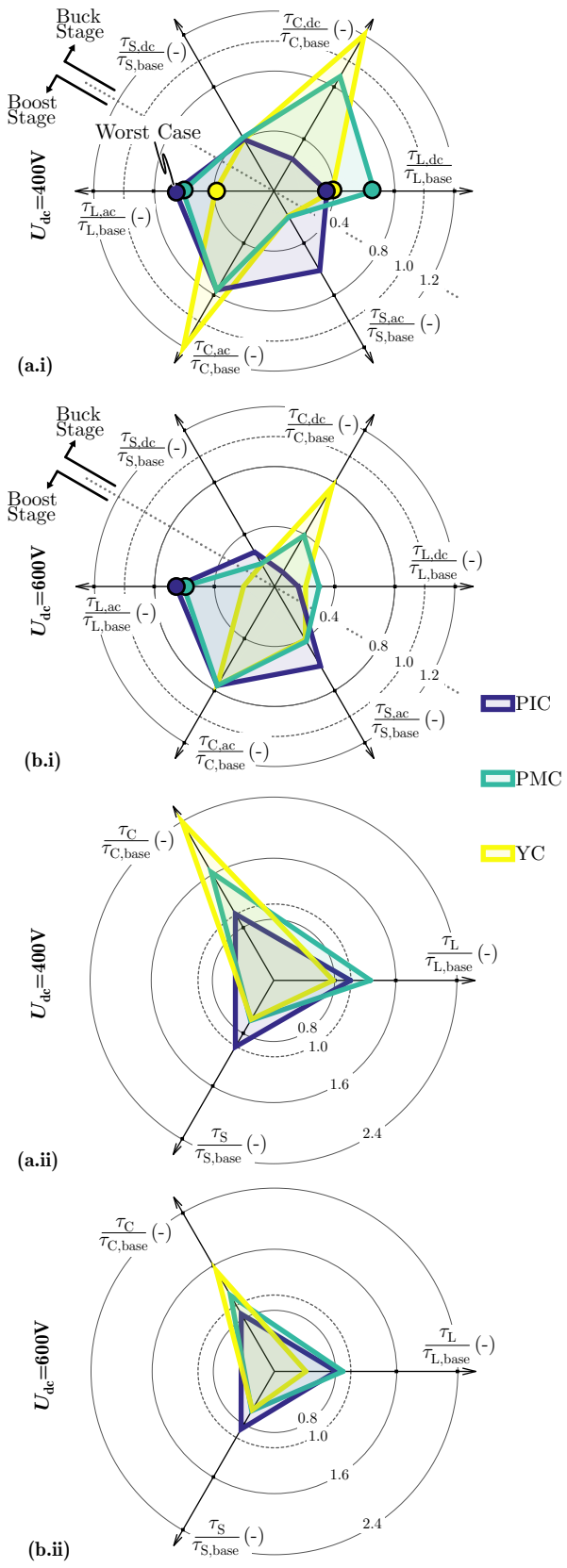

Fig. 7: Comparison of the indices of PIC, PMC and the phase-modular buck-boost YC evaluated for $P = 10\,\mathrm{kW}$ and a DC output voltage of **(a)** $400\,\mathrm{V}$ and **(b)** $600\,\mathrm{V}$, where in **(a.i)**,**(b.i)** the measures are illustrated for the converter parts of boost and buck stage separately and combined for the total converter in **(a.ii)**,**(b.ii)**. The index base values are given by the total PIC system and evaluate to $\tau_{\mathrm{L,base}} = 0.18\,\frac{\mathrm{Vs}}{\mathrm{A}}\mathrm{A}^2$, $\tau_{\mathrm{C,base}} = 283.36\,\mathrm{A}^2$, $\tau_{\mathrm{S,base}} = 13.75\,\mathrm{kVA}$.

DC output current given by the constant power operation. While the latter (i.e. maximum stresses for the buck stage for $U_{\mathrm{dc}} = 400\,\mathrm{V}$) is also true for the PMC, the discontinuous operation due to the single-stage energy conversion modulation strategy of the PMC causes a distribution of the stresses between the boost and buck converter stages depending on U_{dc}, where the boost stage indices are maximal for maximum boost effort (i.e. $U_{\mathrm{dc}} = 600\,\mathrm{V}$). This becomes most obvious when comparing the PMC switching stresses $\tau_{\mathrm{S,ac}}$ and $\tau_{\mathrm{S,dc}}$ for both voltage levels. However, as the same grid currents are impressed in the boost stage half-bridges of the PIC and PMC, an equal value in $\tau_{\mathrm{C,ac}}$ independent of U_{dc} and a slightly lower $\tau_{\mathrm{L,ac}}$ for the PMC (due to the smaller value of L_{AC}) establish. Then, on the DC-side the PMC suffers from increased current values, since the instantaneous power flowing on the AC-side and fluctuating with twice the mains frequency is transferred through both converter stages, where in contrast a DC current is transferring constant power to the DC/DC stage of the PIC, such that a substantially larger $\tau_{\mathrm{C,dc}}$ and also elevated values for $\tau_{\mathrm{L,dc}}$ result for the PMC compared to the PIC. The previously mentioned YC offers also single-stage energy conversion and exhibits equal switching stresses $\tau_{\mathrm{S,ac}}$ and $\tau_{\mathrm{S,dc}}$ as the PMC, while the combined buck and boost inductors (equally accounted to AC and DC-side) yield considerably lower values in $\tau_{\mathrm{L,ac}}$ and $\tau_{\mathrm{L,dc}}$ compared to the PMC. The main drawback of the YC results from the fact that the maximum system current is always impressed in both converter stages, yielding equal conduction stresses $\tau_{\mathrm{C,ac}} = \tau_{\mathrm{C,dc}}$ substantially above the values of the PIC and even the PMC.

Combining now the indices of buck and boost stage allows to compare the complete converter systems (cf. **Fig. 7(a.ii)** and **(b.ii)**), where one can observe that all system indices are maximal for $U_{\mathrm{dc}} = 400\,\mathrm{V}$ (i.e. maximum buck effort), while the overall picture (e.g. the phase modular approaches showing elevated conduction losses) remains unchanged for all DC output voltages. For $U_{\mathrm{dc}} = 400\,\mathrm{V}$ and compared to the cascaded PIC, the discontinuous modulation of both phase modular converters allows a reduction of τ_{S} by $40\,\%$, while τ_{C} increases by $63\,\%$ for the PMC and by $148\,\%$ for the YC. Finally, the index for the inductor volume τ_{L} reveals an inherent limitation of the PMC with respect to the converter volume, as the inductors on the DC- and AC-side have to be dimensioned for the respective worst case operating point and the expected limit in terms of τ_{L} is located $26\,\%$ above the limits of the cascaded PIC, while the YC profits from the reduced number of inductive components and exhibits a decrease in τ_{L} by $21\,\%$ and hence promises a very compact realization.

In closing, it can be stated that this simplified indices-based evaluation nicely illustrates the advantages and disadvantages of the different converter systems of interest. For a given switching frequency f_{s} and maximum peak current ripple ΔI, the PIC is showing the lowest current stresses τ_{C} enabling therefore a very cheap realization, the YC exhibits the minimal value in τ_{L} and therefore promises a very compact system and finally the PMC with a low value in τ_{S} and a moderate τ_{C} indicates that highest efficiency can be expected. It reveals that none of the three topologies is able to outperform its competitors in all aspects. In order to refine the evaluation a more elaborate comparison for the PIC and PMC is conducted in a next step.

B. Multi-Objective Optimization

Given the large number of degrees of freedom in the design of the converters, a multi-objective optimization comparison with respect to power density and efficiency between the two topologies is conducted, where also the component cost is evaluated for completeness. It is assumed that the buck stage and the boost stage of the PMC and PIC are effectively decoupled and therefore can be optimized separately. In order to further simplify the comparison, the converter optimization yields implementations which do not necessarily comply with e.g. *CISPR 11* regulations, but show a switched noise attenuation of $-40\,\mathrm{dB}$ on the AC-side, which implies a LC-filter resonance frequency located a decade below the switching frequency, while on the DC-side, a relative output voltage peak-to-peak ripple of $5\,\%$ is specified. For each converter stage, two electric degrees of freedom can be identified, namely the switching frequency f_s covering the inherent trade-off between switching losses and passive component volume, and the maximum peak inductor current ripple $(\pm)\Delta I$ (cf. **Section IV-A**) representing the ratio of inductive and capacitive component values. Combined with the constraints on resonance frequency and voltage ripple, f_s and ΔI fully define the electric component values of possible implementations, i.e. the converter design space, and a range of $f_\mathrm{s} \in [25, 300\,\mathrm{kHz}]$ and $\Delta I \in \pm[25, 200\,\%]$ is considered, where a value $\Delta I > 100\,\%$ implies complete soft-switching for the respective maximum ripple operating point.
The resulting semiconductor losses are calculated based on the theoretical waveforms (now including the voltage and current ripples due to switching operation) and a loss map for a $10\,\mathrm{m\Omega}$ $900\,\mathrm{V}$ SiC MOSFET [14], where a variable number of parallel switches $N_\mathrm{par} \in \mathbb{R}$ is assumed as the same technology is also available in devices with lower chip area (i.e. with higher $R_\mathrm{ds,on}$ and lower C_oss). The required heatsink volume is then approximated by assuming a *Cooling System Performance Index* [19] $\mathrm{CSPI} = 25{\cdot}10^3\,\frac{\mathrm{W}}{\mathrm{m^3K}}$. Inductive components are designed and evaluated according to [20] and different core geometries, air gap lengths, as well as round wire and litz wire are considered. Finally, only film capacitors were investigated which were assumed to be lossless in a good approximation (in fact, e.g. ceramic capacitor would introduce another tradeoff between volume and cost as they allow for a voltage of $650\,\mathrm{V}$ a realization of a given capacitance value with less than $10\,\%$ of the volume of a film capacitor, however at an increased cost by a factor of 7). The semiconductor and capacitor cost is calculated using the single component price of electronics distributors, while a cost model based on [21] was employed for the inductive components. In order to find converter designs compatible with the full voltage range, each stage is dimensioned for its respective worst case operating point in a first step and subsequently the resulting losses are evaluated for the whole output DC voltage range of the converter system. The average efficiency $\bar{\eta}$ obtained from the efficiencies η at nominal load across the DC output voltage range is of special interest, while the power density and cost are already given from the setup of each practical converter implementation.
Pareto optimal designs are then identified and the resulting limits in terms of power density and average efficiency of PIC and PMC are shown in **Fig. 8(a)**. It reveals that by changing from a phase-integrated to a phase-modular approach the average efficiency of the converter can be increased for any value of power density by up to $0.5\,\%$ and the maximally achievable power density of the PMC is slightly increased compared to the PIC, despite the fact that in general higher switching frequencies are required for

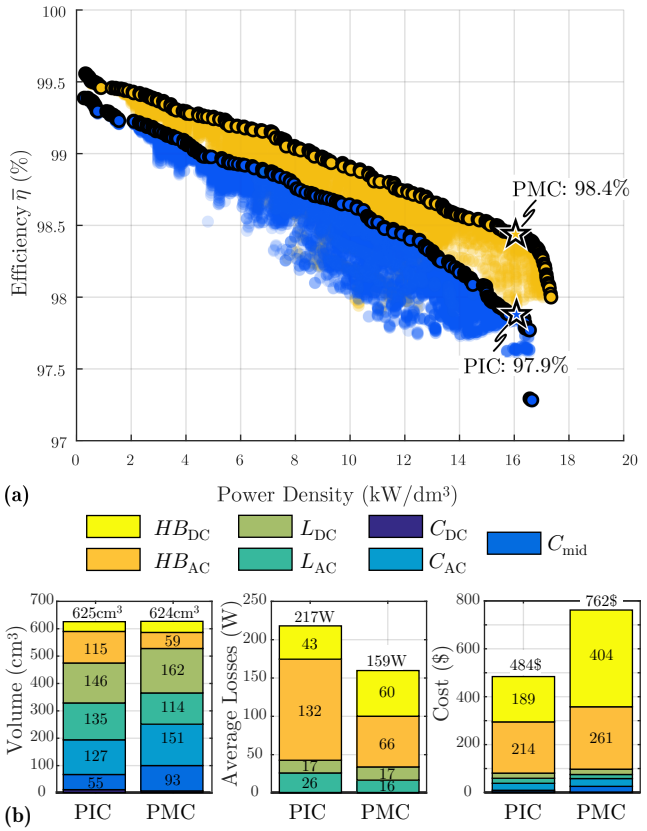

Fig. 8: **(a)** $\bar{\eta}\rho$-Pareto front of PIC and PMC for average efficiency $\bar{\eta}$ and power density, and **(b)** detailed average loss, volume and cost comparison for the indicated designs. The contributors are differentiated between boost stage and buck stage (AC- and DC-side) and are namely semiconductors including heatsink (HB), inductors (L) and capacitors (C).

the PMC in order to reach the same volume as the PIC. As the relative volume share of the heatsink increases with switching frequency, above $f_\mathrm{s,ac} = 175\,\mathrm{kHz}$ no additional gain in power density is possible for the PIC, while due to the alternating operation of the boost and buck stage, the PMC power density increases up to $f_\mathrm{s,ac} = 225\,\mathrm{kHz}$. Two designs with a boxed volume power density of $16\,\mathrm{kW/dm^3}$ are indicated and shown in detail in **Fig. 8(b)** with respect to the average loss, as well as volume and cost contribution of the converter components, where a total of $217.4\,\mathrm{W}$, $624.2\,\mathrm{cm^3}$ and $484.1\,\$$ for the PIC and $159.1\,\mathrm{W}$, $625.3\,\mathrm{cm^3}$ and $761.9\,\$$ for the PMC result, yielding a loss reduction of $27\,\%$ for the PMC. The highlighted PIC design employs $f_\mathrm{s,dc} = 175\,\mathrm{kHz}$ and a maximum $\Delta I_\mathrm{dc} = \pm 150\,\%$ ($L_\mathrm{dc} = 13.4\,\mu\mathrm{H}$) for the DC/DC buck converter which is accordingly completely soft-switched, while the PMC DC-side converter stage B_B is also soft-switched with a current ripple of $\Delta I_\mathrm{dc} = \pm 125\,\%$ ($L_\mathrm{dc} = 9.23\,\mu\mathrm{H}$) at an elevated switching frequency $f_\mathrm{s,dc} = 200\,\mathrm{kHz}$. However, the increase in switching frequency is not sufficient to compensate for the raised passive component count and the enhanced inductor area product and it can be observed in **Fig. 8(b)** that for the phase-modular approach the DC-side inductor and the heatsink, as well as the intermediate DC link capacitor C_mid (i.e. C_pn for the PIC and C_B for the PMC) consume relatively and in absolute numbers a larger share of the total converter volume, loss and cost. Then, the boost stages of both topologies are partially soft-switched in the proximity of the grid current zero crossing with equal current ripples $\Delta I_\mathrm{ac} = \pm 50\,\%$ and switching frequencies $f_\mathrm{s,ac} = 175\,\mathrm{kHz}$ yielding an inductance value of $L_\mathrm{ac} = 50.0\,\mu\mathrm{H}$ for the PIC and $L_\mathrm{ac} = 41.8\,\mu\mathrm{H}$ for the

PMC, where different inductance values result due to the elevated intermediate DC voltage U_{pn} of the PIC compared to the PMC. Almost an identical grid filter volume results for the PMC and the PIC, while the discontinuous operation of the PMC half-bridges allows to significantly reduce the average and worst case semiconductor as well as the HF inductor losses, such that a reduced heatsink volume results and the additional volume and losses of the buck converter stage can be compensated. As discussed in **Section IV-A**, the PMC exhibits increased current stresses on the DC-side which combined with the discontinuous operation yields a larger optimal chip area in order to minimize the total semiconductor losses and the PMC shows therefore a rise in chip cost of $214\,\%$ for the buck stage and of $122\,\%$ for the boost stage which clearly dominates the overall system costs. However, it must be mentioned again that with the PMC the losses are reduced by more than one quarter, which on the other hand especially at such high efficiencies (above $98\,\%$) demands large chip areas and/or results in strongly increasing costs. Therefore, a fair cost comparison can only be performed for systems with same efficiency and power density. Obviously, selecting for the PMC a non Pareto-optimal design, the PMC system cost can be reduced by employing less chip area and accepting higher average losses, and when comparing two designs of equal efficiency $\bar{\eta} = 98\,\%$ and power density $\rho = 16\,\mathrm{kW/cm^3}$ the difference in cost decreases, i.e. the PMC is only $14\,\%$ less cost-effective than the PIC. Furthermore it must be stated that considering the clear trend towards decreasing prices for the relatively new wide bandgap SiC MOSFETs (today SiC MOSFETs are more than three times more expensive than Si devices), the cost difference between PIC and PMC can be further decreased in the future and the PMC could even outperform the PIC converter especially if instead of an average efficiency across the complete voltage range also other voltage and/or load profiles are considered. Finally, due to the modular setup, the PMC also offers more options concerning modularity and scalability (which in turn also reduces costs), where not only all phase modules are equal but also the buck stage and the boost stage are realized with the same components and are used in a back-to-back configuration.

V. Conclusion

In this paper, a new phase-modular bidirectional three-phase boost-buck DC/AC converter system is introduced, which is an alternative to the combination of a AC/DC boost-type voltage source rectifier and a DC/DC buck converter. The three independent phase modules with individual variable intermediate DC link voltages allow to limit the modulation to one half-bridge at a time in each phase, such that single-stage energy conversion and therefore a higher converter efficiency is enabled. A control structure for PFC rectifier operation was provided and discussed in detail, where a smooth transition between boost and buck operation was verified by means of a closed loop simulation for various operating conditions. A detailed Pareto comparison between the proposed and the conventional topology shows a reduction of the overall converter losses by $27\,\%$ at an equal power density of $16\,\mathrm{kW/dm^3}$. Furthermore, a slightly higher maximum power density can be achieved. However, the improved efficiency of the PMC demands more semiconductor chip area which combined with the increased component count causes elevated total system costs, while for equal efficiency very similar costs results for both topologies. Also, given the trend of decreasing SiC MOSFET prices, the difference in the system costs between PIC and PMC can be expected to decrease in the near future. Furthermore, the modular structure of the PMC shows additional advantages with respect to the scalability as it can be built out of six identical converter stages, yielding not only less design effort but potentially also reduced component costs. Also, in case of a single-phase failure only one module has to be replaced, yielding reduced maintenance cost. Therefore, a further investigation of the PMC approach and an implementation in hardware is very promising.

References

[1] O. Tremblay, L. A. Dessaint, and A. I. Dekkiche, "A generic battery model for the dynamic simulation of hybrid electric vehicles," in *Proc. of the IEEE Vehicle Power and Propulsion Conference*, Sept. 2007, pp. 284–289.

[2] J. W. Kolar and T. Friedli, "The essence of three-phase pfc rectifier systems−part i," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 176–198, Jan. 2013.

[3] J. A. Houldsworth and D. A. Grant, "The use of harmonic distortion to increase the output voltage of a three-phase pwm inverter," *IEEE Transactions on Industry Applications*, vol. IA-20, pp. 1224–1228, 1984.

[4] D. Elizondo and A. Urtasun, "Dual-mode soft-transition control for single-phase grid-connected photovoltaic inverters," in *Proc. of the 19th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2018.

[5] W. Wu and F. Blaabjerg, "Aalborg inverter - a new type of "buck in buck, boost in boost" grid-tied inverter," in *Proc. of the 28th IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2013, pp. 460–467.

[6] N. A. Ahmed, H. W. Lee, and M. Nakaoka, "Dual-mode time-sharing sinewave-modulation soft switching boost full-bridge one-stage power conditioner without electrolytic capacitor dc link," *IEEE Transactions on Industry Applications*, vol. 43, no. 3, pp. 805–813, May 2007.

[7] Z. Zhao, M. Xu, Q. Chen, J. S. Lai, and Y. Cho, "Derivation, analysis, and implementation of a boost-buck converter-based high-efficiency pv inverter," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1304–1313, Mar. 2012.

[8] W. Wu, H. Geng, P. Geng, Y. Ye, and M. Chen, "A novel control method for dual mode time-sharing grid-connected inverter," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 2010, pp. 53–57.

[9] W. Wu and T. Tang, "Dual-mode time-sharing cascaded sinusoidal inverter," *IEEE Transactions on Energy Conversion*, vol. 22, no. 3, pp. 795–797, Sept. 2007.

[10] K. Kovàcs, I. Ràcz, and H. Theil, *Transiente Vorgänge in Wechselstrommaschinen (in German)*. Verlag der Ungarischen Akademie der Wissenschaften, 1959.

[11] G. Pfaff, A. Weschta, and A. F. Wick, "Design and experimental results of a brushless ac servo drive," *IEEE Transactions on Industry Applications*, vol. IA-20, no. 4, pp. 814–821, Jul. 1984.

[12] K. Taniguchi, Y. Ogino, and H. Irie, "Pwm technique for power mosfet inverter," *IEEE Transactions on Power Electronics*, vol. 3, no. 3, pp. 328–334, Jul. 1988.

[13] M. Antivachis, D. Bortis, D. Menzi, and J. W. Kolar, "Comparative evaluation of y-inverter against three-phase two-stage buck-boost dc-ac converter systems," in *Proc. of the IEEE International Power Electronics Conference (IPEC - ECCE Asia)*, May 2018.

[14] J. A. Anderson, C. Gammeter, L. Schrittwieser, and J. W. Kolar, "Accurate calorimetric switching loss measurement for 900v 10mΩ sic mosfets," *IEEE Transactions on Power Electronics, vol. 32, no. 12*, Dec. 2017.

[15] C. W. T. McLyman, *Magnetic Core Selection for Transformers and Inductors: A User's Guide to Practice and Specifications*. CRC Press, 1997.

[16] *C.I.S.P.R., Industrial, Scientific and Medical (ISM) Radio-Frequency Equipment - Electromagnetic Disturbance Characteristics - Limits and Methods of Measurement*, International Electrotechnical Commission (IEC) Std.

[17] T. Nussbaumer, M. L. Heldwein, and J. W. Kolar, "Differential mode input filter design for a three-phase buck-type pwm rectifier based on modeling of the emc test receiver," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1649–1661, Oct. 2006.

[18] M. Antivachis, D. Bortis, L. Schrittwieser, and J. W. Kolar, "Novel buck-boost inverter topology for fuel-cell powered drive systems," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2018.

[19] U. Drofenik, G. Laimer, and J. W. Kolar, "Theoretical converter power density limits for forced convection cooling," in *Proc. of the Intern. Power Conversion and Intelligent Motion Conference (PCIM Europe)*, Jun. 2005, pp. 608–619.

[20] P. Papamanolis, F. Krismer, and J. W. Kolar, "Minimum loss operation of high-frequency inductors," in *Proc. of the 33rd Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2018.

[21] R. Burkart and J. W. Kolar, "Component cost models for multi-objective optimizations of switched-mode power converters," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 2013, pp. 2139–2146.