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***Abstract*—With the deployment of PV energy generation increasing, the need to optimize efficiency of the power conversion from the PV panel to the AC grid while minimizing the material effort and the realization cost has gained significant importance. Accordingly, this paper presents a 12.5 kW 99.35 % efficient three-phase inverter using commercially available low-voltage silicon power semiconductors. A hybrid seven-level topology is employed, with each phase comprising an Active Neutral Point Clamped (ANPC) front-end connected to a Flying Capacitor Converter (FCC) stage, which leads to a low overall volume and weight, i.e. a volumetric power density of 3.4 kW/dm^3 (55.9 W/in^3) and a gravimetric power density of 3.2 kW/kg. Additionally, this topology shows a smaller capacitance requirement and consists of less switches than the conventional FCC topology. Finally, a comprehensive optimization shows that with the next generation of 200 V silicon devices it is feasible to achieve a peak efficiency of 99.5 %.**

***Index Terms*—Multi-level, Hybrid Active Neutral Point Converter, Ultra-high efficiency, PV inverter, Flying Capacitor Converter.**

I. Introduction

Due to the massive deployment of photovoltaic (PV) systems in China in recent years, the renewable energy production is constantly breaking records [1]. In 2017, PV energy generation contributed 7.2 % of the net electricity supply in Germany, where on sunny weekends and holidays it can reach up to 50 % of the instantaneous electric energy supply [2]. Hence, there is a clear incentive to drive research towards high performance power electronics inverters that can support the renewable energy growth, with more efficient, more power dense, light weight and cost effective solutions [3,4]. For PV systems with high capacity factors, which are in operation for many hours a day, a high energy conversion efficiency is of major importance. With the goal of exploring the efficiency limits, this paper presents an ultra-efficient multi-level three-phase inverter solution for a typical PV installation, as conceptually shown in **Fig. 1,** targeting a peak efficiency of up to 99.5 % for a nominal power of 10 kW.

When aiming for ultra-efficient converters, the trade-off with respect to losses and volume between active (power semiconductors) and passive (magnetic and capacitive) components has to be evaluated in detail. As typically three-phase converters are hard-switched, there is an optimum

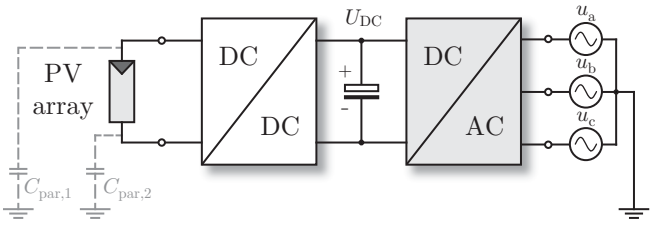

Fig. 1. System overview for transformerless PV power transfer into the low-voltage three-phase grid (400 V_{rms}, line-to-line), where the PV array is typically followed by a DC/DC converter for maximum power point tracking and a three-phase PWM inverter (highlighted), which is the subject of this paper.

between conduction and switching losses that favors large die areas and low switching frequencies [5]. However, low switching frequencies lead to bulky magnetics, which can be solved by the use of multi-level topologies like the Flying Capacitor Converter (FCC), illustrated in **Fig. 2(a)** for seven levels. Multi-level converters reduce the inductance requirement of the AC-side inductors for a given current ripple amplitude quadratically with respect to the number of levels, due to the multi-level output voltage characteristic and the increase of effective switching frequency, leading to smaller and more efficient magnetic components [6,7]. Additionally, multi-level converters take advantage of employing low-voltage power MOSFETs which have a higher hard-switching Figure of Merit (FOM) compared to high-voltage power semiconductors [8]. To achieve a multi-level output voltage characteristic with an FCC, capacitors carrying an integer multiple of the lowest cell voltage are alternatingly connected to the output during operation. However, the capacitance requirement for the Flying Capacitors (FCs), driven by the need to constrain the switching frequency voltage ripple across the capacitors, is directly proportional to the load current (and hence, output power) and inversely proportional to the switching frequency [6]. Ultra-high power densities can be achieved at a cost of efficiency, by using high switching frequencies (in the hundreds of kHz) that favor the utilization of ceramic capacitors with high energy density [9,10]. However, as already mentioned, ultra-efficient hard-switching converters designed for high power ratings

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TABLE I
INVERTER SPECIFICATIONS

P_{nominal}	10 kW
$P_{\text{rated,max}}$	12.5 kW
$U_{\text{dc,nominal}}$	720 V
U_{ac}	400 V_{rms}
f_{mains}	50 Hz
EMI Filter Requirement	Class A

are typically operated at a low switching frequency (low tens of kHz) [11,12]. These low switching frequencies lead to higher capacitance requirements of the FCs, which gives a clear incentive to research alternatives to the FCC approach that offer multi-level voltage characteristics with a smaller capacitance demand. A topology that allows to reduce by more than half the number of capacitors is presented in [13,14], where a hybrid approach between the Active Neutral Point Clamped (ANPC) converter and the FCC is proposed (cf. **Fig. 2(b)**), which hereafter is referred to as the Hybrid Active Neutral Point Clamped (HANPC) converter. This topology, besides reducing the number of capacitors, saves additional volume as only the capacitors with the lowest voltages remain. This is advantageous, since the higher the voltage rating of the capacitors, the lower the capacitance density, and hence, the more the capacitors that have to be arranged in parallel and/or series, as can be seen e.g. for a thirteen-level FCC in [15]. These characteristics of the HANPC converter allow to achieve a higher power density for ultra-efficient converters than with a FCC, in particular for 10 kW range three-phase inverters targeting 99.5 % efficiency [6].

Therefore, this paper focuses on the hardware realization of an all-silicon ultra-efficient passively-cooled 12.5 kW three-phase seven-level HANPC (7L-HANPC) inverter, achieving a peak efficiency of 99.35 % and a power density of 3.4 kW/dm^3 (55.9 W/in^3). Firstly, the principle of operation of the HANPC converter is reviewed in **Section II**, secondly a design optimization is presented in **Section III** for the specifications given in **Table I**, thirdly, the hardware design and the measurement results are presented in **Section IV**, and finally the paper is concluded in **Section V**.

II. PRINCIPLE OF OPERATION OF THE HANPC

Each bridge leg of the HANPC inverter, illustrated in **Fig. 2(b)** for seven levels, consists of two cascaded stages: the ANPC stage connected to the DC input voltage and the FC stage finally generating the AC output voltage. The ANPC stage switches ($T_{1...4}$) connect the points I and II for positive output voltages $u_i > 0$ to the positive DC-link voltage rail (DC+) and the DC-link midpoint M respectively, and to M and the negative DC-link voltage rail (DC-) for $u_i < 0$. This results in grid frequency operated ANPC stage switches, as shown in **Fig. 3**, that have to be rated to withstand $U_{\text{DC}}/2$. Following, there is a FC stage (a four-level FC stage in **Fig. 2(b)**), whose semiconductors are operated at switching frequency using phase shifted PWM, and have to be rated for $U_{\text{DC}}/6$. A detailed analysis of the modulation and switching states of the HANPC converter can be found in [14,16,17].

The fundamental difference between the HANPC converter and the FCC structure is that by actively clamping the FC

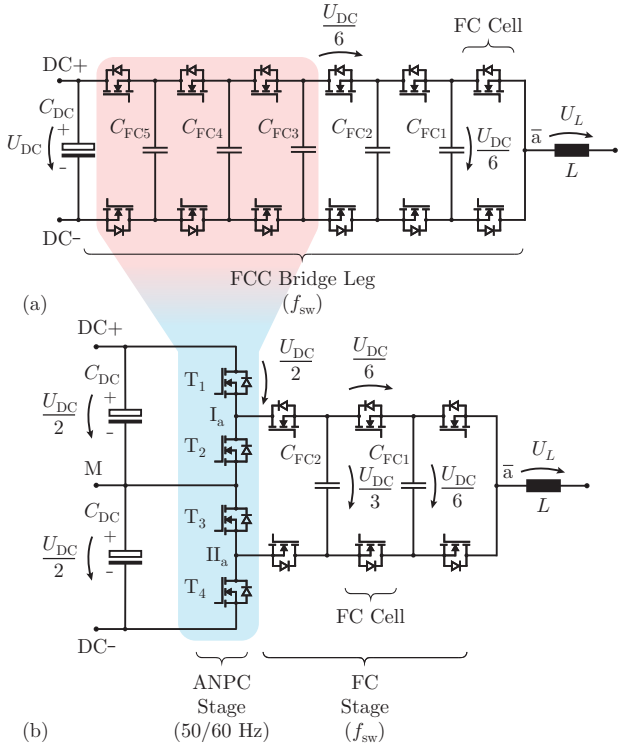

Fig. 2. Topology of a 7L-FCC bridge leg, which is purely composed of low-voltage semiconductors operated at switching frequency **(a)** and the 7L-HANPC bridge leg structure, which is a hybrid approach composed of an ANPC stage with semiconductors switching at 50/60 Hz, and a FC stage, with semiconductors operating at switching frequency **(b)**; both arrangements are shown for phase a of the three-phase (phases a, b, c) inverter topology.

stage to either the high-side or the low-side of the DC-link, the same number of levels can be obtained with a HANPC converter compared to a FCC. For the HANPC converter, the number of levels is given by

$$N_{\text{lev,HANPC}} = 2 \cdot N_{\text{FCcell}} + 1 \ , \tag{1}$$

where N_{FCcell} is the number of FC cells, whereas for the FCC bridge leg the number of levels is

$$N_{\text{lev,FCC}} = N_{\text{FCcell}} + 1 \ . \tag{2}$$

From Eqs. (1) and (2) it can be seen that the HANPC converter needs half the FC cells compared to the FCC to generate the same number of levels. For the case shown in **Fig. 2**, both the FCC and HANPC converter produce a seven-level voltage output, but for the FCC the output number of cells is $N_{\text{FCcell}} = 6$, and for the HANPC converter $N_{\text{FCcell}} = 3$ is implemented.

The effective switching frequency applied to the AC-side inductor and/or filter stage, which affects the filter design, losses and volume, is $f_{\text{sw,eff}} = N_{\text{FCcell}} \cdot f_{\text{sw}}$, with f_{sw} being the switching frequency of the individual stages. The difference in N_{FCcell} between both topologies however, has a minor effect on the effective switching frequency as will be made visible by the following qualitative analysis: if it is assumed that there is a certain loss budget allocation

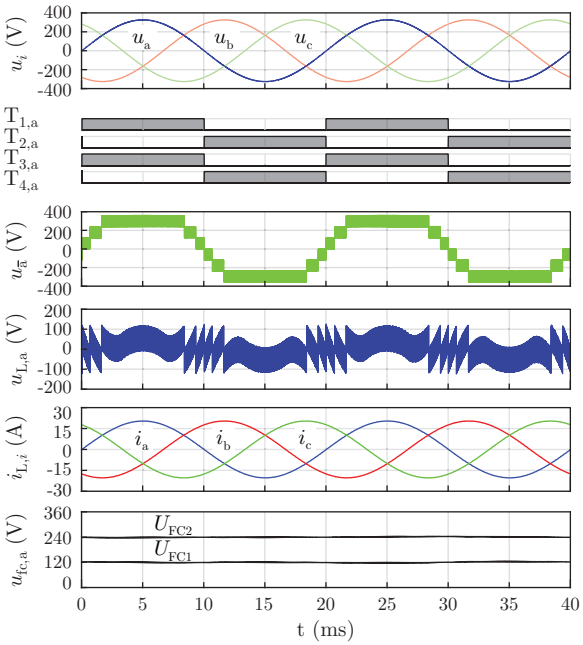

Fig. 3. Main waveforms of the 7L-HANPC inverter (cf. **Fig. 2(b)** and **Fig. 5**): mains phase voltages, gate signals for the ANPC stage switches of phase a, multi-level voltage output of node ā (cf. **Fig. 2(b)**) referenced to the DC midpoint and filter inductor (L) voltage waveform of phase a, grid phase currents, and FC voltages of phase a. A third harmonic component is superimposed in the modulation to reduce the low-frequency component of the DC-link midpoint current, with an amplitude of one fourth of the phase output voltage.

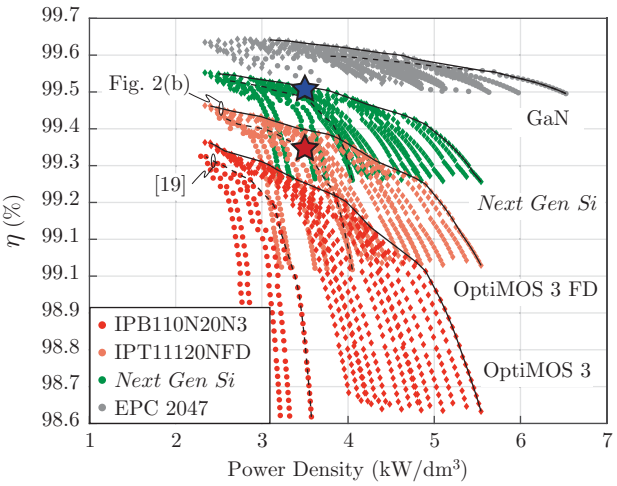

Fig. 4. Pareto optimization results for the different considered semiconductor devices and realizations of the ANPC stages. Results for the ANPC stage with 31 mΩ 600 V *CoolMOS CFD7* (*Infineon*) are shown with rhombi and continuous black Pareto lines, and the results for a quasi-three-level variant (series connection of the same low-voltage MOSFETs that are used for the FC stage in each case) [19] of the ANPC stage are shown with circles and dashed black Pareto lines. The efficiency is calculated at the operating point of 10 kW of the three-phase system, where the hardware prototype presented in this paper is represented by a red star (four parallel devices for each switch of the ANPC stage), and the achievable performance with *next generation* 200 V silicon switches (estimation resulting from an extrapolation of recent FOM improvement) is shown by a blue star (six parallel devices for each ANPC stage switch).

for the power semiconductors of the converter, and that for optimizing semiconductor losses the die areas of the switches are chosen such that the conduction losses and hard-switching losses are similar [5,18], then the FCC can be designed to have approximately equal conduction losses and switching losses. To adapt the design to the HANPC converter, following **Fig. 2**, if the conduction losses of half the FC cells of the FCC stage are chosen to be the same as the conduction losses of the ANPC stage switches, which are switching at line frequency and hence have negligible switching losses, then the avaiable budget for the switching losses of the FC stage of the HANPC converter is equal to that of the six cells of the FCC. Therefore, the last three HANPC FC cells can switch at twice the switching frequency of their FCC counterpart switches, hence imposing the same effective switching frequency on the filter stage. Following the same argumentation, the dimensioning of the capacitance of the FCs remains similar [6,9], since the product of $N_{\text{FC,cell}}$ and f_{sw} remains similar,

$$C_{\text{FC,min}} = \frac{I_{\text{ac,pk}}}{N_{\text{FCcell}} f_{\text{sw}} \Delta U_{\text{FC,max}}} \ , \tag{3}$$

where $I_{\text{ac,pk}}$ is the peak AC current, and $\Delta U_{\text{FC,max}}$ the maximum peak-to-peak FC voltage ripple allowed.

The main waveforms of the 7L-HANPC inverter are shown in **Fig. 3** for an AC-side, i.e. output filter structure with the star-point of the filter capacitors connected to the DC-link midpoint (cf. **Fig. 5**). The seven output voltage levels together with the voltage applied to L_1 are shown, as well as the grid phase currents and the FC voltages, which are naturally balanced using phase shifted PWM [20]. Finally, it has to be mentioned that as for all NPC converters, a DC-link voltage difference arises due to a DC-link midpoint current which has a dominant third harmonic component [21]. This can however be reduced by either superimposing a third harmonic to the modulation in such a way that the amplitude of the low-frequency part of DC-link midpoint current is minimized, or by increasing the DC-link capacitance [16,22].

III. Design Optimization

To evaluate the most suitable component selection for the final hardware demonstrator, a comprehensive optimization of the 7L-HANPC inverter is performed. The optimization routine is conducted following the converter dimensioning guidelines presented in [6], where for the FC stage, four different types of switches are considered, switching in a frequency range between 10 kHz and 40 kHz: two commercial 200 V silicon *OptiMOS 3* devices (*Infineon*), a virtual prototype of a *next generation* 200 V silicon device (*Infineon*), for which confidential data has been provided by the manufacturer, and GaN power seminconductors of type *EPC2047* (*EPC*). For the ANPC stage however, both 600 V *CoolMOS CFD7* switches (*Infineon*) and a series-connection

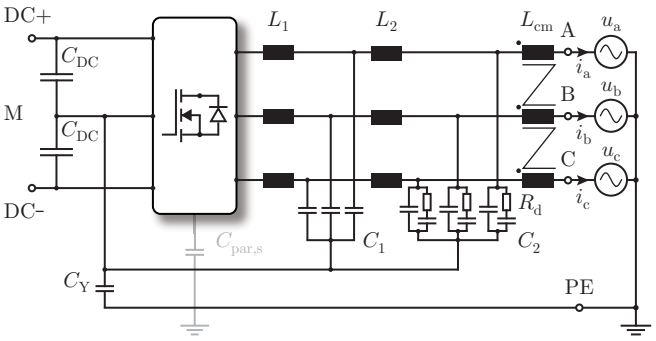

Fig. 5. EMI filter structure of the final prototype, with two L-C filter stages attenuating DM and CM components of the output voltages of the inverter bridge legs (with reference to the DC voltage midpoint) and a CM choke placed before the grid connection.

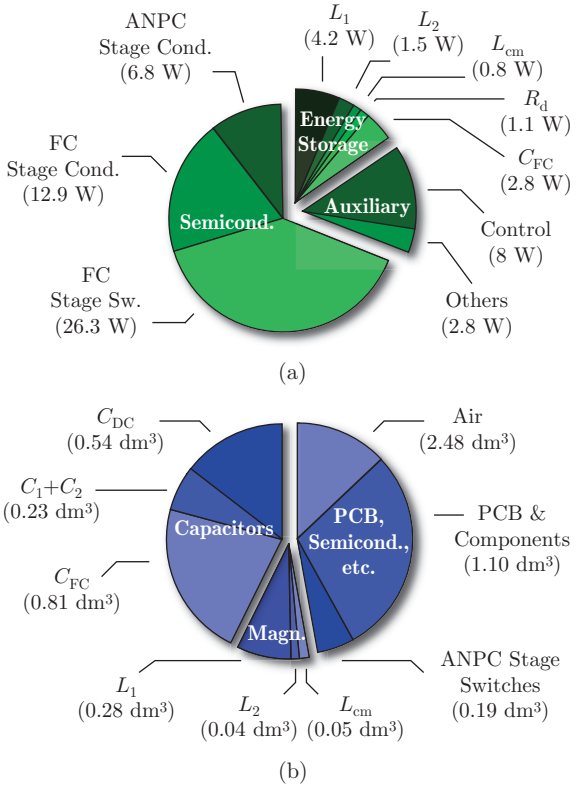

Fig. 6. Loss **(a)** and volume **(b)** distribution of the realized hardware (cf. **Fig. 7**), where the loss breakdown is shown for operation at 10 kW.

of the same low-voltage switches as used in the FC stage are considered in a quasi-three-level configuration as proposed in [19], where essentially each 600 V switch of the ANPC bridge leg is replaced by three 200 V switches connected in series. To comply with the International Special Committee on Radio Interference (CISPR) 11 Class A standard [23] on the AC-side, a n-stage L-C EMI filter structure is considered in the optimization routine ($n \in \{1,2,3\}$), which simultaneously attenuates Differential-Mode (DM) and Common-Mode (CM) noise [24] as the filter stages are referenced to the DC midpoint (cf. **Fig. 5**). For the filter inductor L_1, nanocrystalline cores with helical windings are used in order to reduce the losses [11], whereas for the further stage inductors (L_2, cf. **Fig. 5**) commercially available inductors are considered. Since low losses can be achieved with the L-C structure (cf. **Fig. 6**), a separation of the filter into dedicated DM and CM stages which would increase the component count is not considered.

Given the efficiency barriers obtained for different semiconductor technologies (indicated with Pareto curves in **Fig. 4**), for the final design the all-silicon approach shown with a red star is chosen, since the calculated efficiency difference between the commercially available silicon devices and GaN devices is only 0.2 % for the same power density, which with the introduction of the *next generation* silicon devices, is expected to be reduced to 0.1 %. Regarding the ANPC stage configuration, the optimization results shown in **Fig. 4** yield that using 600 V switches for the ANPC stage (solid line Pareto front) offers superior performance both in terms of efficiency and power density compared to the quasi-three-level variant of series-connected 200 V devices (dashed line Pareto front). Hence, the design that is chosen for the hardware demonstrator reserves place for up to six parallel connected 31 mΩ *CoolMOS CFD7* devices for the ANPC stage, and two parallel 11.1 mΩ *IPT111N20NFD* devices switching at 16 kHz, resulting in an effective switching frequency of 48 kHz for the filter stage. It has to be noted that for the case of the 600 V switches, the more switches connected in parallel, the lower the losses (negligible switching losses at grid frequency), however, at the price of increased cost and volume. Hence, in this optimization a limit of six paralleled switches is considered for the ANPC switches. The loss distribution of the selected design for the realized hardware demonstrator is shown in **Fig. 6(a)** for a power of 10 kW, where it can be observed that the semiconductors account for 68 % of the total converter losses, out of which 85 % are caused by the FC switches. The resulting contribution of the magnetic components to the loss and volume distributions is in the range of 10...15 %, since with the relatively high output effective frequency and the multi-level output voltage waveform, only a small voltage-time area is applied to the inductors.

The final filter structure comprises two L-C filter stages, whose star point is connected to the midpoint to provide a return path for the CM current, as shown in **Fig. 5.** To further mitigate the effects of the unavoidable parasitic capacitance from the switching stage $C_{par,s}$ to ground, an additional CM-choke is placed and a Y-rated capacitor C_Y is connected between earth (PE) and the DC-link midpoint. Finally, R-C damping is provided in the second filter stage with damping resistors R_d similar to [12], in order to avoid larger damping losses that would arise due to the switching voltage ripple if damping the first stage.

The volume distribution of the hardware is given in **Fig. 6(b)**, where it can be seen that the capacitors are the main volume contributors. The FC capacitance is dimensioned by the minimum capacitance requirement that is obtained by imposing a maximum switching frequency ripple of the FC voltage (see Eq. (3)), limited here to $\Delta U_{FC,max} = 5$ V. Given the low switching frequency and high output current, the capacitance requirement is large (107 µF

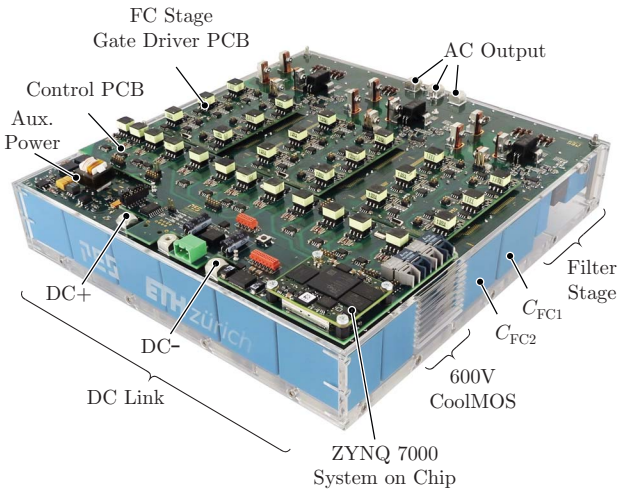

Fig. 7. Hardware prototype of the 12.5 kW three-phase 7L-HANPC inverter, measuring 256 mm × 269 mm × 53 mm (10.1 in × 10.6 in × 2.1 in). The final volumetric power density is 3.4 kW/dm^3 (55.9 W/in^3), and the gravimetric power density is 3.2 kW/kg.

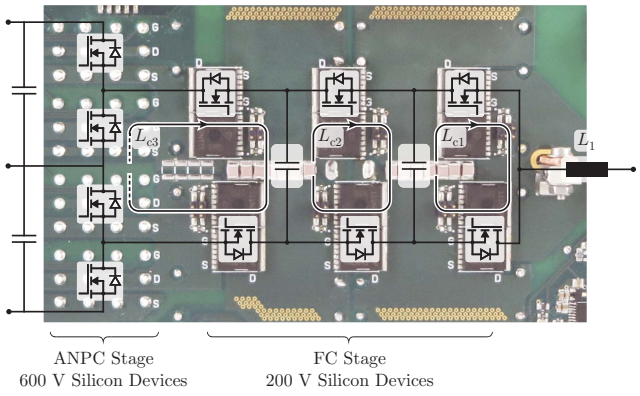

Fig. 8. Realization of the hardware layout of a three-phase 7L-HANPC inverter bridge leg, where the FCs (film-type) are placed underneath the PCB, and ceramic capacitors are placed on top to improve the switching behavior of the MOSFETs. The commutation loop introduced by the connection the FC stage to the HANPC stage L_{c3} is the most critical.

for capacitors which operate at nominal voltages of 120 V and 240 V), for which film capacitors are chosen to avoid the need of having to parallel-connect ≈ 200 capacitors per FC, which would also lead to an approximate price increase of × 15 of the capacitors. However, for converters with a lower power rating (and lower load currents) and higher switching frequencies, ceramic capacitors are more suitable, since a higher volumetric energy density can be achieved [9,15,25,26].

IV. Hardware Implementation and Measurement Results

To validate the presented calculations and the suitability of the 7L-HANPC topology for ultra-high efficiency applications, a 12.5 kW hardware demonstrator shown in **Fig. 7** was built, whose volumetric power density is 3.4 kW/dm^3 (55.9 W/in^3) and gravimetric power density is 3.2 kW/kg. A list of the

Table II
Main components of the final design, divided into semiconductor and filter components. The EMI filter component values are given per phase

Component	Value	Part Number
ANPC Stage Switches	31.0 mΩ	4 paralleled Infineon CoolMOS CFD7 600 V IPW60R031CFD7
FC Stage Switches	11.1 mΩ	2 paralleled Infineon Optimos 3 FD 200 V IPT111N20NFD
Gate Driver		10 A Infineon 1EDI60N12AF
L_1	113.3 µH	22 turns, Core: F3CC0008 2 mm × 5 mm wire
C_1	2.2 µF	Epcos TDK B32923H3225
L_2	15 µH	Wuerth Elek. 7443641500
C_2	13.2 µF	Epcos TDK B32924D3335
L_{cm}	400 µH (at 100 kHz)	4 turns, 2.5 mm wire Vacuumschmelze 2 x T60006-L2030-W358
C_{DC}	240 µF	Epcos TDK B32776G4406
C_{FC}	120 µF	Epcos TDK B32776G4406
C_Y	40 nF	Epcos TDK B32022A3103
R_d	1.65 Ω	pulse withstanding, through hole

main power components used in the hardware prototype and their part numbers can be found in **Table II**. It has to be noted, that for the presented measurements four power MOSFETs were connected in parallel for implementing each switch of the ANPC stage, however, for future research, space was provided in the layout to accommodate a total of six parallel switches. The semiconductor stage of one bridge leg and its schematic arrangement are shown in **Fig. 8.** Since there are three FC cells per bridge leg, there are three switching frequency commutation loops that require additional care in the layout, namely L_{c1}, L_{c2} and L_{c3}, out of which L_{c3} is the most critical for two reasons. Firstly, the commutation path of L_{c3} always closes through either the high-side or the low-side DC-link capacitor, for which layout symmetry has to be maximized such that L_{c3} is equal for both cases, as seen in **Fig. 8**. Secondly, given that the high-side and low-side (partial) DC-link voltages are not always equal in value due to the nature of the topology, care has to be taken if commutation capacitors are placed between the ANPC stage and FC stage switches, since two capacitors of unequal voltage, i.e. the respective DC-link capacitor and the commutation capacitor, which has previously been connected to the opposite DC-link capacitor, would be connected in parallel, creating current spikes and ringing when commutating the ANPC stage switches. Note that although space is provided to place ceramic capacitors between the ANPC and FC stages, this has not finally been done in the current setup (cf. **Fig. 8**). However, L_{c1} and L_{c2} can easily be optimized by placing ceramic (commutation)

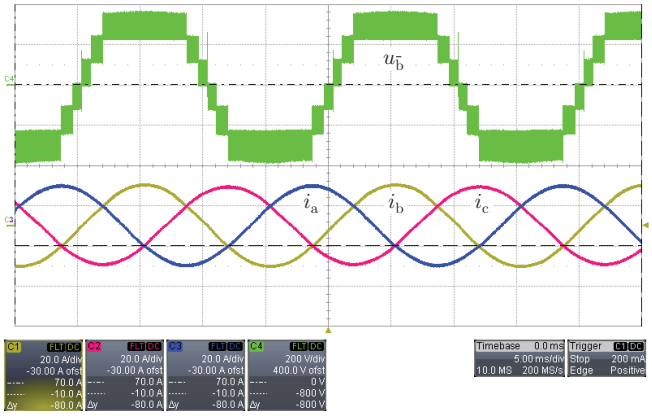

Fig. 9. Measurements of the seven-level output voltage of a bridge leg of the 7L-HANPC inverter shown in **Fig. 7** (200 V/div, referenced to the DC-link midpoint voltage, 5 ms/div) and the three phase mains currents (20 A/div) during operation at 10 kW.

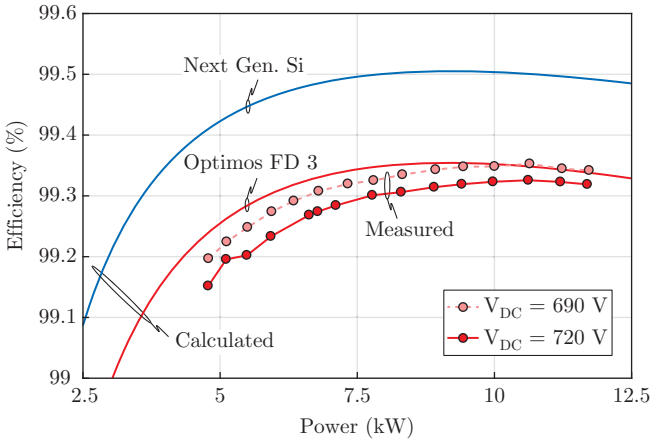

Fig. 10. Measured efficiency of the hardware demonstrator (cf. **Fig. 7**) reaching peak values of 99.35 % for U_{DC} = 690 V and 99.32 % for U_{DC} = 720 V, and the calculated efficiency for the prototype with the current semiconductor configuration at V_{DC} =720 V and with the configuration using *next generation* silicon switches from *Infineon* (solid lines), which will reach a peak efficiency of 99.5 %.

capacitors in parallel to the (film-type) FCs to reduce the size of the commutation loop (cf. **Fig. 8**). All the gate drivers are placed on separate PCBs, which on the one hand has the advantage of keeping the power PCB free from the gate driver circuitry for an optimized layout, but on the other hand has the disadvantage of increasing the gate loop inductance. This inductance is however kept at a minimum by using low-profile board-to-board connectors (*Samtec TMM* and *CLT* types) that result in distance between the PCBs of only 2.77 mm. Each switch has its own isolated power supply, for which dedicated transformers are used to obtain isolated gate voltages of 15 V and -5 V.

Given the high efficiency nature of the converter, there is no need for an active cooling system, and hence, neither fans nor heat sinks are required, thus minimizing the implementation effort and increasing the overall reliability of the system. This is particularly true for the converter at hand, where the semiconductor losses are distributed among many switches: the estimated losses of a single ANPC stage switch, housed in a TO-247 three-lead package, are of 0.14 W on average, whereas the losses for an individual SMD FC stage switch are 1.1 W.

The main measured waveforms taken with a resistive load are presented in **Fig. 9** for 10 kW operation, where the unfiltered seven-level phase voltage measured at the output node $\bar{b}$ with respect to the DC-link midpoint and the three phase currents are shown. The voltage spikes that can be seen during the voltage zero crossings are due to the unequal switching times of the ANPC stage and FC stage switches, and last only for some few tens of nanoseconds not affecting the overall system performance. The DC-link voltage midpoint is controlled by superimposing a third harmonic to the sinusoidal modulation of one fourth of the output voltage amplitude, achieving a low maximum instantaneous voltage deviation between the high-side and low-side DC-link of 8.9 V during nominal operation. The FC voltages are naturally balanced by phase shifted PWM [20] at their nominal voltages, i.e. at average values of U_{FC2} =240.5 V and U_{FC1} =120.9 V.

The efficiency of the three-phase 7L-HANPC inverter has been measured with a *Yokogawa WT3000* high-precision power analyzer, and is reported in **Fig. 10** together with the calculated efficiency. A peak efficiency of 99.35 % is achieved for U_{DC} = 690 V and 99.32 % for U_{DC} = 720 V, where all the converter losses are included, also those of the EMI filter stage and the auxiliary power. The calculated European weighted efficiency is 99.05 %, whereas the California Energy Commission (CEC) weighted efficiency is 99.23 % [27]. Although the electric and calorimetric loss measurements matched correctly in [12] for a 99.3 % efficient 8 kW all-SiC three-phase buck-type rectifier, as reported in [28], the precision of electric measurements for ultra-high efficiency power converters is typically not sufficient for guaranteeing the accuracy of the measurements. Hence, in future work, the efficiency of the converter at hand will also be measured calorimetrically.

V. Conclusions

In this paper, a 99.35 % efficient 3.4 kW/dm^3 (55.9 W/in^3) all-silicon seven-level three-phase inverter is presented, setting a new benchmark for ultra-high efficient and power-dense converters. For this, an alternative topology to the conventional FCC is employed, which has the advantage of halving the amount of FC cells by making use of a DC-link midpoint connection, which is easily accessible in hardware due to the need of serializing capacitors to be able to withstand the rated DC voltage, and an ANPC stage front-end that uses switches rated for half the DC-link voltage switching at grid frequency. Substantial volume savings are obtained by halving the number of FC cells, particularly for the case of low switching frequencies, since the capacitance requirement to guarantee a certain voltage ripple in the FCs is inversely proportional to the switching frequency, which is selected with low values for ultra-efficient converters. Additionally, no active cooling is required given the high efficiency of the system and the fact that the losses are spread

among many switches and/or power components, reducing the design effort and increasing reliability.

With recently available 18 mΩ 600 V *CoolMOS CFD7* power MOSFETs (*Infineon*), which have a lower on-state resistance compared to the 31 mΩ switches used in this work, the efficiency and/or volume can be further improved, as the switching losses are negligible at grid frequency. Furthermore, a comprehensive optimization shows that it is feasible to reach the boundary of 99.5 % efficiency with *next generation* 200 V silicon devices.

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