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A 4.6 W/mm^2 Power Density 86% Efficiency On-Chip Switched Capacitor DC-DC Converter in 32 nm SOI CMOS

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***Abstract*—The future trends in microprocessor supply current requirements represent a bottleneck for next generation high-performance microprocessors since the number of supply pins will constitute an increasingly larger fraction of the total number of package pins available. This leaves few pins available for signaling. On-chip power conversion is a means to overcome this limitation by increasing the input voltage – thereby reducing the input current – and performing the final power conversion on the chip itself. This paper details the design and implementation of on-chip switched capacitor converters in deep submicron technologies. High capacitance density deep trench capacitors with a low parasitic bottom plate capacitor ratio available in the technology facilitate high power density and efficiency in on-chip switched capacitor converter implementations. The measured performance of a 2 : 1 voltage conversion ratio on-chip switched capacitor converter implemented in 32 nm SOI CMOS technology with 1.8 V input voltage results in a power density of 4.6 W/mm^2 at 86% efficiency when operated at a switching frequency of 100 MHz.**

I. Introduction

Package pins in modern high-performance microprocessors are distributed between signal pins and supply pins. According to the 2011 International Technology Roadmap for Semiconductors (ITRS) [1], 50% of the total package pins in high-performance microprocessors are utilized as supply pins (power and ground). The percentage is 66.7% for high-volume microprocessors. Hence, only less than half of the total package pins are used for signals. The maximum allowable current per pin determines the required number of supply pins based on the microprocessor power specification.

The ITRS predicts that the supply voltage for high-performance microprocessors will decrease as shown in Fig. 1, however, the predicted power density is expected to remain close to constant, revealing an expected increase in supply current. In [2], a survey of 30 years of microprocessor history concludes that if future microprocessors continue to follow the historical trends identified in [2], the number of supply pins will constitute an increasingly larger fraction of the total package pins available with increasing supply current as shown in Fig. 2.

Implementing on-chip dc-dc power conversion in next-generation microprocessor architectures is a way to decrease the number of supply pins required. Since an increased input voltage leads to reduced input current for the same power specification, the bottleneck depicted in Fig. 2 can be drastically reduced. The primary design target, besides high efficiency, is to achieve a high power density to exploit the advantages of on-chip power conversion with a relatively low increase

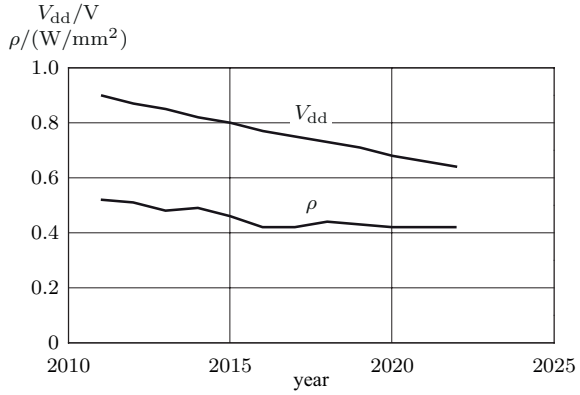

Fig. 1. The decreasing supply voltage and close to constant power density in high-performance microprocessors as predicted by the ITRS suggest an expected supply current increase.

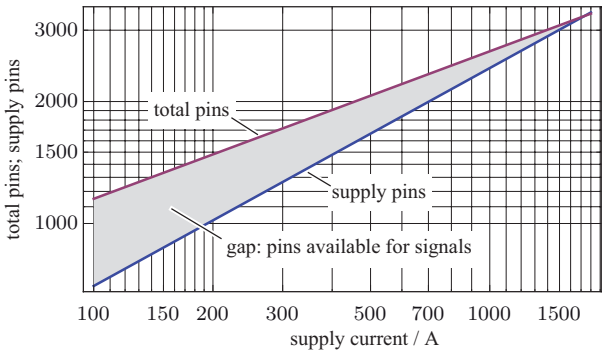

Fig. 2. Projections of power pin allocation over supply current resulting from a survey of 30 years of published microprocessor architectures [2]. Increasing supply currents stemming from the continuation of technology downscaling in combination with more cores added in multicore microprocessors represents a bottleneck in signal pin availability in next-generation microprocessors. (This figure is adapted from [2] with permission from its author.)

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of silicon estate. On-chip power conversion may furthermore be an enabler for high granularity power distribution in multicore processors with per-core regulation [3, 4] and for 3D System On Chip (SOC) integration for More-than-Moore systems [5, 6].

Switched capacitor (SC) converters have become popular for on-chip power conversion since no inductors, which on-chip are large and difficult to manufacture with sufficiently low losses, are required [7–13]. Using only switches and capacitors available in the technology, SC converters have the potential to meet the strict power density and efficiency requirements set by the microprocessor power specification.

This paper presents the design and evaluation of a $2:1$ voltage ratio down conversion on-chip switched capacitor converter implemented in $32\,\mathrm{nm}$ SOI CMOS technology. The main results and contributions described in the paper are:

- Design and implementation of an extremely high power density on-chip SC converter. The high power density is mainly achieved through the use of high capacitance density deep trench capacitors available in the technology.
- High efficiency power conversion, which is achieved from the small parasitic bottom plate capacitor of the deep trench capacitor as well as using the technology's fast transistors, which have low specific on-state resistance (conduction losses) and specific gate charge (gate driver losses) product.
- Implementation of a simple charge recycling circuit that reduces the losses associated with the bottom plate capacitor to give a slight improvement in efficiency at very low chip area cost.

Section II presents the circuit analysis of the $2:1$ SC converter to determine the design parameters based on the power specification. Section III describes the implemented building blocks including the SC power stage, stacked voltage domain gate driver, and charge recycling circuit. Experimental results of the implemented converter are presented in Section IV, where also regulation capabilities of SC converters are discussed. The measured power density is more than a factor of two higher than what has been presented in prior art.

II. $2:1$ Switched Capacitor Converter Analysis

In this section, an analysis of the SC converter power stage depicted in Fig. 3 is performed to determine the design parameters required to fulfill a given power specification. The power stage consists of a flying capacitor C and four switches with on-state resistances R_{on}. The output consists of a decoupling capacitor C_{load} in parallel with the load resistor R_{load}. In the following analysis, C_{load} is assumed to be infinite to ensure a constant output voltage.

In steady state, the flying capacitor is switched with 50% duty cycle between a) the charging phase, where the flying capacitor is in series between the input and the output (switches S_1 and S_3 are on), and b) the discharging phase, where the flying capacitor is in parallel with the output (switches S_2 and S_4 are on). Disregarding the parasitic resistances ($R_{\mathrm{on}} = R_{\mathrm{C}} = 0\,\Omega$) and assuming the flying capacitor

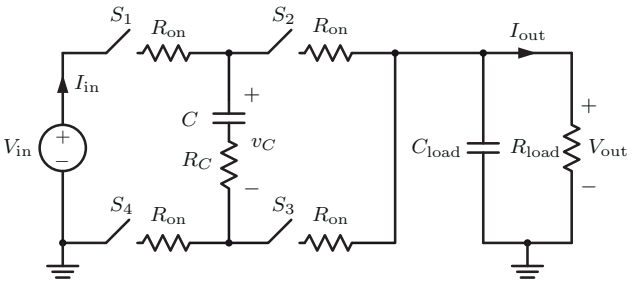

Fig. 3. Basic $2:1$ down conversion voltage ratio switched capacitor converter power stage and load. The parasitic on-state resistances R_{on} of the switches and the equivalent series resistance R_{C} of the flying capacitor are included.

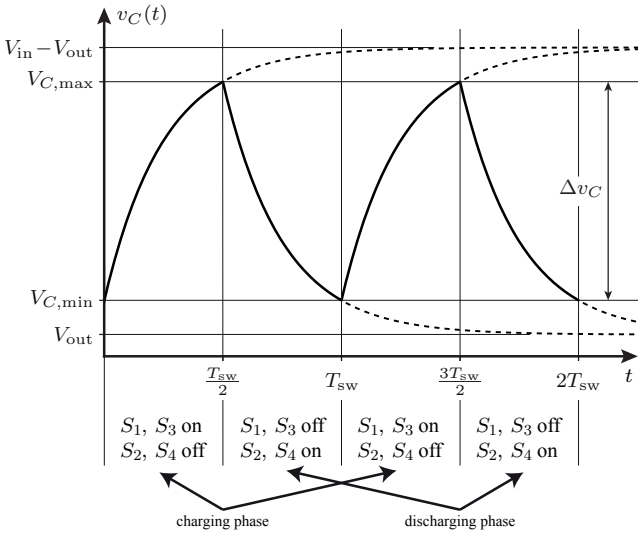

Fig. 4. Steady state voltage of the flying capacitor voltage $v_C(t)$. The voltage difference Δv_C is used to determine the charge delivered to the output load per switching period T_{sw}. Switches S_1 and S_3 are conducting in the charging phase, and switches S_2 and S_4 are conducting in the discharging phase.

voltage to be $v_C(t) = V_{\mathrm{out}}$, the ideal voltage conversion ratio of this SC converter is $2:1$ [8]. When the parasitic resistances are included, two periods of the steady state capacitor voltage $v_C(t)$ are depicted in Fig. 4. In the charging phase, the capacitor charges towards $V_{\mathrm{in}} - V_{\mathrm{out}}$, and in the discharging phase, the capacitor discharges towards V_{out}. The voltages $V_{C,\max}$ and $V_{C,\min}$ denote the actual voltages that the capacitor charges or discharges to, respectively, within one switching period $T_{\mathrm{sw}} = 1/f_{\mathrm{sw}}$, where f_{sw} is the switching frequency.

Using the standard charging behavior of a capacitor, the equations for $V_{C,\max}$ and $V_{C,\min}$ in the charging and discharging phases, respectively, shown in Fig. 4 become

$$V_{C,\max} = V_{\mathrm{in}} - V_{\mathrm{out}} + (V_{C,\min} - V_{\mathrm{in}} + V_{\mathrm{out}}) e^{-1/(2 f_{\mathrm{sw}} R_{\mathrm{eq}} C)}, \quad (1)$$

$$V_{C,\min} = V_{\mathrm{out}} + (V_{C,\max} - V_{\mathrm{out}}) e^{-1/(2 f_{\mathrm{sw}} R_{\mathrm{eq}} C)}, \quad (2)$$

where

$$R_{\mathrm{eq}} = 2R_{\mathrm{on}} + R_C + R_{\mathrm{wiring}} \quad (3)$$

denotes the total resistance in series with the flying capacitor, with R_C being the equivalent series resistor of the flying

capacitor, and R_{wiring} representing any wiring resistances stemming from the layout. R_{eq} is assumed to be equal in both switching phases.

Solving (1) and (2) for $V_{C,\max}$ and $V_{C,\min}$, the capacitor voltage difference Δv_C can be found to be

$$\Delta v_C = V_{C,\max} - V_{C,\min} = (V_{\mathrm{in}} - 2V_{\mathrm{out}})\, k, \tag{4}$$

where

$$k = \frac{1 - e^{-1/(2f_{\mathrm{sw}}R_{\mathrm{eq}}C)}}{1 + e^{-1/(2f_{\mathrm{sw}}R_{\mathrm{eq}}C)}}. \tag{5}$$

The flying capacitor delivers an equal amount of charge $C\Delta v_C$ to the output in each switching phase, so the total charge delivered per switching period is

$$Q_{\mathrm{tot}} = 2C\Delta v_C, \tag{6}$$

hence the output current becomes

$$I_{\mathrm{out}} = Q_{\mathrm{tot}} f_{\mathrm{sw}} = 2C\,(V_{\mathrm{in}} - 2V_{\mathrm{out}})\, k f_{\mathrm{sw}}. \tag{7}$$

In the following, the above equation for the output current is used to determine the design parameters to fulfill a given power specification.

A. Switched Capacitor Converter Loss Components

The main SC converter power losses are conduction losses from charging and discharging the flying capacitor, and switching losses from the parasitic bottom plate capacitor, the transistor parasitic gate-source and drain-source capacitances, and the gate driver.

1) Conduction Losses: The charging and discharging of the flying capacitor through R_{eq} is a lossy operation that results in conduction losses, which are included in the output current analysis above by the exponential terms in k from (5). Due to current balance of the flying capacitor, the output current is $I_{\mathrm{out}} = 2I_{\mathrm{in}}$, and the resulting converter efficiency becomes

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{V_{\mathrm{out}}I_{\mathrm{out}}}{V_{\mathrm{in}}I_{\mathrm{in}}} = \frac{2V_{\mathrm{out}}}{V_{\mathrm{in}}}. \tag{8}$$

Hence, (8) shows that the efficiency when including conduction losses is given by the input and output voltage specifications only.

In the un-loaded case, i.e. $I_{\mathrm{out}} = 0\,\mathrm{A}$, the output voltage is half the input voltage, however, the output voltage is less than half the input voltage when loaded due to conduction losses [14]. For fixed input voltage, the efficiency in (8) is seen to drop linearly with decreasing output voltage, hence the output voltage specification directly determines the conduction losses.

2) Switching Losses: One of the main contributors to switching losses stems from the flying capacitor's parasitic bottom plate capacitor, which is always referenced to ground. The bottom plate capacitance to main capacitance ratio, which is used to characterize bottom plate capacitor losses, depends heavily on the on-chip capacitor solutions available in the technology. As described in the next section, the SC converter presented in this paper includes a charge recycling circuit to reduce the parasitic bottom plate capacitor losses.

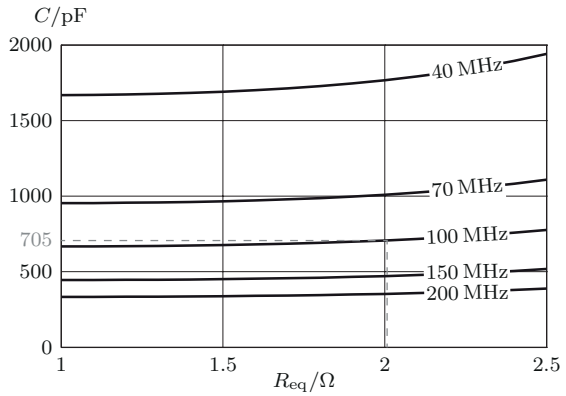

Fig. 5. Required capacitance of the flying capacitor versus total series resistance for a power specification of $V_{\mathrm{in}} = 1.8\,\mathrm{V}$, $V_{\mathrm{out}} = 825\,\mathrm{mV}$, and $I_{\mathrm{out}} = 20\,\mathrm{mA}$, evaluated at different switching frequencies.

Another switching loss stems from the parasitic drain-source capacitors of the transistors in the SC converter power stage. Assuming a constant output voltage, all transistors $S_1 - S_4$ have one terminal connected to a constant voltage potential (either V_{in}, V_{out}, or ground). Hence in an ac analysis where constant voltage potentials are ac ground, each drain-source capacitor is effectively in parallel with the flying capacitor's parasitic bottom plate capacitance. The drain-source capacitor power loss may therefore be directly included in the bottom plate capacitor power loss; note however that the drain-source capacitance is usually significantly smaller than the parasitic bottom plate capacitance.

The gate driver, which is discussed in the next section, also introduces switching losses, which are mainly due to driving the transistor's parasitic gate-source capacitances. Also, losses in the clock generation building blocks contribute to the gate driver switching losses.

B. Nominal Switched Capacitor Converter Design

Inspection of the output current from (7) (together with (5)) shows that for a power specification containing V_{in}, V_{out}, and I_{out}, the design parameters are C, R_{eq}, and f_{sw}. In the following, the design parameters will be determined based on a power specification of $V_{\mathrm{in}} = 1.8\,\mathrm{V}$, $V_{\mathrm{out}} = 825\,\mathrm{mV}$, and $I_{\mathrm{out}} = 20\,\mathrm{mA}$. With this power specification, the resulting efficiency including conduction losses is from (8) determined to be 91.7%. Of course, switching losses will result in an overall converter efficiency below this value.

Using (7), Fig. 5 shows the capacitance required to fulfill the power specification over a feasible range of R_{eq} for different switching frequencies. The choice of C is seen to be highly dependent on f_{sw}, but only slightly dependent on R_{eq}. The switching frequency will therefore be chosen based on a trade-off between low capacitance, which is proportional to the capacitor chip area and therefore influences the power density, and low switching losses, which influence the converter's overall efficiency. Based on this trade-off, $f_{\mathrm{sw}} = 100\,\mathrm{MHz}$ is chosen for the nominal design point.

Having chosen the switching frequency, the range of suitable capacitance values using Fig. 5 is narrowed, but the final capacitance still depends on R_{eq}. With C almost fixed, the equivalent series resistance of the flying capacitor R_C is also almost fixed. The wiring resistance R_{wiring} is minimized through an optimal layout, so the main design parameter in R_{eq} is the on-state resistance R_{on} of the transistors. The on-state resistance may – as the switching frequency – be chosen as a trade-off between power density and efficiency: the on-state resistance is inversely proportional to transistor area, thereby influencing the power density, but the gate-source and drain-source capacitances (switching losses) are proportional to transistor area, thereby influencing the efficiency. The R_{eq} used in the nominal design point was chosen based on a series of simulations and layout considerations. As a result thereof, $R_{\mathrm{eq}} = 2\,\Omega$ was found to be a good trade-off between power density and efficiency for this power specification.

With $f_{\mathrm{sw}} = 100\,\mathrm{MHz}$ and $R_{\mathrm{eq}} = 2\,\Omega$, the required capacitance for this design is $C = 705\,\mathrm{pF}$; this selection of design parameters is shown in gray in Fig. 5. Simulation results of this design point using hardware-correlated models shows that conduction losses constitute 66%, bottom plate capacitor losses 20%, and gate driver losses 14% of the total losses.

III. Design and Implementation

This section discusses the design and implementation of the $2:1$ SC converter integrated in a $32\,\mathrm{nm}$ SOI CMOS technology. This particular technology includes the deep trench capacitor [15], which has much larger capacitance density and much lower relative parasitic bottom plate capacitance compared to other on-chip capacitor solutions, e.g. transistor-based or metal-insulator-metal capacitors. In [7], the use of deep trench capacitors in an on-chip SC converter implemented in a $45\,\mathrm{nm}$ SOI CMOS technology is seen to result in high power density ($2.19\,\mathrm{W/mm^2}$) and efficiency (90%).

The complete circuit schematic of the implemented on-chip SC converter is depicted in Fig. 6. The SC converter power stage is split into power stages, SC1 and SC2, to facilitate the charge recycling circuit. Another advantage of the split power stage is that current is drawn from the input supply in both switching phases, and not only in the charging phase which is the case with a single power stage; this reduces the input current ripple by a factor of 2.

A. Stacked Voltage Domain Gate Driver

The breakdown voltage of the transistors in the $32\,\mathrm{nm}$ technology is lower than the high input voltage. Hence, the gate driver, which generates the clock signal for the power transistors $S_1 - S_4$, has to be designed in such a way that no single transistor is exposed to more than $V_{\mathrm{in}}/2$. Therefore, the gate driver in Fig. 6 employs a stacked voltage domain, where the upper voltage domain driving S_1 and S_2 is supplied between V_{in} and V_{d} and the lower voltage domain driving S_3 and S_4 is supplied between V_{d} and gnd.

The input clock $\mathrm{clk_{in}}$ is supplied externally in the lower voltage domain. Therefore, the level shifter circuit is implemented to shift the input clock to the upper voltage domain. In each voltage domain, the clock signal is passed through a latch with built-in delay (non-overlapping clock) to generate a deadtime interval between the clock edges to avoid shoot-through currents in the power transistors. In the delay unit, the number of logic inverters (buffers) determines the duration of the deadtime interval. In this design, the deadtime is designed to match the requirements of the charge recycling circuit discussed in the next subsection. Tapered buffers are inserted after the deadtime circuits to provide sufficient drive strength to turn on and off the power transistors $S_1 - S_4$.

In this design, the middle supply potential V_{d} is sustained between two decoupling capacitors in series from V_{in} to gnd. This setup provides safe start-up of the stacked voltage domains as V_{d} will follow $V_{\mathrm{in}}/2$ during ramp-up of the input voltage. However, an issue occurs if the converter is operated at low output voltages, which is the case for high load and/or low switching frequency operation. The nmos type power transistor S_2, with its source terminal connected to V_{out}, will in that case have a non-zero gate-source voltage when turned off, and will therefore conduct current in both switching phases. This behavior is evident from the low output voltage measurement points presented in the next section. A potential solution would be to connect V_{d} to V_{out}, but then special care has to be taken to ensure start-up of the stacked voltage domains. Regardless of V_{d} implementation, safe start-up of the stacked voltage domains is crucial, since failure to do so will expose some transistors to the full input voltage, thereby causing breakdown of the exposed transistors and destroying the converter.

B. Charge Recycling

The parasitic bottom plate capacitors C_{bp1} and C_{bp2} shown in gray in Fig. 6 are the main contributors to switching losses as discussed in Sec. II-A. Therefore, a charge recycling circuit that reduces the bottom plate capacitor power loss is implemented, as shown in Fig. 6. By the end of SC1's charging phase, C_{bp1} is charged to V_{out} and C_{bp2} is discharged. During the following deadtime interval, the charge recycling transistor S_{cr} is turned on, and charge from C_{bp1} is recycled to C_{bp2}. When SC2's charging phase (SC1's discharging phase) begins, it will require less energy to charge C_{bp2} to V_{out} and less energy is lost when C_{bp1} is discharged to ground. In the next deadtime interval, which occurs after SC2's charging phase, charge is recycled from C_{bp2} to C_{bp1}.

Fig. 7 shows the simulated efficiency improvement obtained with the charge recycling circuit. Since bottom plate capacitor losses do not depend on the absolute output power, the efficiency improvement is most noticeable at low output power, whereas the improvement is smaller at high output power. Still, the use of the charge recycling circuit is suggested since the efficiency increase comes at very low chip area cost (see layout in Fig. 8).

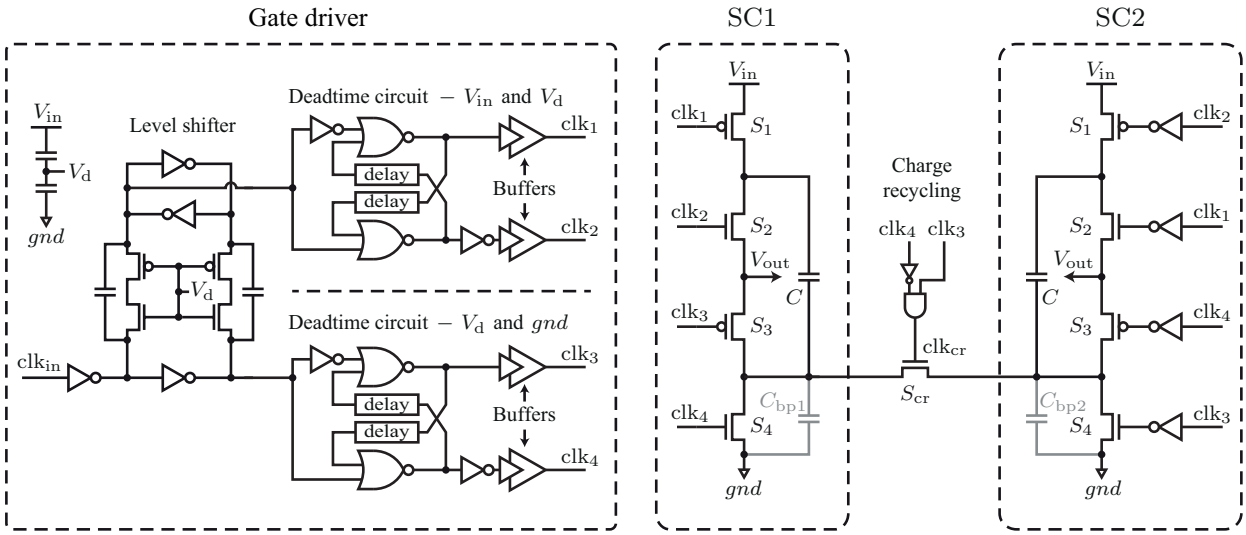

Fig. 6. Complete circuit diagram showing the two switched capacitor power stages, SC1 and SC2, that enable the implementation of the charge recycling circuit. The parasitic bottom plate capacitors of each power stage, C_{bp1} and C_{bp2}, are shown in gray. The gate driver is designed in a stacked voltage domain since the input voltage is higher than the breakdown voltage of the transistors in the technology. It consists of a level shifter that shifts the input clock clk_{in} from the lower voltage domain between V_d and gnd to the upper voltage domain between V_{in} and V_d and two identical non-overlapping clock circuits that generate the deadtime interval in each voltage domain.

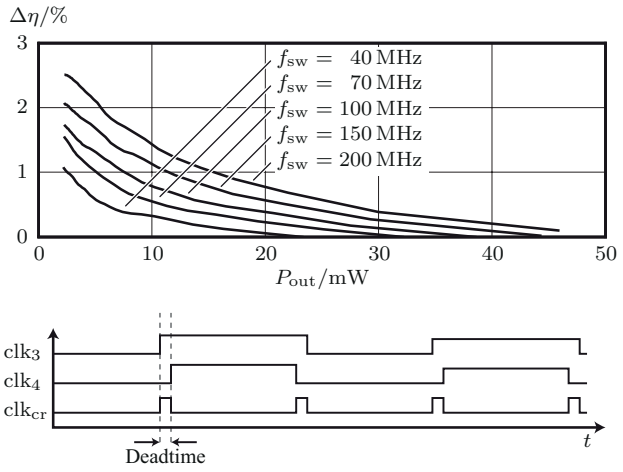

Fig. 7. Simulated effect of the charge recycling circuit on efficiency over output power for different switching frequencies. The charge recycling event occurs during the deadtime interval when transistor S_{cr} is turned on.

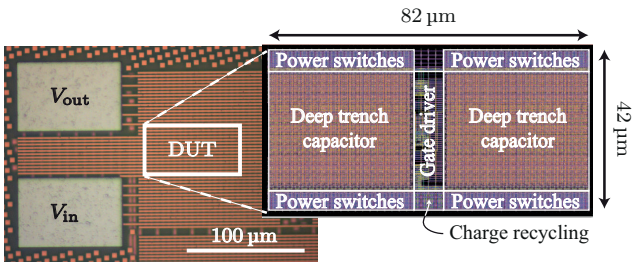

Fig. 8. Chip photo with magnified layout view of the implemented $2:1$ switched capacitor converter. The input clock and ground pads are not shown. The total active converter area is $0.00344\,mm^2$.

C. Converter Layout

A chip photo of the implemented SC converter with magnified layout view is shown in Fig. 8. The converter is laid out in a symmetrical fashion which is compatible with the possibility of paralleling and / or interleaving several SC converter units to supply higher output power and / or lower the inherent output voltage ripple. From simulations, the total capacitance of both flying capacitors is estimated to be $C \approx 690\,pF$, and the total series resistance is estimated to be $R_{eq} \approx 2\,\Omega$ in typical conditions. The total active chip area, which includes the gate driver and the charge recycling circuit, is $0.00344\,mm^2$. The flying capacitor accounts for 65%, the power switches for 26%, and the gate driver for 9% of the total converter area.

IV. Experimental Results

This section discusses the measurement results of the on-chip SC converter and shows the high power density and efficiency achieved by using the deep trench capacitors available in the $32\,nm$ SOI CMOS technology. The measurements are performed on the unpackaged wafer die using GBB PicoProbes. The input and output currents are measured using Keithley 2400 series Sourcemeters, and the on-chip input and output voltages are measured on Kelvin contacts using an Agilent 34970 Data Acquisition / Switch Unit. The load resistor is connected externally to the chip. Since there is no on-chip output decoupling capacitor in this design, the output decoupling is also connected externally to the chip, and a larger than required capacitance of $33\,nF$ is added to the measurement setup to ensure a negligible output voltage

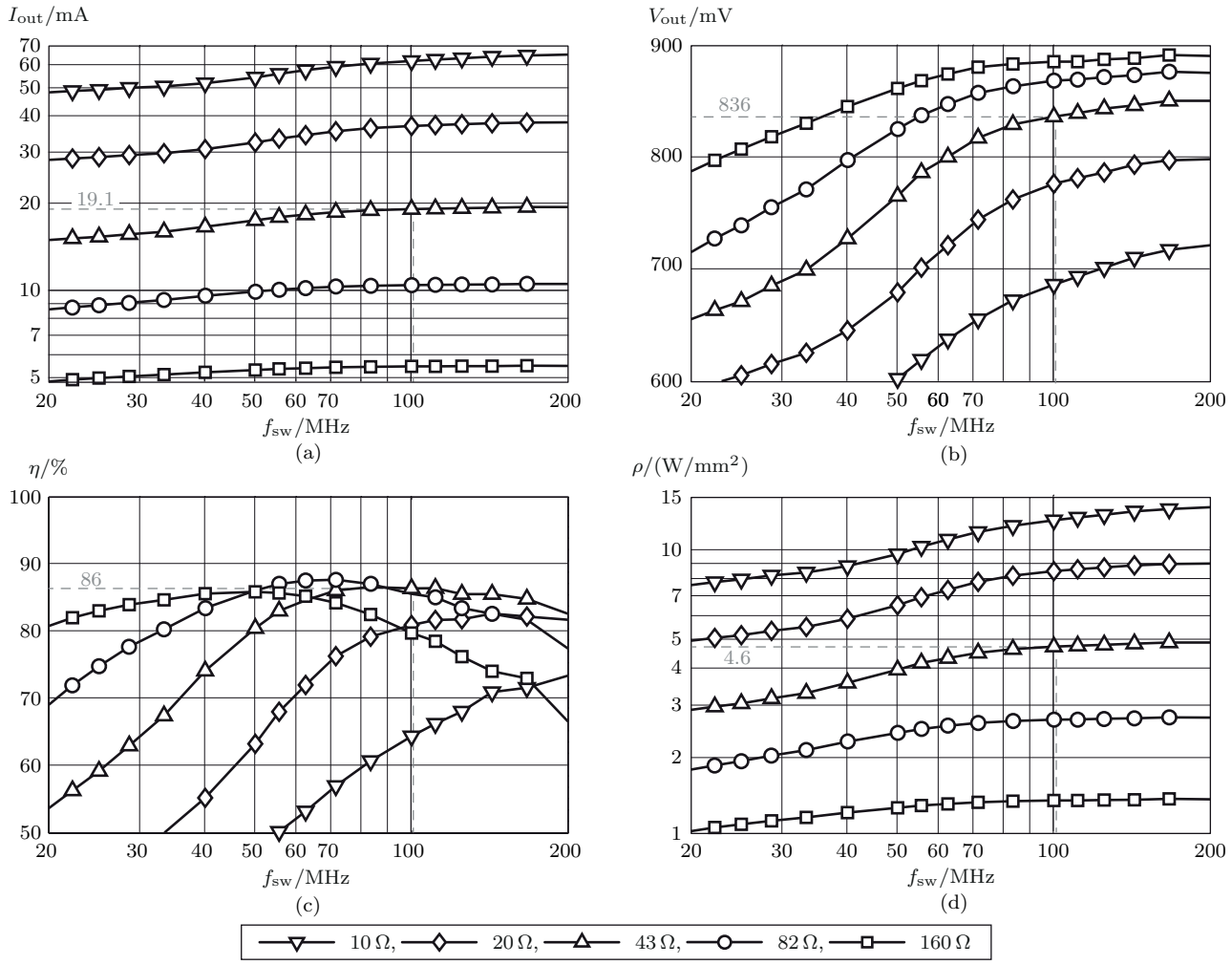

Fig. 9. Measured performance showing (a) output current, (b) output voltage, (c) efficiency, and (d) power density versus switching frequency for different load resistors. The measurements are performed with $V_{\mathrm{in}} = 1.8\,\mathrm{V}$. The nominal design point, which corresponds to the $43\,\Omega$ measurement series at $100\,\mathrm{MHz}$, is marked in gray; the achieved performance is $I_{\mathrm{out}} = 19.1\,\mathrm{mA}$, $V_{\mathrm{out}} = 836\,\mathrm{mV}$, $\eta = 86\%$, and $\rho = 4.6\,\mathrm{W/mm^2}$.

ripple. This enables a good characterization of the on-chip SC converter performance. However, it should be noted that the required output decoupling capacitance can be drastically lowered, or even omitted, by employing interleaving as is shown in [9–12]; this is also the course that will be followed by the authors of this paper in future on-chip converter designs. For this reason, the output decoupling capacitor is not included in the power density measurements.

Fig. 9 shows the measured output current, output voltage, efficiency η, and power density ρ. The converter has been designed for the power specification discussed in Sec. II-B, and this corresponds to the $R_{\mathrm{load}} = 43\,\Omega$ measurement series at $f_{\mathrm{sw}} = 100\,\mathrm{MHz}$. As seen in gray in Fig. 9, the performance achieved is $I_{\mathrm{out}} = 19.1\,\mathrm{mA}$, $V_{\mathrm{out}} = 836\,\mathrm{mV}$, $\eta = 86\%$, and $\rho = 4.6\,\mathrm{W/mm^2}$. Furthermore, measurement series for different load levels are presented in Fig. 9 to thoroughly characterize the converter's performance over load and frequency.

The decrease in output voltage and efficiency shown in Figs. 9(b) and 9(c) at low frequencies is a typical characteristic of SC converters [8, 9]. The deviation to the slope at output voltages below $700\,\mathrm{mV}$ is due to the stacked voltage domain middle potential $V_{\mathrm{d}} \approx 900\,\mathrm{mV}$, which results in a non-zero gate-source voltage for transistor S_2 when turned off, as discussed in Sec. III-A; however, operating the converter at such low output voltages results in efficiencies below 70% and is included here for completeness of the converter characterization only. Above a certain switching frequency, the output current remains constant as seen in Fig. 9(a), and increasing the switching frequency further will only bring higher switching losses, as can be seen in the eficiency measurements in Fig. 9(c).

A. Regulation Capabilities

SC converters are often referred to as fixed conversion ratio converters, where the conversion ratio is determined by the SC converter topology. Conceptually, any rational conversion ratio may be designed using a large number of switches and flying

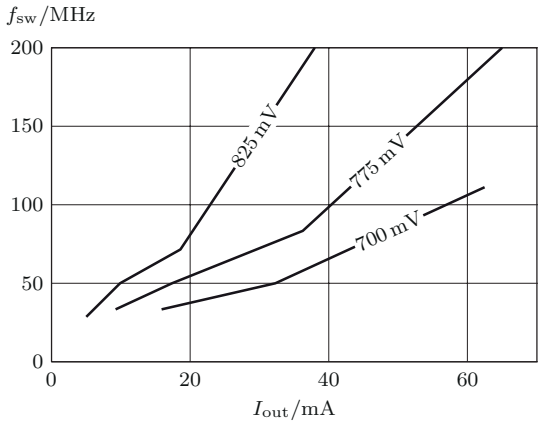

Fig. 10. Measured output current regulation capability by frequency modulation shown for three fixed output voltages. The input voltage is $V_{\mathrm{in}} = 1.8\,\mathrm{V}$.

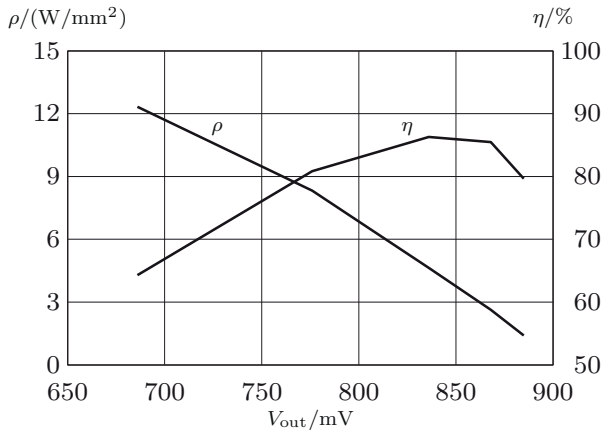

Fig. 11. Power density and efficiency over output voltage measured with different loads. The switching frequency is 100 MHz and the input voltage is $V_{\mathrm{in}} = 1.8\,\mathrm{V}$.

capacitors [16], and output regulation could be achieved by changing between the different conversion ratio configurations. For on-chip SC converters, implementing a large number of flying capacitors is usually impractical because of the high bottom plate capacitor losses. However, even with the simple $2:1$ converter considered here, regulation of the output voltage and current is possible.

Within the frequency and load ranges included in the measurement series, a fixed output voltage may be sustained by modulating the switching frequency as shown in Fig. 10. Possible implementations to perform this regulation task is a current starved voltage controlled oscillator (VCO), where the oscillation frequency depends on the output voltage [12], or hysteretic boundary control, where a clocked comparator triggers the next clock event whenever the output voltage is below the reference voltage [8].

The measured power density and efficiency over output voltage at $f_{\mathrm{sw}} = 100\,\mathrm{MHz}$ are shown in Fig. 11. The efficiency is at the maximum at $V_{\mathrm{out}} = 836\,\mathrm{mV}$, which is below the unloaded output voltage of $900\,\mathrm{mV}$. Operating the converter at voltages below $836\,\mathrm{mV}$ results in a decreasing efficiency, but at the same time an increasing power density. Hence the trade-off between efficiency and power density when operating SC converters is visible; this trade-off is further highlighted in the following subsection.

B. Cooling requirements

For each measurement point in Fig. 9, the corresponding efficiency and power density has been mapped to the $\eta - \alpha$ plane. The envelope resulting from the highest achieved efficiency per power density is shown in Fig. 12 for three different input voltages. This serves to illustrate the entire operating of the converter. It also shows what efficiency can be achieved for a given power density, and furthermore highlights the trade-off between achievable efficiency and power density, e.g. a power density of more than $10\,\mathrm{W/mm^2}$ for $V_{\mathrm{in}} = 1.8\,\mathrm{V}$ is achievable, but the corresponding maximum efficiency is below 75%. It is seen in Fig. 12 that the maximum efficiency

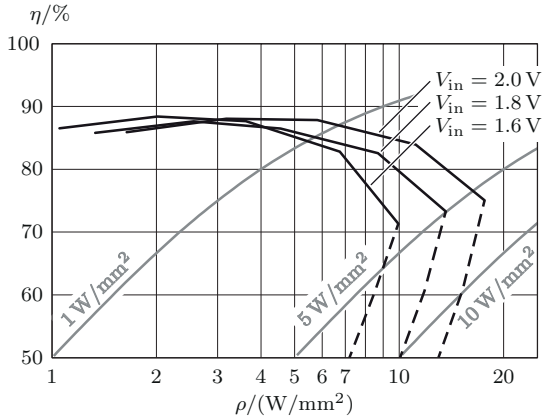

Fig. 12. Envelope of the highest efficiency per power density measured with different input voltages. The minimum efficiency required to fulfill cooling requirements are superimposed for three different cooling power densities illustrating that cooling must be taken into account for high power density on-chip SC converters.

is independent of input voltage, whereas the maximum power density increases with input voltage.

Cooling requirements become an issue for very high power density designs since the power loss density will also be high. This becomes even more profound for the high power density measurement points in Fig. 12 where the efficiency is low. The converter's minimum efficiency η_{min} can be expressed in terms of the cooling power density $\rho_{\mathrm{cool}} = P_{\mathrm{loss}}/A$, that can be effectively cooled by the chosen cooling technology:

$$\eta_{\mathrm{min}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{loss}}} = \frac{P_{\mathrm{out}}/A}{P_{\mathrm{out}}/A + P_{\mathrm{loss}}/A} = \frac{\rho}{\rho + \rho_{\mathrm{cool}}}, \quad (9)$$

where P_{loss} is the total power loss and A is the converter area. The minimum efficiency requirements for three different cooling power densities have been included in gray in Fig. 12. It is seen that a cooling power density of minimum $5\,\mathrm{W/mm^2}$ is required to operate the converter at the complete maximum efficiency per power density envelope. If the cooling power

TABLE I
COMPARISON OF THE WORK PRESENTED IN THIS PAPER TO PREVIOUSLY PUBLISHED WORK ON ON-CHIP SWITCHED CAPACITOR CONVERTERS SHOWING THE BENEFIT OF DEEP TRENCH CAPACITORS AND SUBMICRON TECHNOLOGY CONVERTER IMPLEMENTATIONS.

Reference	[10]	[11]	[7]	This work
Technology	90 nm bulk	32 nm SOI	45 nm SOI	32 nm SOI
Voltage ratio	2:1	2:1, 3:1, 3:2	2:1	2:1
Input voltage	2.4 V	2 V	2 V	1.8 V
Output voltage	1 V	0.88 V	0.95 V	0.836 V
Output power	1650 mW	208 mW	2.6 mW	15.6 mW
Capacitor technology	MOS capacitor	MOS capacitor	Deep trench	Deep trench
Interleaving / Decoupling	21x interleaved	32x interleaved	External decoupling	External decoupling
Charge recycling	Yes	No	No	Yes
Efficiency	69%	81% (2:1)	90%	86%
Power density	0.77 W/mm^2	0.55 W/mm^2	2.19 W/mm^2	4.60 W/mm^2

density is below $5\,\mathrm{W/mm^2}$, the converter's allowed operating region must be limited accordingly. From [17], a cooling power density of more than $7\,\mathrm{W/mm^2}$ can be achieved using ultrathin manifold microchannel heat sinks.

C. Comparison to Other Work

In Tab. I, the results presented in this paper are compared to previously published results on on-chip SC converters focusing on power density. The high power density and efficiency achievable when using deep trench capacitors are clearly visible from this work and from [7]. This work is implemented in a $32\,\mathrm{nm}$ technology node compared to $45\,\mathrm{nm}$ in [7], hence the capacitance density of the deep trench capacitor is higher, and a higher power density is expected. From Tab. I, the power density achieved in this design is more than a factor of two higher than previously reported on-chip SC converter designs.

V. CONCLUSION

In this paper, a $2:1$ voltage conversion ratio on-chip switched capacitor converter is designed to overcome the bottleneck of increased power pin requirements in next-generation high-performance microprocessors. For a given power specification, the design parameters are determined from an analytical analysis of the steady state capacitor voltage. The complete circuit schematic of the implemented on-chip switched capacitor converter including the power stage and the gate driver building blocks is discussed. A charge recycling circuit is implemented to reduce the power loss associated with the flying capacitor's parasitic bottom plate capacitor.

The designed converter is implemented in a $32\,\mathrm{nm}$ SOI CMOS technology that features very high capacitance density deep trench capacitors. Measurements of the implemented on-chip switched capacitor converter with $V_{\mathrm{in}} = 1.8\,\mathrm{V}$ and $f_{\mathrm{sw}} = 100\,\mathrm{MHz}$ results in $V_{\mathrm{out}} = 836\,\mathrm{mV}$ and $I_{\mathrm{out}} = 19.1\,\mathrm{mA}$; the power density is $4.6\,\mathrm{W/mm^2}$ and the efficiency is 86%. This power density is more than a factor of two higher compared to prior art.

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