Analysis and Design of a 1200 V *All-SiC* Planar Interconnection Power Module for Next Generation More Electrical Aircraft Power Electronic Building Blocks

Mattia Guacci, Dominik Bortis, Ivana F. Kovačević-Badstübner, Ulrike Grossner, and Johann W. Kolar

***Abstract*—Compact, light weight and efficient Power Electronic Building Blocks are seen as fundamental components of future *More Electric Power Systems*, e.g. *More Electrical Aircraft*. Core elements supporting the trend are power modules employing solely SiC MOSFETs. In order to take advantage of the high switching speed enabled by SiC, novel modules concepts must be investigated. For example, low inductance planar interconnection technologies, integrated buffer capacitors and damping networks are possible solutions to mitigate switching overvoltages and oscillations at the switching node occurring for conventional modules. In this paper, the analysis and the design of a novel ultra-low inductance 1200 V SiC power module featuring an integrated buffer-damping network are discussed. The power module is first described and characterized with impedance measurements. Afterwards, a general optimization procedure for the sizing and the selection of the integrated components is presented and measurements are performed to verify the analysis and to highlight the improvements of the proposed solution.**

***Index Terms*—*All-SiC* Power Module, Damping Network, Integrated Buffer Capacitor, Planar Interconnection Technology.**

I. Introduction

THE *More Electrical Aircraft* (MEA) concept targets the replacement of mechanic, pneumatic and hydraulic systems of commercial aircraft with electric power converters and actuators, aiming for decreased fuel consumption and/or emissions reduction, increased reliability and/or lower maintenance effort [1]. The turning point of the trend can be traced back to 2010, when the milestone of 1 MVA of electric power was reached on board of *Boeing*™ B787. An electric power requirement of 1.6 MVA is planned for the next generation of aircraft [2], motivating the increased interest of the power electronics community in MEA. In particular, the *Horizon*2020 European. Project 636170 - Integrated, Intelligent Modular Power Electronic Converter (I2MPECT) [3], building on the expertise in device packaging, thermal management, converter design and reliability analysis of European industry and academia, intends to demonstrate significant advances in terms of powerto-weight ratio and efficiency of power converters for MEA. The primary goal is the realization of a *Power Electronic Building Block* (PEBB), i.e. a 99% efficient 3-phase inverter (cf. TABLE I) achieving a power-to-weight ratio of 10 $\frac{\text{kW}}{\text{kg}}$, i.e. three times higher than nowadays available solutions [4].

TABLE I
Electrical Specifications of the I2MPECT Power Electronic Building Block

	Description	Value
V_{dc}	input DC voltage	540 V, ... 700 V
f_{sw}	switching frequency	30 kHz
v_{out}	output AC voltage	110 V_{RMS}
$i_{out,\,ph}$	output AC current per phase	190 A_{pk}
$P_{out,\,ph}$	output power per phase	15 kVA
f_{out}	output frequency	400 Hz, ... 2 kHz

PEBBs, i.e. modular power converters with defined functionality and simplified interfaces, combined with switching stages based on power modules employing solely Silicon Carbide (SiC) semiconductors (*All-SiC* PMs), can push the already strict requirements concerning compactness and light weight established in the aircraft industry even further, while still enabling reduced complexity and costs. The PEBBs approach reduces the engineering effort both in the design and in the maintenance phase of a power electronic system while SiC intrinsic qualities, e.g. higher switching speed, lower on-state voltage and improved temperature withstanding capability allow a reduction of the losses, output filter downsizing and low cooling requirements [5]. However, in order to guarantee the reliability of the PEBB and to fully utilize SiC performance, an ultra-low inductance PM designs is required. In fact, parasitic inductances in combination with the enabled high switching speed could cause significant overvoltages and undesired ringing [6]. This ultimately compromises the lifetime of the PM and increases its electromagnetic noise emissions [7].

To explore the state-of-the-art in terms of commutation

Manuscript received November 8, 2017. This work was supported by the Swiss State Secretariat for Education, Research and Innovation (SERI) under contract 15.0161. The opinions expressed and arguments employed herein do not necessarily reflect the official views of the Swiss Government.

M. Guacci, D. Bortis and J. W. Kolar are with the Power Electronic Systems Laboratory, ETH Zurich, Switzerland. I. F. Kovačević-Badstübner and U. Grossner are with the Advanced Power Semiconductors Laboratory, ETH Zurich, Switzerland. (e-mail: guacci@lem.ee.ethz.ch). *(corresponding author:Mattia Guacci.)*

Digital Object Identifier 10.24295/CPSSTPEA.2017.00029

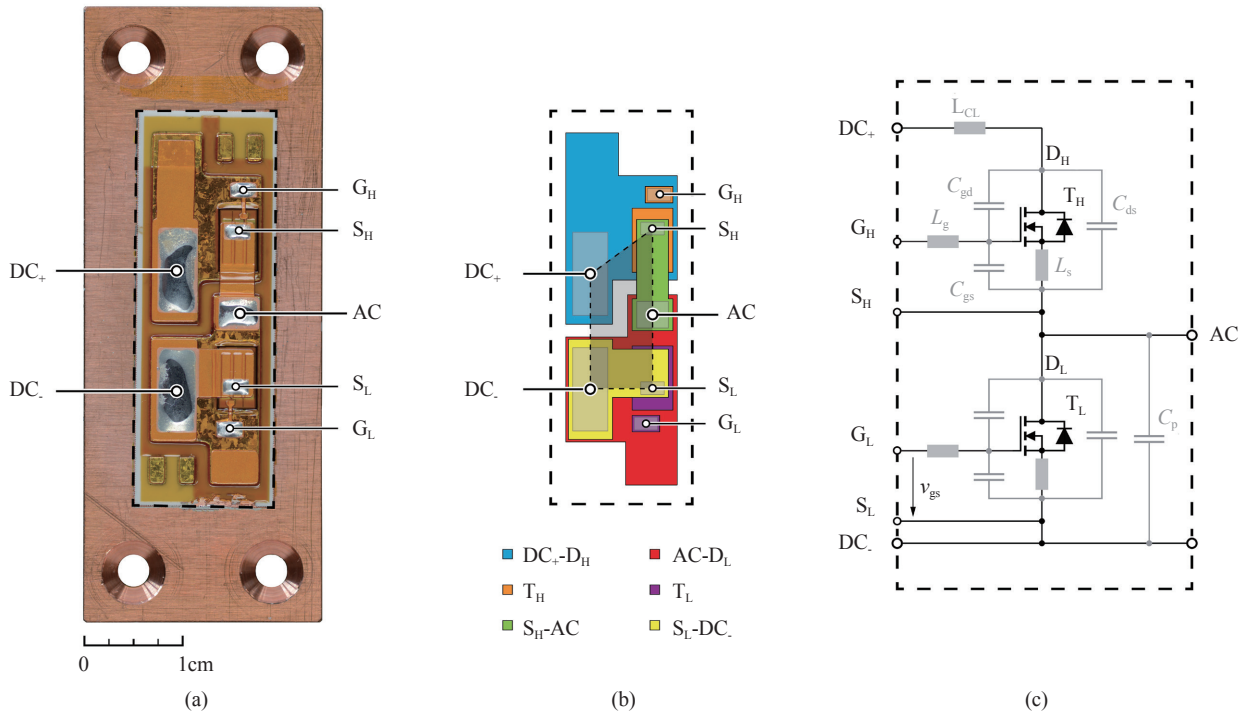


Fig. 1. Prototype of the designed PM including two 1200 V SiC power MOSFETs (*Cree*™ CPM2-1200-0025). The solder pads for gate (G_L, G_H) and Kelvin source (S_L, S_H) connections are highlighted, as well as the DC and AC terminals of the half-bridge (a). The structure of the PM is clarified with colors (b): the planar interconnections (green and yellow) and the substrate copper layer (blue and red) enable an ultra-low inductance design. The area of the average commutation loop is highlighted. Finally, the equivalent circuit of the PM, including parasitic capacitances and inductances, is illustrated in a schematic (c).

loop inductance L_{CL} in 1200 V *All-SiC* PMs [8]–[10], a comprehensive analysis of commercially available PMs is conducted. Most of nowadays available designs employ bond wires to interconnect the dies and feature L_{CL} values in the range of 10 nH to 30 nH (cf. TABLE II). In order to allow a fair comparison between the PMs, a figure-of-merit is defined as

$$\mathrm{FOM} = \left(\frac{R_{\mathrm{ds}} I_{\mathrm{ds}}^2}{V_{\mathrm{dc}} I_{\mathrm{ds}}} \; 100 \; \frac{L_{\mathrm{CL}}}{1\,\mathrm{nH}} \right)^{-1}. \tag{1}$$

The lower limit of L_{CL} only slightly reduces to around 6 nH if research prototypes are considered [11]–[15]. Differently, when planar interconnection technologies are considered [16], [17], i.e. bond wires are replaced by wide coplanar structures [18], L_{CL} can be reduced below 2 nH [19], [20] (cf. TABLE III). PMs adopting this solution provide benchmarks for the next generation of PMs. Additionally, planar interconnection technologies facilitate symmetric designs and enable doublesided cooling [7], [21] aiming towards an even increased power density.

A second measure allowing the utilization of SiC high switching speed is the integration of a buffer capacitor in the PM. It allows the decoupling of L_{CL} from the parasitic inductance (L_{ext}) of the connection between the PM and the external input filter capacitor [11]. If a sufficient amount of capacitance is selected, the current during the switching transient is provided from the integrated capacitor and only the portion of inductance inside the PM (L_{CL}) experiences a fast current variation di/dt [22], mitigating the overvoltage. On the other hand, the paralleling of the buffer capacitor with the external capacitor introduces an undamped resonance network. Therefore, in order to prevent prolonged oscillations, a suitable damping network must be additionally integrated.

Ultimately, the sizing of the buffer capacitor and of the optimized damping network result from a trade-off between required volume and effectiveness of the solution. Moreover, the impact of parasitic inductances, e.g. L_{CL} and L_{ext}, on the performance of the buffer-damping network is not known in advance and therefore a widely applicable approach is desired. Accordingly, the focus of this paper is first on the design and experimental analysis of an *All-SiC* PM half-bridge arrangement featuring planar interconnections; second, the design procedure for an optimized integrated buffer-damping network with low sensitivity towards parasitic inductance is discussed. In order to experimentally validate the benefits enabled from a low inductance PM design and explore its limit, the PM prototype of Fig. 1 (a), featuring a planar interconnection technology, is characterized in Section II. The effectiveness of an integrated buffer capacitor against overvoltage is proven with measurements in Section III. Subsequently, in Section IV, the optimization of an integrated damping network is discussed and its performance are analyzed. Afterwards, a guideline for a general design procedure is described in Section V. Finally, conclusions are

TABLE II
COMMUTATION LOOP INDUCTANCE OF COMMERCIALLY AVAILABLE 1200 V *ALL-SIC* PMS

Manufacturer	I_{ds} (A)	$R_{ds,on}$ (mΩ)	L_{CL} (nH)	FOM
Cree™	138	13.0	15	0.45
	285	5.0	14	0.60
	256	3.6	5	2.60
Rohm™	180	7.8	25	0.34
	300	4.7	13	0.65
Semikron™	523	5.6	15	0.27

TABLE III
COMMUTATION LOOP INDUCTANCE OF *ALL-SIC* PMS IMPLEMENTING PLANAR INTERCONNECTIONS

Research Facility	V_{dc} (V)	I_{ds} (A)	L_{CL} (nH)
Univ. of Notthingham, et al. [23]	2500	-	1.7, ... 2.6
Univ. of Grenoble, et al. [7]	1200	144	< 2
Univ. of Tennessee, et al. [24]	1200	-	2.6
Fraunhofer™ IZM, et al. [19]	-	-	0.9
Semikron™ [20]	1200	400	1.4

drawn in Section VI.

II. ULTRA-LOW INDUCTANCE *ALL-SIC* PM

The one to one replacement of Si MOSFETs and IGBTs in PMs with SiC MOSFETs does not allow the full exploitation of SiC performance: the enabled high switching speed, in fact, sets more severe constraints on the values of parasitic elements that can be tolerated. Therefore, new challenges during the design phase of *All-SiC* PMs must necessarily be faced.

In this section, the PM prototype shown in Fig. 1 is characterized, stressing the importance of dies positioning and interconnection technology in order to achieve an ultra-low inductance design. Considerations are deliberately limited to a basic but modular half-bridge structure (i.e. only one die per switch), designed for the specifications reported in TABLE I but for one sixth of the power rating.

A. Analysis of the PM Prototype

The PM shown in Fig. 1 consists of two *Cree*™ CPM2-1200-0025 SiC power MOSFETs (4 mm×6.4 mm) connected in bridge-leg configuration by a patented planar interconnection technology [16]. In Fig. 1 (b), the arrangement of dies and the terminals are highlighted. The high-side MOSFET T_H (orange) is pressure silver sintered on the upper (blue) substrate copper layer (300 µm thick) connecting its drain D_H (on the back-side of the die) to the positive supply terminal DC_+. Similarly, the low-side MOSFET T_L (purple) is sintered on the bottom (red) substrate copper layer connecting its drain D_L to the AC output. The source contacts of the MOSFETs (S_H and S_L on the top-side of the dies) are connected depositing a copper layer forming the planar interconnections (100 µm thick) from S_H to AC (green) and from S_L to DC_ (yellow). A 50 µm thick polyamide-base material isolates the substrates from the interconnections.

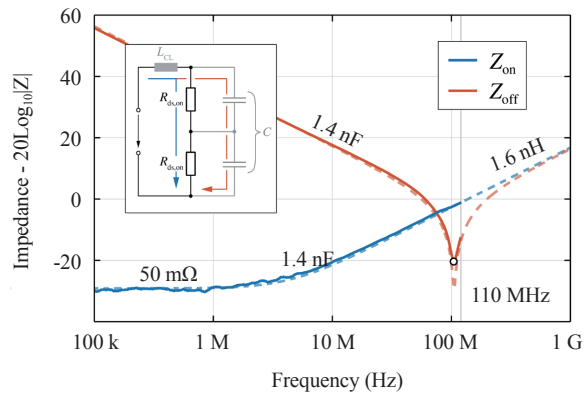


Fig. 2. Impedance measured from the DC terminals of the PM shown in Fig. 1 when (blue) both MOSFETs are conducting and (red) blocking. Series *RL* and *LC* equivalent circuits (dashed) with the values given in the figure match the measurements respectively. For frequency higher than 110 MHz, only the simulated curves converging to L_{CL} = 1.6 nH are shown.

Because of the selected technology, only one copper layer is available, therefore is not possible to overlap yellow and green connections aiming to a vertical design which would yield to an even lower L_{CL} [18]. The area of the horizontal commutation loop (highlighted in grey), including the DC terminals and the MOSFETs, is minimized, whereas the distances are only constrained by the manufacturing process and/or isolation requirements. The overall size of the Al_2O_3 ceramic substrate (dashed in Fig. 1 (a)-(c)) results 39.4 mm×13.8 mm with an overall maximum thickness of 1.3 mm.

B. Commutation Loop Inductance

In order to verify the effectiveness of this design solution, L_{CL} is characterized with multiple impedance measurements. The measurements are conducted with a precision impedance analyzer *Agilent*™ 4294A in combination with the adapters 42941*A* and 16047*E*. Different adapters and connections to the PM influence the measurement, however the relative standard deviation results below 10%.

More in detail, when both MOSFETs are conducting, the circuit seen from the DC terminals of the PM can be approximated by a *RL* series connection, where $R = 2R_{ds,on}$ and $L = L_{CL}$. Differently, when both MOSFETs are in the blocking state, the impedance resemble a *LC* series connection, where $L = L_{CL}$ and

$$C = \frac{1}{2}\left(\frac{C_{gs}C_{gd}}{C_{gs}+C_{gd}} + C_{ds}\right) = \frac{1}{2}\left(C_{oss} - \frac{C_{rss}^2}{C_{iss}}\right) \quad (2)$$

is defined by the parasitic capacitances of the two SiC MOSFETs connected in series (neglecting C_P). The impedance of ideal *RL* and *LC* equivalent circuits are analytically calculated in the frequency domain and the value of *R*, *L* and *C* are selected in order to best approximate the measured curves, as

shown in Fig. 2. The value of $R_{ds,on}$ is additionally measured during the conduction of a DC current where, in accordance with [25], approximately 25 mΩ results for each MOSFET; moreover, inserting in (2) the values of the parasitic capacitances specified in [25] for v_{ds} = 0 V, an equivalent capacitance C = 1.4 nF results as expected. Even if the frequency measurement range of the instrument is limited to 110 MHz, the analytical curves clearly converge to the extrapolated value of L_{CL} = 1.6 nH.

Remark: nowadays, the evaluation of L_{CL} is typically entrusted to the electromagnetic modelling of the PM supported by specialized softwares, such as *Ansoft*™ *Q3D* [12]–[14]. According to the trend, the 3D CAD file provided from the PM manufacturer is imported in *Q3D* and, after simulating the described experiment, L_{CL} = 2.7 nH results. The relative discrepancy is significant and the simulated value shows excessive variations depending on the setting of the excitation ports in the simulation tool. This issue is under investigation [26], however the cause is identified in the hypothesis of equipotential excitation ports, ultimately representing the boundary conditions for the simulated electromagnetic problem.

C. Gate Loop Inductance

The connection from the PM to the gate driver plays an important role in the shaping of the voltage and current waveforms during a switching transient. In a first approximation, the path from the driver to the gate connection on the die can be represented with the inductance L_g shown in Fig. 1 (c). Intuitively, L_g limits the changes of the gate current, reducing the bandwidth of the driver. This consequently increases the delay time and the current rise time, ultimately increasing the switching losses [27].

Additionally, the charging process of C_{gs} excites a resonance at $f_g = 1/2\pi\sqrt{L_g C_{gs}}$ and, in order to limit v_{gs} below the gate voltage rating of the MOSFET, a lower boundary for the gate resistance $R_{g,lim}$ is set. $R_{g,lim}$ is proportional to L_g, but while being effective in damping the resonance, it also limits the maximum switching speed.

Based on the premises above, it is clear that the minimization of the gate connections length should be of main concern for the design of a PM. The integration of the gate driver is only ideally a valid option, because it requires additional effort, leads to higher costs and size, and increases the failure rate of the PM [28]. Short, wide and coplanar connections are more realistically advised as best practice. For convenience, however, gate and source terminals are typically routed all together and next to each other to one side of the PM. Adopting this approach, the value of L_g can easily reach 30 nH [11], resulting in the mentioned drawbacks.

Additionally, if the connection to the source of a MOSFET is partially shared between gate driver and bridge-leg, a fraction of L_g (L_s in Fig. 1 (c)), known as common source inductance, is shared with the path defining L_{CL}. Consequently, a change on i_{ds} directly affects v_{gs} according to

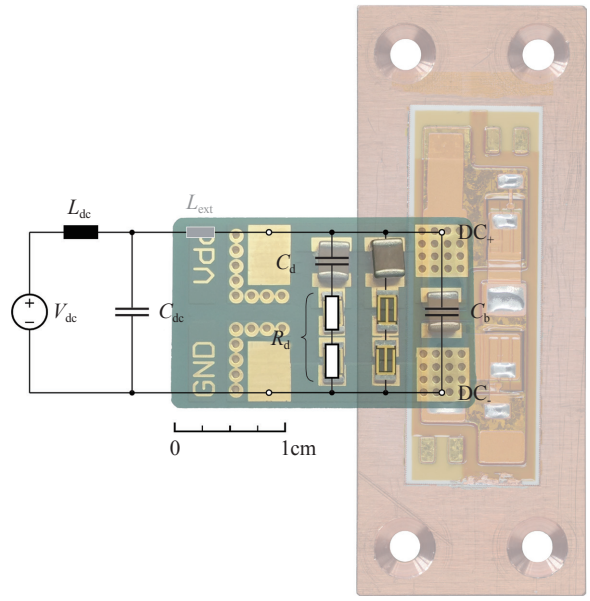


Fig. 3. 1 mm-thick PCB providing a practical and low inductive solution to integrate the buffer capacitor C_b and the damping network R_dC_d in the PM. One undamped and two damped 1210 *Kemet*™ 1500 V *X7R* ceramic capacitors find place together with power resistors of different values.

$$v_{gs} = v_{gs,0} - L_s \frac{di_{ds}}{dt}. \tag{3}$$

E.g. with a current slope of 10 $\frac{A}{ns}$, each 100 pH of L_s subtracts 1 V from $v_{gs,0}$ during a turn-on transition, providing a negative feedback reducing the switching speed. This issue is well known and can be avoided splitting the power source and the gate source connection, i.e. Kelvin source. It is less transparent, instead, that even if L_g and L_{CL} are physically independent, the magnetic coupling between them ($M_{g,CL}$) basically plays the same role as L_s. Although it is difficult to experimentally quantify the impact of $M_{g,CL}$ on v_{gs}, it is important to be aware of its consequences once the gate driver is arranged in the close proximity of the PM.

In the considered PM, gate and Kelvin source solder pads are directly accessible from the top of the dies (G_L, G_H and S_L, S_H indicated in Fig. 1 (a)). In particular, S_H directly contacts T_H and is separated from the copper interconnection carrying the load current to AC (yellow); the same applies for S_L, separated from DC_. Short and wide copper connections are used to connect the solder pads to the driver, reducing L_g to only 6 nH. In this way, low values of R_g could be selected, achieving high switching speed therefore minimizing the switching losses without the risk of damaging the gate dielectric. With the aim of further reducing L_g, a solution featuring overlapping gate connections on a flexible PCB could be used. In the case at hand, *Q3D* simulations performed on the complete setup [26], obtained by merging the CAD file of the PM and of the gate driver PCB, showed negligible coupling.

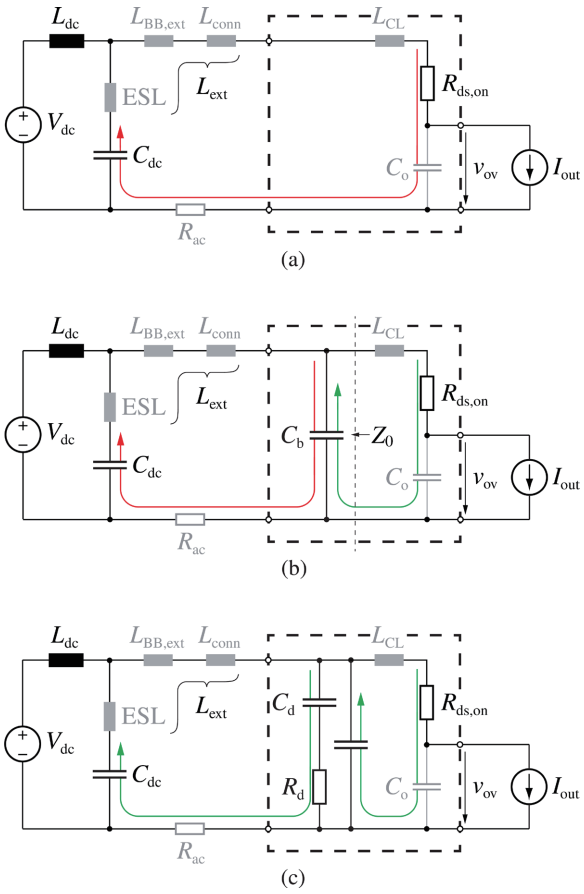


Fig. 4. Equivalent circuit of the analyzed half-bridge in a DPT setup during a hard turn-on switching transition. In (a), the high-frequency current components excited from the switching transition flow through L_{ext}, leading to overvoltage across the low-side MOSFET T_L (i.e. v_{ov}) after turn-off. With the integration of C_b (b) in the PM (dashed box), the high-frequency currents are confined (green), but a resonance network between L_{ext} and C_b is created, causing severe ringing at v_{ov}. In (c), a damping network R_dC_d is additionally integrated to damp the ringing. The output impedance Z_0 of the input filter is measured as indicated.

III. Integrated Capacitive Snubber

The amount of capacitance necessary at the DC side of a converter (C_{dc}) can vary in a wide range depending on the power rating and input voltage V_{dc} and it typically results in a bulky structure (e.g. $C_{dc} \approx 100$ µF in the considered setup) that hardly finds place in the closest proximity of the switching stage, i.e. the PM. The inductances of the conductors connecting C_{dc} to the DC terminals of the PM significantly contribute to the total power loop inductance $L_{PL} = L_{ext} + L_{CL}$. In particular, its ideal lower boundary is limited by the parasitic inductance of C_{dc} (ESL), typically in the order of 10 nH to 20 nH [29]. A significant L_{ext} vanishes the benefit of a low inductance PM design, therefore a possible solution, i.e. the integration of a buffer capacitor in the PM (cf. Fig. 3), is analyzed in this section.

The circuit supporting the first part of the explanation is shown in Fig. 4 (a). It represents the PM of Fig. 1 (dashed box) connected in a Double Pulse Test (DPT) setup and simplified for the case of a hard turn-on switching transition of the high-side MOSFET T_H. The parameters of the DPT setup and the values of the parasitic elements introduced in Fig. 4 (a) are summarized in TABLE IV (herein L_{ext} = 15 nH and R_g = 1.5 Ω if not differently specified).

TABLE IV
Parameters of the DPT Setup and Parasitic Elements of the PM

	Description	Nominal Value
T_H, T_L	*Cree*™ CPM2-1200-0025	1200 V, 90 A
I_{out}	switched output current	30 A
V_{dc}	input DC voltage	540 V
C_{dc}	external film capacitor	94 µF, 800 V
L_{dc}	input inductor	1 mH
R_g	gate resistance	1.5 Ω or 5 Ω
L_g	parasitic gate inductance	6 nH
v_{gH}	T_1 gate driver voltage	$V_{on} = 20$ V
v_{gL}	T_2 gate driver voltage	$V_{off} = -5$ V
C_b	buffer capacitor	0, ... 24 nF
C_d	damping capacitor	0, ... 24 nF
R_d	damping resistor	0.5 Ω, ... 4.7 Ω
$R_{ds,on}$	high-side MOSFET on-state resistance	25 mΩ
R_{ac}	frequency dependent resistance	0.2 Ω, ... 0.7 Ω
C_o	switching node parasitic capacitance	260 pF
L_{CL}	commutation loop in the PM	1.6 nH
L_{conn}	PM connectors	6 nH
$L_{BB,ext}$	from PM connectors to C_{dc}	0 nH or 20 nH
ESL	C_{dc} parasitic inductance	9 nH
L_{ext}	$L_{conn} + L_{BB,ext} + \text{ESL}$	15 nH or 35 nH

A current step through *Lext*, originating from the switching transition, excites the resonance between L_{PL} and C_o ($C_{dc} \rightarrow \infty$). C_o represents the parallel connection of the output capacitance (C_{oss}) of the low-side MOSFET T_L with the parasitic capacitance of the PM from the switching node to DC_ (C_p cf. Fig. 1 (c)). While the latter depends only on the geometry of the PM (i.e. C_p = 45 pF), C_{oss} is non-linear, i.e. $C_{oss}(v_{ds})$; however, in order to best model the resonance occurring on a DC voltage bias, $C_{oss}(V_{dc})$ = 215 pF [25] is considered. This results in C_o = 260 pF.

The frequency dependent parasitic resistance $R_{ac}(f) > R_{ds,on}$ of the $L_{PL}C_o$ resonant network, typically much smaller than its characteristic impedance, $\sqrt{L_{PL}/C_o} \approx 8$ Ω, is the only damping element present. Consequently, a voltage spike and a prolonged oscillation at the voltage v_{ov} across T_L occurs, as shown in blue in Fig. 5. v_{ov} reaches 896 V ($v_{ov,pk}$), more than 300 V above V_{dc}, and strongly oscillates when R_g = 1.5 Ω. This waveform provides other information on the parameters of the equivalent circuit of Fig. 4 (a). Knowing C_o, L_{PL} can be calculated from the resonant frequency $f_{tot} = 1/2\pi \, {}^{1}\!/_{2\pi\sqrt{(L_{CL}+L_{ext})C_o}}$ = 77 MHz and 16.6 nH results as expected ($L_{PL} = L_{ext} + L_{CL}$ = 15 nH + 1.6 nH). Additionally, analyzing the exponential decay of

$$v_{ov}(t) = V_{dc} + (v_{ov,pk} - V_{dc})e^{-t/\tau}, \tag{4}$$

with a time constant of τ = 48 ns, $R_{ac}(f_{tot})$ = 0.7 Ω results. The

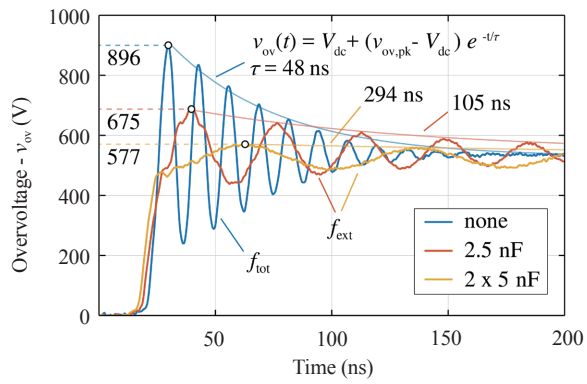


Fig. 5. Measured waveforms of the voltage across T_L during hard turn-on switching transition of T_H (i.e. R_g = 1.5 Ω, L_{ext} = 15 nH) with (red and yellow) and without (blue) integrated buffer capacitor C_b. A C_b bigger than 2.5 nF already significantly reduces the peak of v_{ov}, however, without a proper damping network, a prolonged oscillation occurs.

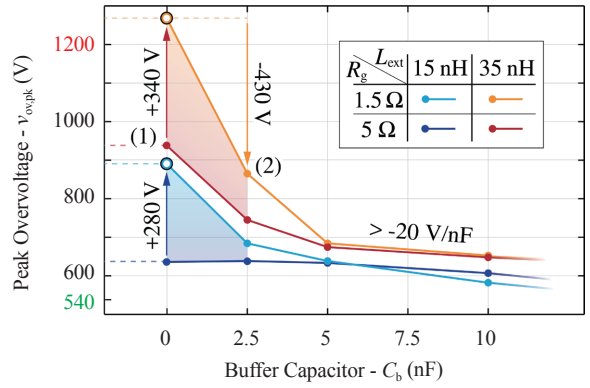
value of R_{ac} completes the linear model shown in Fig. 4 (a), enabling the simulation of the waveforms of v_{ov}; hence, the oscillation after the switching transient and its decay can be compared with measurements. However, correct initial conditions, i.e. the amplitude of the current step $i_{out,pk}$ exciting the resonance, must be set and therefore must be known in advance. For this reason, a measurements-based approach is initially preferred to optimize the buffer-damping network.

With the integration of the buffer capacitor C_b in the PM, as shown in Fig. 4 (b) and Fig. 3, L_{PL} is split in L_{ext} and L_{CL}, and L_{CL} is minimized. Consequently, the high frequency current components excited during the switching transient are confined in a smaller loop (green in Fig. 4 (b)) and bypass L_{ext}, significantly reducing $v_{ov,pk}$. With the final goal of quantifying the achievable improvements and dimensioning C_b, several experiments are performed.

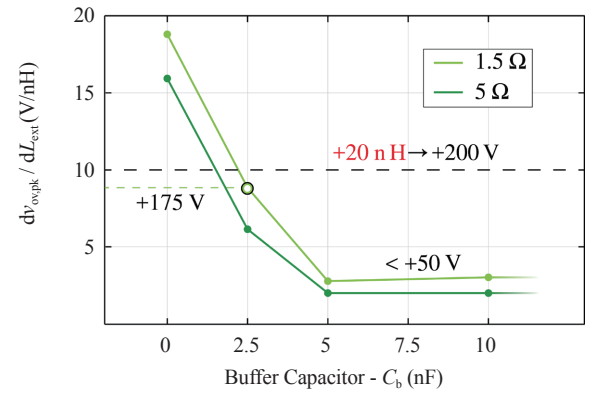
Two measured waveforms (red and yellow) are shown in Fig. 5 for two different values of C_b = 2.5 nF and 10 nF. The main resonant frequency is now shifted to $f_{ext} = 1/2\pi\sqrt{L_{ext}C_b} < f_{tot}$ (f_{ext} = 26 MHz and 13 MHz, respectively) because $C_b > C_o$ and $L_{ext} \approx L_{PL}$. Due to the lower resonant frequency, R_{ac} reduces ($R_{ac}(f_{ext}) \approx 0.1$ Ω,...0.2 Ω) and correspondingly increases to 105 ns and 294 ns, prolonging the oscillation.

Moreover, connecting C_b, a second resonant network resonating at $f_{int} = 1/2\pi\sqrt{L_{CL}C_{oss}}$ = 247 MHz > f_{tot} (because $L_{CL} < L_{PL}$) is formed. The associated oscillation is only partially visible on the waveforms, given the ultra-low inductance design and the higher value of frequency dependent resistance. Nevertheless, if needed, it can be damped at the AC side of the PM [30]. However, it is worth noticing that, if f_{int} exceeds the parasitic frequency of the output filter, less attenuation might be guaranteed from it.

Fig. 5 provides an additional information on the effective capacitance of C_b. In this setup, C_b is implemented by connecting one or more *Kemet*™ 1500 V *X7R* ceramic capacitors [31] with values between 4.7 nF and 12 nF in parallel (cf. Fig. 3). A reduction of capacitance, due to the DC voltage offset, is expected and confirmed from the measurements.



(a)



(b)

Fig. 6. Measured peak of v_{ov} during hard turn-on switching transition of T_H with respect to C_b for four different combinations of L_{ext} and R_g (a). Without C_b, L_{ext} = 35 nH and R_g = 1.5 Ω cause v_{ov} to exceed the voltage rating of CPM2-1200-0025 (i.e. 1200 V). Additionally, the sensitivity of $v_{ov,pk}$ towards L_{ext} is plotted (b). Without C_b it is above 15 $\frac{V}{nH}$, while with C_b bigger then 5 nF, it is limited below 3 $\frac{V}{nH}$ in both cases.

Knowing L_{ext} and measuring f_{ext}, the effective value of C_b can be calculated in the different cases; the resulting capacitance is always approximately half of the nominal value $C_{b,nom}$. For the sake of clarity, the reported value of capacitance always refers to the effective one.

Overvoltage and oscillation can become more severe in case of higher switching speed or in designs featuring bigger L_{ext}. Fig. 6 (a) summarizes $v_{ov,pk}$ for different combinations of R_g and L_{ext} which, without C_b, have a strong influence on $v_{ov,pk}$. As can be noted, L_{ext} = 35 nH and R_g = 1.5 Ω cause v_{ov} to exit the Safe Operating Area (SOA) of the MOSFET. Increasing R_g to 5 Ω (1-red) or integrating C_b = 2.5 nF (2-orange) is almost equally effective against $v_{ov,pk}$. However, the second option guarantees a better trade-off with respect to switching losses [32]. Clearly, the setup featuring smaller L_{ext} (light and dark blue) shows reduced $v_{ov,pk}$ in the same conditions.

C_b = 2.5 nF is sufficient to maintain $v_{ov,pk}$ < 900 V for all the considered combinations. Increasing C_b to 5 nF is only effective on the worst case (orange), whereas C_b > 5 nF brings no real further improvement from this point of view. This is clarified in Fig. 6 (b), where the sensitivity of $v_{ov,pk}$ towards L_{ext} is plotted. Almost independently from R_g, the sen-

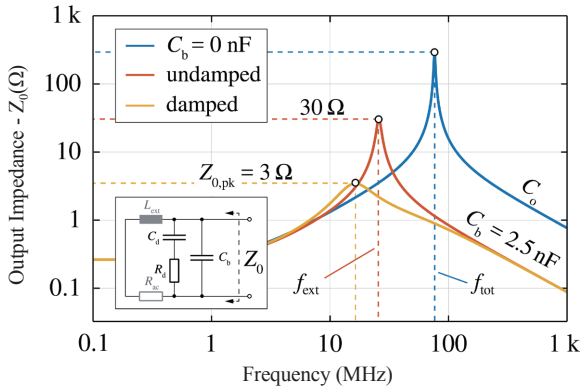


Fig. 7. Output impedance of the C_b-R_dC_d network (Z_0) for C_b = 2.5 nF with (yellow) and without (red) the damping network. The optimized damping network (R_d = 1.5 Ω and C_d = 5 nF) reduces $Z_{0,pk}$ from 30 Ω to 3 Ω according to the specifications. The impedance without C_b seen from the AC terminal is also plotted (blue) to highlight the shifting of the main resonance from f_{tot} to f_{ext}.

sitivity $\mathrm{d}v_{\mathrm{ov,pk}}/\mathrm{d}L_{\mathrm{ext}}$ drops from 15 $\frac{\mathrm{V}}{\mathrm{nH}}$ (without C_b) to 3 $\frac{\mathrm{V}}{\mathrm{nH}}$ (C_b > 5 nF). For the rest of the analysis the value of C_b is fixed to 2.5 nF ($C_{b,nom}$ = 4.7 nF).

To conclude, it is worth mentioning once again that the performance of this solution (i.e. integration of C_b) are supported by the ultra-low inductance PM design (i.e L_{CL} = 1.6 nH). For example, assuming L_{CL} = 15 nH, it is clear that no value of C_b could reduce $v_{ov,pk}$ below the limit obtained with L_{ext} = 15 nH and without C_b integrated in the PM (i.e. 896 V).

IV. Damping Network Optimization

As discussed in Section III, C_b effectively limits $v_{ov,pk}$ and relaxes the design constraints on L_{PL}, but indirectly modifies the impedance of the input filter (Z_0 in Fig. 4 (b)) as shown in Fig. 7. As a consequence, the main resonant frequency, clearly visible at the output voltage v_{ov}, is shifted from f_{tot} to $f_{ext} < f_{tot}$. As described in Section III, due to the reduction of R_{ac}, less damping is provided and the oscillation is prolonged. Then, with the considered values, fext enters the regulated EMC spectrum (f_{ext} < 30 MHz) negatively affecting the electromagnetic noise compatibility of the PEBB. Finally, the ringing at v_{ov} reflects on the current flowing through C_{dc}; the comparable amplitude and reduced damping degrade its lifetime.

This premise motivates the analysis and the optimization of a damping network presented in this section. Different damping solutions are discussed in literature [33]; the simplest damping approach avoiding steady-state losses is a series R_dC_d network in parallel with C_b [34], [35] (cf. Fig. 3 and Fig. 4 (c)). This approach is selected to facilitate the integration in the PM. In first place, a design procedure should be defined to dimension R_d and C_d, once L_{ext} and C_b are fixed. [33] proposes an optimization routine that, given the maximum allowed peak of the buffer-damping (C_b - R_dC_d) network output impedance ($Z_{0,pk}$), provides the value for R_d and C_d ensuring optimal damping, i.e. minimizing C_d.

TABLE V
Components Value for the Optimized Snubbers with $Z_{0,pk}$=3 Ω

L_{ext} (nH)	C_b	$C_{b,nom}$ (nF)	C_d	$C_{d,nom}$ (nF)	R_d (Ω)
15	2.5	4.7	5.0	12	1.5
35	2.5	4.7	10	24	2.0

This closed form procedure is preferred over an analytical approach [36]. In order to explore the effectiveness of this solution, a wide set of measurements with damping network featuring different combinations of R_d and C_d is performed and the results are commented in the following.

Fig. 8 (a) shows $Z_{0,pk}$ for different R_d-C_d pairs in the range 0.5 Ω < R_d < 10 Ω and 2 nF < C_d < 10 nF with L_{ext} = 15 nH, C_b = 2.5 nF and R_{ac} = 200 mΩ. Onlythree values for R_d (0.5 Ω, 1.5 Ω and 4.7 Ω) and C_d (2.5 nF, 5 nF and 10 nF) are considered in the experiments. Thus, the highlighted nine different combinations for R_d and C_d, having $Z_{0,pk}$ in the range between 1.8 Ω and 9.4 Ω, are analyzed. The performance of the damping network outside this range rapidly decay. In Fig. 8 (b)-(d), the corresponding measured waveforms of v_{ov} are illustrated.

Because of the additional capacitance C_d and resistance R_d, $v_{ov,pk}$ is now limited to values below 600 V, even if C_b = 2.5 nF is considered. As shown in red in Fig. 8 (c), $Z_{0,pk}$ = 3 Ω (e.g. R_d = 1.5 Ω and C_d = 5 nF) results to be sufficient to limit $v_{ov,pk}$ below V_{dc} + 50 V and to cancel the oscillation after its first peak in the considered conditions. Correspondingly, Fig. 7 (yellow) shows how the integration of this R_dC_d network reduces $Z_{0,pk}$ from 30 Ω to 3 Ω, effectively damping the resonance. A C_b-R_dC_d network featuring a smaller $Z_{0,pk}$ (yellow in Fig. 8 (c)) does not show significant improvement on the damping performance, however, the associated value of C_d increases, complicating the integration.

Fig. 8 (b) and (d) additionally confirm how $Z_{0,pk}$ is a good indicator of the performance of the damping network. Given the shape of the isolines, Fig. 8 (d) shows three measurements where, even changing the value of C_d, $Z_{0,pk}$ remains between 4 Ω and 5 Ω. As a consequence, the resulting vov waveforms are similar in the three cases. Differently, the three measurements reported in Fig. 8 (b) cover almost the full range of $Z_{0,pk}$ (i.e. 2.5 Ω, ... 9.4 Ω) and the performance of the damping network significantly improves (i.e. from almost ineffective to comparable with the optimized design). Ultimately, the values reported in the first row of TABLE V (L_{ext} = 15 nH) are selected.

In Fig. 8 (a), the locus of [33]-optimum solutions, revisited to consider the influence of R_{ac}, is additionally marked with a white dashed line. As expected, fixed $Z_{0,pk}$ (i.e. an isoline), it selects the corresponding design featuring minimum C_d. Therefore, an alternative usage of the 2D-plot of Fig. 8 (a) consists in finding the value of R_d minimizing $Z_{0,pk}$ once the maximum value of C_d is given, e.g. from volume constraints. The entire optimization procedure is repeated for L_{ext} = 35 nH and the values of the resulting components are also reported in TABLE V for comparison. Intuitively, a bigger C_d

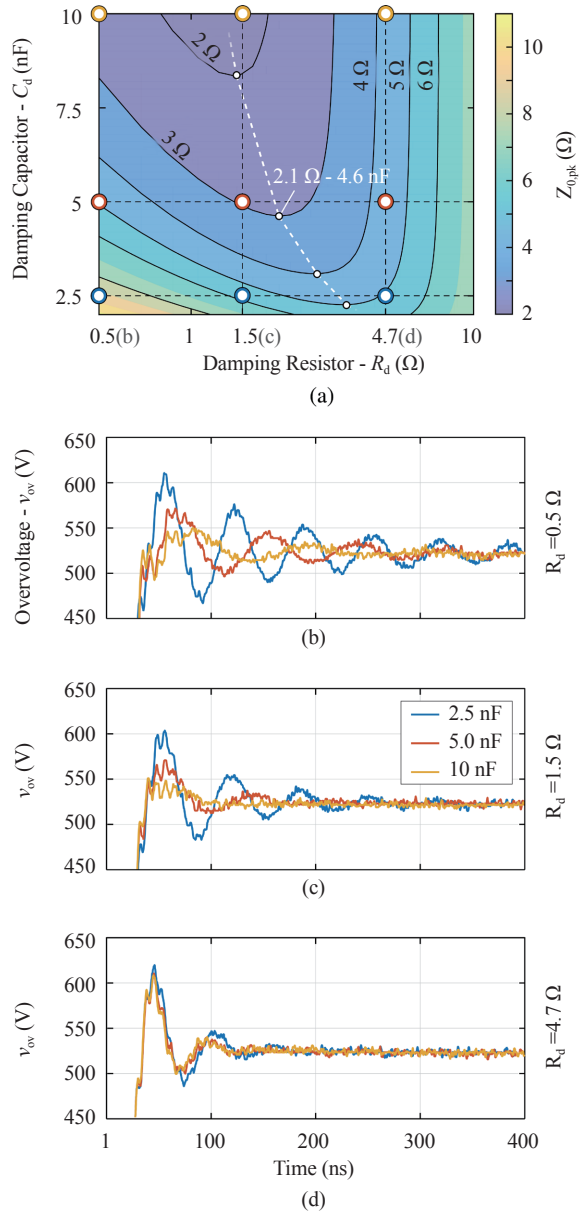


Fig. 8. Peak of the output impedance of the buffer-damping network ($Z_{0,pk}$) for 0.5 Ω < R_d < 10 Ω and 2 nF < C_d < 10 nF (a). The colored dots highlight the combinations of R_d and C_d whose associated v_{ov} measured waveforms are shown in (b), (c) and (d). Finally, the white dashed line represents the locus of the optimum designs according to [33]. C_b is fixed to 2.5 nF, L_{ext} to 15 nH and R_{ac} to 200 mΩ.

is now required to limit $Z_{0,pk}$ to 3 Ω, given the bigger L_{ext}. In order to understand the correlation between the optimized designs and the value of L_{ext}, the sensitivity of $Z_{0,pk}$ towards L_{ext} is calculated and the results are reported in Fig. 9, where the orange and light green curves are relative to the networks of TABLE V. Given the same C_b = 2.5 nF, the damping network designed for L_{ext} = 15 nH requires only half of the overall capacitance but features four times higher sensitivity compared to the design optimized for L_{ext} = 35 nH. Being $Z_{0,pk}$ the figure-of-merit of the damping network, depending on the application, the second solution could be preferred. In fact, for the first design, considering 152 $\frac{m\Omega}{nH}$ only 10 nH

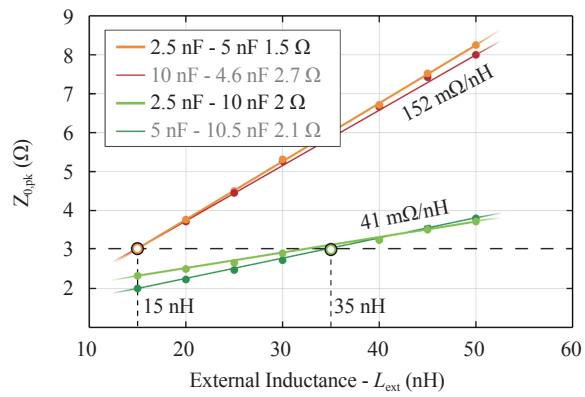


Fig. 9. Sensitivity of Z_0, representing the figure of merit of the C_b-R_dC_d network, towards L_{ext} for different [33]-optimized combinations. When the network is designed ($Z_{0,pk}$ = 3 Ω) for 15 nH (orange and red), the required overall capacitance is less than in the case of 35 nH (light and dark green), however the sensitivity is almost four times higher.

more than expected results in $Z_{0,pk}$ = 4.5 Ω and sub-optimal performance comparable to Fig. 8 (c). This information is important because Lext is typically unknown to the PM designer who is sizing the C_b-R_dC_d network. Consequently, $Z_{0,pk}$ should be set with a certain margin to the desired limit (e.g. $Z_{0,pk}$ = 1.5 Ω to obtain 3 Ω when L_{ext} is 10 nH more than expected) or a worst case L_{ext} should be considered.

The behavior of the two optimized snubbers (TABLE V) is finally examined. The measured peak voltage across R_d amounts to around 50 V in both cases and is therefore not of concern. Differently, the occurring losses could be problematic: in the considered setup, with a switching frequency of 30 kHz, the losses amount to 0.75 W and 1.25 W in the case of L_{ext} = 15 nH and 35 nH respectively. Intuitively, a more critical situation (i.e. L_{ext} = 35 nH) generates more losses to achieve the same performance. Nevertheless, in both cases a power resistor rated for 2 W (*Vishay™ Thin Film* power resistors [37]) can be used, as shown in Fig. 3.

V. Design Procedure Guideline

After clarifying the optimization of the damping network, a guideline of the described procedure for the design of the C_b-R_dC_d network (Section III and IV) is provided in this section (cf. Fig. 10). First, the followed measurements-based approach is considered:

(i) *Worst Case Conditions:* setup the DPT in the worst case scenario, i.e. for the highest V_{dc}, I_{out}, L_{ext} and L_g.

(ii) *Optimization Constraints:* define the safety margins $v_{gs,max}$ and $v_{ov,max}$. Limit the maximum value of C_b and C_d that can be integrated in the PM, e.g. a 1210 ceramic chip (C_{max}) due to limited volume.

(iii) ***Buffer Capacitor:*** measure $v_{ov,pk}$ after a hard turn-off switching transition of T_L in the DPT setup. Iteratively decrease the value of R_g and increase the value of C_b until the highest switching speed (R_g = 0 Ω or v_{gs} > $v_{gs,max}$) limiting $v_{ov,pk}$ < $v_{ov,max}$ with C_b < C_{max} is reached (cf. Fig. 6 (a)). Further increasing L_{ext} only slightly

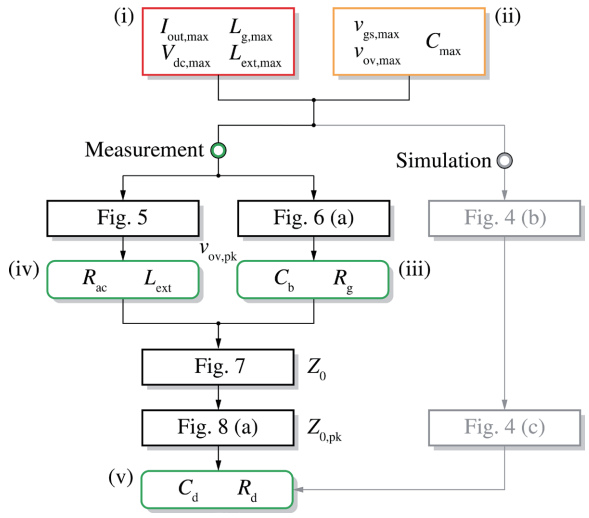


Fig. 10. Flow-chart providing a guideline for the design of the C_b-R_dC_d network as presented in this paper. Set the worst case conditions, the experiments described in Fig. 6 (a) define the required value for C_b, while the procedure presented in Fig. 8 (a) results in the optimized damping network R_dC_d. A simulation based approach, considering the equivalent circuit of Fig. 4 (c), gives accurate results once precise initial conditions and values of the parasitic elements are set.

increases $v_{ov,pk}$ (cf. Fig. 6 (b)).

(iv) *Parasitic Elements:* extract the values of L_{ext} and R_{ac} from the ringing and the damping at v_{ov} (cf. Fig. 5).

(v) ***Damping Network:*** for given C_b, L_{ext} and R_{ac} calculate Z_0 for a defined range of R_d and $C_d < C_{max}$ (cf. Fig. 7). Plot $Z_{0,pk}$ as a function of R_d and C_d (cf. Fig. 8 (a)) and select the R_dC_d pair minimizing $Z_{0,pk}$.

(vi) *Verification:* $v_{ov,pk}$ is reduced further below $v_{ov,max}$ and the oscillation is optimally damped (cf. Fig. 8 (c)). Measure the losses occurring in R_d to guarantee continuous operation. Further increasing L_{ext} only slightly worsen the damping performance (cf. Fig. 9).

If at the end of the procedure the result is too conservative, the constraints on $v_{ov,max}$ and C_{max} can be tightened and the steps from (iii) on repeated. A more compact or more efficient, but as well effective, design is obtained. Differently, if the specifications cannot be met, the mentioned constraints must be loosened or L_{ext} must be reduced.

A simplified simulation-based approach is validated in parallel to the entire analysis. The equivalent circuit shown in Fig. 4 can reproduce the damped and undamped measured waveforms of v_{ov} once all its parameters are correctly set. While the values of the parasitic elements $R_{ac}(f)$, L_{ext} and L_{CL} can be entrusted to FEM simulators, the amplitude of the current step exciting the circuit, i.e. the peak of the switched current $i_{out,pk}$ is unknown. Unfortunately, the capacitive current peak and the reverse recovery current peak, non-linear and correlated to the MOSFETs' characteristics and dynamics, add to the load current i_{out}. Therefore, either full confidence is placed on the *Spice* model of the MOSFETs (when available), or conservative assumptions, based on the MOSFETs datasheet, are necessary. Nevertheless, the analytical approach summarized in Fig. 4 (c) and TABLE IV is valuable, especially for a preliminary analysis of the problem.

Finally, it is worth noticing that the applicability of the guideline can be generally extended to PMs without integrated buffer capacitors and to PCB-based converters where C_{dc} does not find place in the closest proximity of the bridge-leg.

VI. Conclusion

A novel, ultra-low inductance (i.e. 1.6 nH) *All-SiC* PM for *More Electrical Aircraft* application featuring a planar interconnection technology is analyzed in this paper.

Despite the low parasitic inductance of the PM, the full exploitation of SiC power MOSFETs' high switching speed requires precautions concerning switching overvoltages and ringing at the switching node. Measurements proved that the integration of a buffer capacitor is generally an effective measure to minimize the drawbacks associated to the parasitic inductance of the connection to the external capacitor. However, although this solution mitigates the overvoltage, it even aggravates the oscillation, as now a resonant network is formed by the two capacitors and the inductance of the interconnection. Consequently, the integration of a R_dC_d damping network is recommended. At the expenses of only 1 W of losses and in a limited footprint, the switching overvoltage peak is significantly reduced (-80%) and the oscillation is optimally damped. Both solutions are analyzed in detail, optimized for the considered setup, verified with measurements and finally commented.

Ultimately, the designed PM is operated with a gate resistance of only 1.5 Ω (in order to minimize the switching losses) without experiencing any undesired effect due do the achieved high switching speed. This outcome validates the effectiveness of the buffer-damping network and allows the designers to explore the limit performance enabled from *All-SiC* PMs featuring planar interconnection technologies.

Acknowledgment

The authors would like to thank *Siemens*™ AG, in particular O. Raab, for the realization of *ad-hoc All-SiC* 1200 V SiC power modules featuring a planar interconnection technology.

References

[1] J. Bourdon, P. Asfaux, and A. M. Etayo, "Review of power Electronics opportunities to integrate in the More Electrical Aircraft," in *Proc. of the International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS),* Aachen, Germany, 2015.

[2] X. Roboam, B. Sareni, and A. D. Andrade, "More electricity in the air," *IEEE Ind. Electron. Mag.*, vol. 6, no. 4, pp. 6–17, 2012.

[3] *Research and Innovation action, I2MPECT*, European Commission -innovation and networks executive agency, 4 2015.

[4] C. Schner, A. Hensel, and J. C. Zambrano Cambero, "Investigation of 3-level-topology MNPC for aerospace applications with SiC-MOSFETBased power modules," in *Proc. of the IET 8th International Conference on Power Electronics, Machines and Drives (PEMD),* Glasgow, UK, 2016.

[5] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si -evaluation of potentials for performance improvement of inverter

and DC-DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron.,* vol. 58, no. 7, pp. 2872–2882, 2011.

[6] D.-P. Sadik, J. Colmenares, G. Tolstoy, D. Peftitsis, M. Bakowski, and H.-P. Nee, "Short-circuit protection circuits for silicon carbide power transistors," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 1995–2004, 2015.

[7] G. Regnat, P. O. Jeannin, J. Ewanchuk, D. Frey, S. Mollov, and J. P. Ferrieux, "Optimized power modules for silicon carbide MOSFET," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE),* Cincinnatti, OH, USA, 2017.

[8] "*Wolfspeed™ All-SiC* power module," [Online]. Available: www.wolfspeed.com/powerproducts/sic-power-modules, accessed: 2017-03-01.

[9] "*Rohm™ All-SiC* power module," [Online]. Available: www.rohm.com/web/eu/full-sicpower-modules, accessed: 2017-03-01.

[10] "*Semikron™ All-SiC* power module," [Online]. Available: www.semikron.com/innovationtechnology/silicon-carbide-power-modules.html, accessed: 2017-03-01.

[11] M. Kegeleers, J. Koerner, S. Matlok, M. Hofmann, and M. Maerz,"Parasitic inductance analysis of a fast switching 100kW full SiC inverter parasitics of the commutation cell," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe),* Nuremberg, Germany, 2017.

[12] Z. Chen, Y. Yao, W. Zhang, D. Boroyevich, K. Ngo, P. Mattavelli, and R. Burgos, "Development of a 1200V, 120A SiC MOSFET module for high-temperature and high-frequency applications," in *Proc. of the IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA),* Columbus, OH, USA, 2013.

[13] Y. Ren, X. Yang, F. Zhang, L. Tan, and X. Zeng, "Analysis of a low-inductance packaging layout for full-SiC power module embedding split damping," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC),* Long Beach, CA, USA, 2016.

[14] M.Wang, F. Luo, and L. Xu, "An improved wire-bonded power module with double-end sourced structure," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE),* Cincinnatti, OH, USA, 2017.

[15] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET multichip phase-leg module for high-temperature, high-frequency applications," *IEEE Trans. Power Electron.,* vol. 29, no. 5, pp. 2307–2320, 2014.

[16] K. Weidner, M. Kaspar, and N. Seliger, "Planar interconnect technology for power module system integration," in *Proc. of the 7th International Conference on Integrated Power Electronic Systems (CIPS)*, Nuremberg, Germany, 2012.

[17] P. Beckedahl, S. Bütow, A. Maul, and M. Roeblitz, "400A, 1200V SiC power module with 1nH commutation inductance: the problem of high speed switching power module design SKiN technology," in *Proc. of the 9th International Conference on Integrated Power Electronic Systems (CIPS),* Nuremberg, Germany, 2016.

[18] D. Reusch and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high frequency gallium-nitride-based point of load converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2008–2015, 2014.

[19] E. Hoene, A. Ostmann, B. T. Lai, C. Marczok, A. Müsing, and J. W. Kolar, "Ultra-low-inductance power module for fast switching semiconductors," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)*, Nuremberg, Germany, 2013.

[20] P. Beckedahl, M. Spang, and O. Tamm, "Breakthrough into the third dimension sintered multi layer flex for ultra low inductance power modules," in *Proc. of the 8th International Conference on Integrated Power Electronics Systems (CIPS),* Nuremberg, Germany, 2014.

[21] H. Ishino, T. Watanabe, K. Sugiura, and K. Tsuruta, "6-in-1 silicon carbide power module for high performance of power electronics systems," in *Proc. of the IEEE 24th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, San Jose, CA, USA, 2014.

[22] M. Meisser, M. Schmenger, M. Bernd, B. Leyrer, H. Demattio, D. Hamilton, P. Mawby, and T. Blank, "Highly integrated SiC module with thick-film dielectric allows for high frequency operation," in *Proc. of the 9th International Conference on Integrated Power Electronic Systems (CIPS),* Nuremberg, Germany, 2016.

[23] B. Mouawad, J. Li, A. Castellazzi, C. M. Johnson, T. Erlbacher, and P. Friedrichs, "Low inductance 2.5kV packaging technology for SiC switches," in *Proc. of the 9th International Conference on Integrated Power Electronic Systems (CIPS)*, Nuremberg, Germany, 2016.

[24] Z. Q. Wang, X. J. Shi, L. M. Tolbert, F. Wang, Z. X. Liang, D. Costinett, and B. J. Blalock, "A high temperature silicon carbide MOSFET power module with integrated silicon-on-insulator-based gate drive," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1432–1445, 2015.

[25] *C2M0025150D, Cree™*, 10 2015, rev. B.

[26] I. F. Kovačević-Badstübner, R. Stark, M. Guacci, J. W. Kolar, and U. Grossner, "Parasitic extraction procedures for SiC power modules," in *Proc. of the 10th International Conference on Integrated Power Electronics (CIPS)*, Stuttgart, Germany, 2018.

[27] Y. Lobsiger and J. W. Kolar, "Closed-loop IGBT gate drive featuring highly dynamic di/dt and dv/dt control," *IEEE Trans. Power Electron.,* vol. 30, no. 5, pp. 4754–4761, 2012.

[28] S. Guo, L. Zhang, Y. Lei, X. Li, F. Xue, W. Yu, and A. Q. Huang, "3.38 MHz Operation of 1.2kV SiC MOSFET with integrated ultra-fast gate drive," in *Proc. of the IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Blacksburg*, VA, USA, 2015.

[29] *"EPCOS TDK™* Europe power capacitors," [Online]. Available: en.tdk.eu/tdken/1641622/products/product-catalog/film-capacitors/power-capacitors, accessed: 2017-03-01.

[30] R. Blecic, R. Gillon, B. Nauwelaers, and A. Bari, "SPICE analysis of RL and RC snubber circuits for synchronous buck DC-DC converters," in *Proc. of the 38th International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO),* Opatija, Croatia, 2015.

[31] *High Voltage X7R Dielectric, 500 3,000 VDC, Kemet™*, 7 2016.

[32] A. Barkley, M. Schupbach, and A. Scott, "High speed, thermally enhanced, small footprint SiC power modules for cost sensitive applications," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe),* Nuremberg, Germany, 2017.

[33] R. Erickson, "Optimal single resistors damping of input filters," in *Proc. of the 14th Annual Applied Power Electronics Conference and Exposition (APEC),* Dallas, TX, USA, 1999.

[34] B. N. Torsaeter, S. Tiwari, R. Lund, and O. M. Midtgard, "Experimental evaluation of switching characteristics, switching losses and snubber design for a full SiC half-bridge power module," in *Proc. of the 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG),* Vancouver, Canada, 2016.

[35] A. Lemmon, R. Graves, J. Gafford, and C. Bank, "Evaluation of 1.2kV, 100A SiC module for high-frequency, high-temperature applications," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC),* Charlotte, NC, USA, 2015.

[36] W. McMurray, "Optimum snubbers for power semiconductors," *IEEE Trans. Ind.* Appl., vol. IA-8, no. 5, pp. 593–600, 1972.

[37] *High Power Aluminum Nitride, Wraparound Surface Mount, Precision Thin Film Non-Magnetic Chip Resistor (up to 6W), Vishay™*, 6 2016.

Mattia Guacci studied Electronic Engineering at the University of Udine, Italy where in July 2013 and in October 2015 he received his B.Sc. summa cum laude and his M.Sc. summa cum laude, respectively. In 2014 he was with Metasystems SpA in Reggio nell'Emilia, Italy working on EV onboard battery chargers. In November 2015 he joined the Power Electronic Systems Laboratory (PES) at ETH Zurich as a scientific assistant investigating innovative inverter topologies. In September 2016 he started his Ph.D. at PES focusing on integrated modular high efficiency and weight optimized power electronic converters for aircraft application.

Dominik Bortis received the M.Sc. degree in electrical engineering and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2005 and 2008, respectively. In May 2005, he joined the Power Electronic Systems Laboratory (PES), ETH Zurich, as a Ph.D. student. From 2008 to 2011, he has been a Postdoctoral Fellow and from 2011 to 2016 a Research Associate with PES, co-supervising Ph.D. students and leading industry research projects. Since January 2016 Dr. Bortis is heading the newly established research group Advanced Mechatronic Systems at PES.

Ivana F. Kovăcević-Badstübner received the Dipl.Ing degree from the Faculty of Electrical Engineering, Department for Electronics, the University of Belgrade, Serbia, in 2006 (with Hons.) and the M.Sc. and Ph.D. degrees in Electrical Engineering and Information Technology from the Swiss Federal Institute of Technology (ETH Zurich), Switzerland, in 2008 and 2012, respectively. From 2008 to 2012, she was Ph.D. student in the Power Electronic Systems (PES) laboratory at ETH Zurich. From 2012, she continued as Post-Doctoral researcher and further as project scientist in the PES Laboratory working on the lifetime modeling of power semiconductor modules, the multi-domain modeling and optimization of power electronic systems and components, and the prediction of electromagnetic behavior of power electronics circuits based on the developed numerical techniques. In March 2016, she joined the Advanced Power Semiconductor Laboratory at ETH Zurich. Her research interests include novel packaging technologies for SiC devices, the optimization of power module layout with respect to electromagnetic interference, and multi-domain modelling of power semiconductor devices and their modules.

Ulrike Grossner earned the Dipl.-Phys. and the Dr. rer. nat. degree from the Friedrich-Schiller-University Jena, Germany in 1997 and 2000, respectively. In 2014, she was appointed Full Professor at ETH Zurich, Switzerland, where she established the Advanced Power Semiconductor Laboratory (APS), working on devices and packaging for advanced power semiconductors.

Johann W. Kolar received his M.Sc. and Ph.D. degree (summa cum laude / promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria, in 1997 and 1999, respectively. Since 1984, he has been working as an independent researcher and international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel PWM converter topologies, and modulation and control concepts and has supervised over 60 Ph.D. students. He has published over 650 scientific papers in international journals and conference proceedings, 3 book chapters, and has filed more than 140 patents. The focus of his current research is on ultra-compact and ultra-efficient SiC and GaN converter systems, wireless power transfer, solid-state transformers, power supplies on chip, and ultra-high speed and bearingless motors. Dr. Kolar has received 23 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Middlebrook Award, and two ETH Zurich Golden Owl Awards for excellence in teaching. He initiated and/or is the founder of four ETH Spin-off companies. He is a member of the steering committees of several leading international conferences in the field and has served from 2001 through 2013 as an Associate Editor of the IEEE Transactions on Power Electronics. Since 2002 he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering.