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# Comprehensive Conceptualization, Design, and Experimental Verification of a Weight-Optimized All-SiC 2 kV/700 V DAB for an Airborne Wind Turbine

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**Abstract**—This paper details the design, implementation, and experimental verification of a minimum weight input series output parallel structured dual active bridge (DAB) converter for an airborne wind turbine system. The main power components of the DAB converter, particularly the bridge circuits, the actively cooled high-frequency transformer and inductor, and the cooling system, which largely contribute to the total system weight, are designed and realized based on multiobjective considerations, i.e., with respect to weight and efficiency. Furthermore, the design includes all necessary considerations to realize a fully functional prototype, i.e., it also considers the auxiliary supply, the control for a stable operation of the system, which also comprises an input filter, over the specified operating range, and the start-up and shut down procedures. These considerations show the complex interactions of the various system parts and reveal that a comprehensive conceptualization is necessary to arrive at a reliable minimum weight design. Experimental results validate the proposed design procedure for a realized lightweight DAB hardware prototype with a rated power of 6.25 kW. The prototype weighs 1.46 kg, i.e., features a power-to-weight ratio of 4.28 kW/kg (1.94 kW/lb), and achieves a maximum full-load efficiency of 97.5%.

**Index Terms**—Aerospace electronics, airborne wind turbine (AWT), dc–dc power converters, power electronics, renewable energy, wind power generation.

## I. INTRODUCTION

INCREASING consumption of electric energy, environmental issues, and limited availability of fossil fuels have led to a multitude of developments related to the generation of electricity from renewable energy sources. One innovative system in this context is the airborne wind turbine (AWT) detailed in [1], which generates electricity from high-altitude winds. High-altitude winds are known to be more stable and faster than the winds close to the ground level and thus enable a more reliable and effective generation of electric energy [1], [2]. The considered AWT is a flying wing with

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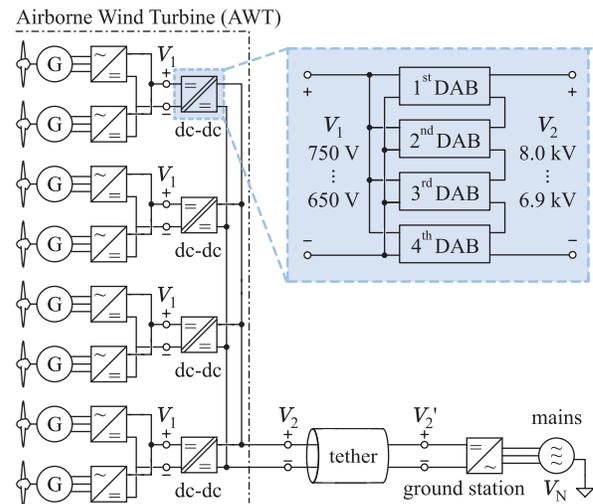


Fig. 1. Electrical system of the AWT. Four bidirectional dc–dc converters link eight voltage source rectifiers to a power transmission tether ( $\approx 1$  km). The ground station, i.e., a bidirectional dc–ac converter, connects the tether to the three-phase grid. Four single converter cells form a bidirectional dc–dc converter with a dc port voltage  $V_2$  of up to 8 kV.

air-powered on-board power generators and is tied to the ground with an approximately 1-km-long tether. The tether, a combination of fiber and cable, provides both the required mechanical strength and the electrical link to the ground station [1]–[4], which is connected to the medium-voltage (MV) grid.

The greatest challenge with respect to the realization of the electric system of the considered AWT, with a total maximum input power of 100 kW, is to achieve a lightweight tether [1]–[4], lightweight generators [1], [5]–[10], and power converters [1], [11]–[27]. From related investigations detailed in [1], the electrical system shown in Fig. 1 emerges, which uses low-voltage (LV) generators and inverters, operated from a dc bus voltage ranging from 650–750 V, dc–dc converters that convert the LV dc bus voltage into a high tether voltage of up to 8 kV, the tether itself, and the ground station. The AWT system considers four identical dc–dc converters for safety reasons. With the proposed electrical system structure, a failure of any on-board power conversion system component will result at most in the loss of two propulsion systems.

TABLE I  
SPECIFICATIONS FOR THE AWT DC–DC TRANSMISSION SYSTEM

	AWT	DC–DC Converter	Converter Cell
input voltage	$650 \text{ V} < V_1 < 750 \text{ V}$		
output voltage	$6.9 \text{ kV} < V_2 < 8 \text{ kV}$	$1733 \text{ V} < V_{2,i} < 2 \text{ kV}$	
rated power	100 kW	25 kW	6.25 kW
allowable weight	25 kg	6.25 kg	1.65 kg

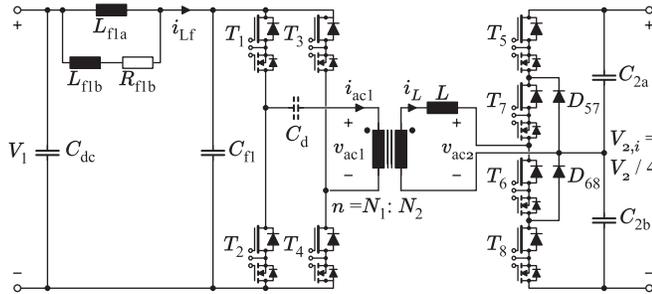


Fig. 2. Modified DAB converter topology used to realize a single cell of the bidirectional dc–dc converter. The rated output power is 6.25 kW, the maximum MV side port voltage is 2 kV, and the maximum allowed weight is 1.65 kg.

In the case of a system malfunction, six propellers provide sufficient propulsion to safely land the AWT for maintenance. Furthermore, each dc–dc converter is composed of four single converter cells that are arranged in an input series output parallel (ISOP) structure, i.e., the cells are connected in parallel on the LV side and in series on the high-voltage side in order to reduce the maximum tether side port voltage of each converter cell to 2 kV. The complete electrical system needs to allow for bidirectional energy transfer at rated power in order to enable the start-up of the AWT. These and further considerations presented in [1] yield the specifications for the dc–dc transmission system summarized in Table I. Each converter cell is essentially a dual active bridge (DAB) converter with a full-bridge (FB) circuit on the LV side (dc port voltage  $V_1$ ), a high-frequency (HF) transformer and inductor, and a neutral point clamped (NPC) circuit on the high-voltage side [dc port voltage  $V_{2,i}$  (Fig. 2)].

A literature research on lightweight power electronic converters reveals current publications to focus on the following three main topics:

- 1) *Semiconductors*: Highly efficient power converters, and converters operated at high temperatures [1], [12]–[16]. The high-efficiency/temperature operation reduces the system weight predominately by reducing the cooling system requirements.
- 2) *Lightweight Magnetic Components*: Multiphysics modeling and design optimization of transformers and inductors in reference to the geometric optimization, magnetic material properties, medium/HF operation, and high-voltage isolation stress analysis [18]–[24].
- 3) *Cooling Systems*: Optimizations that yield cooling systems, which feature minimal weight for a required thermal resistance [25]–[27].

However, so far, no fully functional design of a lightweight converter system that includes a comprehensive description

of all relevant interactions of different converter components and further aspects has been presented. No experimental verification of the achievable performance in terms of a power-to-weight ratio in kW/kg (or kW/lb) for a 2 kV/700 V isolated bidirectional dc–dc converter exists to the best of our knowledge. Because the weight of a fully functional power electronics converter provides the only meaningful measure, any weight-optimized converter must also include, besides its main functionality, the auxiliary supply, considerations on the analysis of stability of the control over the specified operating range, which involves the considerations on the input filter design. Furthermore, e.g., the size and the weight of capacitor  $C_{dc}$  (see Fig. 2) depend on the design of the control and associated delay time, which in turn depend on the hardware implementation of the control circuitry.

This paper presents a comprehensive overall design method for the realization of a weight-optimized 2 kV/700 V DAB converter and, in order to include most recent findings, it revisits and refines the corresponding contents in [1], [16], and [27]. In this context, the design procedures for the remaining converter components that are required for the converter operation and the integration into the final electrical AWT system, e.g., gate drivers, digital control, filters, and auxiliary power supplies, are thoroughly explained.

The weight optimization of a power converter involves not only the weights of the power components themselves but also the components' dissipated losses, since the weight of the cooling system increases with increasing losses and may substantially contribute to the total converter weight. For this reason, the presented weight-optimized design is performed as multiobjective optimization and takes, besides the actual components' weights, the losses of the converter components and the associated weight of the optimized cooling system into account. The task of minimizing the weight of the complete DAB converter system is split into the subtasks listed as follows:

- 1) selection of a suitable switching frequency that allows for a lightweight converter realization;
- 2) efficient operation of the DAB and the calculation of corresponding turns ratio  $n$  and inductance  $L$  in Section II-A;
- 3) selection of the most suitable power semiconductors (see Section II-B);
- 4) analytical multiobjective optimization of the DAB transformer and inductor in Section II-C;
- 5) weight optimization of the cooling system in Section II-D;
- 6) realization of filter networks (Section II-E);
- 7) *implementation of the control circuitry*: consideration of aspects related to the converter weight (Section III);
- 8) lightweight auxiliary power supplies (Section IV-A).

The switching frequency denotes a key design parameter: at very low switching frequencies, heavy passive components result, and at very high switching frequencies, high switching losses, core losses, and HF losses result. In this paper, it has been assumed that the sensitivity of the final converter weight with respect to the switching frequency is relatively low for a

switching frequency close to the optimal switching frequency, i.e., a flat optimum. For this reason, the complete AWT system has initially been optimized for six different switching frequencies ( $f_s = 50$  kHz, 80 kHz, 100 kHz, 125 kHz, 160 kHz, and 200 kHz), using simplified models and practice-oriented assumptions; the obtained results suggest a switching frequency of approximately 100 kHz. With the determined switching frequency, the remaining items 2)–8) of the list can be processed in the given sequence in order to optimize the DAB converter with respect to minimum weight. Finally, Section V presents the experimental results demonstrating the achieved performance of 4.28 kW/kg (1.94 kW/lb) of a prototype system, and this paper concludes with an outlook in Section VI.

## II. MINIMUM WEIGHT POWER CONVERTER

This section details the design or the selection of power components suitable for a lightweight power converter, i.e., power semiconductors, HF transformer and inductor, and the components of the filter networks. Prior to this, however, the converter's turns ratio,  $n$ , and HF inductance,  $L$ , need to be determined in order to allow for the calculation of all operating-point-dependent voltage and current waveforms the DAB converter is subject to.

### A. Optimal Converter Operation, Optimal $n$ and $L$

The investigated DAB converter is operated most efficiently at  $V_1/n \approx V_{2,i}/2$  with the conventional phase shift modulation (CPM) scheme [28]. Thus, the turns ratio of the DAB transformer is

$$n = \frac{V_1}{V_{2,i}/2} = \frac{750 \text{ V}}{1 \text{ kV}} = 0.75. \quad (1)$$

The CPM scheme needs to be slightly modified, since the MV side NPC converter requires a minimum freewheeling time of 250 ns in order to ensure an equal distribution of the blocking voltages across the switches  $T_5, \dots, T_8$  [16]. With this, the voltage and the current waveforms shown in Fig. 3(a) result, i.e., a maximum duty cycle of the NPC converter of  $D_2 = (0.5 - 250 \text{ ns} \cdot f_s) = 0.475$  results. The corresponding maximum allowable DAB inductance,  $L$ , for a maximum duty cycle of the NPC converter and the specified rated power is determined with

$$L = \frac{\min(V_1 V_{2,i})}{4n f_s \frac{P_{i,\max}}{\eta_{\text{exp}}}} \left[ \frac{\varphi_{\max}}{\pi} \left( 1 - \frac{\varphi_{\max}^2}{\pi^2} \right) - \left( \frac{1}{2} - D_2 \right)^2 \right] = 107 \text{ } \mu\text{H} \quad (2)$$

calculated for  $P_{i,\max} = 6.25$  kW, a conservative value of the expected efficiency,<sup>1</sup>  $\eta_{\text{exp}} = 95\%$ , and the maximum steady-state phase angle  $\varphi_{\max} = \pi/4$  (in order to maintain a good controllability at low output power, typically

<sup>1</sup>For a more accurate estimation of the expected efficiency, it needs to be part of the converter optimization, i.e.,  $\eta_{\text{exp}}$  is a result of each particular converter design. However, a relatively small impact of a minor change of  $\eta_{\text{exp}}$ , e.g., from 95%–97.5%, on the final losses and total weight is expected and, therefore,  $\eta_{\text{exp}} = 95\%$  is maintained throughout the whole converter design procedure. The conservative value of 95% is selected in order to take a slight safety margin for the required cooling system into account.

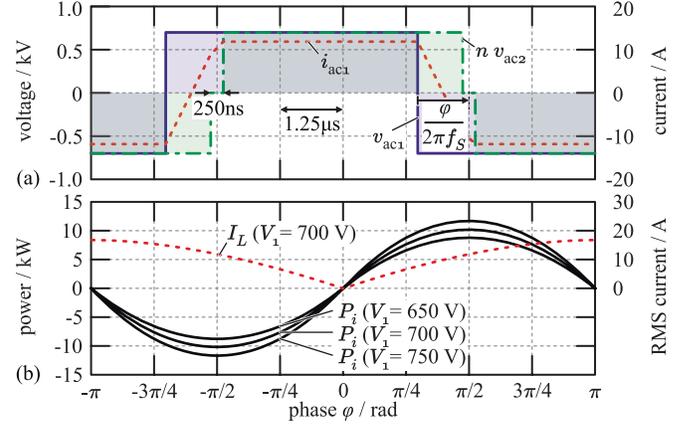


Fig. 3. (a) Voltage and current waveforms calculated for a single DAB converter ( $V_1 = 700$  V,  $V_{2,i} = 1.9$  kV,  $P_i = 6.25$  kW/ $\eta_{\text{exp}}$ ,  $\eta_{\text{exp}} = 95\%$ ,  $n = 0.75$ ,  $L = 107$   $\mu\text{H}$ , and  $f_s = 100$  kHz); the NPC converter on the MV side requires a freewheeling time of 250 ns. (b) Power transfer characteristics of the DAB (see [28]),  $V_1/V_{2,i} = 0.375 = \text{constant}$ ; maximum power transfer is achieved for  $\varphi = \pm\pi/2$ . Dashed line: rms inductor current  $I_L(\varphi)$  at the nominal operation.

TABLE II  
TRANSFORMER, CAPACITOR, AND SEMICONDUCTOR CURRENTS  
OF A SINGLE DAB CONVERTER MODULE WITH  
 $P_i = 6.25$  kW/ $\eta_{\text{exp}}$  AND  $\eta_{\text{exp}} = 95\%$  [1]

Property	Value	Description
$\max(I_{ac1})$	12.2 A	Max. rms transformer current, LV side
$\max(I_L)$	9.2 A	Max. rms transformer current, MV side
$\max(I_{L,\text{peak}})$	10.2 A	Max. peak inductor current
$\max(I_{T_1})$	8.65 A	Max. rms current in switches $T_1 \dots T_4$
$\max(I_{T_5})$	6.5 A	Max. rms current in switches $T_5 \dots T_8$
$\max(I_{C1})$	7.0 A	Max. rms capacitor current of $C_{f1}$
$\max(I_{C2})$	5.0 A	Max. rms capacitor current of $C_{2a}$ and $C_{2b}$

$\varphi_{\max} \in [\pi/4, \pi/3]$ ). With known values of  $n$  and  $L$ , the characteristic converter currents can be calculated using the methods presented in [28]. These currents are summarized in Table II.

### B. Power Semiconductors

SiC power semiconductors are considered to be most suitable with respect to low losses and, subsequently, low weights of the heat sinks required for active cooling. For the MV side NPC converter, normally ON SiC JFETs in a TO-247 package with breakdown voltages of 1700 V and low ON-state resistances of 150 m $\Omega$  at 125  $^\circ\text{C}$  are selected. Each SiC JFET is connected in series to a LV p-channel Si MOSFET (FDMS6681Z,  $R_{DS,ON} = 3.2$  m $\Omega$ ), and a gate driver especially dedicated to SiC JFETs operates both devices (here Infineon's 1EDI30J12CP EiceDriver is used), to gain normally OFF properties. The LV side FB converter employs SiC JFETs with breakdown voltages of 1200 V and ON-state resistances of 100 m $\Omega$  at 125  $^\circ\text{C}$ . Again, one LV p-channel Si MOSFET (FDMS6681Z,  $R_{DS,ON} = 3.2$  m $\Omega$ ) is connected

in series to each JFET, and the 1EDI30J12CP EiceDriver is used.<sup>2</sup>

1) *Considered Weight*: The weight attributed to the power semiconductors is equal to the sum of the weights of the eight JFETs, p-channel MOSFETs, and gate drivers, and the belonging PCB. This weight does not include the cooling systems' weights, which are separately considered in Section II-D.

The total weight of all JFETs and p-channel MOSFETs is  $m_{\text{semi}} = 48.8$  g, and the PCB and connector's weight is 49 g. The total weight of all gate drivers is  $m_{\text{drv}} = 24$  g. This includes eight 1EDI30J12CP EiceDriver devices, the connected SMD resistors and capacitors, and the corresponding part of the PCB with an estimated total surface of 500 mm<sup>2</sup> (for the two layer PCB with a height of 1.6 mm, an average density of 2.24 g/cm<sup>3</sup> is assumed).

2) *Conduction and Switching Losses*: For the optimization of the cooling system, presented in Section II-D, the losses generated by the converter's semiconductors need to be known. The considered loss model accounts for conduction and switching losses.

The conduction losses are calculated based on the ON-state channel resistance at an assumed junction temperature of 125 °C (see [29])

$$P_{T_{1,2,3,4},\text{cond}} = 4 \cdot R_{\text{DS,ON,I}} I_{T_{1,2,3,4},\text{rms}}^2 = 4 \cdot R_{\text{DS,ON,I}} \frac{I_{\text{ac1,rms}}^2}{2} \quad (3)$$

$$P_{T_{5,6,7,8},\text{cond}} = 4 \cdot R_{\text{DS,ON,II}} I_{T_{5,6,7,8},\text{rms}}^2 = 4 \cdot R_{\text{DS,ON,II}} \frac{I_{L,\text{rms}}^2}{2} \quad (4)$$

with  $R_{\text{DS,ON,I}} = 100$  mΩ and  $R_{\text{DS,ON,II}} = 150$  mΩ.

In the realized converter prototype, each previously used cascode circuit of a JFET and an n-channel MOSFET (see [16]) is replaced by a series connection of a JFET and a p-channel MOSFET in order to reduce the effective output capacitance of each power switch and to achieve a further reduction of the switching losses. Dedicated gate drivers featuring direct drive technology (1EDI30J12CP manufactured by Infineon) ensure normally OFF properties of the power switches. The corresponding switching losses have been measured according to [16] (double pulse measurement) on the final converter PCB in order to account for the implications of parasitic components, e.g., the inductance of the commutation loop. The JFETs are thermally connected to a heat plate to enable switching loss measurements at different junction temperatures ( $T_j = 25$  °C and 125 °C are considered). Different switching operations result for the half-bridge (HB) and the NPC converters, due to structural differences of these circuits. In this context, the reader is kindly referred to [1],

<sup>2</sup>No competitive SiC MOSFETs have been available at the time when the design of the investigated converter has started. Meanwhile, competitive 1200 V MOSFETs are available. Thus, the SiC JFETs of the LV side FB could be replaced by SiC MOSFETs (e.g., C2M0025120D manufactured by CREE), which would lower the losses at full load by approximately 20 W and increase the full-load efficiency by 0.3%. Thus, some further weight reduction is feasible with SiC MOSFETs, since the series-connected LV p-channel MOSFETs are not required. The lower losses, furthermore, would allow a slight reduction of the weight of the heat sink.

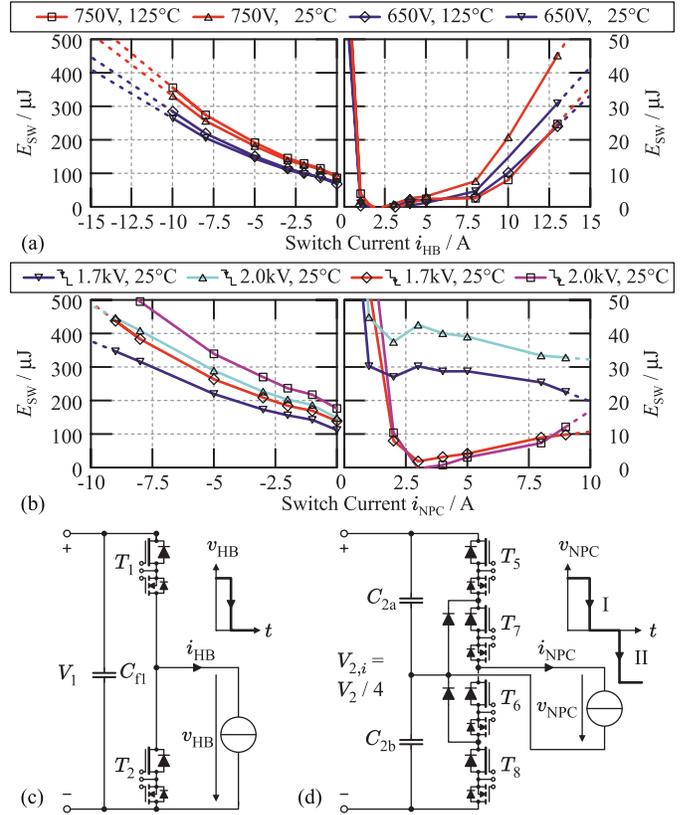


Fig. 4. Measured SiC JFET switching energies with the (1EDI30J12CP) and external gate resistances  $\{R_{\text{OFF}}, R_{\text{ON}}\} = \{1 \Omega, 2.6 \Omega\}$  being used. (a) Infineon IJW120R070T1 1.2 kV/70 mΩ in an HB configuration. (b) Infineon sample 1.7 kV/100 mΩ in an NPC configuration. (c) and (d) Circuit diagrams used to measure the switching energies in (a) and (b), respectively.

which thoroughly discusses the respective details. In summary, the switching losses of a HB converter, shown in Fig. 4(a), thus only depend on the instantaneous port voltage,  $V_1$ , and output current,  $i_{\text{HB}}$ . The switching losses of the NPC converter [Fig. 4(b)] additionally depend on the previous states of the switches  $T_5$ – $T_8$ : for the NPC converter, different switching losses result if  $v_{\text{NPC}}$  switches from  $\pm V_{2,i}$  to zero [edge with label I in Fig. 4(d)] or if  $v_{\text{NPC}}$  switches from zero to  $\pm V_{2,i}$  (Edge II).

Fig. 4(a) shows the switching losses measured for the FB converter at  $V_1 = 650$  V and 750 V and  $T_j = 25$  °C and 125 °C. For positive currents  $i_{\text{HB}}$ , the condition for ZVS is, theoretically, fulfilled and for negative currents  $i_{\text{HB}}$  hard switching occurs. According to these results, low switching losses of less than 10  $\mu\text{J}$  can be achieved for 1 A  $< i_{\text{HB}} < 8$  A.

Fig. 4(b) shows the results obtained for the NPC converter. Similar switching losses are measured for the HB and the NPC converter if the switching operation labeled I in Fig. 4(d) is present. For 2 A  $< i_{\text{NPC}} < 10$  A, increased switching losses result for Edge II, due to residual turn-ON losses [1].

In Fig. 4(a) and (b), there is a rapid increase in the switching energies when the current is approaching zero. For currents 0  $< i_{\text{HB}} < 1$  A and 0  $< i_{\text{NPC}} < 2$  A, the semiconductor's effective output capacitances are incompletely charged or discharged during the dead-time intervals, i.e., residual

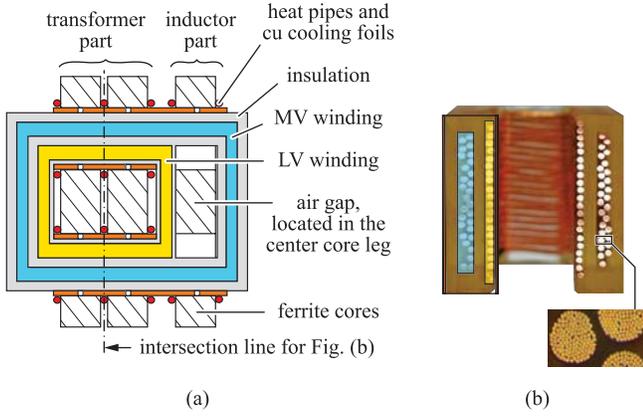


Fig. 5. (a) Considered configuration of the actively cooled HF transformer and inductor (from [1]). (b) Cross section cut through the realized transformer windings showing the HF litz wires being embedded in the epoxy resin, which is used for the isolation; the turns ratio is  $n = N_{LV}/N_{MV} = 21/28$ , both the HF litz are  $200 \times 71 \mu\text{m}$ . The magnified image in the bottom-right corner enables a detailed view on the embedded HF litz wire.

drain-to-source voltages remain for the switches that are turned ON after the dead-time intervals elapsed and, as a consequence, hard switching operations with turn ON losses result [30].

The switching losses generated by the switches  $T_1 \dots T_4$  and  $T_5 \dots T_8$  are calculated with

$$P_{T_{1,2,3,4},sw} = 2f_s[E_{sw}(V_1, i_{HB1}, T_j) + E_{sw}(V_1, i_{HB2}, T_j)] \quad (5)$$

$$P_{T_{5,6,7,8},sw} = 2f_s[E_{sw,I}(V_{2,i}, i_{NPC1}, T_j) + E_{sw,II}(V_{2,i}, i_{NPC2}, T_j)] \quad (6)$$

respectively;  $i_{HB1}$ ,  $i_{HB2}$ ,  $i_{NPC1}$ , and  $i_{NPC2}$  denote the instantaneous switch currents at switching, i.e.,  $i_{HB1}$  denotes the current switched by  $T_1$  and  $T_2$ ,  $i_{HB2}$  is the current switched by  $T_3$  and  $T_4$ ,  $i_{NPC1}$  is the current switched by  $T_5$  and  $T_6$ , and  $i_{NPC2}$  is the current switched by  $T_7$  and  $T_8$  [see Figs. 2 and 4(c) and (d)]. The switching energies are, in the case of negative slopes of the voltages  $v_{HB}$  and  $v_{NPC}$ , evaluated for currents  $i_{HB}$  and  $i_{NPC}$  flowing in the directions defined in Fig. 4(c) and (d), respectively. The switching energies for positive and negative voltage slopes are equal, since in the steady-state operation, only the signs of the bridges' output voltages and currents change during the second half of the switching period.

### C. Optimization of the DAB Transformer and Inductor

The optimization of the DAB transformer and inductor is based on the configuration shown in Fig. 5(a), where both the transformer and the inductor employ ferrite E-cores; the selected configuration realizes active cooling by means of the depicted copper plates and heat pipes, which conduct copper and core losses to a heat sink. The theoretical optimization is conducted in [1], and the obtained results are used for realization; Table III lists the design parameters of the finally implemented DAB transformer and inductor. Compared with the previously obtained optimization results presented in [1], HF litz wires with increased numbers of strands are used in order to lower the maximum hot-spot temperatures of the LV and the MV side windings. The hot spots are located in

TABLE III  
PARAMETERS OF THE DAB TRANSFORMER AND INDUCTOR

Transformer core:	2 stacked E42/21/20 core sets
Inductor core:	single E42/21/20 core set
Number of turns:	$N_{LV} = 21$ , $N_{MV} = 28$
Employed HF litz wire, LV side:	$200 \times 0.071 \text{ mm}$
Employed HF litz wire, MV side:	$200 \times 0.071 \text{ mm}$
Inductor air gap length:	$l_{air} = 3.3 \text{ mm}$

the windings' end turns, where the selected active cooling setup is least effective. Furthermore, the formerly suggested insulation material, Teflon, has been replaced by epoxy resin in order to eliminate the creepage path between the adjacent transformer windings and between the windings and the core. The MV side winding is surrounded with 2-mm-thick epoxy resin and is considered to withstand dc voltages of more than 10 kV [31]–[34]. Fig. 5(b) shows a cross-sectional view through the LV and the MV side transformer windings, embedded in epoxy resin, and reveals that the enlarged HF litz wires could still be situated into the available space. The weight of the realized DAB transformer and inductor, including the copper plates, and the heat pipes is 522 g.

### D. Minimum Weight Cooling System

The DAB converter requires a cooling system with three separate heat sinks to dissipate the heat generated by the JFETs of the NPC and the FB converters and to actively cool the HF transformer and inductor. Due to the ISOP structure of the dc–dc converter system (see Fig. 1), voltages up to 4.75 kV are present between the LV and the MV sides of the first and the fourth DAB converters. Therefore, the galvanic isolation between the MV side heat sink and all LV side components, including the heat sink used to cool the HF transformer and inductor, of which the core is referred to the potential of the minus port of the LV side, needs to be designed accordingly. Furthermore, the heat sink used for the switches of the FB converter is thermally isolated from the heat sink used to cool the magnetic components, because these heat sinks are operated on different temperatures.<sup>3</sup>

The design of the cooling system is based on the previously calculated maximum losses given in [16],<sup>4</sup> which are

$$P_{loss,FB} = 57 \text{ W}, \quad P_{loss,NPC} = 50 \text{ W}, \quad P_{loss,mag} = 80 \text{ W}.$$

Fig. 6 shows the equivalent thermal networks for all three cooling systems. The thermal networks shown in Fig. 6(a) and (b) consider one heat source per JFET, the corresponding junction-to-case thermal resistances,  $R_{th,j-c}$ , the thermal resistances of the isolating thermal interfaces,  $R_{th,c-hs}$ , and the thermal resistances

<sup>3</sup>In the case of a common heat sink for the LV side FB converter and the magnetic components, the LV side semiconductors would heat up the magnetic components additionally.

<sup>4</sup>The revision of the switching loss measurements, using the direct drive technology, presented in Section II-B has been carried out with the final converter setup, which already required the fully functional cooling system. For this reason, the achieved reduction of the switching losses was unknown at the time the cooling system was designed.

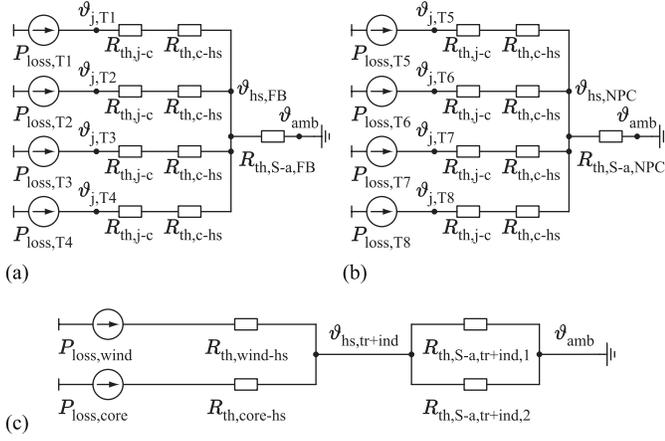


Fig. 6. Thermal networks of the three cooling systems. (a) LV side semiconductors. (b) MV side semiconductors. (c) Transformer and inductor.

of the heat sinks themselves. For reliability, the junction temperatures are limited to  $120\text{ }^{\circ}\text{C}$ . With this, the thermal resistances shown in Fig. 6, and the losses listed in [16], the worst case base plate temperatures of the heat sinks required for the FB and the NPC converters are

$$\vartheta_{\text{hs,max,FB}} = 120\text{ }^{\circ}\text{C} - 14.25\text{ W} \times 0.94\text{ K/W} = 106\text{ }^{\circ}\text{C} \quad (7)$$

$$\vartheta_{\text{hs,max,NPC}} = 120\text{ }^{\circ}\text{C} - 12.5\text{ W} \times 0.94\text{ K/W} = 108\text{ }^{\circ}\text{C} \quad (8)$$

respectively. With a maximum allowed operating ambient temperature of  $\vartheta_{\text{amb,max}} = 40\text{ }^{\circ}\text{C}$ , the thermal resistance required for the two heat sinks is calculated according to

$$R_{\text{th,S-a,max,FB}} = \frac{\vartheta_{\text{hs,max,FB}} - \vartheta_{\text{amb,max}}}{4 \times 14.25\text{ W}} = 1.17\text{ K/W} \quad (9)$$

$$R_{\text{th,S-a,max,NPC}} = \frac{\vartheta_{\text{hs,max,NPC}} - \vartheta_{\text{amb,max}}}{4 \times 12.5\text{ W}} = 1.37\text{ K/W}. \quad (10)$$

A similar calculation is conducted for the heat sink used to cool the HF transformer and inductor, which leads to the corresponding base plate temperature and the required thermal resistance of the heat sink

$$\vartheta_{\text{hs,max,mag}} = 77\text{ }^{\circ}\text{C} \quad (11)$$

$$R_{\text{th,S-a,max,tr+ind}} = \frac{\vartheta_{\text{hs,max,mag}} - \vartheta_{\text{amb,max}}}{80\text{ W}} = 0.46\text{ K/W}. \quad (12)$$

In the quest for achieving a minimum weight DAB converter, different heat sink configurations have been investigated, and the configuration shown in Fig. 7, which employs four heat sink halves, has been identified to be most suitable with respect to minimum weight. Two heat sink halves are used to cool the HF transformer and inductor (due to the comparably low value of  $R_{\text{th,S-a,max,tr+ind}}$ , i.e., a relatively high cooling capability is required) and the remaining two halves cool the HB and the NPC converters, respectively. The heat sink used to cool the magnetic components requires a base plate size of  $A_{\text{hs,tr+in}} = 40\text{ mm} \times 80\text{ mm}$  to accommodate all heat pipes and ferrite cores. The same base plate size is used for the remaining two heat sink halves in order to allow for a simplified construction of the DAB converter and to allow for sufficiently large

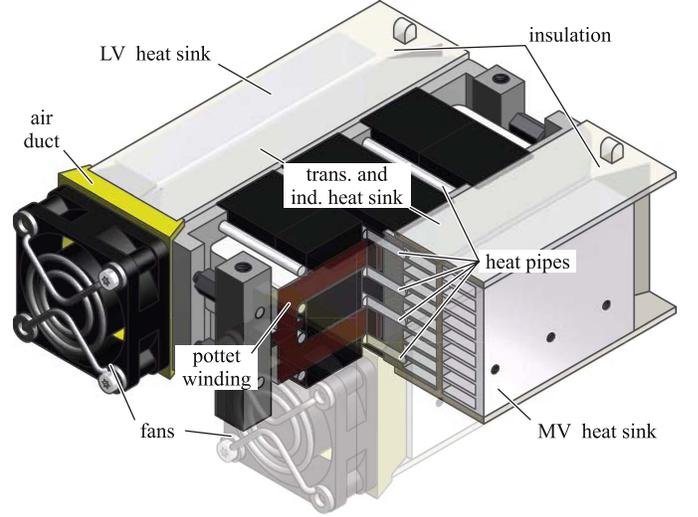


Fig. 7. CAD model of the final cooling system configuration. Heat pipes from the transformer and inductor connect to the heat sinks on both sides. Thermal and electrical insulation separates the heat sinks for the LV and the MV side semiconductors from the heat sinks cooling the transformer and inductor.

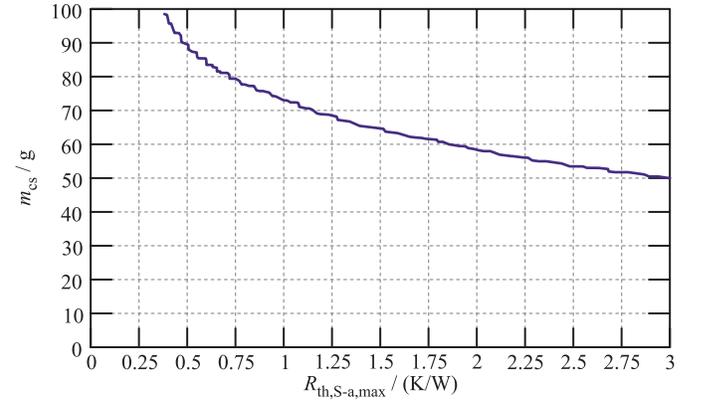


Fig. 8. Minimum cooling system weights, calculated with the optimization algorithm detailed in [27], for different base plates to ambient thermal resistances of the different cooling system halves, i.e.,  $m_{\text{cs}} = m_{\text{heat sink halve}} + (m_{\text{fan}} + m_{\text{duct}} + m_{\text{iso}})/2$ . Only the  $40\text{ mm} \times 40\text{ mm}$  fans in Table IV are considered.

distances between adjacent JFETs due to voltage isolation requirements.

Fig. 8 shows the minimum cooling system weights, calculated with the optimization algorithm detailed in [27], for different base plates to ambient thermal resistances of the different cooling system halves, i.e.,  $m_{\text{cs}} = m_{\text{heat sink halve}} + (m_{\text{fan}} + m_{\text{duct}} + m_{\text{iso}})/2$ ; this optimization considers the fans listed in Table IV. Because the airflows through the heat sinks are coupled, only symmetric heat sink geometries are considered, i.e., the heat sinks cooled by one fan feature the same pressure drop characteristics. The properties of the resulting minimum weight cooling systems are listed in Table V. The total weight of the cooling system is

$$\begin{aligned} m_{\text{cs,total}} &= m_{\text{cs,FB}} + m_{\text{cs,tr+ind}} + m_{\text{cs,NPC}} \\ &= (75 + 2 \times 75 + 75)\text{ g} = 300\text{ g}. \end{aligned} \quad (13)$$

TABLE IV

40 mm × 40 mm AXIAL FANS CONSIDERED IN THE OPTIMIZATION

Name	$\frac{P_{fan}}{W}$	$\frac{L_{fan}}{mm}$	$\frac{m_{fan}}{g}$	$\frac{\dot{V}_{max}}{dm^3/s}$	$\frac{\Delta p_{max}}{Pa}$
GM0504PEV2-8.GN	0.4	6	7.5	2.6	20.0
MC19660	0.5	6	7.5	2.8	25.0
BP402012H-W	1.9	20	40.0	4.0	51.7
1608VL-04W-B60-B00	1.6	20	40.0	5.4	99.3
9GA0412G7001	2.0	15	28.0	6.0	192.0
9GA0412P6G001	2.8	20	35.0	7.1	319.2
412JHH	3.3	25	50.0	6.7	216.3
9L0412J301	3.7	28	55.0	8.5	205.1
9GV0412P3K03	10.1	28	50.0	12.7	416.2
1611FT-D4W-B86-B50	11.4	28	49.0	13.8	736.9
1619FT-04W-B86-B50	12.6	48	71.0	14.1	800.0

TABLE V

COOLING SYSTEM PROPERTIES THAT FEATURE SYMMETRIC HEAT SINKS FOR ALL THREE COOLING SYSTEMS

	MV side NPC	LV side FB	Transformer and ind.
$R_{th,S-a}$	0.97 K/W	0.97 K/W	$1/2 \times 0.97$ K/W
$m_{cs}$	75 g	75 g	150 g
$n$	9	9	9
$c$	12 mm	12 mm	12 mm
fan	9GA0412G7001	9GA0412G7001	9GA0412G7001
power	$1/2 \times 2$ W	$1/2 \times 2$ W	2 W
$L$	80 mm	80 mm	80 mm
$b$	40 mm	40 mm	40 mm
$t$	1 mm	1 mm	1 mm
$d$	3 mm	3 mm	3 mm

### E. Design of the Filter Networks

The dc–dc converter is part of a generator/drive system, i.e., power electronic converters are connected to both sides. The DAB converter, therefore, is not required to fulfill specific conducted electromagnetic compatibility standards. Still, filter networks are needed in order to allow for proper converter operation and to enable the DAB converter cells to be embedded in the ISOP structure, as shown in Fig. 1.<sup>5</sup> Fig. 2 shows the employed filter networks and the following list motivates the need for the different filter components.

- 1) The capacitors  $C_{f1}$ ,  $C_{2a}$ , and  $C_{2b}$  are part of the converter topology, provide low inductive commutation loops, and stabilize the supply voltages of the bridges.
- 2) The network formed with  $L_{f1a}$ ,  $L_{f1b}$ , and  $R_{f1b}$  enables the straightforward paralleling of different DAB converter cells on the LV sides ( $L_{f1b}$  and  $R_{f1b}$  introduce damping at the resonance frequency). For this reason, the LV side port currents of each converter cell,  $i_{Lf}$ , as shown in Fig. 2, are separately measured and controlled (see Section III).
- 3) The capacitor  $C_{dc}$  is used for energy storage. In the ISOP configuration, shown in Fig. 1, a single capacitor is used for four DAB converter cells together. The capacitance of this single dc capacitor then is equal to four times the dc capacitance of a single cell. In the

<sup>5</sup>On the MV side, four 25 kW DAB converter systems, each composed of four single DAB converter cells, are operated in parallel. Therefore, each 25 kW DAB converter system requires a decoupling inductance with a damping network (see the LV side filter network, as shown in Fig. 2) at the corresponding MV side dc port. For each of these networks, a weight of 70 g is estimated, which is less than the additionally allowed weight of 400 g (see Section V-A).

TABLE VI

LV FILTER COMPONENTS OF THE DAB

Symbol	Value	Description	Component	Weight
$L_{com,1}$	40 nH	Half bridge commutation loop inductance	2x TO-247 case, PCB	
$C_b$	100 nF	Commutation loop damping capacitance	2x 2x C4532X7R2J1-04K230KA	304 mg
$R_b$	0.5 $\Omega$	Commutation loop damping	2x 1206 resistor	160 mg
$L_{com,2}$	10 nH	Inductance half bridge to $C_{f1}$	PCB	
$C_{f1}$	4.0 $\mu$ F	Full bridge filter capacitance	2x B32774D0205K	18 g
$L_{Cf1}$	12.5 nH	Equivalent series inductance	$1/2$ x B32774D0205K	
$C_{dc}$	11.0 $\mu$ F	Input filter capacitance	$1/2$ x UCYW6220MHD	8 g
$R_{Cdc}$	1.50 $\Omega$	Equivalent series resistance	2x UCYW6220MHD	
$L_{f1a}$	10.0 $\mu$ H	Input filter inductance	T60-26D core with $N=14$ and AWG 16	12.7 g
$L_{f1b}$	8.2 $\mu$ H	Input filter $R$ - $L$ damping inductance	T50-70B core with $N=17$ and AWG 18	3.7 g
$R_{f1b}$	1.35 $\Omega$	Input filter $R$ - $L$ damping Resistance	2x 1206 SMD resistors	160 mg
		Interconnections	PCB and connectors	15.6 g

case of stand-alone testing of a single cell, e.g., for the purpose of verifying the operability and the achieved efficiency of a single cell (which is the case in this paper),  $C_{dc}$  is populated on the PCB of a single DAB converter cell.

The emphasis of the filter design is to achieve reliable converter operation, and no analytical weight optimization is carried out, because of the relatively little contributions of the weights of both filters to the total weight of a single DAB converter cell, i.e., total weights of 93 g and 59 g and relative weight contributions of 6% and 4% result for the MV and the LV side filters, respectively. For this reason and for better readability of the work at hand, the conducted filter design is presented in the Appendix. Table VI lists the weights of the employed LV filter component.

### III. CONTROL: CONCEPT AND IMPLEMENTATION

At this point, all main power components have been designed or selected. A fully operational DAB converter, however, requires additional circuitries for digital control and auxiliary power supplies, which also add to the total weight. Section III-A details the concept employed for the digital control of four DAB converter cells operated in the ISOP structure. Due to the required galvanic isolation, additional circuit components, i.e., optical transmitters, receivers, and fibers, are needed to establish digital signaling paths between the LV and the MV sides. Section III-B details the implemented circuit, which requires solely six such signal paths in order to achieve low weight. For better readability of this paper, the design of the digital controllers is given in Appendix C.

#### A. Concept

The ground station controls the voltage applied to the tether at the ground  $V'_2$  (see Fig. 1), which defines the voltage at the

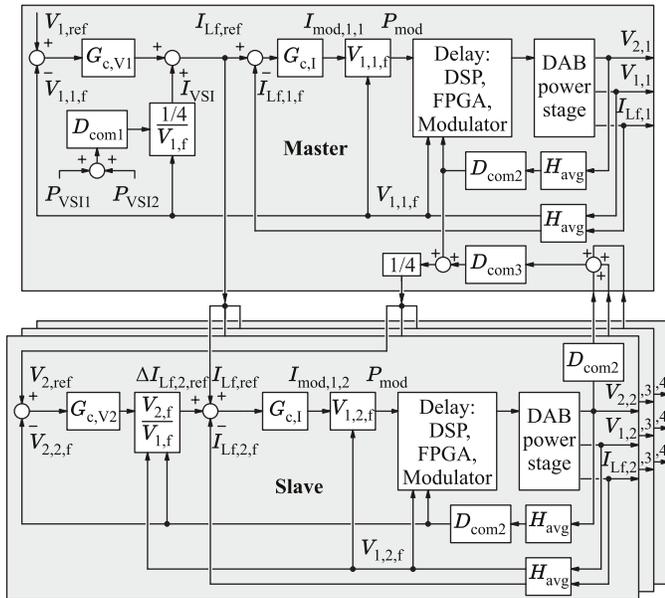


Fig. 9. Master and slave control block diagram of the dc-dc converter with a feedforward of the instantaneous power requirements of the motor inverters  $P_{VSI1}$  and  $P_{VSI2}$ .

MV side dc port of the DAB converter system according to the discussion presented in Appendix A. The DAB can adjust the tether current, since the ground station adapts to the actual tether current. Thus, at the MV dc port, the DAB converter system is free to control the actual operating power by means of current control. This property, in combination with the bidirectional power capability, renders the DAB converter system to be the ideal component regarding the stabilization of the LV side dc voltage,  $V_1$ .

Fig. 9 shows the block diagram for the control of one DAB converter system (out of four), which consists of four series connected DAB converter cells and features a total power of 25 kW. The following list summarizes the functionalities of the different blocks.

- 1) The power management unit determines the set values for the current controllers of all DAB converter cells in order to control the LV side dc bus voltage,  $V_1$ . The calculation of the reference current,  $I_{Lf,ref}$ , in addition, includes the dc port currents of both motor inverters in order to reduce the required energy buffering capability of  $C_{dc} + C_{fl}$  (see Appendix B).
- 2) A master and slave control strategy is chosen to balance the output voltages of all four DAB converter cells: the master module controls the input voltage  $V_1$ , and the slave modules ensure an equal distribution of the output voltage  $V_{2,i} = V_{2,ref} = (1/4)V_2$ . The master module provides the reference value  $V_{2,ref}$  to the slave modules as reference, such that each slave module can adjust its own transferred power, in order to balance the series connected dc links.
- 3) The current control loop of each converter cell is realized on the LV side and according to [35].

### B. Implementation

Fig. 10 shows the block diagram of the implemented digital control hardware. Each converter cell incorporates

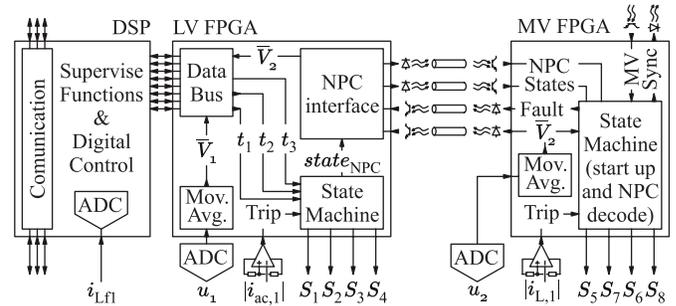


Fig. 10. Schematic of the control hardware implemented on each DAB converter cell.

a microcontroller (TMS320F28335), which handles the communication between the connected converter cells and the LV side FPGA, monitors currents and voltages, implements the digital control, and calculates the switching times  $t_1$ ,  $t_2$ , and  $t_3$  for minimum transformer rms current according to [28]. The FPGA on the LV side (LFXP2-5E-5TN144C) runs a state machine that generates the gate signals for the LV side FB converter and determines the current state of the MV side NPC converter, which is 0, 1, 2, or 3 (for  $v_{ac2} = -V_{2,i}$ , 0,  $V_{2,i}$ , or to turn all switches OFF due to a fault on the LV side, respectively). The state of the NPC converter is transferred to a second FPGA located at the MV side (LCMXO2-640HC-4TG100I) by means of two optical fibers (2 bits). This second FPGA generates the gate signals for the HV side NPC converter. The control of both the HB and the NPC converters considers the dead-time intervals with durations of 120 ns.

The proposed implementation requires two further optical communication lines between the LV and MV sides, to transmit the value of the actual port voltage,  $V_{2,i}$ , using an RS232 protocol with a baud rate of 2.5 MBd and to signalize a fault because of an instantaneous overcurrent.<sup>6</sup> Finally, a daisy chain connection of all four series connected DAB converter cells is achieved with another two optical communication lines. These are needed for an initial synchronization of all four NPC converters and to quickly signalize a fault condition between the different converter cells.

The total weight of the digital control circuitry (including PCB, optical transmitters, receivers, and fibers) is 133 g (for one DAB converter cell), the total weight the optical transmitters, receivers, and fibers is 24.6 g.

### IV. AUXILIARY POWER SUPPLIES AND START-UP

Two auxiliary power supplies, situated at the LV and the MV sides, respectively, provide power to the belonging control, measurement, and gate driver circuits. Section IV-A details the design and the implementation of these auxiliary power supplies, which are based on a resonant *LLC* converter topology, achieve low switching losses (ZVS), high switching

<sup>6</sup>Two protection circuits compare the absolute values of the transformer currents on the LV and the MV sides,  $|i_{ac,1}|$  and  $|i_{L,1}|$ , to maximum set values. The respective FPGA signals a fault in the case of an instantaneous overcurrent situation, which turns OFF the DAB converter system within less than one microsecond.

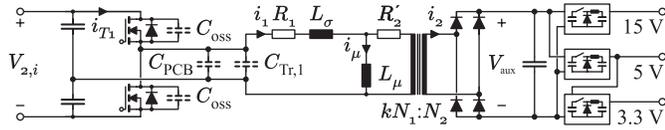


Fig. 11. Equivalent circuit of the proposed two-stage MV auxiliary supply, implemented for each DAB converter cell. A transformer connected to a split dc link and a HB, which is operated with constant duty cycles and provides an approximately constant voltage conversion ratio,  $V_{aux} \approx V_{2,i}/57.4$ . The second stage regulates the required auxiliary voltages using LV buck converters.

frequencies, and low weight. Section IV-B, finally, outlines the start-up of auxiliary and main power converters and presents the corresponding timing diagram.

### A. Auxiliary Power Supplies

Each DAB converter cell employs two auxiliary power supplies, to separately provide power to all MV side and all LV side system components.

- 1) The MV side auxiliary power supply provides power to:
  - a) MV side gate drives;
  - b) MV side control and measurement circuitry.
- 2) The LV side auxiliary power supply provides power to:
  - a) LV side gate drives;
  - b) LV side control and measurement circuitry;
  - c) cooling system fans.

Both auxiliary power supplies are equipped with start-up circuitries and feature self-supply capabilities, according to [37].

1) *MV Side*: The MV side auxiliary supply provides three output voltages (12, 5, and 3.3 V) from an input voltage of up to 2 kV. The total required output power is 3 W. From an initial investigation of different topologies [37], [38], the integrated *LLC* resonant converter topology shown in Fig. 11, which is a modified version of the converter presented in [37], has been identified to allow for a low weight realization, due to negligible switching losses (ZVS), a single magnetic component ( $L_\sigma$  and  $L_\mu$  are integrated into the transformer), a reduced primary side transformer voltage of  $\pm(1/2)V_{2,i}$ , and the need for only two MOSFETs and two gate drivers.

The realized *LLC* resonant converter essentially realizes a constant voltage transfer ratio, i.e., the output voltage changes proportional to the input voltage. Thus, three output side buck converters are connected in series to the *LLC* converter, according to Fig. 11, to provide stable output voltages. The HB is operated with fixed duty cycles, dead-time intervals, and frequency. Fig. 12 shows transformer voltage and current waveforms and the corresponding gate signals attained from an electric circuit simulation of the final MV side auxiliary power supply (see Table VIII).

A high switching frequency is desired in order to achieve a low transformer weight. The selected converter topology features ZVS properties and, thus, negligible switching losses can be achieved if MOSFETs are used [Si-MOSFETs are readily available for blocking voltages up to 4.5 kV (see Table VII)]. A HB circuit realized with MOSFETs, however, only achieves very low switching losses if the input current of the resonant network,  $i_1$ , shown in Fig. 11,

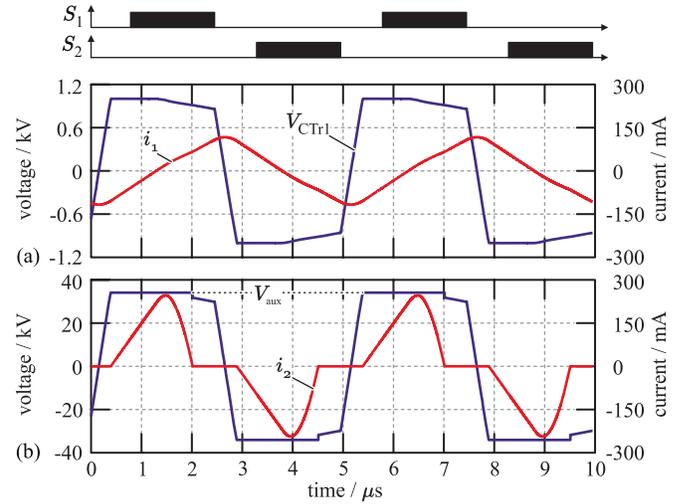


Fig. 12. Transformer voltage and current waveforms of the designed *LLC* converter with the HB being operated with fixed duty cycles, dead-time intervals, and frequency at (a) primary side and (b) secondary side of the transformer for  $V_{2,i} = 2$  kV and  $P_{aux} = 3$  W.

completely charges and discharges the MOSFETs' parasitic capacitances during the dead-time interval  $T_{dead}$  [39], which requires a minimum charge  $Q_{ZVS,min}$

$$Q_{ZVS,min}(V_{2,i}) = \int_0^{V_{2,i}} C_{oss}(v_{HB}) + C_{oss}(V_{2,i} - v_{HB}) dv_{HB} + \int_0^{V_{2,i}} C_{Tr,1} \left( \frac{V_{2,i}}{2} - v_{HB} \right) + C_{PCB} \left( \frac{V_{2,i}}{2} - v_{HB} \right) dv_{HB}. \quad (14)$$

Thus, the input current  $i_1$  of the resonant network needs to provide enough charge  $Q_{ZVS}$  during the dead-time interval

$$Q_{ZVS} = \int_0^{T_{dead}} i_1(t) dt = \int_0^{T_{dead}} \frac{N_2}{kN_1} i_2(t) + i_\mu(t) dt \geq Q_{ZVS,min}. \quad (15)$$

The auxiliary power converter is designed, such that ZVS is maintained even if no load is presented. For this reason, the magnetizing inductance of the HF transformer is appropriately designed and facilitates ZVS by means of the magnetizing current,  $i_\mu(t)$ , independent of the load condition. Furthermore

$$i_\mu(t) \approx i_1(t) \quad (16)$$

is assumed, since initial design results reveal that the magnetizing currents needed to achieve ZVS at the targeted high switching frequency are, for all three MOSFETs listed in Table VII, considerably higher than the currents needed to provide the output power. In addition, a comparably long relative duration of the dead-time interval of

$$T_{dead} = \frac{1}{6} \frac{1}{f_s} \quad (17)$$

provides sufficient time for the resonant voltage transition to complete, in particular with regard to the estimation of the

TABLE VII  
CHARACTERISTIC VALUES DETERMINED FOR THREE DIFFERENT  
Si-MOSFETs WITH MAXIMUM DRAIN SOURCE  
VOLTAGES OF 4.5 kV

Device	$R_{ds,on}$ @ 125 °C	$Q_{oss}$ @ 2 kV	$Q_{ZVS,min}$ @ 2 kV	$f_{s,max}$	weight
IXTA02N450HV	1500 $\Omega$	33.4 nC	43.4 nC	345 kHz	2.5 g
IXTT1N450HV	160 $\Omega$	131.6 nC	141.6 nC	324 kHz	4.0 g
IXTL2N450	40 $\Omega$	438.2 nC	448.2 nC	205 kHz	8.0 g

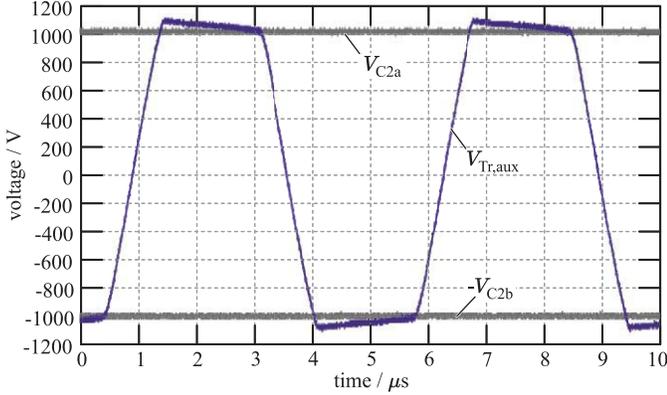


Fig. 13. Voltage waveform at rated input voltage of  $V_{2,i} = 2$  kV and  $P_{aux} = 3$  W. The smooth transitions of the auxiliary transformer voltage waveform show that the ZVS conditions are fulfilled.

maximum feasible switching frequency, which is estimated in the following.

Due to the long relative dead time (17), the waveform of the transformer magnetizing current,  $i_{\mu}(t)$ , is approximated with a sinusoidal waveform (see Fig. 12)

$$i_{\mu}(t) \approx I_{\mu,peak} \sin(2\pi f_s t). \quad (18)$$

With this and (15), the charge  $Q_{ZVS}$  can be calculated

$$Q_{ZVS} = \int_{-1/(12f_s)}^{1/(12f_s)} I_{\mu,peak} \cos(2\pi f_s t) dt = \frac{I_{\mu,peak}}{2\pi f_s}. \quad (19)$$

Subsequently, under the assumption that  $Q_{ZVS} = Q_{ZVS,min}$  and with (16)–(18), the conduction losses of the MOSFETs

$$P_{T,loss} = R_{ds,ON} I_{T,rms}^2 = R_{ds,ON} I_{\mu,peak}^2 \frac{4\pi - 3\sqrt{3}}{24\pi} \quad (20)$$

can be calculated, which are limited to

$$P_{T,loss,max} = \frac{T_j - T_{amb}}{R_{th,j-c} + R_{th,c-a}} \approx \frac{80 \text{ }^{\circ}\text{C}}{60 \text{ K/W}} \approx 1.3 \text{ W} \quad (21)$$

per MOSFET, since passive cooling without additional heat sink is considered [40]. The maximum switching frequency is obtained from (19) and (20), by eliminating  $I_{\mu,peak}$ , for  $Q_{ZVS} = Q_{ZVS,min}$

$$f_s \leq \sqrt{\frac{6P_{T,loss,max}}{\pi(4\pi - 3\sqrt{3})}} \frac{1}{\sqrt{R_{ds,ON} Q_{ZVS,min}}}. \quad (22)$$

Table VII summarizes the characteristic values for three Si-MOSFETs with blocking voltages of 4.5 kV and for  $C_{Tr,1} = 2$  pF and  $C_{PCB} = 3$  pF. Based on this result, the

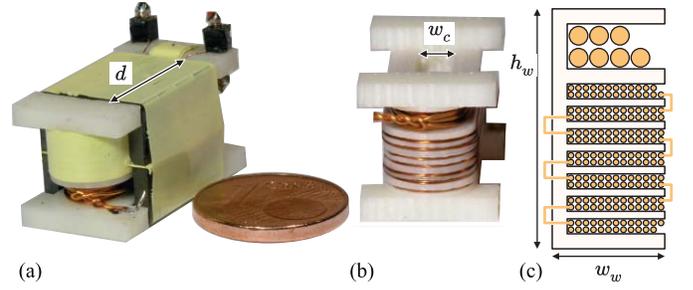


Fig. 14. (a) MV side auxiliary transformer with four E 13/7/4 N87 core pairs next to a one cent (Euro) coin. (b) 3-D printed bobbin, with 180 turns of 0.1-mm-diameter and 7 turns of 0.45-mm-diameter enameled copper wire. (c) Schematic of the chosen winding topology, which features a low primary winding capacitance  $C_{Tr,1}$  [41].

switch IXTA02N450HV is selected. However, a reduced final switching frequency of  $f_s = 200$  kHz, well below the calculated theoretical maximum frequency of  $f_{s,max} = 345$  kHz is selected, since (22) is an approximation and neglects turn OFF losses and conduction losses due to the load current.

According to (19) and (20), the peak value of the magnetizing current is bounded to

$$2\pi f_s Q_{ZVS,min} < I_{\mu,peak} < \sqrt{\frac{24\pi}{4\pi - 3\sqrt{3}}} \frac{P_{T,loss,max}}{R_{ds,ON}} \\ 55 \text{ mA} < I_{\mu,peak} < 94 \text{ mA} \quad (23)$$

which requires a transformer primary inductance of

$$L_1 = L_{\sigma} + L_{\mu} = \frac{V_{2,i}/2}{I_{\mu,peak}} \frac{1}{2\pi f_s} \in [8.45 \text{ mH}, 14.5 \text{ mH}]. \quad (24)$$

In order to adjust the primary inductance independent of the number of primary turns and yield a great number of degrees of freedom, stacked E-core transformer designs with an air gap in the magnetic path are considered. The winding topology is chosen, such that a small parasitic primary winding capacitance results [41]. Fig. 13 shows the implemented MV auxiliary transformer and a schematic of the winding topology.

For a given core cross-sectional area  $A_c$ , the number of primary turns must be

$$N_1 \geq \frac{V_{2,i}/2}{4f_s A_c B_{max}} \quad (25)$$

with the maximum flux density  $B_{max} = 150$  mT for the considered ferrite cores. In order to calculate the number of secondary turns, the leakage inductance  $L_{\sigma}$  needs to be estimated first to determine the transformer coupling

$$k = \sqrt{\frac{L_{\mu}}{L_{\mu} + L_{\sigma}}}. \quad (26)$$

The number of secondary turns is chosen, such that the transformer output voltage does not exceed the maximum tolerated auxiliary dc-link voltage  $V_{aux,max} = 36$  V provided to the auxiliary buck converters under no-load conditions (see Fig. 11)

$$N_2 = \frac{V_{2,i}/2}{k N_1} \cdot V_{aux,max}. \quad (27)$$

TABLE VIII  
PARAMETERS OF THE EQUIVALENT CIRCUIT OF THE MV SIDE  
AUXILIARY SUPPLY'S HF TRANSFORMER DEPICTED  
IN FIGS. 14 AND 15

$N_1 = 180$	$N_2 = 7$	$k = 89.3 \%$
$R_1 = 21 \Omega$	$L_\mu = 7.46 \text{ mH}$	$L_\sigma = 1.89 \text{ mH}$
$R'_2 = 30 \Omega$	$C_{Tr,1} = 2 \text{ pF}$	$C_{PCB} = 3 \text{ pF}$

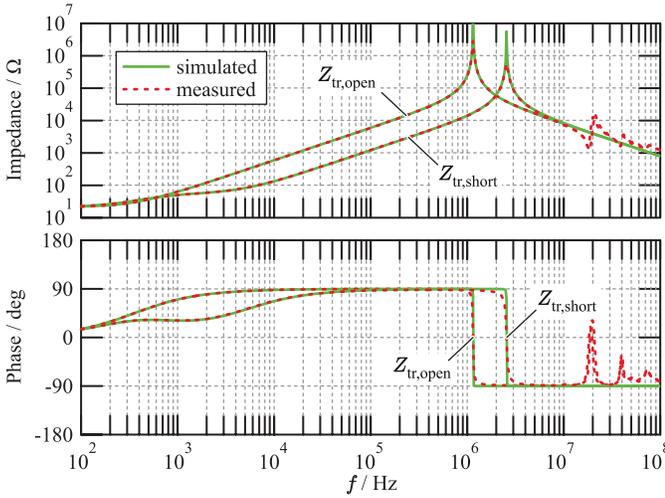


Fig. 15. Measured and simulated impedance of the MV auxiliary transformer seen from the primary side terminals with secondary side open,  $Z_{tr,open}$ , and short-circuited,  $Z_{tr,short}$ , terminals.

The leakage inductance is estimated as

$$L_\sigma \approx \mu_0 \left( \underbrace{N_1^2 \frac{2}{3} \frac{dh_w}{w_w}}_{\text{inside core}} + \underbrace{N_1^2 \frac{\pi(w_w + 2w_c)^2}{16h_w}}_{\text{outside core}} \right) \quad (28)$$

with the height  $h_w$  and the width  $w_w$  of the core's winding window, the width of the core center leg  $w_c$ , and the depth of the E-core stack  $d$ .

The chosen transformer consists of four E 13/7/4 N87 core pairs, a 3-D printed bobbin, 180 turns of 0.1-mm diameter and 7 turns of 0.45-mm diameter enameled copper wire. The equivalent circuit parameters are listed in Table VIII. They were obtained with a least squares fit of the transformer model impedance and the impedances measured with the Agilent 4294A precision impedance analyzer. Fig. 15 shows the measured and simulated impedances of the MV auxiliary transformer seen from the primary side terminals with the secondary side terminals open- and short-circuited.

Fig. 14 shows that the chosen equivalent circuit (see Fig. 11) models the transformer behavior well for frequencies below 1 MHz.

Fig. 15 shows the measured ac voltage applied to the transformer of the MV side auxiliary power supply and the voltages across  $C_{2a}$  and  $C_{2b}$  at  $V_{2,i} = 2 \text{ kV}$ . The shown smooth transitions of the auxiliary transformer voltage indicate that zero voltage turn ON is achieved.<sup>7</sup>

<sup>7</sup>It is to be mentioned here that the input capacitance of the differential voltage probe, which was used to measure the auxiliary transformer voltage, adds  $\sim 7 \text{ pF}$  to  $C_{Tr,1}$  and  $C_{PCB}$ .

TABLE IX  
SUMMARY OF THE MV AUXILIARY SUPPLY COMPONENTS

Component	Weight	Component	Weight
2×4.5 kV Switches	5 g	2× R10 Gate Transformers	2 g
2× SLF7055 inductors	1.6 g	4× E13/7/4 N87 core pairs	8 g
PCB	8 g	Components and connectors	9.4 g
Total weight 34 g			

TABLE X  
SUMMARY OF THE LV AUXILIARY SUPPLY COMPONENTS

Component	Weight	Component	Weight
2×1.2 kV Switches	8 g	2× R10 Gate Transformers	2 g
3× SLF7055 inductors	2.4 g	4× E13/7/4 N87 core pairs	8 g
PCB	7 g	Components and connectors	4.6 g
Total weight 32 g			

The point of load (POL) buck converters shown in Fig. 11 are designed for an operating input voltage range of  $V_{aux} \in [16 \text{ V}, 36 \text{ V}]$ , which maps to a useful operating input voltage range of the MV side auxiliary power supply of

$$V_{2,i} \approx 2 \frac{kN_1}{N_2} \frac{L_\sigma + L_\mu}{L_\mu} V_{aux} \in [1 \text{ kV}, 2 \text{ kV}]. \quad (29)$$

The load dependence of  $V_{aux}$  is negligible, as long as

$$\frac{N_2}{kN_1} i_2(t) \ll i_\mu(t) \quad (30)$$

i.e.,  $V_{aux}$  is not load dependent in this paper. Table IX summarizes all weights of the MV side auxiliary power supply components.

2) *LV*: The same converter topologies and the same power supply structures are selected for the LV and the MV auxiliary power supplies (see Fig. 11). However, devices with a lower  $\sqrt{(R_{ds,ON})Q_{OSS}}$  product are available for the LV side, due to the lower input voltage requirements,  $V_1 \in [650 \text{ V}, 750 \text{ V}]$ , and thus the design of the LV side supply is less challenging. Table X summarizes all weights of the LV side auxiliary power supply components.

### B. Start-Up

The ground station provides initial power to the AWT system and gradually increases the voltage  $V_2$  with a maximum voltage slope of  $(dV/dt)_{max} = 200 \text{ V/ms}$  in order to avoid over voltage at the MV port of the dc–dc converter system. This initial power is used to successively start the dc–dc converter system and the inverters, i.e., the connected motor inverters are deactivated during this time interval, to avoid any unnecessary load. With the AWT's power system being fully functional, the AWT system can be lifted from the ground and rise to the operational altitude, where it transitions into the generation trajectory, i.e., switches from the motor to the generator mode of operation.

The following list summarizes how the dc–dc converter system is started, and Fig. 16 shows the corresponding timing diagram.

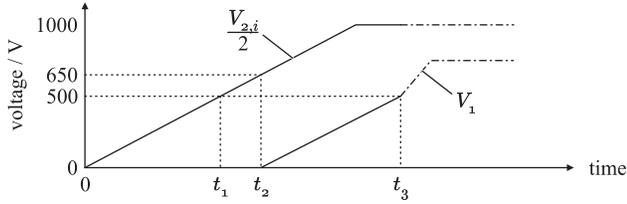


Fig. 16. Timing diagram of the DAB start-up sequence.

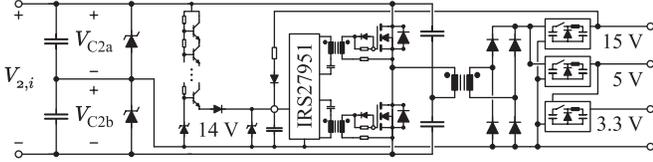


Fig. 17. Equivalent circuit of the additional circuitry facilitating a smooth start-up of the system. The transient voltage suppression (TVS) diodes clamp the voltages across  $C_{2a}$  and  $C_{2b}$  in order to protect the NPC dc-link capacitors and semiconductor switches. The linear regulator, implemented as a series connection of bipolar transistors, [42], provides the initial power and is turned OFF when the 15 V buck converter provides its regulated output voltage.

- 1)  $V_{2,i}/2 < 500 \text{ V}$  ( $0 < t < t_1$  in Fig. 16): A linear regulator, realized with 12 bipolar transistors (FCX605TA) connected in series [42], supplies the IRS27951 self-oscillating IC of the MV side auxiliary power supply continuously. The converter system is designed, such that the linear regulator does not overheat for  $V_{2,i} < 1 \text{ kV}$ . Furthermore, unequal voltages  $V_{C2a}$  and  $V_{C2b}$  result due to unequal currents being drawn from  $C_{2a}$  and  $C_{2b}$ . TVS diodes with clamping voltages of 1.2 kV (see Fig. 17) are used to prevent critical over voltage situations.
- 2)  $500 \text{ V} < V_{2,i}/2 < 650 \text{ V}$  ( $t_1 < t < t_2$  in Fig. 16): Above 1 kV, the 15 V POL buck converter provides a stable output voltage to the MV side auxiliary supply. Thus, the auxiliary power supply operates in the self-sustainable mode, and the linear regulator is turned OFF. All three POL converters shown in Fig. 17 provide stable output voltages.
- 3)  $V_{2,i}/2 > 650 \text{ V}$  (Start-Up Mode of the DAB Converter,  $t_2 < t < t_3$  in Figs. 1 and 2): The MV side NPC converters are in active operation while the LV side FB remains passive as a diode rectifier. The FPGAs located at the DAB converters' MV sides communicate with each other to achieve a synchronous start at  $t = t_2$  and, thereafter, linearly increase the duty ratios  $D_2$  from 0 to 0.475 within 2 s. With this strategy, the LV side dc-link voltage,  $V_1$ , is built up at a limited maximum tether rms current of 1 A.
- 4)  $V_1 > 500 \text{ V}$  ( $t_4 < t$  in Fig. 16): All LV side auxiliary power supplies and the complete circuitries needed for the digital control are started up and self-sustaining. The main microcontrollers initiate the respective DAB converters in order to make them ready for closed-loop control.

## V. EXPERIMENTAL RESULTS

### A. Hardware Prototype

Fig. 18 shows the Pareto-front determined for a single DAB converter cell. Based on this Pareto-front, the design

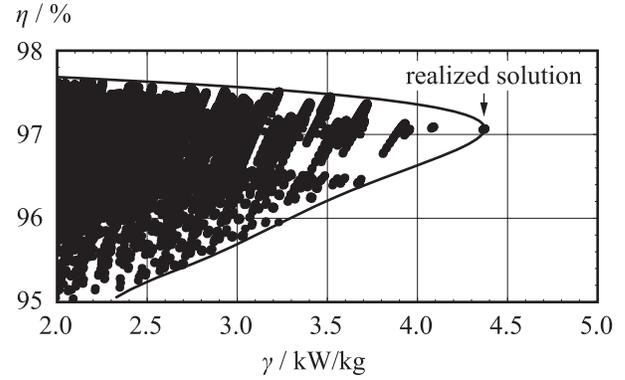


Fig. 18. Pareto-front calculated for a single DAB converter cell; the different dots depicted in this graph correspond to different designs of the HF transformer and inductor presented in [1, Fig. 27]. The presented hardware prototype is a realization of the rightmost design point, which leads to the maximum feasible power to the weight ratio of 4.35 kW/kg at a calculated efficiency of 97.1%.

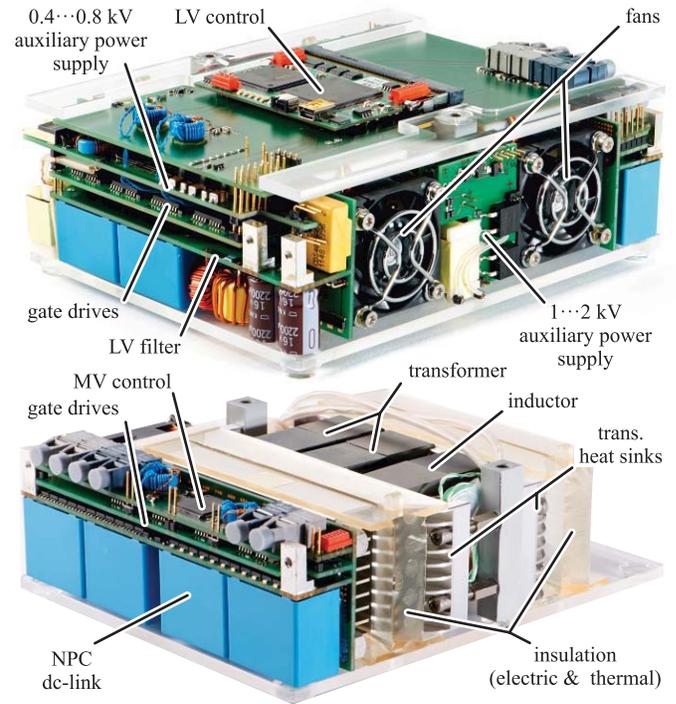


Fig. 19. 6.25 kW converter prototype. (top) Front view. (bottom) Rear view without the LV side components. The total system weight is 1.46 kg. The achieved power to the weight ratio is 4.28 kW/kg, and the power density is 5.15 kW/dm<sup>3</sup>.

point which leads to the maximum power to the weight ratio of 4.35 kW/kg, at a calculated efficiency of 97.1%, has been selected for the hardware implementation. The corresponding realized converter prototype is shown in Fig. 19. The total weight of this 6.25 kW converter system is 1.46 kg, its power to weight ratio is 4.28 kW/kg (1.94 kW/lb), and the power density is 5.15 kW/dm<sup>3</sup>. This leaves a margin of 100 g/cell, with respect to the specifications listed in Table I, to facilitate the interconnections and eventually required additional filter components (see Section II-E). Fig. 20(a) and (b) shows the partitioning of the DAB weight by function and materials, respectively.

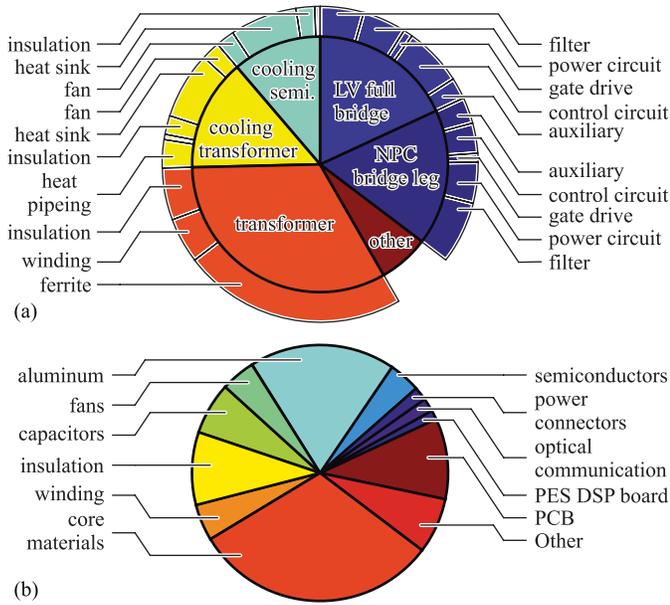


Fig. 20. Pie charts of the partitioning of the DAB weight by (a) function and (b) materials. The total system weight is 1.46 kg.

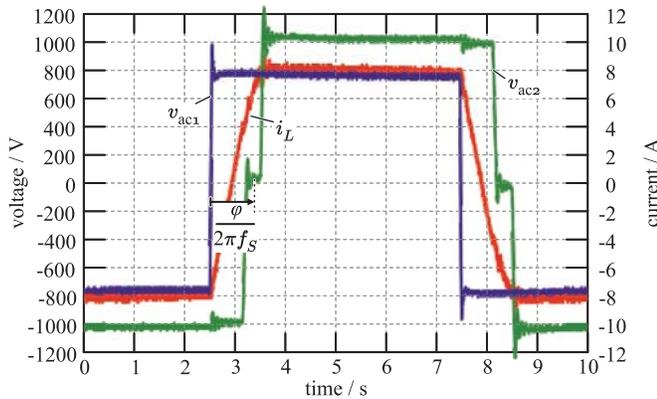


Fig. 21. Measured voltage and current waveforms at nominal load.

According to Fig. 20(a), the total weight of transformer, inductor, and cooling system is  $\sim 60\%$  of the total system weight. This result confirms the strong impact of these components' weights on the total system weight and justifies the selected optimization strategy. The DAB converter system, however, also requires the remaining converter parts, of which the weights of the remaining circuits add up to 29% and structural elements, e.g., screws, add up to 11% of the total weight.

According to Fig. 20(b), the transformer core and winding account for 31% and 5% of the total system weight, respectively. Furthermore, the weight needed for the transformer cooling system accounts for 14% of the total weight.

### B. Efficiency and Temperature Measurement

Fig. 21 shows the measured voltage and current waveforms at nominal load, and Fig. 22 shows the measurement setup. A series and parallel interconnection of four 600 V/10 A dc power supplies (Xantrex XDC 600-10) provides sufficient

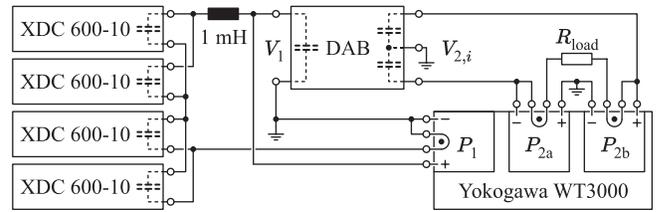


Fig. 22. Schematic of the measurement setup with four Xantrex XDC 600-10 dc-power supplies and a Yokogawa WT3000 precision power analyzer.

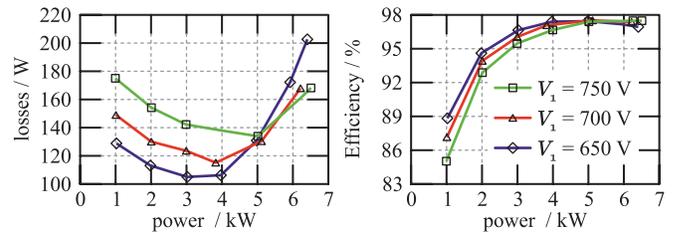


Fig. 23. Measured losses and efficiency of the DAB converter cell prototype. All operating points feature the voltage conversion ratio  $V_{2,i} = 2V_{1}/n$ .

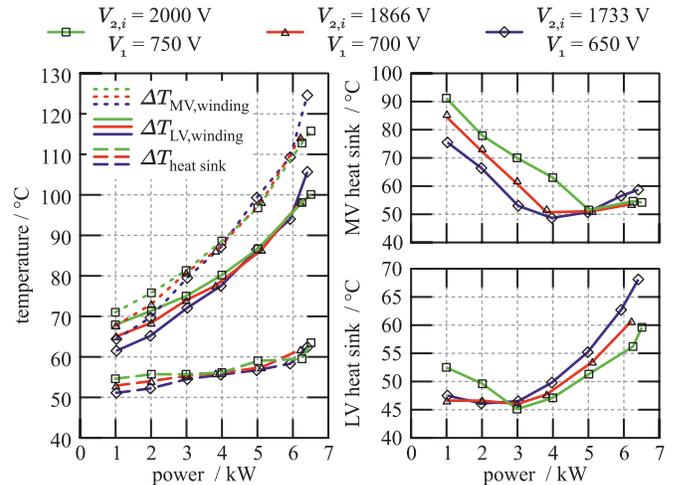


Fig. 24. Measured temperatures of the DAB converter cell prototype. The temperatures are scaled to 40 °C ambient temperature. All operating points feature the voltage conversion ratio  $V_{2,i} = 2V_{1}/n$ .

voltage and current to the LV side of the DAB converter. The 1 mH inductor decouples the dc power supplies from the DAB converter in order to prevent parasitic oscillations between the output capacitors of the dc power supplies and the LV side dc link. A Yokogawa WT3000 precision power analyzer measures the dc input and output powers. The DAB converter controls the output voltage to  $V_{2,i} = 2V_{1}/n$ . An adjustable resistive load, attached to the positive and negative terminals of the MV side dc link, is used to set the requested output power. The converter has reached thermal equilibrium in every single measurement point. Fig. 23 summarizes the obtained loss and the efficiency measurement results. The converter achieves a maximum efficiency of 97.5% at  $V_{1} = 700$  V and  $P_{2,i} = 5$  kW.

Fig. 24 shows the measured temperature rises of the four heat sink halves and the hot spots of the MV and

the LV side transformer windings<sup>8</sup> with respect to an ambient air temperature of 40 °C. The temperature measurements are carried out with *k*-type thermocouples and Fluke 187 multimeters.

Fig. 24 shows the dependence of the loss allocation with varying load  $P_2$ . For the LV side FB, the losses are to be attributed predominantly to conduction losses, while the contribution of the ZVS losses are comparably small at the switching frequency of 100 kHz. The measured ZVS losses and the corresponding temperature rises are well below the losses original estimated in [1]. This difference can be attributed to the use of the dedicated JFET EiceDriver 1EDI30J12CP instead of a JFET n-channel MOSFET cascade configuration, as in [16]. The same holds true for the ZVS losses at the MV side NPC bridge leg. However, for loads below  $P_2 = 3$  kW, the switching losses, due to residual turn ON or partial ZVS losses of the NPC bridge leg, are considerably larger than the losses at the rated power of  $P_2 = 6.25$  kW. In this paper, the maximum temperature rise of the MV side heat sink (at  $P_2 = 1$  kW and  $V_{2,i} = 2$  kV) is  $\sim 50$  °C and significantly exceeds the allowed temperature rise of 40 °C. However, with further control efforts, the losses at low transferred powers can be reduced, e.g., through power cycling strategies. This will be the subject of future work. For the transformer and the inductor, the total losses approximately double from  $P_2 = 1$  kW to full output power range  $P_2 = 6.25$  kW, which shows an approximately even distribution between the core and the winding losses. For the magnetic component, the measured MV winding hot-spot temperature is most sensitive to the transferred power. This result is to be expected and underlines the need for an active cooling system that reduces the thermal resistance of the MV winding, which is engulfed by a 2 mm layer of electric insulation.

The power consumption of the MV side auxiliary power supply is  $\sim 7$  W, and the LV side auxiliary power supply requires an input power of approximately 12 W, since it also provides power to the two fans for the cooling system.

At the designed operating point,  $V_1 = 650$  V,  $V_{2,i} = 1733$  V, and  $P_{2,i} = 6.25$  W, the calculated and the measured efficiencies are 97.3% and 97%, respectively.

### C. Cost Decomposition

Besides the weight and the efficiency of the converter, the cost is an important parameter for industry. For this reason, a cost estimation based on the methods and the models presented in [43] is performed. The results are summarized in Fig. 25. The analysis yields material costs at a production volume of more than 5'000 converters of approximately 350 € per DAB converter cell, i.e., 56 €/kW.

The contribution of the passive power components to the total material cost is 8.2%, i.e., the filter components and the transformer and the inductor; the contribution of the DAB power semiconductors is 23.5%, i.e., JFETs, p-channel MOSFET, SiC diodes, and protective TVS diodes; and the

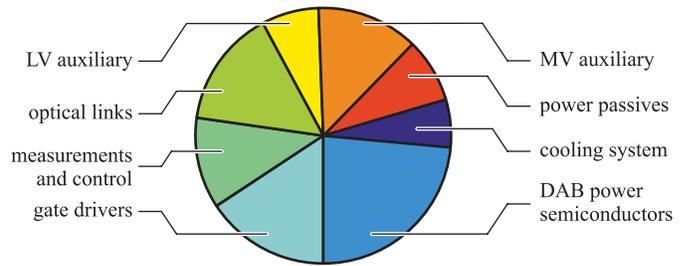


Fig. 25. Cost decomposition of the DAB converter cell prototype. The material costs at a production volume of more than 5000 converters is  $\sim 350$  € per DAB converter cell, i.e., 56 €/kW. Housing and connectors are not considered. Power passives consist of the filter components and the transformer and inductor. The DAB power semiconductors consist of the JFETs, p-channel MOSFETs, SiC diodes, and protective TVS diodes. The cost estimation is based on the methods and models presented in [43]. A price of 7 € per JFET is assumed.

cooling system contributes with 6.1%, where the majority of the costs are attributed to the two fans. According to the result of this estimation, these power components add up to 38% of the total cost. The remaining part, 62% of the material cost, is attributed to ICs and electronics, which enable the operation and the control of the converter. The contribution of the gate driver components is 15.7% and predominantly consists of the eight dedicated JFET EiceDriver ICs and four MAX13256 transformer driver ICs utilized for the isolated gate driver supplies. Fig. 25 further reveals that the material cost for the MV auxiliary supply (12.9%) is almost double the cost of the LV auxiliary supply (7.2%), because of the more expensive high-voltage MOSFETs. The remaining 26% cover all electronics required for the measurements, the control, and the communication, including the printed circuit boards (1.7%) and, with 14.9%, the fiber optic transmitters and receivers (HFBR-1522Z and HFBR-2522Z), which are required due to the high isolation requirements of the converters ISOP structure, significantly contribute to the cost of the electronics. The cost decomposition reveals that an optimization for minimum converter weight minimizes the material cost of the passive components and invests in power semiconductors, which feature minimal losses and reduce the cooling system weight, regardless of the power semiconductor cost.

## VI. CONCLUSION AND OUTLOOK

A comprehensive conceptualization and the design of a weight-optimized all-SiC 2 kV/700 V DAB for an AWT is presented. Experimental results validate the calculated converter performance: the realized converter prototype achieves a power to weight ratio of 4.28 kW/kg (calculated: 4.35 kW/kg) at a weight of 1.46 kg and a power density of 5.15 kW/dm<sup>3</sup>; the efficiency is 97% (at  $V_1 = 650$  V and  $P_{out} = 6.25$  kW; calculated: 97.3%). The realized DAB converter cell fulfills the required specifications (see Table I) and hence confirms the feasibility of the AWT electrical system structure proposed in [1].

The weight of the cooling system and the transformer and inductor is  $\sim 60\%$  of the total system weight. This result confirms the strong impact of the weights of these components

<sup>8</sup>The winding hot spots are assumed to be in the middle of the inductor end turns of the MV side winding and inside the end turns of the LV side winding on the opposite side of the transformer.

on the total system weight and justifies the reason for the weight optimization to focus on these components.

The switching losses are decreased (compared with [1]) through the evolution of the SiC technology, i.e., due to the JFET direct drive technology. This and the fact that the transformer core material accounts for 31% of the total system weight suggest that a DAB operated at a higher switching frequency may have the potential for a further weight reduction.

The MV winding is the first component to reach its thermal limit, in spite of the fact, that the transformer cooling system accounts for 14% of the total system weight. Due to this reason, different transformer topologies, which do not engulf the winding with a large thermal insulation, may allow for a further weight reduction. Respective investigations and optimizations are subject to future work.

The presented comprehensive weight-optimized design of the 6.25 kW DAB converter cell, used as part of a 25 kW ISOP structured dc–dc converter, considers multiobjective optimization and takes, besides the actual components weights, the losses of the converter components and the associated weight of the required optimized cooling system into account. Furthermore, the weights of the additional circuitries required for the converter operation and the integration into the final electrical AWT system, i.e., gate drivers, digital control, filters, and auxiliary power supplies, are also considered. The converter design detailed in this paper, thus points out the technological limits the DAB converter is subject to and is not limited to the considered AWT application.

The weight optimization of components is of utmost importance for not only AWTs but for airborne applications in general, since each additional kilogram of weight carried in an aircraft increases the fuel consumption by 2900 liter kerosene per year [44]. With respect to a power converter not only the weight of the power components but also efficiency plays a major role, since the weight of the converters cooling system increases with increasing losses and, most often, substantially contributes to the total converter weight; from practical experience, it is estimated that 1 kW of losses involves 10 kg of secondary cooling equipment [46]. For this reason, the presented design procedure has to be seen in a more general context as guideline for the realization of lightweight power converters for airborne applications.

## APPENDIX

### DESIGN OF THE FILTER NETWORKS

The presented design approach employs the simplified dynamic DAB converter model developed in [35] and the networks connected to the LV and the MV sides. Fig. 26 shows the considered network, which consists of two current sources to model the inner most part of the DAB converter, a LV side *CLC* filter with damping network, and, on the MV side, the equivalent sum of the MV filter capacitors,  $C_2$ , and the equivalent circuits of the tether and the ground station, i.e., the rectifier/inverter system located on the ground, that are relevant for a single DAB converter cell. For the ground station, no weight limitation applies and, for this reason, a sufficiently large dc-link capacitance  $C_3$  at the ground station

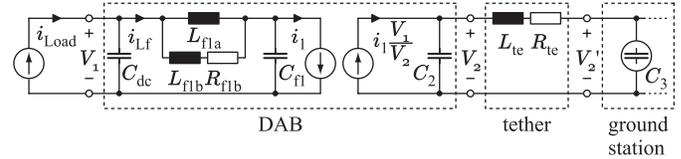


Fig. 26. Equivalent circuit of the AWT power electronic system [1], including the simplified circuit model of the DAB presented in [35] (instead of the assumed ideal transformer in [1]).

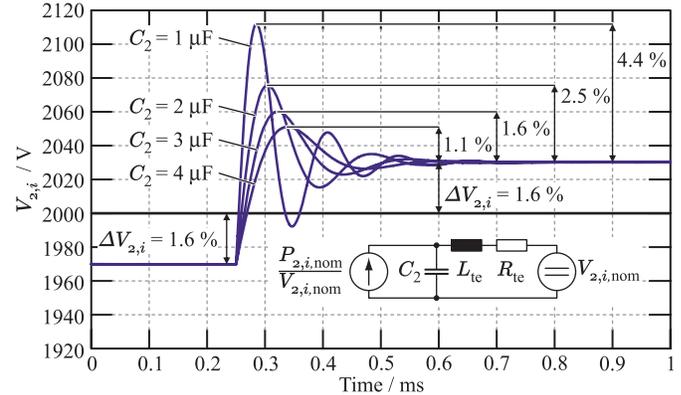


Fig. 27. Transient response of the MV side filter voltage  $V_{2,i}$  to a step, in the dc–dc converters transferred power, from  $-P_{nom}$  to  $P_{nom}$  for different equivalent capacitances  $C_2 = C_{2a}/2$ . The ground station is assumed to be an ideal voltage source. The MV side of the DAB is a controlled current source [35] and the tether provides a damped inductance of 360  $\mu\text{H}$  with a series resistance of 9  $\Omega$  [1].

is assumed, which provides a stabilized dc voltage. Thus, in the simplified network, shown in Fig. 26, the ground station is replaced by a dc voltage source.

#### A. MV Side Filter

The MV side of the DAB converter system shown in Fig. 26 is connected to the ground station by means of the tether, which, in terms of simplified electrical properties, is a 1-km-long cable with a series resistance of 9  $\Omega$  and a series inductance of 360  $\mu\text{H}$ .<sup>9</sup> The network of Fig. 26 corresponds to a single DAB converter cell, and

$$L_{te} = 360 \mu\text{H} \quad \text{and} \quad R_{te} = 9 \Omega \quad (31)$$

apply, since on the MV side, four DAB converter systems are connected in parallel and each of the four converter systems itself is composed of four DAB converter cells that are connected in series (see Fig. 1). Based on these considerations and with the given converter circuit shown in Fig. 2, the values of the capacitances  $C_{2a} = C_{2b}$  denote the only possible degree of freedom related to the design of the MV side filter.

Fig. 27 shows the transient response of the MV side filter voltage  $V_{2,i}$  due to the worst case stepwise change of the MV side current source. The worst case is considered to

<sup>9</sup>Wave propagation effects are not considered in this paper, since the critical frequency related to wave propagation effects calculated for this cable is  $>100$  kHz. Thus, the critical frequency is considerably greater than the bandwidth of the closed current control loop, which is  $<10$  kHz, and the corresponding maximum achievable excitation frequency.

be present if the ground station generates the maximum voltage,  $V_2' = 8$  kV (or, when referring to a single DAB converter,  $V_{2,i}' = 2$  kV), since any transient voltage change may lead to over voltage situations at the MV dc ports of the DAB converters. Furthermore, the maximum possible current change is considered, which, for  $V_2' = V_{2,i,\max}'$ , gives a stepwise change from  $-P_{\text{nom}}/V_{2,i,\max}'$  to  $P_{\text{nom}}/V_{2,i,\max}'$ . From the results shown in Fig. 27, a capacitance value  $C_2 = 3$   $\mu\text{F}$  is selected, which, in combination with  $L_{\text{te}}$  gives a characteristic impedance of

$$Z_0 = \sqrt{\frac{L_{\text{te}}}{C_2}} = 11 \Omega > R_{\text{te}} = 9 \Omega \quad (32)$$

and a sufficiently damped voltage response results. With this, a maximum instantaneous absolute voltage overshoot (transient + static over voltage) of 64 V results, which can be easily handled by all MV side power components that are subject to this over voltage condition.

Due to the required capacitor rms current of 5 A and the capacitor voltage of up to 1 kV, only film capacitors have been considered for  $C_{2a}$  and  $C_{2b}$ . Each capacitor is implemented with two B32774D1305K3  $\mu\text{F}/1300$  V/4 A capacitors operated in parallel in order to achieve the  $C_{2a} = C_{2b} = 6$   $\mu\text{F}$ .

### B. LV Side Filter

According to Appendix C, the worst case dynamic situation is present if the inverters perform a stepwise change of the output current with maximum possible amplitude, e.g., from motor mode at rated power to generator mode at rated power, while the operating mode of the DAB converter system remains unchanged, e.g., the DAB converter system continues to provide energy to the motor inverters at rated power. In this case, a superordinate on-board power management unit coordinates the energy flow, i.e., immediately tells the DAB converter system to change the direction of energy flow. Depending on the realization of this power management unit, however, a certain time delay may occur, which is the time between the instant a transient change at an inverter port occurs until the connected DAB converter system adapts to the new situation. In the meantime, the dc capacitors need to buffer the energy, whereas  $V_1$  may not exceed a maximum voltage of  $V_{1,\max} = 810$  V in order to protect the power electronic switches of the DAB converters and the motor inverters. With a digitally controlled system, a time delay of  $T_{\text{delay}} = 50$   $\mu\text{s}$  is assumed to be reasonable. Thus, in the case of the worst case dynamic situation, the maximum charge absorbed by the sum of the capacitances  $C_{\text{dc}} + C_{\text{fl}}$  is

$$\Delta Q = \frac{T_{\text{delay}} 2P_{i,\max}}{V_{1,\max} \eta_{\text{exp}}} = 877 \mu\text{C} \quad (33)$$

which yields the condition

$$C_{\text{dc}} + C_{\text{fl}} > \frac{\Delta Q}{\Delta V_{1,\text{trans}}} = \frac{877 \mu\text{C}}{810 \text{ V} - 750 \text{ V}} = 14.6 \mu\text{F} \quad (34)$$

for  $C_{\text{dc}} + C_{\text{fl}}$ . Since  $C_{\text{fl}}$  is subject to high rms currents (see Table II), it is implemented with suitable film capacitors. The considered converter prototype operates two 2  $\mu\text{F}/1100$  V

film capacitors (B32774D0205 manufactured by EPCOS) in parallel. These film capacitors allow for a reasonable steady-state voltage ripple, approximately determined with

$$\Delta V_{C_{\text{fl}}} \leq \frac{\sqrt{2} \max(I_{C_{\text{fl}}})}{2\pi 2f_s C_{\text{fl}}} \approx 2 \text{ V}. \quad (35)$$

Aluminum electrolytic capacitors are selected for the realization of  $C_{\text{dc}}$ , due to the better capacitance to weight ratio compared with film capacitors and since  $C_{\text{dc}}$  is subject to comparably low capacitor rms currents. Thus, for a single DAB converter cell,  $C_{\text{dc}}$  is realized with two UCYW6220MHD 22  $\mu\text{F}/420$  V capacitors in series. The maximum allowable rms current is  $2 \times 285 \text{ mA} = 570 \text{ mA}$  (factor 2 due to HF operation) for this capacitor at  $2f_s = 200$  kHz.

$L_{\text{fla}}$ ,  $L_{\text{flb}}$ , and  $R_{\text{flb}}$  limit the rms current that  $C_{\text{dc}}$  is subject to. In this paper,  $I_{L_{\text{f}}} \leq 250$  mA, i.e., a current less than one half of  $C_{\text{dc}}$ 's maximum allowable rms current, is considered to be a useful assumption, since this leaves sufficient remaining capacitor current capability for the connected motor inverters and allows for comparably small and lightweight components  $L_{\text{fla}}$ ,  $L_{\text{flb}}$ , and  $R_{\text{flb}}$  (see Table VI). In the stopband of the filter, the ratio between  $I_{C_{\text{f}}}$  and  $I_{L_{\text{f}}}$  is approximately determined with the fundamental frequency approach

$$\frac{I_{C_{\text{dc}}}}{I_{C_{\text{f}}}} \approx \left| \frac{-j(2\pi 2f_s C_{\text{fl}})^{-1}}{j2\pi 2f_s (L_{\text{fla}} || L_{\text{flb}}) + R_{C_{\text{dc}}} - j(2\pi 2f_s C_{\text{fl}})^{-1}} \right|. \quad (36)$$

Note that the FB converter operates the filter at a fundamental frequency of  $2f_s$ . Furthermore, the dc capacitance is replaced by its equivalent series resistance, due to  $2\pi 2f_s C_{\text{dc}} \ll R_{C_{\text{dc}}}$ . With (36)

$$L_{\text{fla}} || L_{\text{flb}} \approx 4.5 \mu\text{H} \quad (37)$$

applies in order to keep  $|I_{C_{\text{dc}}}/I_{C_{\text{f}}}|$  below 250 mA/7 A. For the filter, a maximum resonance rise of 1.5 dB is tolerated, which, according to [36], yields

$$L_{\text{fla}} = 10 \mu\text{H}, \quad L_{\text{flb}} = 8.2 \mu\text{H}, \quad \text{and} \quad R_{\text{flb}} = 1.35 \Omega. \quad (38)$$

### C. Controller Design

The presented controller design is conducted in continuous time and, for this reason, the bilinear transformation with sampling interval  $T_0$

$$z \rightarrow \frac{2 + sT_0}{2 - sT_0} \quad \text{and} \quad s \rightarrow \frac{2}{T_0} \frac{z - 1}{z + 1} \quad (39)$$

is used to approximately convert transfer functions between the discrete and the continuous time domains [45].

According to the simplified dynamic model given in [35], the DAB converter can be replaced by the two controlled current sources and the respective filter networks, as shown in Fig. 26. The modulator current  $I_{\text{mod},1,i}$  simultaneously controls both the LV and the MV side, current sources  $I_{L_{\text{f}},i}$  and  $I_2$ , the considered simplified dynamic DAB converter model, thus disregards interactions between the LV and the MV sides. The most influential component of the transfer function of the DAB

converter without filter networks,  $G_{DAB,0} = I_{LF,i}/I_{mod,1,i}$ , identified in [35] is the time delay introduced by the digital control system,  $T_c = 50 \mu\text{s}$

$$G_{DAB,0}(s) = \frac{I_{LF,i}}{I_{mod,1,i}} = e^{-sT_c} \quad (40)$$

and the total open-loop transfer function of a DAB converter cell,  $G_{i,ol}(s)$ , is

$$G_{i,ol}(s) = \frac{I_{LF,i}}{I_{mod,1,i}} = \frac{Z_{Cfl}}{Z_{Lfl} + Z_{Cfl}} G_{DAB,0},$$

$$Z_{Lfl} = \frac{sL_{f1a}(R_{f1b} + sL_{f1b})}{sL_{f1a} + (R_{f1b} + sL_{f1b})}, \quad \text{and } Z_{Cfl} = \frac{1}{sC_{fl}}. \quad (41)$$

The transfer functions of the Proportional Integral (PI) controllers are [35]

$$G_c = K_p \frac{z - (1 - T_c/T_i)}{z - 1} \stackrel{z \rightarrow s}{=} K_p \left( 1 - \frac{T_c}{2T_i} + \frac{1}{sT_i} \right) \quad (42)$$

with gain  $K_p$ , integral time constant  $T_i$ , and controller update period time  $T_c$ . The discrete time transfer function of a moving average filter of filter order  $N_s$  is

$$H_{avg} = \frac{1}{N_s} \sum_{k=0}^{N_s-1} \frac{1}{z^k} \stackrel{z \rightarrow s}{=} \frac{1}{N_s} \sum_{k=0}^{N_s-1} \left( \frac{2 - sT_s}{2 + sT_s} \right)^k \quad (43)$$

with  $N_s = 8$  and  $T_s = 1.25 \mu\text{s}$  is applicable in this paper. Hence, the voltages  $V_1$  and  $V_{2,i}$  and the filter currents  $I_{LF,i}$  are sampled and averaged eight times within each switching period.

In order to achieve a high bandwidth of the current controller, and because the transfer function  $G_{i,ol}$  is essentially a second-order low-pass filter with a time delay, the current controllers are designed with the optimum amount method with a selected phase margin of  $\varphi_I = 60^\circ$ . For this, the corner frequency of the current controller's transfer function,  $f_{i,1} = 1/(2\pi T_{i,1})$ , is set equal to the frequency, where  $G_{i,ol}$  shows maximum resonant gain

$$\left| G_{i,ol} \left( j \frac{2\pi}{T_{i,1}} \right) \right| = \max |G_{i,ol}|. \quad (44)$$

The current controller gain  $K_{p,I}$  is adjusted to achieve a phase margin of  $\varphi_I = 60^\circ$  at the cross over frequency  $\omega_{\varphi,I}$  of the loop gain

$$F_{ol,I} = G_{c,I} G_{i,ol} H_{avg} \quad (45)$$

by solving

$$\angle [F_{ol,I}(j\omega_{\varphi,I})]_{K_{p,I} \rightarrow 1} \stackrel{!}{=} \varphi_I - \pi \quad (46)$$

in order to determine  $\omega_{\varphi,I}$  and, subsequently

$$\left| F_{ol,I}(j\omega_{\varphi,I}) \right| \stackrel{!}{=} 1 \quad (47)$$

to determine  $K_{p,I}$ . The loop gain for the voltage controller used to control  $V_1$  then becomes

$$F_{ol,V1} = G_{c,V1} G_{cl,I} H_{avg} \quad \text{with } G_{cl,I} = \frac{F_{ol,I}}{1 + F_{ol,I}} \quad (48)$$

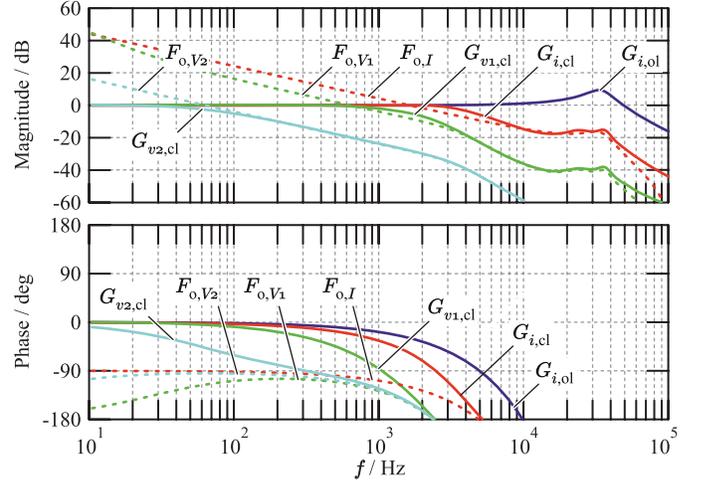


Fig. 28. Bode plots of the plant's transfer function  $G_{i,ol}$ , the open-loop gains  $F_{ol,I}$ ,  $F_{ol,V1}$ , and  $F_{ol,V2}$ , and the closed-loop transfer functions  $G_{cl,I}$ ,  $G_{cl,V1}$ , and  $G_{cl,V2}$ .

TABLE XI  
DC-DC CONVERTER CONTROL PARAMETERS

$G_{c,I}$ for $I_{LF,1}$	$G_{c,V1}$ for $V_1$	$G_{c,V2}$ for $V_{2,i}$
$K_{p,I} = 0.293$	$K_{p,V1} = 44.1 \text{ mA/V}$	$K_{p,V2} = 3.2 \text{ mA/V}$
$T_{i,I} = 28.6 \mu\text{s}$	$T_{i,V1} = 5.83 \text{ ms}$	$T_{i,V2} = 58.3 \text{ ms}$
$\frac{\omega_{\varphi,I}}{2\pi} = 1.64 \text{ kHz}$	$\frac{\omega_{\varphi,V1}}{2\pi} = 640 \text{ Hz}$	$\frac{\omega_{\varphi,V2}}{2\pi} = 64 \text{ Hz}$

i.e.,  $G_{cl,I}$  is the transfer function of the closed current control loop. Fig. 28 shows all resulting open- and closed-loop gains.

The voltage controller of  $V_1$  stabilizes the voltage of the dc bus on the LV side and, for this purpose, alters the reference current  $I_{LF,ref}$ . This voltage controller is designed with the symmetric optimum method [35], for a phase margin of  $\varphi_{V1} = 60^\circ$ . With this, the controller parameters  $K_{p,V1} = 44.1 \text{ mA/V}$  and  $T_{p,V1} = 5.83 \text{ ms}$  result.

Finally, the voltage controllers for the MV side voltages of the slave modules,  $V_{2,2}$ ,  $V_{2,3}$ , and  $V_{2,4}$ , need to be designed. The MV side filter capacitors realize a capacitive voltage divider, which enables voltage balancing in the case of time varying output currents, i.e., ac currents. These voltage controllers, therefore, need to compensate unbalancing due to slowly varying output current deviations of the different modules. For this reason, the respective closed-loop bandwidths can be set to a comparably low value

$$\omega_{\varphi,V2} = \omega_{\varphi,V2,2} = \omega_{\varphi,V2,3} = \omega_{\varphi,V2,4} = \omega_{\varphi,V1}/10 \quad (49)$$

i.e., an order of magnitude below  $\omega_{\varphi,V1}$  is selected (see Fig. 28), in order to avoid interactions between the voltage controller used to stabilize  $V_1$  and the MV side voltage controllers. The controllers are designed according to the symmetric optimum method for a phase margin of  $\varphi_{V1} = 60^\circ$ . Table XI summarizes the resulting controller parameters.

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