Conceptualization of a Cryogenic 250-A Power Supply for High-Temperature-Superconducting (HTS) Magnets of Future Particle Accelerators

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***Abstract*—Future particle accelerators for high-energy physics experiments such as the Future Circular Collider (FCC) at CERN employ high-temperature-superconducting (HTS) magnets to guide and focus the particle beams. However, the high-current/large-cross-section copper conductors used to connect the HTS magnet coils to the power supply conventionally located outside of the cryostat create a thermal leakage path, which ultimately results in high energy consumption of the cryocoolers. The heat leak-in could be reduced by power delivery through the cryostat's heat shield at higher voltage levels and hence with lower currents. However, then a power electronic conversion to the low voltage and high current needed by the HTS magnets must be provided inside of the cryostat. Given the increased complexity, such a concept is only sensible if the resulting total heat load, i.e., the sum of the converter losses and the (then lower) leak-in losses, is so low that a clear improvement of the overall energy efficiency results. In this paper, we therefore conceptualize a cryogenic power supply for a 250-A HTS magnet, which operates at 60 K. Considering the strict EMI limits applicable in the CERN environment, a co-design method for the current leads and a full-bridge multiphase buck dc-dc converter is introduced and used to explore the design trade-offs. The results indicate that a reduction of the total heat load by about a factor of three to four compared to the state of the art seems feasible, i.e., from about 21 W to about 5 W.**

***Index Terms*—Cryogenic power supply, particle accelerators, superconducting magnets.**

I. Introduction

High-energy physics studies the fundamentals of matter and radiation, whereby particle accelerators such as the Large Hadron Collider (LHC) at CERN in Geneva, Switzerland, are used to generate beams of high-velocity/high-energy particles (e.g., electrons or protons). Controlled collisions of particles in opposite beams inside of highly specialized detectors facilitate the experimental study of predictions from fundamental physics theories. Currently, a feasibility study for the LHC's successor is underway [1]. This Future Circular Collider (FCC) would facilitate experiments at even higher collision energy levels than the LHC. As the electricity consumption of the LHC is significant (about 750 GWh/a [2] or the equivalent of the per-year usage of about 150 000 Swiss households), one design objective for the FCC is improved energy efficiency.

As illustrated in **Fig. 1a**, circular colliders employ a high number of very strong electromagnets to deflect/guide and focus the particle beam on its approximately circular trajectory. **Fig. 1b** shows a typical mission profile: after a ramp-up phase, the magnet usually operates for many hours with constant flux density and hence constant current $I_{m,n}$. **Fig. 1c** gives a system-level overview of a magnet power supply unit (PSU). Note that to ensure a very high beam quality, the CERN application requires extreme accuracy (in the 10-ppm range [3]) of the magnet current; the corresponding sensors and processing electronics do exist and are not part of the PSU itself. Instead, the PSU stage closest to the magnet acts as a controlled voltage source with very low EMI emissions at its output to comply with the strict EMC requirements in the

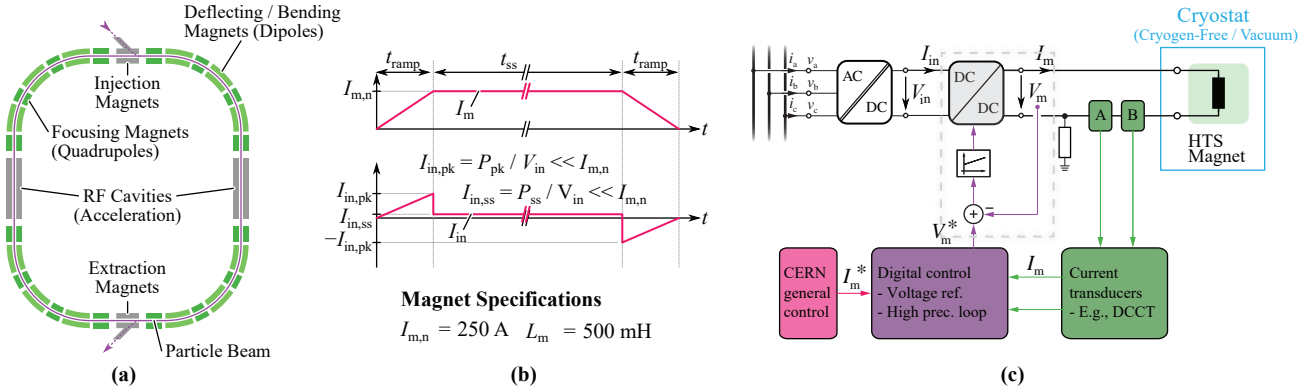

Fig. 1. (a) Conceptual representation of a circular accelerator with its main magnet systems. **(b)** Mission profile of the magnet current, which is kept at a constant dc value for many hours, and of the PSU input current, which is almost zero in the steady state. **(c)** System-level overview of a magnet power supply system; this paper focuses on the dc-dc converter stage closest to the magnet, which acts as a controlled voltage source.

CERN environment [4]; it is this converter stage that this paper focuses on.

Today, the magnets are either normal-conducting, creating high conduction losses, or realized with superconducting coils operating at 1.9 K inside of a cryostat under vacuum, where the thus needed large-scale cryogenic infrastructure is a major contributor to the overall energy consumption. Given that the FCC's target circumference is about three times longer than the LHC's (100 km vs. 27 km), which implies a corresponding increase in the number of magnets, more efficient magnet systems are needed. An interesting option are magnet coils made from high-temperature superconductors (HTS) that can operate at higher temperatures (e.g., around 40 K).

Typically, the complete power converters that supply cryocooled HTS magnets with the necessary high (several 100 A to several kiloamperes) dc currents of high quality (low ripple, high stability, etc.) are placed outside of the cryostat [5]–[8]. Therefore, copper conductors of sufficient cross section to carry the nominal magnet current of here $I_{\mathrm{m,n}} = 250\,\mathrm{A}$ must penetrate the cryostat's heat shield, see **Fig. 2a**. The thus established thermal leak-in path results in a parasitic heat flow into the cryostat, which, together with the Joule heating in these current leads, determines the total heat load that must be removed by the cooling system to maintain the cryostat's temperature.

It is well known that for a given design current and given temperatures on either side of the current lead there is an optimum ratio of length, L_0, to cross section, A_0, that minimizes the total leak-in losses [9]: Given the mission profile from **Fig. 1d**, the L_0/A_0 ratio of the current leads for conventional magnet PSUs (**Fig. 2a**) is thus optimized for the steady-state magnet current of $I_{\mathrm{m,n}} = 250\,\mathrm{A}$, resulting in

$$P_{\text{leak-in}} = 2 \cdot I_{\mathrm{m,n}} \cdot \sqrt{2\left(\frac{\kappa}{\sigma}\right)_T \cdot (T_{\mathrm{a}} - T_{\mathrm{cr}})} \approx 21\,\mathrm{W} \qquad (1)$$

for two current leads (thus the factor 2), where

$$\left(\frac{\kappa}{\sigma}\right)_T = \frac{1}{T_{\mathrm{a}} - T_{\mathrm{cr}}} \int_{T_{\mathrm{cr}}}^{T_{\mathrm{a}}} \frac{\kappa(T)}{\sigma(T)}\, dT \qquad (2)$$

takes into account the temperature-dependencies of the material's electrical (σ) and thermal (κ) conductivities [9]. Consequently, relatively large and thus expensive cryocoolers are needed, which, as mentioned, show a significant energy consumption (typ. 20 W for each 1 W to be extracted, for $T_{\mathrm{cr}} = 60\,\mathrm{K}$ and $T_{\mathrm{a}} = 300\,\mathrm{K}$ [10]). Note that $T_{\mathrm{cr}} = 60\,\mathrm{K}$ refers to a first thermal zone inside of the cryostat where the terminal blocks for the current leads are located; from there, HTS leads carry the current to the HTS magnet that is placed in a second thermal zone with a lower temperature.

By increasing the voltage level at which the power transfer into the cryostat is performed, the current in the leads can be made much lower than the magnet current, but this requires a step-down dc-dc converter that operates inside of the cryostat at a temperature of $T_{\mathrm{cr}} = 60\,\mathrm{K}$, i.e., a cryogenic power supply unit (CryoPSU), see **Fig. 2b**. Especially in the steady state, the input (lead) current is then determined by the small steady-state input power (i.e., mainly needed to cover the losses of the converter itself as the HTS magnet with its wiring and contact resistances has an overall series resistance of a few µΩ at most), delivered to the dc-dc converter and hence $I_{\mathrm{in,ss}} \ll I_{\mathrm{m,n}}$. This reduces $P_{\text{leak-in}}$ accordingly, but the CryoPSU's loss budget is very low (i.e., the sum of the now reduced leak-in losses *and* the CryoPSU's losses must be $\ll 21\,\mathrm{W}$; a reduction by a factor of two to four is targeted). Only then a clear reduction of the cryocooler power rating[1] and a corresponding improvement of the energy efficiency can be achieved, which would justify the increase in complexity.

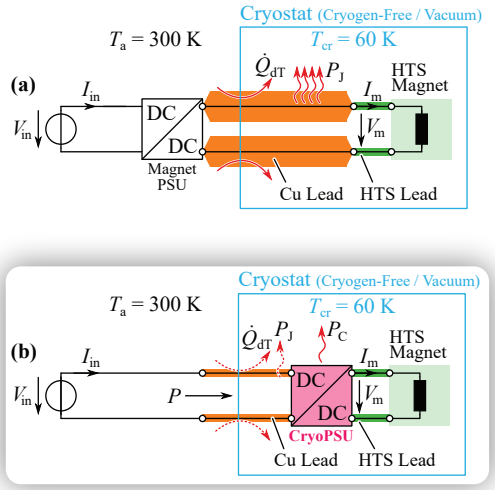

Fig. 2. (a) Conventional magnet power supply, where the magnet current, $I_{\mathrm{m,n}}$, defines the required cross section of the feedthroughs from the warm environment into the cryostat chamber. **(b)** Proposed cryogenic magnet power supply, where a dc-dc step-down converter operating *inside* of the cryostat decouples the feedthrough current from the magnet current. The mains interface shown in **Fig. 1c** has been replaced by a dc voltage source, V_{in}. Note that for simplicity only one thermal zone ($T_{\mathrm{cr}} = 60\,\mathrm{K}$) inside of the cryostat is shown, whereas typically the magnet itself would be placed in a second zone and operate at lower temperatures, e.g., around 40 K.

There are a few studies that propose and analyze CryoPSU concepts based on similar isolated converter topologies as used in conventional systems [11]–[13], and [14] describes a non-isolated step-down dc-dc magnet PSU, but without a detailed analysis of the design trade-offs, the current leads, and EMI filtering aspects. This paper therefore comprehensively analyzes the key trade-offs in the design of a dc-dc CryoPSU system, taking into account also the current leads and the ramp-up/down phases of the magnet current (see **Figs. 1b**). **Section II** first gives more detailed requirements and discusses the system-level operating modes. **Section III** describes the EMI filter design and the loss models of the key components, including the current leads, and **Section IV** presents the design trade-offs and the selection of an exemplary design (total heat load of about 3.9 W, not including control electronics), before **Section V** concludes the paper.

[1]Note that such smaller cryocoolers could ultimately facilitate even wall-pluggable, standalone (i.e., without the need for cooling water supply, etc.) HTS magnet systems, e.g., for off-site medical or research applications.

TABLE I
MAIN SPECIFICATIONS FOR THE CRYOPSU.

Symbol	Description	Value
$I_{m,n}$	Nom. magnet current	250 A
L_m	Max. magnet inductance	500 mH
t_{ramp}	Max. ramp-up time	1000 s
T_a	Ambient (outside) temp.	300 K
T_{cr}	Cryostat (inside) temp.	60 K
$(di/dt)_{corr}$	Max. correction di/dt	±0.5 A/s
$f_{c,v}$	Voltage control bandwidth	10 kHz
L_0	Current lead length	0.3 m

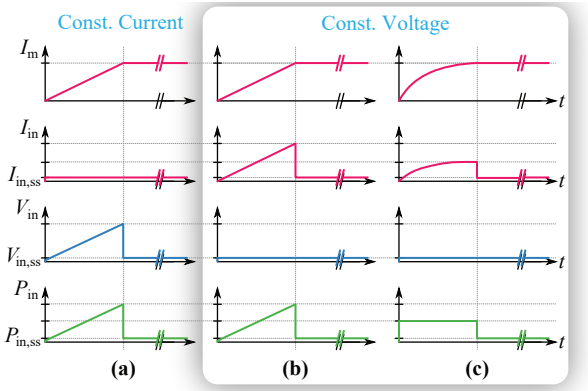

Fig. 3. Operating regimes for the ramp-up (and likewise ramp-down, not shown) phases. **(a)** Constant input current and **(b)** constant input voltage with a linear magnet current ramp. **(c)** Constant input voltage and constant-power charging of the magnet, which advantageously results in lower peak input power compared to (b).

II. System-Level Design Considerations

This section discusses system-level design considerations in more detail and derives the requirements for the CryoPSU.

A. Operating Modes

Considering the mission profile from **Fig. 1b**, the HTS magnet losses are nearly zero in the steady state and hence the input power of the CryoPSU is largely determined by its own losses. These are necessarily low for the concept to be meaningful. However, during the ramp-up phase[2], the HTS magnet's energy increases from zero to $E_m = 1/2 \cdot L_m I_{m,n}^2$, which implies that the input power during this phase must be higher to "charge" the magnet. The ramp-up is typically relatively slow (here $t_{ramp} = 1000\,s$ for $L_m = 500\,mH$) to mitigate the risk of eddy current formation in the HTS magnets [15].

There are two basic options for handling this higher input power: **(i)** The input current is kept constant (see **Fig. 3a**), i.e., the leads operate with the same current as in the steady state and their geometry can thus be optimized accordingly, and the input voltage is increased. This, however, requires coordination between the CryoPSU and the upstream converter (mains interface, see **Fig. 1c**), might further complicate paralleling of several CryoPSUs if needed, and adversely impacts the design of the CryoPSU's EMI filter (higher voltage-time areas

[2]Similar considerations apply to the ramp-down phase.

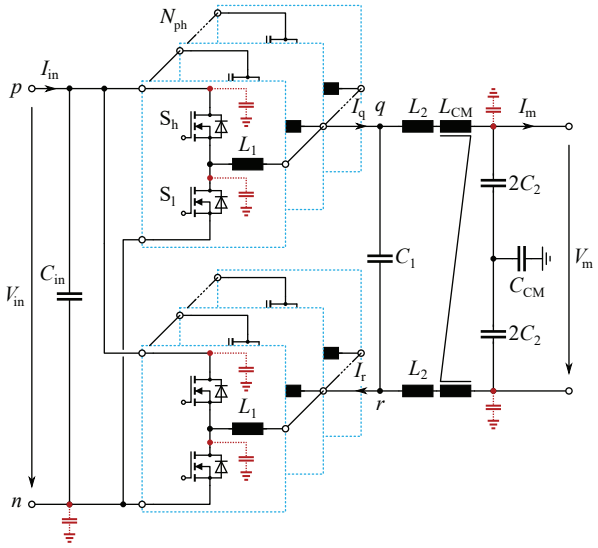

Fig. 4. Schematic of the CryoPSU full-bridge step-down dc-dc converter that consists of two multiphase buck converters and a CM/DM EMI output filter; parasitic earth capacitances are indicated in red.

applied to the inductors); this option is therefore discarded. **(ii)** The input voltage is kept constant but thus the lead current increases with the input power (see **Fig. 3b**). Therefore, the current leads must be designed such that the leads' allowable peak temperature is not exceeded during the ramp-up phase with the higher current. This might necessitate a thicker lead than what would be optimum for the steady-state operation, and hence increase the steady-state leak-in losses.[3] Finally, it is therefore advantageous to charge the magnet with constant power (see **Fig. 3c**) and hence a non-linear magnet current trajectory, which reduces the maximum charging power to $P_{charge} = E_m/t_{ramp} = 15.6\,W$, i.e., half the maximum value from **Fig. 3b**, with an according reduction of the maxim lead current during the ramp-up phase; this is the preferred mode of operation.

B. Specifications and Topology Selection

Tab. I summarizes the key specifications of the CryoPSU, i.e., a step-down dc-dc converter that, essentially, acts as an amplifier with a controlled output voltage. Given the high output (magnet) current and the tight loss budget, paralleling of semiconductors becomes necessary to limit conduction losses. Furthermore, a relatively high voltage control bandwidth (about 10 kHz, to provide sufficient margin for an outer magnet current control loop, see **Fig. 1c**) is needed, as well as very low EMI emissions, i.e., an EMI filter. Hence, instead of simply paralleling semiconductors, parallel-interleaving of multiple half-bridges with output inductors to form a multiphase buck converter is advantageous: ideally, the first switching-frequency harmonics appear at the *effective* switching frequency

[3]Note that in applications where very short ramp times could be used, also the heat capacity of the leads could be leveraged to increase the charging power/current while still not exceeding a defined peak temperature. E.g., this might be of interest for magnet protection concepts if the magnet energy cannot be dissipated inside of the cryostat but should be extracted quickly to a dump resistor on the outside.

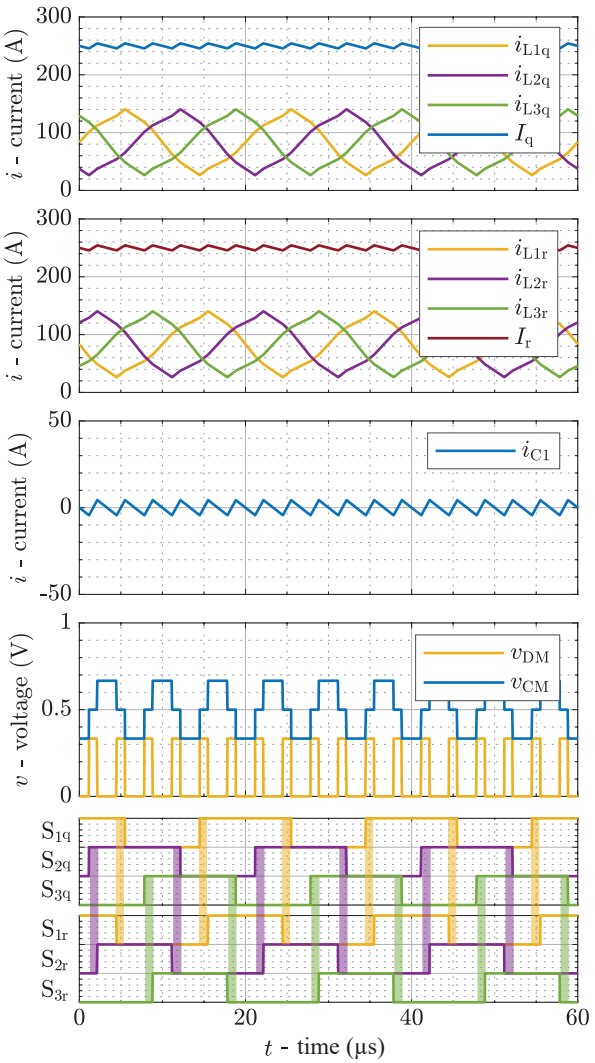

Fig. 5. Exemplary key waveforms of a full-bridge realized from two multiphase buck converters (see **Fig. 4**) with an input dc voltage of $V_{in} = 1\,V$ and $N_{ph} = 3$ phases per converter, each switching with $f_{sw} = 50\,kHz$. Note how the interleaved operation of all six bridge-legs (see the gate signals $S_{i,a}$ and $S_{j,b}$) advantageously creates a DM noise source with an effective switching frequency of $f_{sw,eff} = 2N_{ph}f_{sw} = 300\,kHz$, which is clearly visible in the filter capacitor current, i_{C1}.

$f_{sw,eff} = N_{ph}f_{sw}$, where N_{ph} is the number of phases and f_{sw} the half-bridge switching frequency; advantageously, the EMI filter cutoff frequencies can then be higher and/or the device switching frequency (and hence the switching losses) lower. Therefore, multiphase buck topologies are often used for systems with low output voltages and high output currents such as CPU power supplies [16], but also in non-cryogenic [6], [8] and, recently, in a cryogenic [14] magnet power supply.

Finally, the CryoPSU also should provide negative output voltages to discharge the magnet or to implement correction actions as required by the higher-level current control. To provide a bipolar output voltage, either a multiphase buck structure can be combined with an unfolder bridge-leg [6] (consisting of many parallel-connected semiconductors with the corresponding challenges regarding equal current sharing). Alternatively, two multiphase buck converters can be combined into a full-bridge arrangement [6], [7] as shown in **Fig. 4**. Then, unlike the unfolder case, for the low differential-mode output voltage needed by the magnet (whose resistance is almost zero), all bridge-legs operate with a duty-cycle close to 0.5, resulting in a quite even loss distribution among the semiconductors. Whereas the total switching losses increase (compared to the unfolder approach), the control of an output voltage very close to zero should be smoother, as there is no need for mode-switching to reverse the output voltage polarity (switching of the unfolder bridge-leg, and jumps in the duty cycle of the multiphase buck converter). Furthermore, the operation of the two multiphase buck converters can be phase-shifted, which again doubles the effective switching frequency compared to that of a single multiphase buck converter; this is illustrated by the simulated example waveforms shown in **Fig. 5**.

Whereas the full-bridge multiphase buck topology thus is a natural choice for the application at hand, there are various degrees of freedom in its design, e.g., the number of phases, the switching frequency, the input voltage, the power semiconductor selection, the EMI filter design, etc. Importantly, also the optimum design of the current leads should be considered when evaluating the feasibility of a CryoPSU concept meeting the tight loss budget. These aspects are discussed in the following **Section III**.

III. System Design and Optimization

Aiming at ultimately quantifying the achievable performance of a CryoPSU concept (i.e., the heat load for the cryocooler), this section discusses the EMI filter design, the modeling of the main components' losses (current leads, semiconductors, phase inductors), and finally the employed optimization algorithm.

A. EMI Filter Design

Fig. 6 derives the differential-mode (DM) and common-mode (CM) EMI equivalent circuits for the full-bridge multiphase converter shown in **Fig. 4**, where a two-stage DM EMI filter and a single-stage CM filter are considered. Each individual half-bridge can be represented by a switched current source and a paralleled inductor according to Norton's theorem. By doing so, the multiphase buck converter can be easily modeled as the parallel connection of the Norton equivalents representing each bridge-leg (see **Fig. 6a**). Then, applying Thévenin's theorem, the final representation of a multiphase buck converter by a switched voltage source and a series inductor results. Conveniently, the equivalent DM and CM equivalent circuits (see **Fig. 6bc**, where the EMI filter elements are included, too) of the considered full-bridge arrangement can be achieved by connecting the two equivalent circuits of the two multiphase buck converters either in anti-series (DM) or in parallel (CM). The corresponding voltage noise sources thus become

$$v_{DM} = \sum \frac{v_{swp,i}}{N_{ph}} - \sum \frac{v_{swn,i}}{N_{ph}}, \text{ and} \tag{3}$$

$$v_{CM} = \frac{1}{2} \cdot \left(\sum \frac{v_{swp,i}}{N_{ph}} + \sum \frac{v_{swn,i}}{N_{ph}} \right). \tag{4}$$

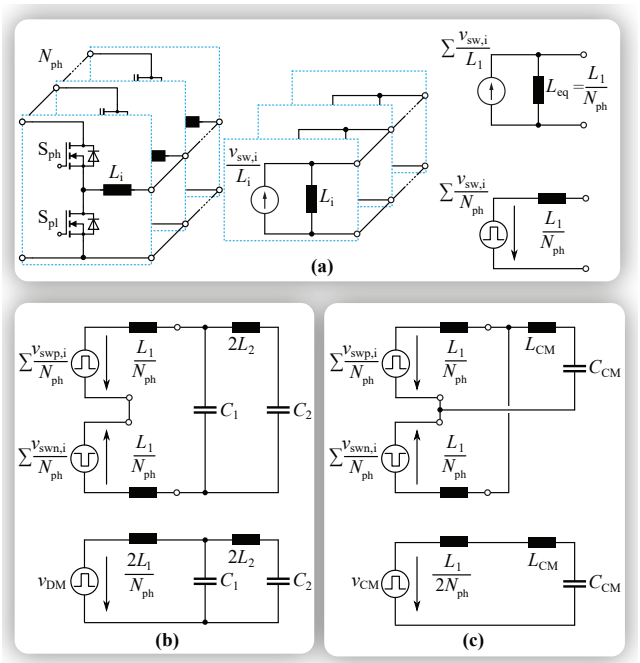

Fig. 6. Derivation of the EMI equivalent circuits of the full-bridge multiphase buck converter shown in **Fig. 4**, from **(a)** bridge-leg level to multiphase buck converter level. Finally, the **(b)** DM and **(c)** CM equivalent circuits result.

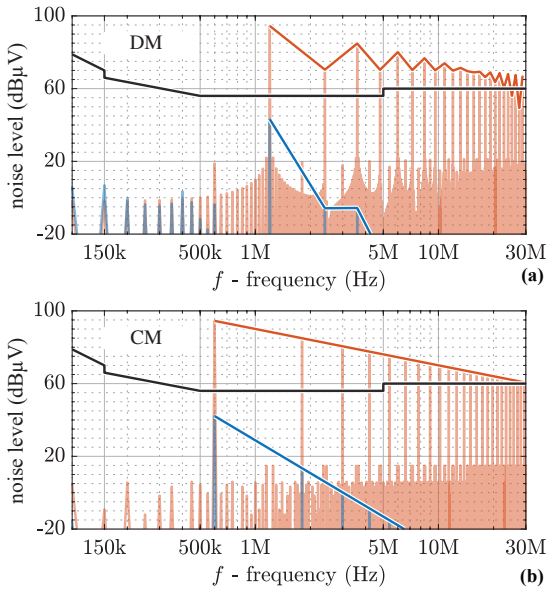

Fig. 7. Simulated DM and CM noise emissions (maximum QP approximation [17]) without (orange) and with (blue) a designed EMI filter for an exemplary converter with $V_{\text{in}} = 1\,\text{V}$, $N_{\text{ph}} = 12$, $f_{\text{sw}} = 50\,\text{kHz}$; an RC damping branch is connected in parallel to C_2 [18]. **(a)** DM and **(b)** CM noise at the respective worst-case operating points. The CERN QP EMI limit [4] is also shown.

The maximum required DM attenuation is required if the duty cycle of v_{DM} (see **Fig. 5**) is 0.5. To consider the worst-case for the CM EMI filter, the parasitic input capacitors are shorted by grounding the negative input terminal such that the CM noise source is directly connected to the CM filter (without the series impedance divider otherwise formed by the parasitic capacitors), see **Fig. 6c**; the worst-case operating

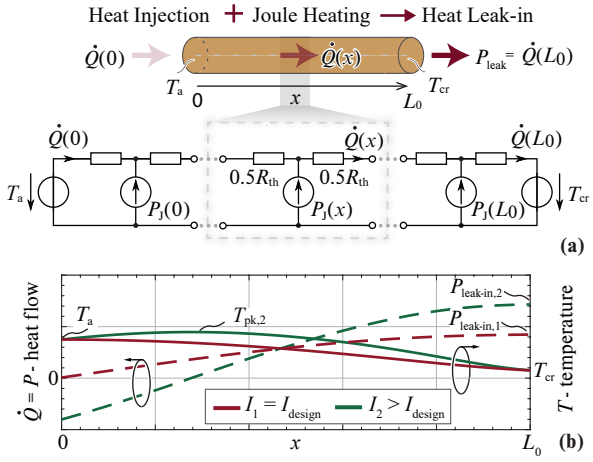

Fig. 8. **(a)** Steady-state 1-D thermal model of a current lead considering both, heat flows because of the temperature difference between input and output, and Joule heating due to the electrical current. **(b)** Exemplary spatial profiles of temperature $T(x)$ and heat flows $\dot{Q}(x)$ for two different lead currents (corresponding either to the design current for which the lead geometry has been optimized, or to a higher current resulting in a peak temperature $T_{\text{pk}} > T_{\text{a}}$).

point occurs if v_{CM} (see **Fig. 5**) is a square wave with full duty ratio. At the respective worst-case operating points, the required DM and CM filter attenuations are estimated based on [19], i.e., the total high-frequency rms noise is assumed to occur at the (effective) switching frequency ($2N_{\text{ph}}f_{\text{sw}}$ for DM and $N_{\text{ph}}f_{\text{sw}}$ for CM, see **Fig. 5** and **Fig. 7**). Furthermore, we consider a 16 dB margin to account for component tolerances and a possible superposition of CM and DM noise.

The DM filter element values are then obtained by first defining that both filter stages should have equal resonant frequencies [19], which can then be found from the required attenuation at the (effective) switching frequency. The first-stage DM inductance, which is given by the series/parallel connection of the phase inductors, is designed to limit the peak-to-peak phase current ripple to 20%. From that, C_1 immediately follows, and by requiring $C_2 = C_1$, so does L_2. Considering the CM filter, $C_{\text{CM}} = 80\,\text{nF}$ is selected as a typical value, and thus L_{CM} follows from the required cutoff frequency. The exemplary simulation results shown in **Fig. 7** validate the filter design approach and confirm the 16 dB margin to the CERN EMI limit from [4].

B. Design and Modeling of Main Components

1) Current Leads: Two coupled mechanisms contribute to the leak-in losses, $P_{\text{leak-in}}$, from the current leads into the cryostat: heat conduction due to the large temperature difference between the ambient temperature, T_{a}, and the temperature T_{cr} inside of the cryostat, and Joule heating caused by the current flowing in the lead. As indicated in **Fig. 8a**, the steady-state thermal behavior of the lead, i.e., the local heat flows $\dot{Q}(x)$ and the spatial temperature distribution along the lead can be modeled with a straightforward thermal network by dividing the lead into many smaller segments [9] (note that the vacuum in the cryostat restricts the heat flow essentially to the axial direction). Each segment features a thermal and

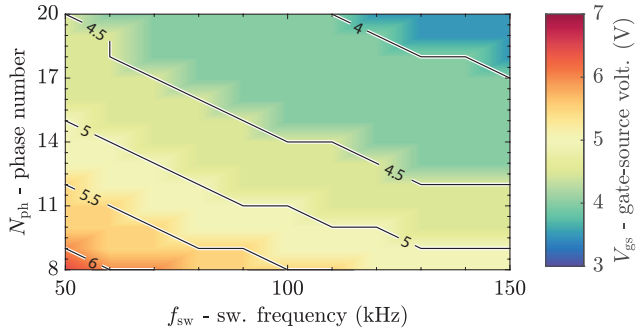

Fig. 9. Selection of the optimal gate-source voltage V_{gs} to minimize the sum of gate driver losses and conduction losses at different switching frequencies f_{sw} and number of phases N_{ph}; the 25 V, 0.65 mΩ Si MOSFET IQE006NE2LM5CG is considered as an example.

an electrical resistance, both defined by the geometry and the temperature-dependent electrical or thermal conductivities. Using superposition, the heat flow contributions from all sources in the thermal network are calculated individually; a few iterations of updating the local heat generation, the heat flows, etc. are sufficient to arrive at precise results. The heat flow at the cold end of the lead is the heat leak-in, i.e., $P_{\text{leak-in}} = \dot{Q}(L_0)$.

Fig. 8b shows the temperature profile along an exemplary current lead and the local heat flow, $\dot{Q}(x)$, for two different lead currents: For operation with the design current (for which the lead's geometry, i.e., its L_0/A_0 ratio, has been optimized), the temperature profile is horizontal at the warm end (i.e., $(dT/dx)_{x=0} = 0$) and then decreases monotonically between T_a and T_{cr}. For higher currents, the Joule heating increases and so do the leak-in losses, and, importantly, the temperature distribution peaks along the lead at $T_{pk} > T_a$. The permissible peak temperature (e.g., from isolation material ratings, etc.) thus limits the maximum current a given lead can carry, e.g., during the ramp-up/down phases as discussed in **Section II**.

2) Power Semiconductors: Si MOSFETs and GaN FETs are commonly seen as promising transistors to operate at cryogenic temperatures with decent losses [20]. The overall semiconductor losses are the sum of three main parts: conduction losses, switching losses, and driver losses. The overall conduction losses of the multiphase full-bridge converter are

$$P_{\text{cond}} = \frac{2}{N_{\text{ph}}} \cdot R_{\text{DS,on}}(V_{\text{gs}}) \cdot {I_{\text{m,n}}}^2. \tag{5}$$

A 70% reduction (compared to room-temperature operation) [20] of the on-state resistance $R_{\text{DS,on}}$ is assumed when operating at $T_{cr} = 60$ K (note that the per-transistor power dissipation is, given the loss budget, necessarily so low that the junction temperature can be assumed to equal that of the cooling interface). Note further that $R_{\text{DS,on}}$ depends on the gate-source voltage V_{gs}, i.e., $R_{\text{DS,on}}$ reduces with increasing V_{gs}; datasheets provide the device-specific non-linear relationships. On the other hand, the total gate driver losses P_{driver} are

$$P_{\text{driver}} = 2 \cdot N_{\text{ph}} \cdot f_{\text{sw}} \cdot Q_{\text{gate}}(V_{\text{gs}}) \cdot V_{\text{gs}}, \tag{6}$$

where the gate charge Q_{gate} is provided in datasheets. Therefore, there is a trade-off between conduction and driver losses, which can be adjusted by the gate voltage selection. This trade-off is especially important in the considered application, where the conduction losses must be extremely low and are hence in the same order of magnitude as the driver losses. Thus, for a given switching frequency f_{sw} and a given number of phases N_{ph}, an optimum gate-source voltage V_{gs} that minimizes the sum of conduction and driver losses exists, see the example in **Fig. 9**. Note that the dc-link voltage V_{in} does not affect this trade-off, but only the switching losses. These, which due to the low switched voltage tend to be very low, are modeled with lookup-tables/polynomial fits [21], [22] based on data extracted from manufacturer's LTspice models.

3) Phase Inductors: The phase inductance is designed to limit the maximum peak-to-peak current ripple for the bridge-leg duty cycle $D = 0.5$ (the worst-case operating point) to 20%, and the physical inductor realization is selected using the Pareto optimization from [23]. Even though the electrical conductivity of copper at cryogenic temperatures can be roughly ten times higher than at room temperature [24], [25], we conservatively assume a reduction of the winding resistance by 70%, i.e., to account for possible temperature gradients along the winding and to include a design margin. Similarly, the properties of magnetic materials change at cryogenic temperatures [20], [26], [27]. Ferrite, for example, can show up to ten times higher core losses and a significantly reduced (by about 80%) permeability [25], [27]. In contrast, powder cores show a more favorable behavior; therefore only Kool-Mu cores are considered, for which we conservatively assume twice the core losses and half the permeability (compared to operation at room temperature) [20], [25]. Finally, from the many inductor designs the Pareto optimization generates, the smallest realization that gives at most 30% higher losses than the minimum possible is selected; the maximum volume is limited to 50 cm^3.

4) EMI Filter: The second-stage DM and CM inductors (see **Fig. 4**) conduct the total magnet current of 250 A, and there are no significant high-frequency components left. Therefore, to limit the losses to essentially zero, the windings can be realized with HTS tapes [26], and core losses are assumed to be negligible; the same holds for the filter capacitor losses.

C. Optimization Algorithm

Using the aforementioned design steps and models, it becomes possible to generate a high number of possible converter designs, which then allows to visualize the design trade-offs and to ultimately identify the configuration that achieves lowest overall heat load for the cryocooler. **Fig. 10** shows a flowchart representation of the MATLAB implementation. Suitable ranges of the main degrees of freedom (input voltage, number of phases, switching frequency, and gate drive voltage) are considered as indicated in the figure. Regarding the semiconductor selection, it is sensible to consider a device with sufficient blocking voltage and the lowest per-package on-state resistance available, i.e., a 25 V, 0.65 mΩ Si MOSFET. On the other hand, if the CryoPSU should *integrate* a quench

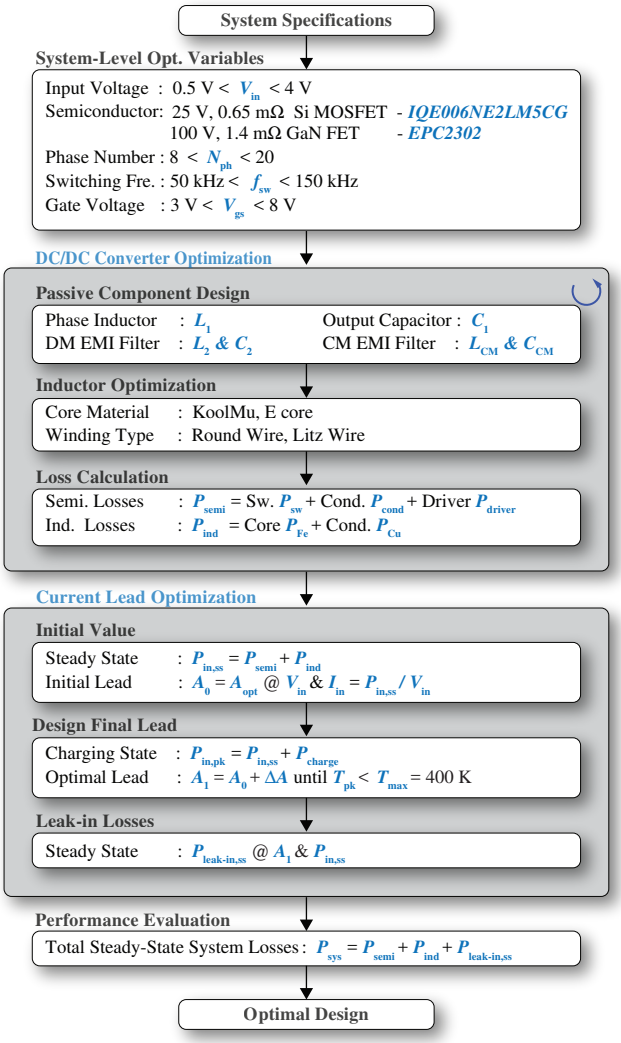

Fig. 10. Flowchart of the optimization procedure for the full-bridge multiphase buck CryoPSU system shown in **Fig. 4**, including the current lead design.

protection mechanism for the HTS magnet, higher blocking voltages would be needed.[4] Therefore, we also include a 100 V, 1.4 mΩ GaN device. The minimum switching frequency is selected as 50 kHz, which ensures sufficient reserves regarding the targeted voltage control bandwidth [28].

For each combination of the design degrees of freedom, the algorithm first designs the EMI filter (see **Section III-A**) and then calculates the converter losses (see **Section III-B**) in steady-state operation; this corresponds to the steady-state input power of the CryoPSU, $P_{\text{in,ss}}$, as losses in the magnet itself are negligible. As ultimately also the heat leak-in through the current leads contributes to the overall heat load, next, the current leads are optimized for the steady-state input current (i.e., since the length is fixed, the optimum cross section A_0 is calculated). However, during the ramp-up phase, the input

[4]A detailed discussion is beyond the scope of this paper and will be considered in future work. Suffice to say that in case of a quench, i.e., local hot-spot formation in the superconducting magnet, it is necessary to quickly reduce the magnet current, which requires relatively high negative voltages.

TABLE II
KEY PARAMETERS OF THE DESIGN HIGHLIGHTED IN **FIG. 11**.

	Description	**Value**
S	Semiconductor	IQE006NE2LM5CGSC (25 V, 0.65 mΩ)
V_{in}	Input voltage	1 V
N_{ph}	Number of phases	12
f_{sw}	Switching frequency	50 kHz
V_{gs}	Gate driver voltage	5.5 V
A_1	Current lead cross section	0.95 mm^2 (1.1 mm diam.)
L_1	Phase ind. (24×)	1.2 µH, KoolMu 90 (2×E30/15, 3 turns × 5.4 mm)
$C_1 = C_2$	Output DM cap.	1.8 µF
L_2	Output DM ind. (2×)	100 nH
L_{CM}	Output CM ind.	370 µH
C_{CM}	Output CM cap.	80 nF
P_{semi}	Semiconductor losses	2.4 W
P_{ind}	Phase ind. losses	0.8 W
$P_{\text{leak-in,ss}}$	Steady-state leak-in losses	0.7 W
P_{sys}	Total steady-state syst. losses	3.9 W

power of the CryoPSU increases by the charging power needed to energize the magnet and the worst-case total input power occurs just before the magnet current reaches the nominal value (see **Fig. 3c**), i.e., $P_{\text{in,pk}} = P_{\text{in,ss}} + P_{\text{charge}}$. The higher input current then leads to a hot-spot along the current lead (see **Fig. 8**), and the leads' cross section must be increased until T_{pk} is below the maximum allowed temperature, i.e., $T_{\text{pk}} \leq 400$ K. Note that therefore the current leads have a higher cross section than what would be optimal in the steady state, which, in turn, implies that finally the steady-state heat leak-in, $P_{\text{leak-in,ss}}$ must be calculated with the modified current leads.

IV. DESIGN RESULTS AND DISCUSSION

Fig. 11 summarizes the results obtained with the algorithm discussed above, and visualizes the design trade-offs for three different scenarios (i.e., combinations of switching frequency and power semiconductor), and various combinations of input voltage and phase count. For each design, the optimum gate drive voltage is used (note that this accounts for the difference in conduction losses observed for the Si-MOSFET-based designs operating at different switching frequencies in **Fig. 11a** and **Fig. 11b**, respectively). The first column shows the steady-state total system losses (the total heat load), P_{sys}, which is the *sum* of the steady-state leak-in losses and the CryoPSU losses. The losses of the two subsystems are coupled, e.g., a high input voltage V_{in} leads to increased switching losses and to higher inductor losses (due to the larger voltage-time areas applied to the inductors), but reduces the input current, and thus the leak-in losses.

In general, the high output current leads to dominating conduction losses and thus increasing the phase count, N_{ph}, reduces the total heat load. However, the increasing realization effort and complexity impose a soft upper limit on N_{ph}, e.g., more gate drives, current sensors, etc. are needed and

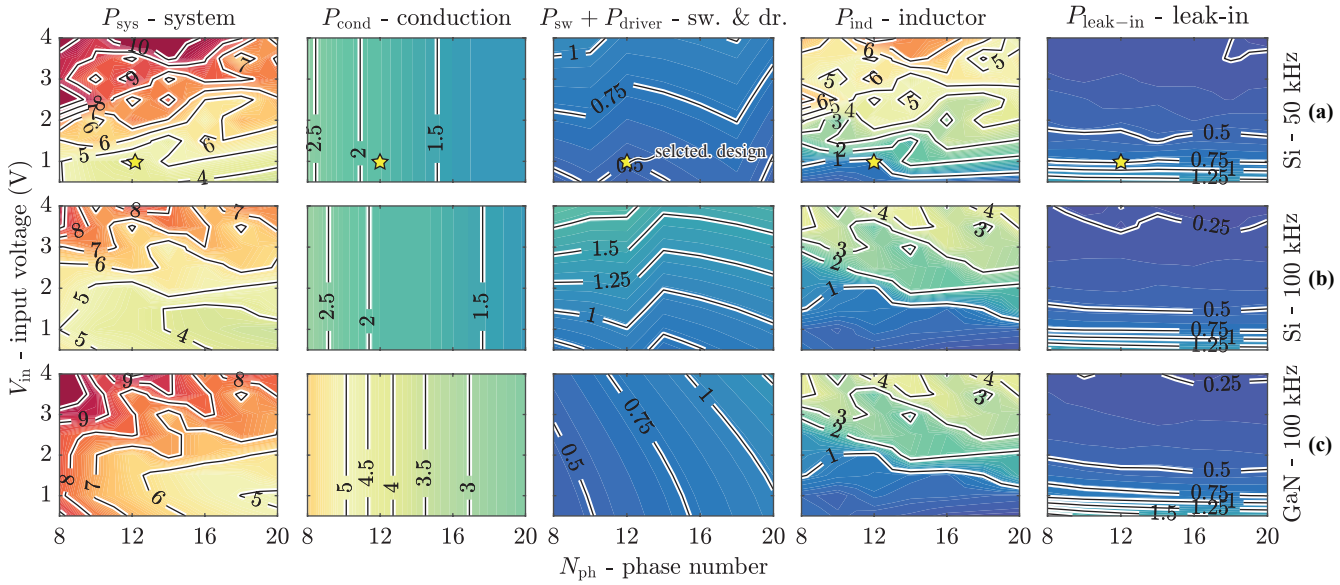

Fig. 11. Visualization of design trade-offs for the full-bridge multiphase buck CryoPSU (see **Fig. 4**), i.e., P_{sys} is the total steady-state heat load generated by the converter's main power components (conduction losses, P_{cond}; switching plus gate driver, $P_{sw} + P_{driver}$; phase inductor losses, P_{ind}) plus the leak-in losses, $P_{leak\text{-}in,ss}$. Three different scenarios are shown, i.e., **(a)** 25 V Si MOSFET with f_{sw} = 50 kHz and **(b)** with f_{sw} = 100 kHz, and **(c)** 100 V GaN FET with f_{sw} = 100 kHz. The star indicates an exemplary design that achieves low heat load with sensible realization effort, see details in **Tab. II**.

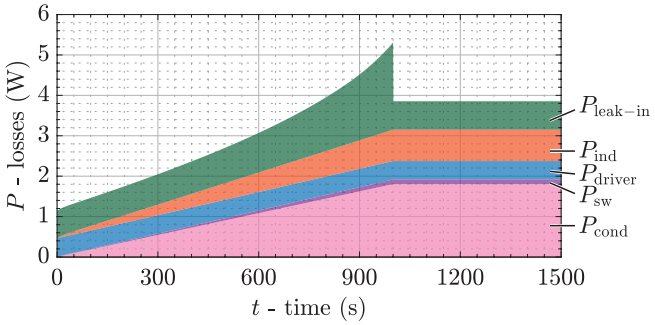

Fig. 12. Loss breakdown the CryoPSU design highlighted in **Fig. 11a** during the first part of a typical mission profile, i.e., ramping up the magnet current to 250 A within 1000 s, using constant-power charging.

the converter's reliability likely decreases with increasing component count. Thus, we select N_{ph} = 12 as a sensible compromise between realization effort and low heat load. Then, an exemplary CryoPSU realization with 25 V, 0.65 mΩ Si MOSFETs and a switching frequency of f_{sw} = 50 kHz yields a total steady-state heat load of about P_{sys} = 3.9 W. This design is highlighted in **Fig. 11a** and **Tab. II** lists its main parameters and performance indices. The target of a fourfold reduction of the heat load compared to the baseline (power supply outside of the cryostat) and hence a loss budget of 21 W/4 = 5.25 W leave ample margin for the power dissipation of the control electronics, which are not included in the calculated P_{sys} = 3.9 W.

As an aside, note that a realization with 100 V GaN FETs results in a higher heat load of about 6.5 W (considering again about N_{ph} = 12, see **Fig. 11b**), which is a consequence of the higher per-package on-state resistance. Still, including some margin for the control electronics, a reduction by about a factor of three compared to the conventional realization seems achievable. On the other hand, the higher blocking voltage would advantageously allow to integrate the quench protection functionality for the HTS magnet into the CryoPSU; a comparison of different protection concepts for CryoPSU-fed HTS magnets is, however, in the scope of future work.

Finally, again considering the selected Si-based design, **Fig. 12** shows the input power and the loss components during the first part of the typical mission profile (see **Fig. 1b** and **Fig. 3c**), i.e., the constant-power-charging (P_{charge} = 15.6 W = *const.*) ramp-up phase for t < 1000 s and then steady-state operation for t > 1000 s. Note that the leak-in losses towards the end of ramp-up phase are significantly higher than in the steady state, since the charging power leads to a corresponding increase of the input current; the design of the current leads still ensures that their peak temperature remains below 400 K. In steady state, the conduction losses account for about 45% of the total losses. However, still the leak-in losses contribute another 18%, which confirms the necessity of co-designing the current leads and the CryoPSU converter, as mentioned earlier. Interestingly, the gate driver losses contribute more than 10% of the total losses, i.e., much more than the switching losses (which, as a consequence of the low switched voltages, are low). Thus, resonant gate driver technology [29] could be a promising approach to further reduce the losses; but, this has to be weighed against the higher complexity.

V. Conclusion

Conventionally, the power supply units (PSUs) for high-temperature-superconducting (HTS) magnets are placed outside of the magnet's cryostat chamber and hence the current leads penetrating the cryostat's heat shield carry the magnet current. For the considered exemplary HTS magnet with a nominal dc current of 250 A, this results in a minimum heat leak-in

of about 21 W for optimally designed current leads. As each 1 W to be extracted requires at least about 20 W of cryocooler power consumption [10], there is a significant potential for improving the energy efficiency by reducing the heat load for the cryocoolers.

Any alternative solution necessarily must reduce the current in the leads and hence requires a step-down converter that operates inside of the cryostat at a temperature of 60 K. The sum of the then reduced heat leak-in and the converter losses must be significantly lower than 21 W for the concept to be sensible. Therefore, this paper introduces a co-design method for the current leads and a full-bridge multiphase buck converter, a CryoPSU, which meets the strict EMI limits applicable in the CERN environment. Considering a 250 A, 500 mH HTS magnet and an initial ramp-up (charging) time of 1000 s (note that magnets with lower inductance can be charged correspondingly faster with the same charging power and hence with the same CryoPSU), we first investigate the design trade-offs (e.g., the selection of the input voltage, etc.). Then, using a design with 1 V input voltage and two times twelve phases realized from 25 V Si MOSFETs switching at 50 kHz, we find total steady-state system losses (leads and converter) of about 3.9 W. Even when allowing some margin for the power dissipation of the control electronics, the resulting heat load is about four times lower than that of the conventional approach. All in all, the feasibility analysis presented in this paper indicates that moving the PSU of an HTS magnet into the cryostat, where it operates at a temperature of 60 K, can reduce the power consumption of the cryocoolers by a factor of three to four and hence contribute to more energy-efficient HTS magnet systems.

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