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Hardware Verification of a Hyper-Efficient (98%) and Super-Compact (2.2kW/dm^3) Isolated AC/DC Telecom Power Supply Module based on Multi-Cell Converter Approach

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***Abstract*—Due to the increasing electricity demand of data centers driven by the emergence of cloud computing and big data, the focus on the development of telecom and data center power supplies is shifted towards high efficiencies. In this paper, a multi-cell converter approach for a telecom rectifier module breaking through the efficiency and power density barriers of traditional single-cell converter systems is shown. The comprehensive optimization of the entire system with respect to efficiency and volume is described and the applied component loss models are explained. Furthermore, the design of a hardware demonstrator based on the optimization results is presented and several important design aspects are explained in detail.**

I. Introduction

Due to the increasing popularity of cloud based internet services and the trend around big data, the electricity consumption of data centers has grown tremendously in the past decade and is projected to grow in the future even further, e.g. around 70% from 2013 to 2020 in the US alone [1]. As a consequence, data centers are now one of the largest consumers of electricity and therefore also under a growing financial and political pressure to increase their energy efficiency.

Nowadays, conventional single-phase telecom power supplies typically consist of a PFC rectifier stage in connection with an isolated DC-DC converter stage in order to generate an output voltage of 48 V for the subsequent conversion stages. The rectifier stage is usually a boost-type PFC converter with a full bridge diode rectifier, that creates considerable conduction losses due to the forward voltage drops of the employed diodes. This has initiated a trend towards bridgeless topologies as an alternative topology [2], [3]. One example of a highly efficient power supply for telecom applications is a triple-parallel-interleaved TCM PFC rectifier system [4] in combination with a double-parallel-interleaved phase-shifted full-bridge isolated DC-DC converter (rated power $P_{\text{out}} = 3.3\,\text{kW}$, output voltage $V_{\text{out}} = 48\,\text{V}$) featuring a power density of $\rho = 3.3\,\text{kW/dm}^3$ and an efficiency of $\eta = 97\,\%$ at half of the rated power. As shown in [5], this concept currently presents the leading edge technology for telecom power supplies.

A new and very different approach towards a hyper-efficient and super-compact telecom rectifier design beyond the barriers of traditional converter concepts has been presented in [6]. The approach is based on a multi-cell converter concept with series connection of the converter cells at the input side and parallel connection at the output side (i.e. ISOP), as shown in **Fig. 1**. Each converter cell formed by an AC-DC rectifier stages which is operated with a Totem-Pole modulation and an isolated DC-DC converter stage consisting of phase-shifted full bridge converter. This multi-cell ISOP configuration allows to share the input voltage among the converter cells and thus enables the use of low-voltage rated semiconductors throughout the converter cells. According to the scaling laws of [7] with this approach significant benefits in terms of reduced conduction and switching losses and smaller volume of inductive components and heat sinks, among others, can be achieved. Based on the specification of **Tab. I** the system performance targets that should be reached by utilizing the advantages of the multi-cell converter topology are an output power of $P_{\text{out}} = 3.3\,\text{kW}$ with

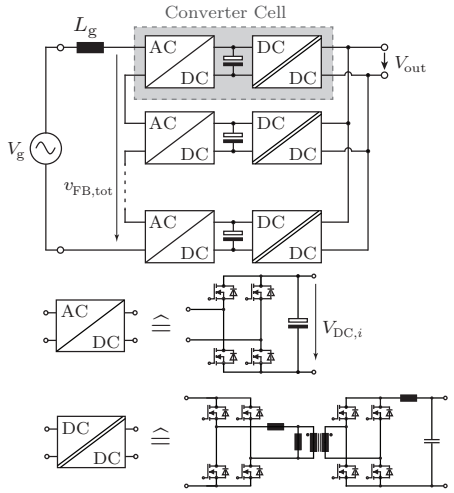

Fig. 1: Multi-cell telecom power supply module with input-series output-parallel connection of the converter cells. Each cell consists of a full bridge AC-DC rectifier input stage and an isolated DC-DC converter comprising a phase-shifted full-bridge converter.

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Tab. I: Specifications of the multi-cell telecom rectifier module.

Parameter	Variable	Value
Nominal grid voltage	$V_{\text{grid,RMS,nom}}$	230 V / 50 Hz
Grid voltage range	$V_{\text{grid,RMS}}$	180 V - 270 V
Rated output power	P_{out}	3.3 kW
Nominal output voltage	$V_{\text{out,nom}}$	48 V
Output voltage range	V_{out}	40 V - 60 V
Total DC-link voltage	V_{DC}	400 V
Hold-up time	T_{hold}	10 ms @ rated power
Switching freq. per cell	f_{sw}	$\geq$ 18 kHz
EMI standards		CISPR Class A and B

a conversion efficiency of 98% at part load operation and a power density of $\rho = 2.2\,\text{kW/dm}^3$.
In this paper, at first the optimization and of the system is discussed in detail and the results are analyzed in **Sec. II**. Afterwards, the realization of the hardware demonstrator is described in **Sec. III** and different design aspects are addressed. Finally, conclusions are drawn in **Sec. IV**.

II. System Optimization and Results

In [7] a comprehensive system modeling and optimization in terms of efficiency and power density of the ISOP multi-cell telecom rectifier module has been presented. In this optimization all available degrees of freedom for the design of the AC-DC and the DC-DC converter stages have been considered such as

- *Switching frequency*: The effective switching frequency of the AC-DC rectifier stage equals the switching frequency of a single cell multiplied by the number of cells due the interleaved operation of the rectifier stages, i.e. $f_{\text{sw,eff}} = N_{\text{cells}} \cdot f_{\text{sw}}$. A natural lower limit of the switching frequency of a single cell can be deducted from the range of audible frequency which should be avoided by choosing $f_{\text{sw}} \geq 18\,\text{kHz}$. The upper boundary of feasible switching frequencies can be derived by the CISPR EMI standards that impose limits on harmonics at frequencies above $f_{\text{EMI}} \geq 150\,\text{kHz}$ [8]. As a consequence the switching frequency per cell should be limited to $f_{\text{sw}} < f_{\text{EMI}}/N_{\text{cells}}$. This applies only to the AC-DC stages. The switching frequency of the DC-DC converter stages was swept over a wide frequency range ($50 - 500\,\text{kHz}$).
- *Design of inductive components*: The optimization of inductive components represents a Pareto trade-off on its own as several degrees of freedom for the design of the inductor and transformer, respectively, are given, like the core size, core material, conductor type, number of turns and air gap. With core and winding loss models the η-ρ Pareto-optimal designs can be found [9].
- *MOSFET chip size and junction temperature*: The chip size of the MOSFETs is an important parameter for the trade-off between conduction and switching losses [4], as given for the AC-DC stage which is operated under hard-switching. Furthermore, the thermal resistance between the junction and the case of the semiconductor changes with the chip size, which also influences the design and volume of the heat sink.

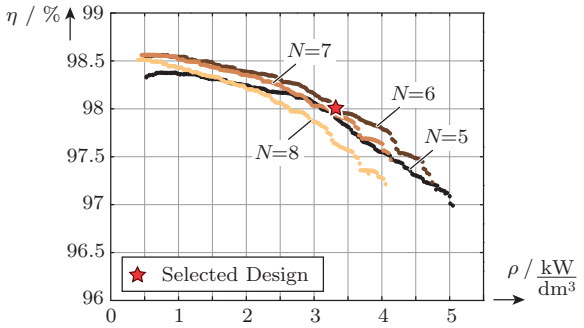

Fig. 2: Pareto-optimal (efficiency / power-density) designs of the multi-cell telecom power supply module for different numbers of converter cells and a drop of the DC-link voltage during the hold-up time of $k_{\text{DC,drop}} = 20\%$.

- *DC-link capacitor realization*: The size and type of the employed DC-link capacitors offers an trade-off between the overall volume of the DC-link capacitors and the losses caused by the equivalent series resistance (ESR).

These parameters, among others, are subject to a trade-off between the power-density and the efficiency of the entire system. Therefore, for all combinations of design parameters the system performance has to be determined by employing component loss and volume models.
The volumes of the converter designs have been determined by considering the sum of all component boxed volumes, such as the volume of the

- DC-link capacitors
- Inductive components
- EMI filter components
- Heat sink.

The volume of PCBs and control electronics have not been considered since they are layout dependent and thus not available for the optimization. For the calculation of the conversion efficiency following losses have been included:

- AC-DC Full-bridge MOSFETs
  - Switching losses
  - Conduction losses
  - Gate drive losses
- Phase-shifted Full-bridge MOSFETs
  - Conduction losses
  - Gate drive losses
- Synchronous rectifier MOSFETs
  - Conduction losses
  - Reverse recovery losses
  - Gate drive losses
- Inductive components
  - Core losses
  - Winding losses (incl. HF-losses).

In addtion, the losses caused by the equivalent series resistance of the electrolytic capacitors and constant losses caused by auxiliary and control electronics have been included. Design specific losses such as the conduction losses of the PCB have been omitted in the calculation as they vary with the layout.
As a result of this comprehensive system optimization a clear

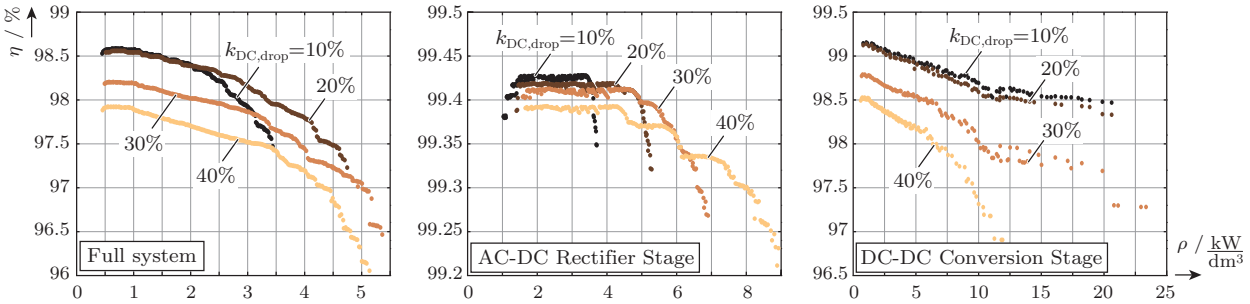

Fig. 3: Impact of different values of the maximum permissible drop of the DC-link voltage during the hold-up time, $k_{\mathrm{DC,drop}}$, on the achievable Pareto-optimal results of the entire system, the AC-DC rectifier stages and the DC-DC converter stages.

optimum can be found for the number of employed converter cells at $N_{\mathrm{opt}} = 6$. Even though the scaling laws derived in [7] predict a better performance with increasing number of cells, external and other practical constraints outweigh the benefits of a larger cell number, such as EMI limiting standards beginning at $f_{\mathrm{EMI}} = 150\,\mathrm{kHz}$, the package resistance of MOSFETs, and communication and control overhead.

The telecom supply is required to feature a hold-up time of $T_{\mathrm{hold}} = 10\,\mathrm{ms}$ (cf. **Tab. I** for the full set of specifications) which necessitates electrolytic capacitors within each cell. The voltage drop of these capacitors during the hold-up time was found to be another optimization parameters that exhibits an optimum at a value of $k_{\mathrm{DC,drop}} = 20\%$.

The Pareto-optimal results of the system optimization are shown in **Fig. 2** for full load operation at the nominal operating point for different numbers of converter cells and a maximum permissible drop of the DC-link voltage during the hold-up time of $k_{\mathrm{DC,drop}} = 20\%$.

The influence of $k_{\mathrm{DC,drop}}$ on the achievable system performance is depicted in **Fig. 3(a)** for the entire system and in **Fig. 3(b)** and **(c)** for the AC-DC and DC-DC stage, respectively. In the calculations the electrolytic DC link capacitors have been allocated to the AC-DC converter.

III. Hardware Demonstrator Design

The design which is selected for the hardware demonstrator with a calculated maximum efficiency of $\eta = 98\%$ at 75% of the rated output power and a power density above $\rho_{\mathrm{calc}} = 3\,\mathrm{kW/dm^3}$ is marked in **Fig. 2**. The main system parameters of the selected design are listed in **Tab. II**. A picture of the assembled prototype is shown in **Fig. 4** which features a volume of $\mathrm{Vol} = 30.4\,\mathrm{cm}{\cdot}4.5\,\mathrm{cm}{\cdot}11\,\mathrm{cm} = 1.504\,\mathrm{dm^3}$ and thus an overall power density of $\rho_{\mathrm{sys}} = 2.2\,\mathrm{kW/dm^3}$. The power density of the prototype is lower than the calculated value since the space between the components adversely affects the achievable power density and the volume of the PCB and the control boards have not been included in the calculations.

A detailed break down of the calculated losses and volumes is provided in **Fig. 5** for full load operation.

In the following paragraphs different design aspects of the converter system are described in detail.

Tab. II: Main system parameters of the selected design for the hardware demonstrator with $N = 6$ converter cells. (All values given per component, e.g. parallel MOSFETs, if not otherwise noted.)

AC-DC rectifier	
Switching frequency	$f_{\mathrm{sw,cell}} = 20\,\mathrm{kHz}$
Boost inductance	AMCC-4, 2605SA1, 36 µH, 5 turns
MOSFETs	2xBSC046N10NS3G, 100 V, 4.6 mΩ
DC-link cap.	4xPanasonic ECO-S1KA222CA, alum. elect., 80 V, 2.2 mF
EMI filter	3 stages, 2x common mode chokes (EPCOS R40 cores T38, 10 turns), 3x680 nF
DC-DC converter	
Switching frequency	$f_{\mathrm{sw}} = 200\,\mathrm{kHz}$
Transformer	turns ratio 7:7, ETD34/17/11, N87, EPCOS litz wire (600x71 µm)
Inductance	ETD34/17/11, N87, EPCOS, 20.5 µH
Prim. MOSFETs	BSC046N10NS3G, 100 V, 4.6 mΩ
Sec. MOSFETs	BSC046N10NS3G, 100 V, 4.6 mΩ

Phase-shifted full bridge converter

The phase-shifted full bridge converter (PSFB) with full bridge synchronous rectification (SR) is chosen for the isolated DC-DC converter stage since it allows to achieve a comparably high efficiency by operating the semiconductors under zero-voltage switching (ZVS) and still provides an easy way to control the power flow by means of the phase shift between the bridge legs on the primary side at a constant switching frequency. For a proper operation of the converter, however, certain design guidelines have to be considered [10]. While ZVS can be achieved for the lagging leg of the primary full bridge easily by utilizing both the energy stored in the output inductor and in the leakage inductor of the transformer, the operation of the leading leg with ZVS relies solely on the energy stored in the leakage inductance during the freewheeling phase

$$E_{\mathrm{L}\sigma} = \frac{1}{2} L_\sigma \left(I_{\mathrm{Load}} \cdot n_{\mathrm{tr}} + I_{\mathrm{mag}}\right)^2 \qquad (1)$$

This energy has to be sufficient to charge/discharge the parasitic output capacitances of the MOSFETs in the leading bridge leg. An energy analysis reveals that soft switching can only be achieved if the energy $E_{\mathrm{L}\sigma}$ is larger than the energy which is fed back into the DC input voltage during discharge

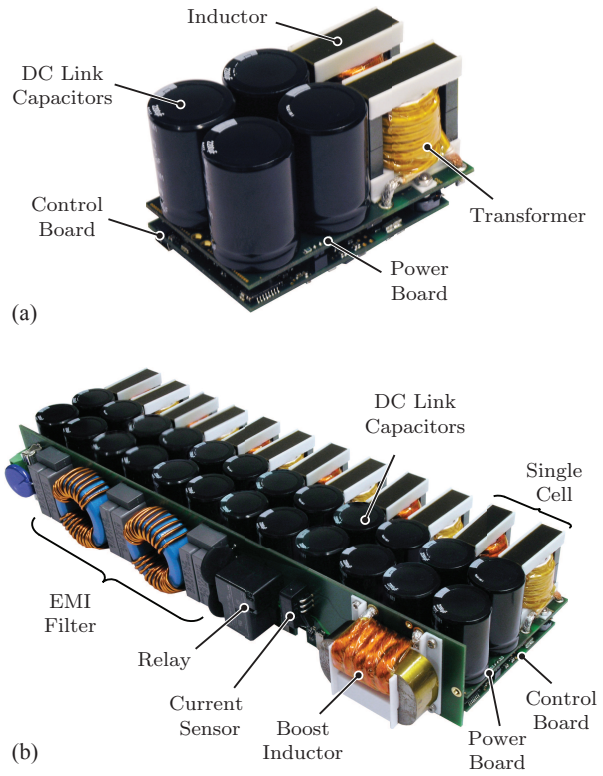

Fig. 4: Multi-cell single-phase AC-DC telecom rectifier prototype with 6 converter cells in ISOP configuration for a rated power of 3.3 kW and a power density of $\rho = 2.2\,\mathrm{kW/dm^3}$: (a) single cell and (b) full system ($30.4\,\mathrm{cm} \cdot 11\,\mathrm{cm} \cdot 4.5\,\mathrm{cm}$ / $12\,\mathrm{in} \cdot 4.3\,\mathrm{in} \cdot 1.8\,\mathrm{in}$).

of the charge equivalent capacitance of a MOSFET, i.e.

$$E_{\mathrm{C,sw}} = C_{\mathrm{oss,Qeq}} \cdot V_{\mathrm{DC}}^2. \tag{2}$$

In the prototype at hand, the leakage inductance of the transformer was selected to be $L_\sigma = 1\,\mu\mathrm{H}$ by adjusting the winding arrangement. This allows to achieve soft-switching in the leading leg at levels of the output current above $I_{\mathrm{Load}} \geq 3.4\,\mathrm{A}$ (i.e. 30%) according to (1) and (2).

Increasing the leakage inductance even further for a broader range of load currents for soft switching would introduce the drawback of a larger duty cycle loss caused by the time required to reverse the current in the leakage inductance from $(-I_{\mathrm{Load}} \cdot n_{\mathrm{trafo}})$ to $(+I_{\mathrm{Load}} \cdot n_{\mathrm{trafo}})$ or vice versa, thus rendering it as an unpractical solution.

Another issue in the operation of the PSFB is the voltage ringing at the secondary rectifier MOSFETs after the freewheeling phase. The ringing is caused by the resonant circuit comprising the leakage inductance L_σ of the transformer and the parasitic capacitances of the rectifier MOSFETs ($2 \cdot C_{\mathrm{OSS}}$) since the voltage across the output rectifier is decoupled by the output inductor from the output voltage and therefore not clamped to a fixed voltage (cf. **Fig. 6(b)**). The resonant frequency of this resonant circuit equals

$$\omega_{\mathrm{res}} = 1/\sqrt{2C_{\mathrm{oss}} L_\sigma n_{\mathrm{tr}}^2} \tag{3}$$

and the characteristic impedance amounts to

$$Z_{\mathrm{res}} = \sqrt{L_\sigma n_{\mathrm{tr}}^2/(2C_{\mathrm{oss}})}. \tag{4}$$

The worst case voltage overshoot can reach the value of twice the transformed primary voltage $V_{\mathrm{SR,peak}} = 2V_{\mathrm{sec}} = 2n_{\mathrm{tr}}V_{\mathrm{DC}}$, as shown in **Fig. 6(d)**. In the case at the hand, the DC-bus voltage in each cell equals $V_{\mathrm{DC}} = V_{\mathrm{DC,tot}}/N_{\mathrm{cells}} = 400\,\mathrm{V}/6 = 66\,\mathrm{V}$ and with a transfomer turns ratio of $n_{\mathrm{tr}} = 1$ the worst case voltage spike could reach around $V_{\mathrm{SR,peak}} = 133\,\mathrm{V}$ which would lead to the destruction of the synchronous rectification MOSFETs with a voltage rating of $V_{\mathrm{DS,max}} = 100\,\mathrm{V}$. Since the diodes in the rectifier MOSFETs are prone to reverse recovery effects, the voltage spike increases depending on the peak reverse recovery current I_{RR} and can be calculated as

$$V_{\mathrm{SR,pk}} = V_{\mathrm{DC}} n_{\mathrm{tr}} + \sqrt{(V_{\mathrm{DC}} n_{\mathrm{tr}})^2 + (Z_{\mathrm{res}} I_{\mathrm{RR}})^2} \tag{5}$$

In order limit the voltage spike a loss-less snubber circuit consisting of a snubber capacitor C_{Snub} and two diodes is added to the converter [11]. An alternative snubber that works with an additional transformer winding can be found in [12]. By introducing the snubber the equivalent circuit of

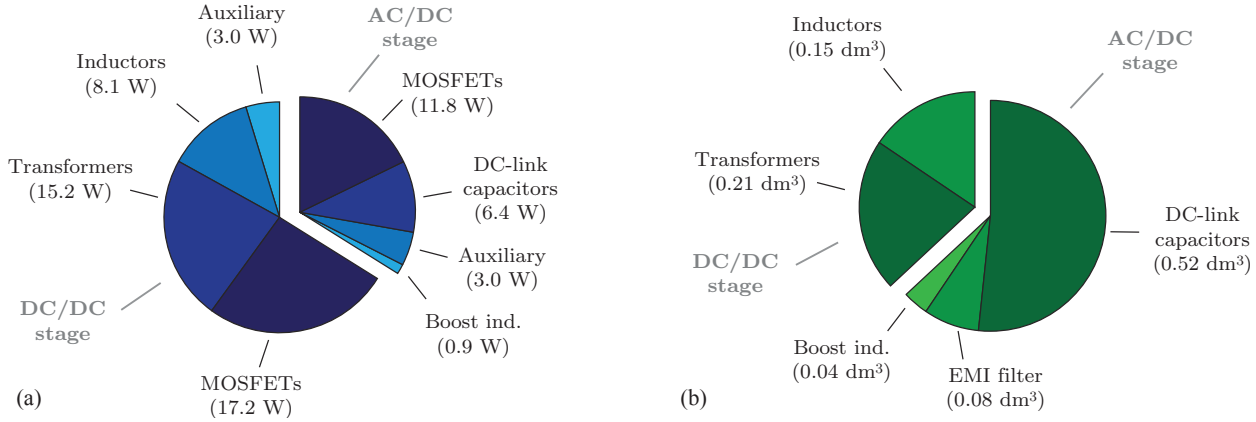

Fig. 5: Calculated break-down of the losses (a) and the volume (b) for the selected converter design of the multi-cell telecom power supply module at full load.

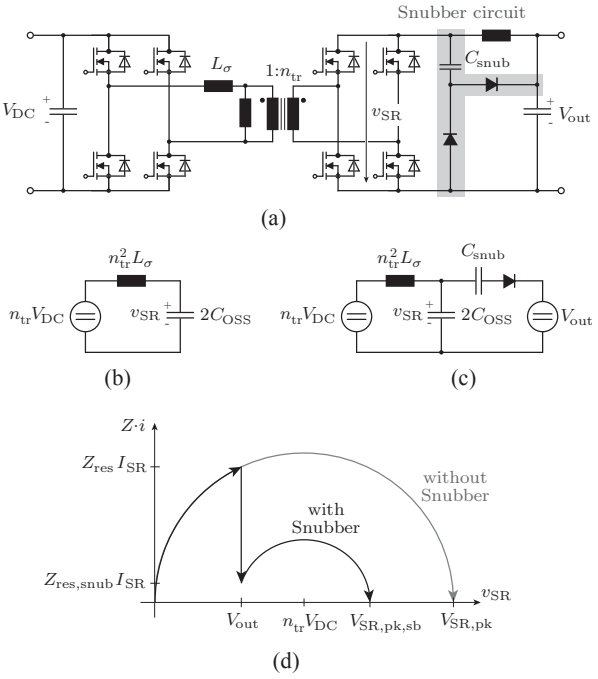

Fig. 6: Phase-shifted full bridge converter with over-voltage limiting loss-less snubber circuit [11] for the secondary rectifier MOSFETs: (a) application of the snubber circuit to the converter; (b) equivalent circuit of the resonant network for the case without snubber; (c) modified resonant network for case with snubber elements; (d) comparison of the resonant trajectories for the cases with and without snubber elements and their resulting voltage peaks $V_{SR,pk,sb}$ and $V_{SR,pk}$, respectively. (The influence of the reverse recovery current of the MOSFET body diodes is not shown.)

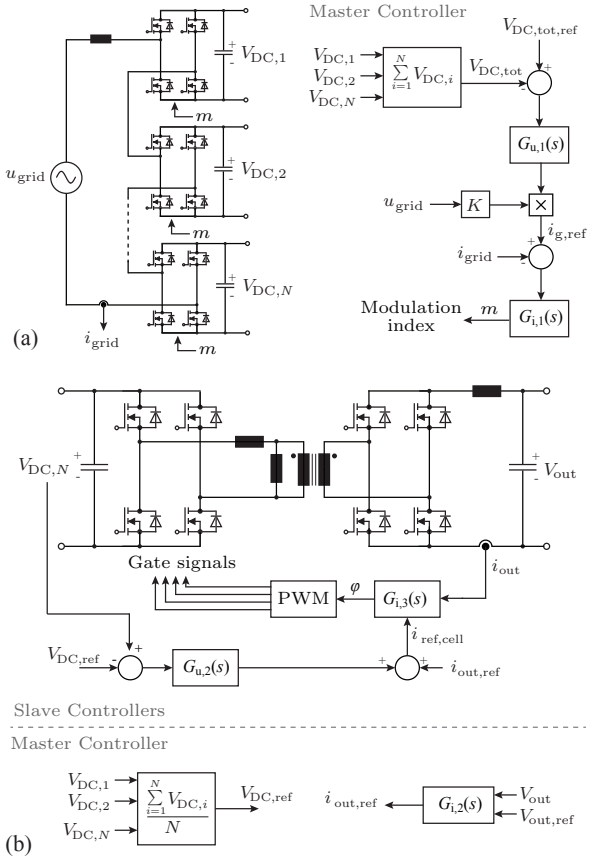

Fig. 7: Control implementation of the multi-cell telecom rectifier: (a) total DC-bus voltage controller and input current controller; (b) output current controller and DC-link voltage controller.

the resonant network changes as shown in **Fig. 6(c)** and the resonant frequency becomes

$$f_{res,snub} = 1/\sqrt{L_\sigma n_{tr}^2 (2C_{oss} + C_{snub})} \tag{6}$$

while the resonant impedance becomes

$$Z_{res,snub} = \sqrt{L_\sigma n_{tr}^2 / (2C_{oss} + C_{snub})} \tag{7}$$

after the voltage v_{SR} has risen above the level of the output voltag V_{out}. This is also depicted in **Fig. 6(d)** where the sudden change of the resonant impedance leads to a drop in the $v_{SR} - Z \cdot i$ plane. The maximum voltage spike can then be derived as a function of the output voltage to be

$$V_{SR,pk,sb} = V_{DC} n_{tr} + \sqrt{(V_{DC} n_{tr} - V_{out})^2 + (Z_{res,snub} I_{SR})^2}. \tag{8}$$

The snubber capacitor is chosen to have a value of $C_{Snub} = 15\,\mathrm{nF}$ which limits the worst case voltage spike at the lowest output voltage of $V_{out,min} = 40\,\mathrm{V}$ to $V_{SR,peak,snub} = 92\,\mathrm{V}$ without considering the influence of the reverse recovery current. For the material of the ceramic snubber capacitors the C0G (NP0) dielectric is chosen since it provides a stable capacitance value under varying temperature and voltage. In order minimize the reverse recovery currents of the diodes, the conduction time of the diodes in the SR MOSFETs is kept to a minimum (around $10\,\mathrm{ns}$) by adjustments of the timings of the gate signals [13].

Control implementation

One of the main challenges regarding the control of multi-cell converters in general is the unbalance of the DC-link voltages of the cell. In order to overcome this problem different control strategies have been proposed [14]–[18]. The basic idea behind those concepts is to perform voltage balancing control either by the cascaded H-bridge rectifier or the isolated DC-DC converters. In [14] a voltage balance control is presented which is based on the single-phase dq-control for the rectifier, and a power balance control method to regulate the power transferred through the DC-DC converter that are connected in parallel at their outputs. This allows to individually adjust the power transfer from each DC-link to the output in order to balance the DC-link voltages. In contrast, [15] presents a method to control and balance the voltage of the DC-links by operating the rectifier stages with a mixture of low and high frequency PWM. However, both of the aforementioned methods result in rather complicated controller implementations since the voltage balancing requires additional control loops. A simpler way to operate the ISOP system is presented in [16] which uses a common-duty-ratio control method which relies on the natural balancing behavior of ISOP multi-cell converters [17]. However, this method is not actively balancing the DC-link voltages. Therefore, any mismatch between the converters,

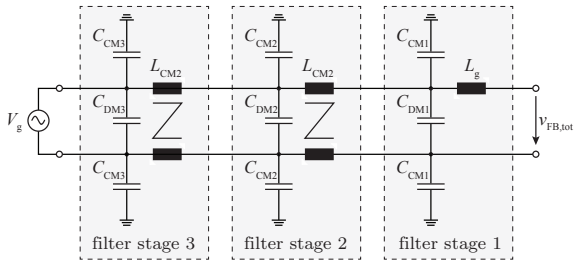

Fig. 8: Schematic of the employed 3-stage common-mode and differential-mode EMI filter.

such as e.g. slightly different transformer terminal behaviors, will lead to different AC voltage ripples on the DC-link capacitors caused by the pulsating power of the mains. These differences in the DC-link voltages will generate circulating currents at the parallel connected converter outputs which decreases the efficiency of the system. Thus, the control scheme which is selected for the implementation in the prototype has a total dc-link voltage regulator on the rectifier side in order to have a constant total dc-link voltage (i.e. the sum of all DC-link voltages). In addition, each cell possesses individual DC-link voltage and load current control for the isolated DC-DC converters [18]. **Fig. 7** shows the control block implementation of the entire system. The control loops can be implemented as a master-slave control regime where the slower outer voltage control loops are processed by the master cell and the faster inner control loops like the current controllers are computed locally on each cell. The communication between the cells is realized by the serial peripheral interface (SPI).

EMI Filter Design

For the design of the EMI filter the influence of the differential-mode and the common-mode noise have to be considered. The filter design can be performed individually for the common-mode and the differential-mode noise if the required attentuation for each case is calculated with a margin of around $16\,\mathrm{dB}$ to the limits, i.e. $6\,\mathrm{dB}$ for the worst case addition of the two noise signals and $10\,\mathrm{dB}$ to account for component tolerances.

In order to calculate the required attenuation for the differential-mode noise, the first harmonic that falls into the EMI constrained spectrum ($f_{\mathrm{EMI}} \geq 150\,\mathrm{kHz}$) is considered, since the amplitude of the harmonic spectrum of square wave voltage decreases with $-20\,\mathrm{dB}$ per frequency decade, whereas the filter attenuation increases with $-40 \cdot N_{\mathrm{s}}\,\mathrm{dB}$ with N_{s} being the number of filter stages. For the case at hand, the first harmonic in the constrained frequency range is at twice the effective switching frequency $f_{\mathrm{sw,eff}} = 120\,\mathrm{kHz}$ of the interleaved AC-DC stages, i.e. $f_{\mathrm{filt}} = 240\,\mathrm{kHz}$. The compliance with EMI standards is evaluated by determining the quasi-peak emission levels of the converter. The quasi-peak voltage of the harmonic at $f_{\mathrm{filt}} = 240\,\mathrm{kHz}$ is calculated by considering a $9\,\mathrm{kHz}$ band around that harmonic and by synthesizing a time domain signal which is fed into the non-linear quasi-peak detection network [19] and results in a quasi-peak noise voltage of the converter at $f_{\mathrm{filt}} = 240\,\mathrm{kHz}$ of $V_{\mathrm{filt,qp}} = 17.2\,\mathrm{V}$ and/or a required attenuation of $92.8\,\mathrm{dB}$ including the margin previously mentioned. Following the filter volume optimization guidelines presented in [20] the number of filter stages for a minimum volume and its associated volume can be found at $n_{\mathrm{filt}} = 3$ as shown in **Fig. 8**. The maximum value of the total differential mode capacitance is limited by the maximum allowable reactive power consumption of the filter. The limit was set such that a power factor of $\cos\phi = 0.9$ can be reached above 10% of the nominal power. This leads to total differential mode capacitance of $C_{\mathrm{DM,tot}} = 2\,\mu\mathrm{F}$, which means each differential mode capacitance amounts to $C_{\mathrm{DM}} = 660\,\mathrm{nF}$. This leads to differential mode inductances of $L_{\mathrm{DM}} = 18\,\mu\mathrm{H}$ in order to achieve the required attenuation in combination with the boost inductor L_{g}.

The precise modeling of the common-mode noise is challenging since it requires the exact knowledge of the stray capacitances of all electric nodes in the converter cells to the ground. Since this is practically impossible to determine for multi-cell converter systems, an approach as presented in [21] was followed which deduces an equivalent circuit for the common-mode noise. By applying a worst-case approximation and neglecting small capacitances compared to larger ones, it can be found that due to the nature of the series connection of the converter inputs the measured common-mode voltage at the line impedance stabilization network (LISN) depends on which cell of the series stack is switching. So, for example each time the lowest cell of the series stack switches, all upper cells are also moved in respect to their potential to ground. Since the cells are operated interleaved, the common-mode voltage resembles a staircase like voltage waveform with the levels being

$$v_{\mathrm{CM}}(i) = \frac{N_{\mathrm{cells}} - i}{N_{\mathrm{cells}}} \cdot V_{\mathrm{DC}} \tag{9}$$

for $i \in [1, N_{\mathrm{cells}}]$where $i = 1$ means that the lowest cell of the stack is switched and $i = N_{\mathrm{cells}}$ means the uppermost cell is switched. Based on that voltage waveform the quasi-peak voltage spectrum can be derived by means of simulations and the required common-mode filter attenuation can be determined to be $78\,\mathrm{dB}$. The maximum allowable total common-mode filter capacitance is limited by the maximum total leakage current to earth (e.g. $3.5\,\mathrm{mA}$ RMS) which leads to $C_{\mathrm{CM,tot}} = 36\,\mathrm{nF}$ and thus the value for each common-mode capacitor is selected as $C_{\mathrm{CM}} = 4.7\,\mathrm{nF}$. Usually, the smallest common-mode filter volume is obtained by utilizing the maximum allowable amount of common-mode filter capacitance [22]. As a result, the common-mode inductances can be determined to be $L_{\mathrm{CM}} = 1.6\,\mathrm{mH}$. In the protoype, the leakage inductance of the common-mode chokes is utilized as differential-mode filter inductances.

IV. Conclusion

A new approach towards a highly efficient and very compact telecom recitifier module beyond the limits of state-of-the-art systems is presented. The degrees of freedom in the design procedure of a multi-cell telecom power supply module in ISOP configuration are outlined and the optimization process

is described in detail. The optimization results show that a converter design with an efficiency of $\eta = 98\%$ and a power density of $\rho = 2.2\,\mathrm{kW/dm^3}$ can be achieved. The results also reveal an optimum value of $N = 6$ for the number of converter cells and an optimum maximum permissible drop of 20% the DC-link voltage during the hold-up time. Based on the optimization results a hardware demonstrator realization is presented and specific design aspects are explained. First measurement results verify the operation of the system and will be summarized in future publication.

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