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Comparative Evaluation of Three-Phase AC-AC Voltage/Current-Source Converter Systems Employing Latest GaN Power Transistor Technology

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Comparative Evaluation of Three-Phase AC-AC Voltage/Current-Source Converter Systems Employing Latest GaN Power Transistor Technology

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***Abstract*—The emergence of monolithic bidirectional GaN power transistors sparks renewed interest in AC-AC current-source converters (CSCs) as an alternative to AC-AC voltage-source converters (VSCs) for motor drive applications. This paper compares the two approaches with the CSC utilizing novel 600 V, 140 mΩ monolithic bidirectional GaN transistors. Aiming for a comparison of next-generation plug-and-play motor drives, both systems must fulfill the same EMI limits that cover an extended frequency range from 9 kHz to 30 MHz at the grid and at the motor interface. Designing both systems with roughly the same total chip area for the same AC-AC efficiency of 97 % at a nominal power of 1.4 kW (200 V nominal line-to-line RMS voltage, 4 A nominal RMS current), we identify a suitable switching frequency of 72 kHz, and we discuss efficiency characteristics over the motor current (torque) and voltage (speed) ranges. A comparison of the total magnetic component volumes finds advantages for the VSC system, which disappear if motor-integration (voiding the need for a motor-side differential-mode EMI filter) is considered.**

I. Introduction

Electric motor applications currently account for 45 % of the world's total electricity usage [1]. Thus, increasing the efficiency of the motors but also of variable speed drives (VSDs) can significantly contribute to lowering energy usage and, ultimately, reducing greenhouse gas emissions from power generation. Wide-bandgap (WBG) power semiconductors such as SiC and GaN enable much higher switching frequencies of VSDs compared to state-of-the-art silicon IGBTs and, simultaneously, higher efficiencies [2]. Furthermore, high switching frequencies facilitate the integration of relatively compact output filters into standard voltage-source-converter (VSC) VSDs [2]–[4], see **Fig. 1a**. This results in continuous, sinusoidal output voltages, which in turn reduce harmonic losses in the motor. Such drive systems achieve higher overall efficiency despite the higher switching frequency and the output filter component losses [2]. VSDs with sinusoidal output voltages furthermore enable plug-and-play installation by preventing issues caused by switched output voltages such as transient overvoltages resulting from impedance mismatches in case of long motor cables, common-mode ground currents that can damage motor bearings, and radiated electromagnetic emissions whose suppression would otherwise require expensive shielded motor cables [5].

Current-source converters (CSCs), see **Fig. 1b**, inherently feature continuous output voltages. CSCs have been employed in high-power (megawatt) drive systems for decades, but the notion of a relatively large DC-link inductor has hindered their application in VSDs in the kilowatt power range. However,

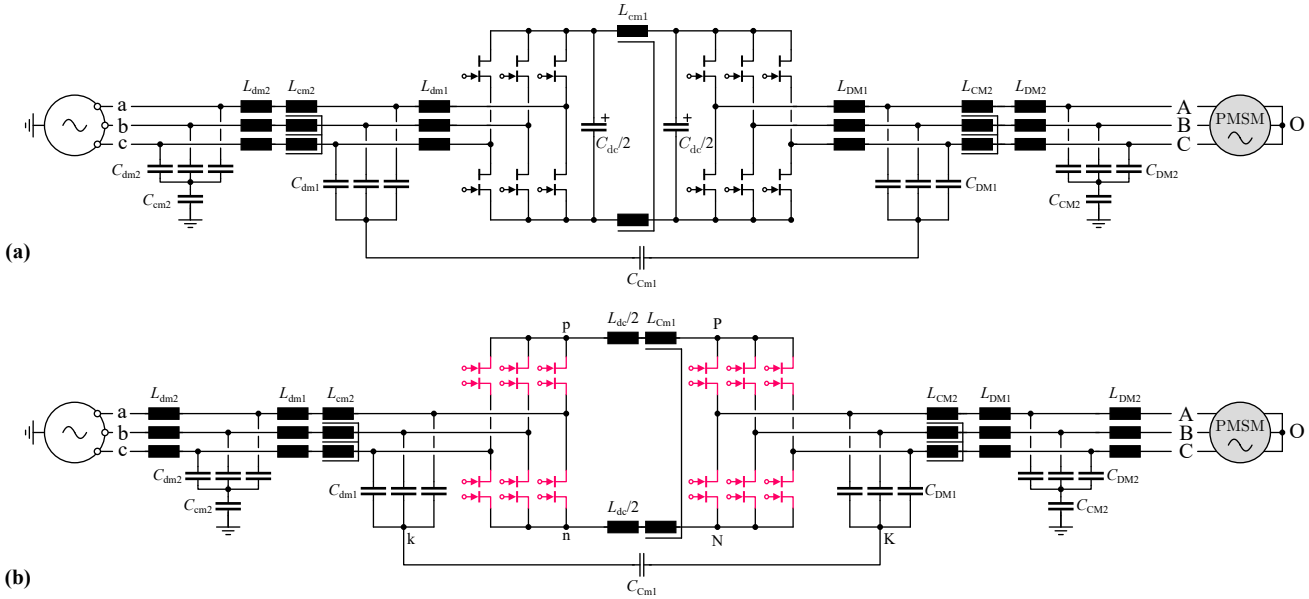

Fig. 1. **(a)** AC-AC voltage-source converter (VSC), i.e., a back-to-back configuration of a voltage-source rectifier (VSR) and a voltage-source inverter (VSI), both employing GaN power transistors, and **(b)** AC-AC current-source converter (CSC), i.e., a back-to-back configuration of a current-source rectifier (CSR) and a current-source inverter (CSI), employing monolithic bidirectional/bipolar GaN transistors. Both topologies are shown with exemplary two-stage EMI filters towards the grid and towards the motor (permanent-magnet synchronous machine, PMSM).

TABLE I
KEY SPECIFICATIONS OF THE AC-AC VSC AND CSC.

Parameter		Value	Unit
Grid line-to-line RMS voltage	$V_{g,n}$	200	V
Grid frequency	f_g	50	Hz
Nom. motor line-to-line RMS voltage	$V_{m,n}$	200	V
Nom. motor phase current	$I_{m,n}$	4	A
Max. motor line-to-line peak voltage	$\hat{V}_{m,m}$	400	V
Max. motor frequency	f_m	200	Hz
Design junction temp.	$T_{j,n}$	100	°C
Design heat sink temp.	$T_{hs,n}$	80	°C
Switching frequency	f_s	72	kHz

Note: Capital V denote line-to-line RMS voltages, capital I denote phase RMS currents.

the emergence of WBG devices that enable higher switching frequencies and hence imply smaller magnetic components has sparked renewed interest in CSCs also for low-power VSD applications [6]–[9].

Various comparisons between voltage-source and current-source topologies have been reported in the literature, considering silicon IGBTs but also, more recently, WBG devices [7], [10]–[19]. However, CSCs suffer from the need for power semiconductors with bipolar voltage blocking capability, which, if realized from widely available devices such as MOSFETs that provide only unipolar blocking capability, incur a factor of four penalty in terms of chip area required for comparable conduction characteristics [5].

Recent research regarding GaN *monolithic* bidirectional switches (M-BDSs[1]) [24]–[27] has lead to first-generation samples of a 600 V, 140 mΩ GaN M-BDS [22], [23], [28] (see **Fig. 2**), which removes this structural disadvantage of the CSC topology almost completely, i.e., facilitates a fair comparison of a VSC and a CSC with approximately equal total chip area. Therefore, based on experimentally verified loss characteristics of the 600 V, 140 mΩ GaN M-BDS [22], this paper provides an unbiased comprehensive comparative evaluation of an AC-AC VSC and an AC-AC CSC, see **Fig. 1**, with key specifications (see **Table I**) suitable for operation in Japanese or U.S. grids, e.g., driving compressors in HVAC units. Both systems use roughly the same chip area, meet the same EMI limits at the grid and at the motor interfaces, and are designed for equal efficiency at the nominal operating point, which ultimately facilitates a fair comparison of the resulting converter volume as well as of the different loss characteristics in dependence of motor current (torque) and voltage (speed).

II. SEMICONDUCTOR LOSSES

Fig. 2d presents calorimetrically measured hard-switching loss energies (i.e., sum of turn-on and turn-off losses) of first-generation 600 V, 140 mΩ GaN M-BDSs in a CSC commutation cell configuration, i.e., considering the necessary four-step commutation sequence (see [22] for details). The dependence on the switched voltage, v, and on the switched current, i, is approximated with a fit as

$$E_{sw,bd}(i,v) = k_{bd,1} \cdot i \cdot v + k_{bd,2} \cdot v^2 \qquad (1)$$

[1]In addition to CSIs [20]–[22], such M-BDSs can also advantageously be employed in T-Type three-level VSC topologies [23].

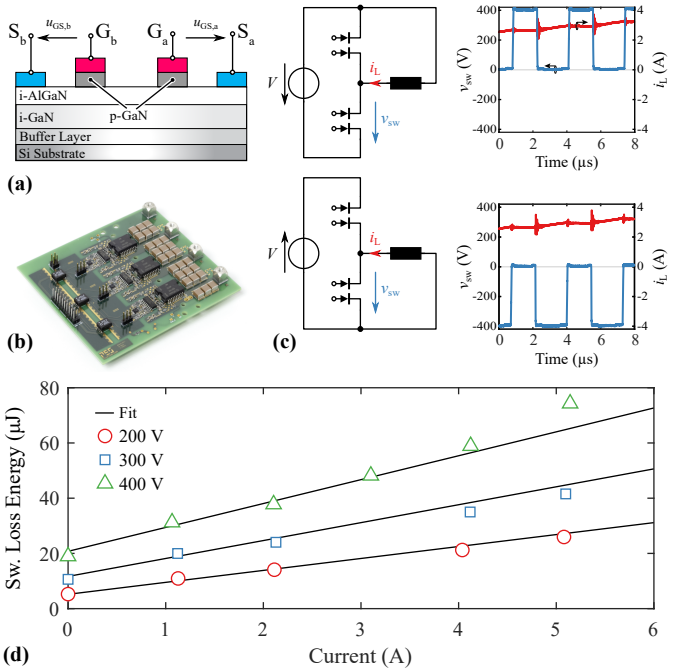

Fig. 2. **(a)** Structure of the employed first-generation dual-gate monolithic bidirectional GaN transistor [28]. **(b)** Characterization PCB with one CSC commutation cell. **(c)** Exemplary switching waveforms for continuous operation in two different quadrants (two different voltage polarities). **(d)** Calorimetrically measured switching energies for hard-switching commutations between two of the three GaN M-BDSs forming a CSC commutation cell [22]. Note that due to the four-step commutation required for CSCs, switching energies are not directly comparable to those specified for unipolar devices in a half-bridge configuration.

with $k_{bd,1} = 2.16 \times 10^{-8}\,\mathrm{J/(VA)}$ and $k_{bd,2} = 1.3 \times 10^{-10}\,\mathrm{J/V^2}$. For the VSC, measured switching energies of a 600 V, 70 mΩ GaN transistor presented in [29] are scaled to the same on-state resistance as the GaN M-BDS (implying roughly equal total chip area), which leads to

$$E_{sw,ud}(i, v = 400\,\mathrm{V}) = k_{up,0} + k_{up,1} \cdot i \qquad (2)$$

with $k_{up,0} = 1.55 \times 10^{-5}\,\mathrm{J}$ and $k_{up,1} = 2.3 \times 10^{-6}\,\mathrm{J/A}$. Note that for both 600 V devices the maximum switched voltage should not exceed 400 V, implying that value for the VSC's DC link voltage and for the maximum peak line-to-line voltage of the CSC (see $\hat{V}_{m,m}$ in **Table I**).

The semiconductor losses of both systems can be estimated for different operating points defined by the motor line-to-line RMS voltage V_m and the motor phase current I_m. We consider unity power factor only (as is approximately achieved for permanent-magnet synchronous machines). Neglecting losses, the required grid phase current follows as

$$I_g = \frac{V_m}{V_g} I_m. \qquad (3)$$

In a CSC, the switched current is the DC-link current I_{dc}, which is advantageously adapted to the operating point[2] as

$$I_{dc} = \max\left(\sqrt{2} I_m, \sqrt{2} I_g\right), \qquad (4)$$

[2]For typical DC-link current ripples such as 20 % (peak-to-peak), the current level can be adapted to changing load conditions within a few switching cycles.

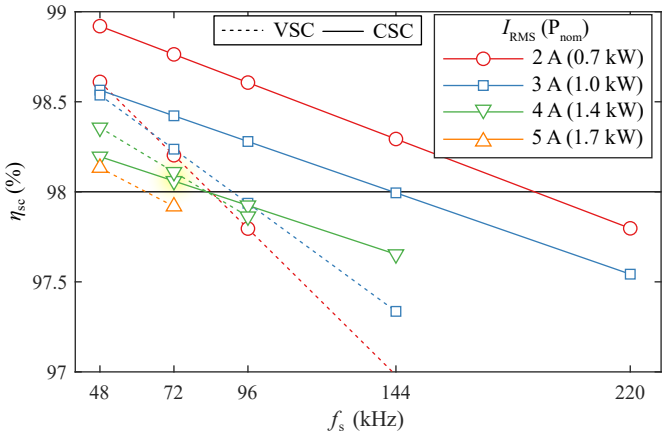

Fig. 3. AC-AC CSC and VSC semiconductor efficiency, η_{sc}, at the nominal operating point ($V_{m,n} = V_{g,n} = 200\,\text{V}$, and various nominal motor currents, $I_{m,n}$) in dependence of the switching frequency. Designs that would violate $T_{j,n} = 100\,°\text{C}$ are not shown. The selected designs with $\eta_{sc} \approx 98\,\%$ at $I_{m,n} = 4\,\text{A}$ and $f_s = 72\,\text{kHz}$ are highlighted.

i.e., the minimum possible (constant[3]) value is used. The conduction and switching losses of the CSR ($V_{g/m} = V_g$) or of the CSI ($V_{g/m} = V_m$) stage become [6], [22]

$$P_{C,c} = 2I_{dc}^2 R_{on} \quad \text{and} \tag{5}$$

$$P_{C,s} = \frac{3\sqrt{2}V_{g/m}f_s}{\pi}\left(k_{bd,1}I_{dc} + k_{bd,2}\sqrt{2}V_{g/m}\frac{4\pi - 3\sqrt{3}}{12}\right). \tag{6}$$

Similarly, the losses of the VSR ($I_{g/m} = I_g$) or of the VSI ($I_{g/m} = I_m$) stage are [30]

$$P_{V,c} = 3I_{g/m}^2 R_{on} \text{ and} \tag{7}$$

$$P_{V,s} = 6f_s\left(\frac{k_{up,0}}{2} + \sqrt{2}I_{g/m}\frac{k_{up,1}}{\pi}\right), \tag{8}$$

whereby a constant DC-link voltage of 400 V is considered. In both cases, $R_{on} = 140\,\text{m}\Omega$ ($166\,\text{m}\Omega$ at $T_{j,n} = 100\,°\text{C}$).

Fig. 3 shows that the VSC and the CSC achieve an AC-AC semiconductor efficiency of $\eta_{sc} \approx 98\,\%$ at the nominal output voltage ($V_{m,n} = V_{g,n} = 200\,\text{V}$) for $I_{m,n} = 4\,\text{A}$ and $f_s = 72\,\text{kHz}$, which we therefore consider for the further analysis.[4] The nominal power becomes $P_n = \sqrt{3}V_{m,n}I_{m,n} = 1.4\,\text{kW}$.

Fig. 4a shows semiconductor losses normalized to the nominal power and indicates the eight representative operating points defined in EN 50 598 [31] to characterize the energy efficiency of motor drive systems. Note that the same maximum losses occur for both systems, which implies equal heat sink volumes. **Fig. 4b** compares the semiconductor efficiency characteristics of the VSC and the CSC over the operating range, indicating advantages for the CSC for part-load operation.

III. EMI Filter

For a fair comparison, both systems should meet the same EMI limits. With the aim of realizing plug-and-play motor drive systems (e.g., compatible with standard motors, no need for

[3]Note that here we do not consider advanced control/modulation methods such as synergetic control [22].

[4]Selecting a higher $I_{m,n}$, e.g., 5 A, would result in junction temperatures higher than $T_{j,n}$; selecting a lower $I_{m,n}$ would favor the CSC (higher f_s for $\eta_{sc} \approx 98\,\%$) but, conversely, imply low utilization of the power semiconductors.

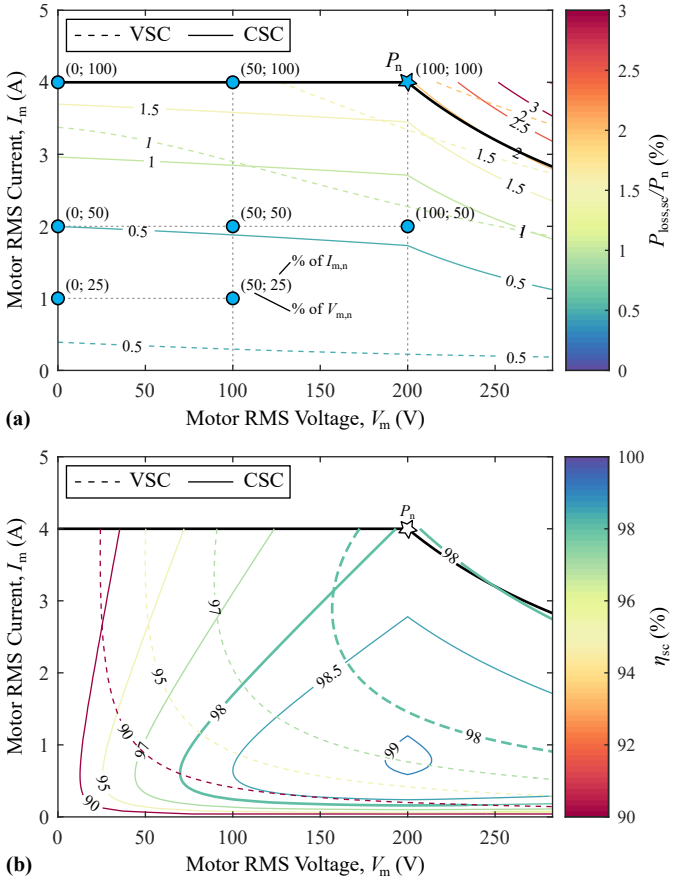

Fig. 4. Semiconductor loss/efficiency characteristics of VSC and CSC motor drives with $f_s = 72\,\text{kHz}$, $V_{g,n} = 200\,\text{V}$, and $I_{m,n} = 4\,\text{A}$ (resulting in a nominal power of $P_n = 1.4\,\text{kW}$ at $V_{m,n} = 200\,\text{V}$). **(a)** Semiconductor losses normalized to the nominal power, P_n, and the eight representative operating points defined in EN 50 598 [31]. **(b)** Semiconductor efficiency, $\eta_{sc} = 1 - P_{loss,sc}/P$.

shielded motor cables, etc.), we consider essentially the same EMI limits for the motor (IEC 61800-3 PI) and for the grid (CISPR 11 Class A) interface, see **Fig. 5**. In addition to these limits that currently must be considered for EMI compliance measurements and cover the frequency range of 150 kHz to 30 MHz, we also take into account proposed EMI limits for the lower frequency range of 9 kHz to 150 kHz to ensure a future-proof design.

A. EMI Equivalent Circuits

1) AC-AC VSC: **Fig. 6ab** show the differential-mode (DM) and common-mode (CM) EMI equivalent circuits of the AC-AC VSC from **Fig. 1a**. The DM EMI circuits for the VSR and the VSI stages are identical but independent, and the DM noise source of each phase of a VSR ($v_{dmx,V}$) and of a VSI ($v_{DMX,V}$) is calculated as

$$\begin{aligned} v_{dmx,V} &= v_x - v_{cmr,V} \quad x \in [a,b,c] \quad \text{and} \\ v_{DMX,V} &= v_X - v_{CMI,V} \quad X \in [A,B,C], \end{aligned} \tag{9}$$

where v_a, v_b, and v_c denote the switch-node voltages of the VSR stage and v_A, v_B, and v_C of the VSI stage with respect to a (virtual) DC bus midpoint, and $v_{cmr,V}$ and $V_{CMI,V}$ are the respective common-mode voltages, i.e.,

$$v_{cmr,V} = \frac{1}{3}(v_a + v_b + v_c), \quad v_{CMI,V} = \frac{1}{3}(v_A + v_B + v_C). \tag{10}$$

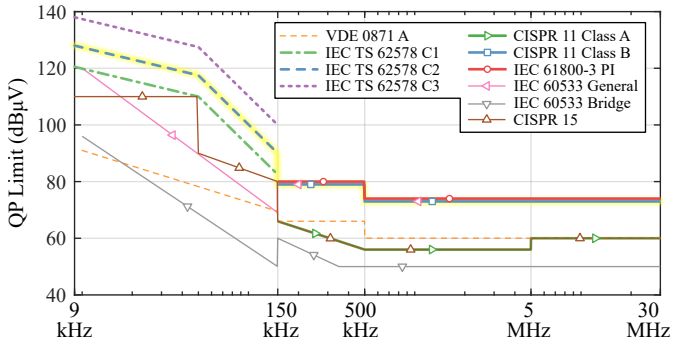

Fig. 5. Quasi-peak (QP) EMI limits for the frequency range of 9 kHz to 30 MHz defined in various standards [32]–[37]. Dashed lines indicate withdrawn (VDE 0871A) or proposed limits (IEC TS 62578). Aiming for a next-generation plug-and-play motor drive, we consider the highlighted limits (IEC TS 62578 C2 and CISRP 11 Class A) for both, the grid and the motor interface (note that IEC 61800-3 for power interfaces in drive systems defines limits that are just 1 dBµV higher than those defined in CISPR 11 Class A).

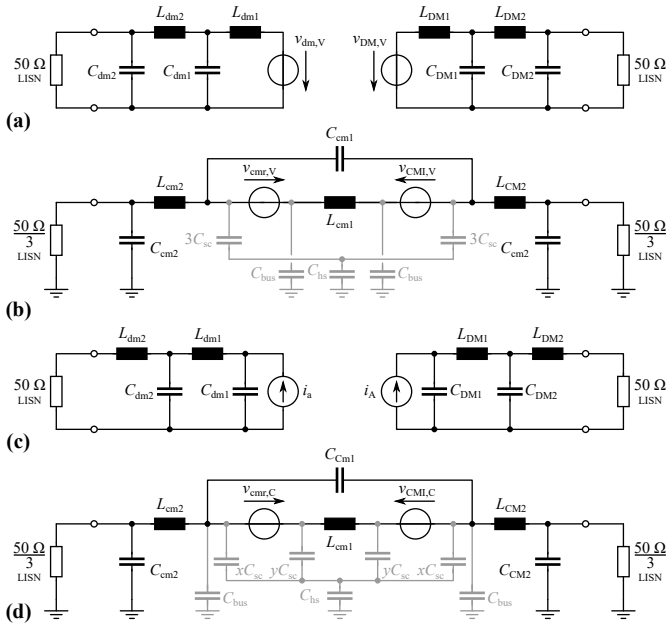

Fig. 6. Simplified EMI equivalent circuits. **(a)** VSC DM; **(b)** VSC CM; **(c)** CSC DM; **(d)** CSC CM. Additional small CM filter stages may be added to achieve compliance with radiated EMI limits [38]; filter damping elements are not shown.

The first CM filter stage is implemented with the CM capacitor C_{cm1} connected between the two star points formed by the first-stage DM filter capacitors of the rectifier and the inverter, respectively. As there is no connection to protective earth (PE)[5], a relatively large C_{cm1} can be employed [40, p. 37]. Furthermore, we place the first-stage CM inductor L_{cm1} on the DC side [40, p. 36], which in individual VSI or VSR systems advantageously results in a significant reduction of the current stress. In an AC-AC VSC, additionally the first-stage CM inductors of both stages can be realized with a shared single component. In case PWM with symmetric carrier signals is employed, this shared CM inductor is subject to a lower worst case peak-to-peak voltage-time area $Vt_{\mathrm{LCMpp,max}}$ compared to

[5]Parasitic capacitances of the semiconductors etc. to PE are shown in the CM EMI equivalent circuits (cf. **Fig. 6bd**) for completeness, however, they are not considered for the design of the EMI filter [39].

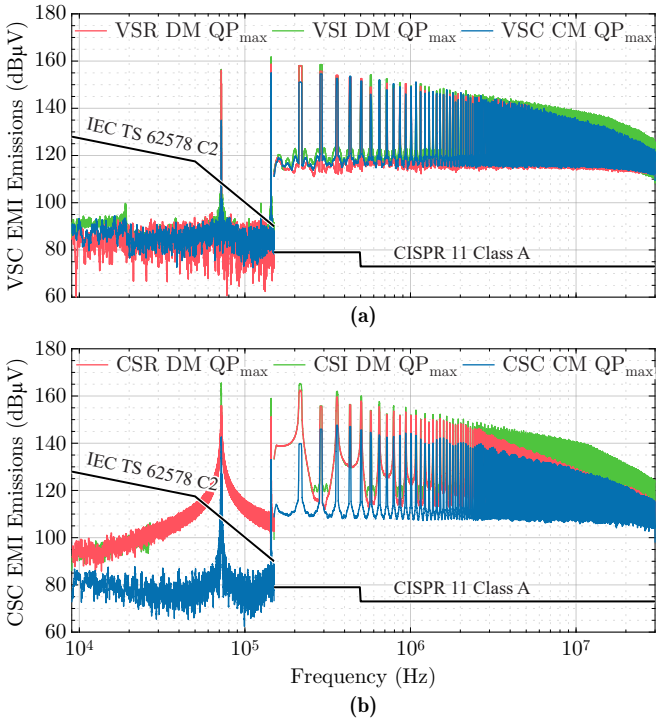

Fig. 7. Simulated DM and CM emissions (maximum QP approximation [41]) without any EMI filter of **(a)** the VSC and **(b)** the CSC (the DM emissions in dBµV are obtained as $i_{\mathrm{a}}R_{\mathrm{LISN}} = i_{\mathrm{a}} \cdot 50\,\Omega$, see **Fig. 6c**). The targeted EMI limits are indicated as well (see **Fig. 5**).

individual AC-side CM inductors, see **Fig. 9**. The total common mode voltage $v_{\mathrm{cm,V}}$ of an AC-AC VSC is thus given by the difference of the CM voltages of the VSR and the VSI stage as

$$v_{\mathrm{cm,V}} = v_{\mathrm{cmr,V}} - v_{\mathrm{CMI,V}}. \tag{11}$$

Note that the DC-side CM inductor in the AC-AC VSC requires splitting the DC bus into two separate DC-link capacitors (see **Fig. 1a**). To prevent potential oscillations with the CM inductor's stray inductance, some damping may be required.

2) AC-AC CSC: **Fig. 6cd** show the DM and CM EMI equivalent circuits of the AC-AC CSC from **Fig. 1b**. Again, the DM EMI circuits for the CSR and CSI stages are independent and identical. The DM noise sources are current sources that correspond to the (discontinuous) AC-side currents of the respective switching stages. Therefore, the DM filter structure for a CSR or a CSI is of the CL-type (in contrast to the LC-type needed for filtering the voltage noise in the other three cases).

The first CM filter stage is again implemented with C_{cm1} connected between the two star points formed by the first-stage DM capacitors of the CSR and CSI stages without a connection to PE. L_{cm1} is placed on the DC side with the same associated advantages as described above for the AC-AC VSC. Furthermore, as it is placed in series to the DC-link inductor, the CM inductor's stray inductance is of no concern. The total CM voltage of the CSC system is given by the difference of the CM voltages of the CSR and CSI stages as

$$v_{\mathrm{cm,C}} = v_{\mathrm{cmr,C}} - v_{\mathrm{CMI,C}} = \frac{1}{2}\left(v_{\mathrm{pk}} + v_{\mathrm{nk}}\right) - \frac{1}{2}\left(v_{\mathrm{PK}} + v_{\mathrm{NK}}\right), \tag{12}$$

where k and K denote the respective star-points of the first-stage DM filter capacitors (see **Fig. 1b**).

B. EMI Filter Design

Fig. 7 shows the simulated EMI emissions of the VSC and the CSC for the nominal operating point and without any EMI filter. We consider a fundamental frequency of 50 Hz for the rectifier but only 10 Hz for the inverter. Such lower output frequencies are clearly valid operating points and constitute a worst-case regarding EMI emissions in the frequency range below 150 kHz, where a lower RBW of only 200 Hz (compared to 9 kHz otherwise) applies. If the fundamental frequency is too high, no sideband harmonics fall within this RBW, resulting in a too optimistic filter design.

Based on these spectra, the required first-stage cutoff frequency of an idealized two-stage EMI filter (with $f_{c2} = k\,f_{c1}$) can be obtained as

$$\min_{m} f_{c1} = 10^{A_m/80} \cdot \frac{f_m}{\sqrt{k}}, \tag{13}$$

where A_m (a negative dB value) is the required attenuation, i.e., the difference between the EMI limit and the unfiltered emission level, at the frequency f_m with $f_m \in [9\,\text{kHz}, 30\,\text{MHz}]$. Considering a margin of 10 dB to account for component tolerances and a possible superposition of CM/DM noise and $k = 3$ (to decouple the filter resonances), **Fig. 8** shows the maximum filter cutoff frequencies over the intended operating range, which facilitates to identify the worst-case operating points regarding the EMI filter design. **Table II** lists the resulting required filter cutoff frequencies considered for the filter design (full compliance with current and upcoming EMI limits covering the full frequency range from 9 kHz to 30 MHz). Furthermore, we also show the (higher) cutoff frequencies that would result if only CISPR 11 Class A, which is in force, would be considered. Clearly, upcoming EMI standards extending to lower frequency ranges ultimately require larger EMI filters. The DM cut-off frequencies $f_{c1,DM}$ and $f_{c2,DM}$ are selected equal to the respective minima of the cut-off frequencies found for the rectifier and the inverter stage to allow a symmetric filter design. Note that in both cases the required cutoff frequencies for the VSC and the CSC are similar, implying similar effort for the EMI filter realization.

1) DM Filters: The two-stage DM filters are designed for the required cut-off frequencies and considering a maximum (capacitive) reactive power of 5 % on both, the grid and the motor side at the nominal operating voltage of 200 V and a fundamental frequency of 50 Hz.[6]

TABLE II
REQUIRED CUTOFF FREQUENCIES OF IDEALIZED TWO-STAGE EMI FILTERS FOR FULL COMPLIANCE WITH CURRENT AND UPCOMING EMI REGULATIONS COVERING THE FREQUENCY RANGE FROM 9 KHZ TO 30 MHZ.

	DM		CM	
	$f_{c1,DM}$	$f_{c2,DM}$	$f_{c1,CM}$	$f_{c2,CM}$
VSC	6.7 kHz	20.1 kHz	7.7 kHz	23.1 kHz
CSC	5.9 kHz	17.7 kHz	6.5 kHz	19.5 kHz
Only CISPR 11 Class A EMI limits (in force, 150 kHz to 30 MHz)				
VSC	9.4 kHz	28.2 kHz	9.2 kHz	27.6 kHz
CSC	7.1 kHz	21.3 kHz	11.6 kHz	34.8 kHz

In case of the VSC, the boost inductors, whose inductance is given by a maximum peak-to-peak current ripple of 40 % (i.e., $L_{dm1} = L_{DM1} = 297\,\mu\text{H}$, see **Section IV**), also serve as the first-stage DM filter inductors. Thus, $f_{c1,DM}$ directly defines $C_{dm1} = C_{DM1} = 2\,\mu\text{F}$. The remaining reactive power budget (3.2 %) allows $C_{dm2} = C_{DM2} = 3.6\,\mu\text{F}$, and with $f_{c2,DM}$, we find $L_{dm2} = L_{DM2} = 17.4\,\mu\text{H}$.

Unlike the VSC, the CSC needs dedicated first-stage DM filter inductors. We design the CSR's and the CSI's first-stage DM capacitor C_{DM1} for a maximum peak-to-peak voltage ripple of 5 %. A capacitance value large enough to meet the voltage ripple criteria while minimizing the combined volume and losses of the two DM filter inductors results in a reactive power budget division of 3:2 between the first-stage and second-stage DM filter capacitors. With the required cutoff frequencies we then find $C_{dm1} = C_{DM1} = 3.3\,\mu\text{F}$, $L_{dm1} = L_{DM1} = 220\,\mu\text{H}$, $C_{dm2} = C_{DM2} = 2.2\,\mu\text{F}$ and $L_{dm2} = L_{DM2} = 36.5\,\mu\text{H}$.

2) CM Filters: As the CM equivalent circuits of the VSC and the CSC are essentially identical (see **Fig. 6bd**), the CM filter design procedures follow the same steps. The first-stage CM filter inductor L_{cm1} is designed to limit the peak-to-peak current ripple through the first-stage CM filter capacitor C_{cm1} to

[6]Note that the reactive power on the motor side will vary directly proportional to the output frequency and will be higher than 5 % at motor frequencies above 50 Hz.

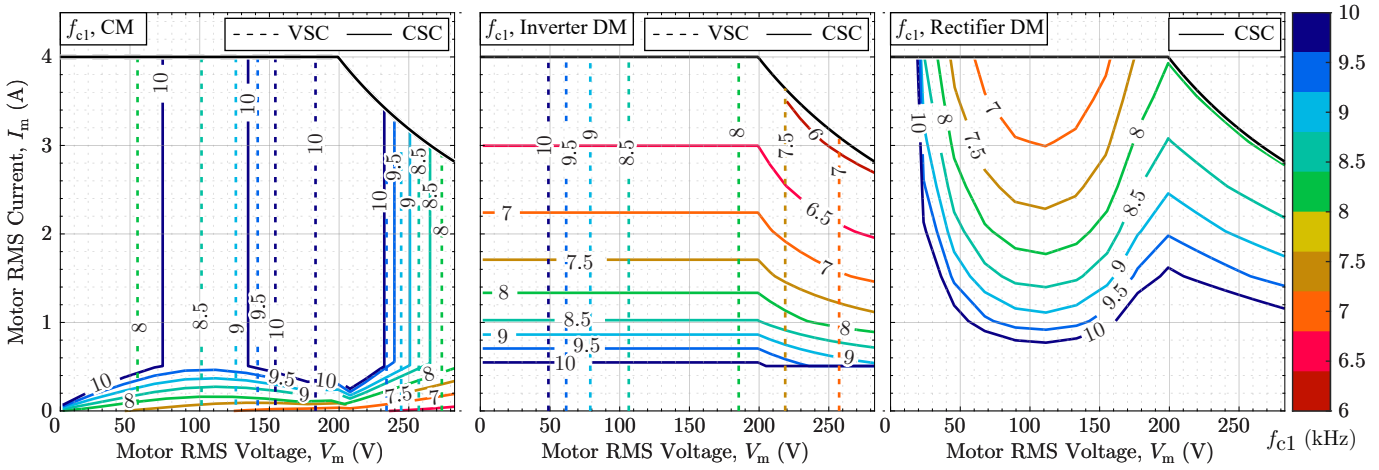

Fig. 8. Required first-stage cutoff frequencies for the VSC and the CSC over the motor operating range, considering current and upcoming EMI limits covering the frequency range from 9 kHz to 30 MHz (cf. **Fig. 5**). **(a)** CM filter, **(b)** inverter DM filter, **(c)** rectifier DM filter (note that for the VSC, the cutoff frequency is 7.8 kHz and independent of the operating point, since the grid voltage is fixed to 200 V). **Table II** summarizes the worst-case cutoff frequencies.

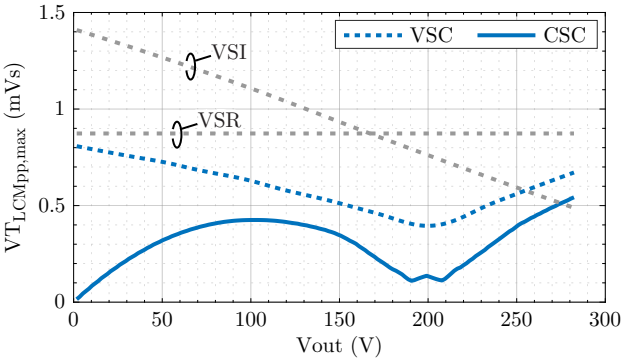

Fig. 9. Maximum peak-to-peak voltage-time area applied across the first-stage DC-side CM inductors of the VSC and the CSC. For reference, also the voltage-time areas that the VSR and VSI stage would apply to individual AC-side first-stage CM inductors are shown.

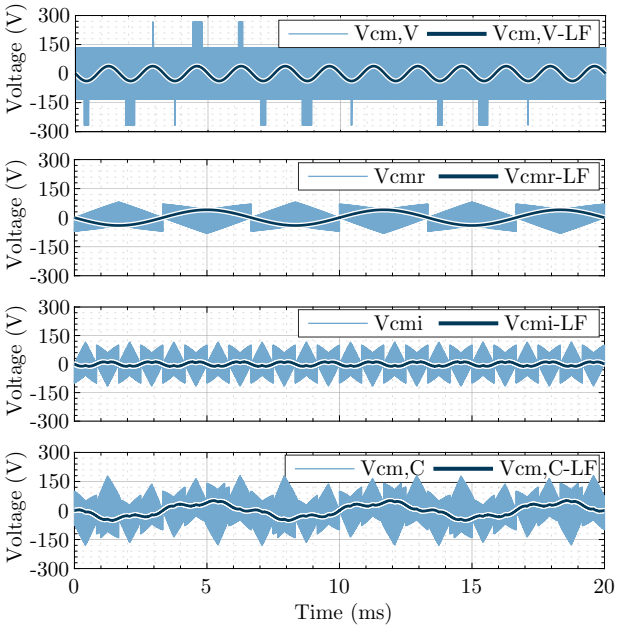

Fig. 10. Simulated CM voltages and their low-frequency components for the VSC, the CSR stage, the CSI stage, and the full CSC, for an input line-to-line rms voltage of 200 V, a grid frequency of 50 Hz, a worst-case output line-to-line rms voltage of 283 V and a motor frequency of 200 Hz.

1 A. To identify the worst-case operating point, **Fig. 9** shows the maximum peak-to-peak voltage-time area $Vt_{Lcm1pp,max}$ across L_{cm1} for the VSC and CSC in dependence of the motor voltage V_m (it is independent of the motor current). Also shown are the $Vt_{Lcm1pp,max}$ that would be applied to individual AC-side CM inductors of the VSR and VSI stage, highlighting one of the advantages of having a single DC-side CM inductor for an AC-AC VSC system (see above). Finally, for the considered DC-side CM inductors and with the required $f_{c1,CM}$, we find $L_{cm1} = 0.8\,\text{mH}$ and $C_{cm1} = 0.53\,\mu\text{F}$ for the VSC, and $L_{cm1} = 0.6\,\text{mH}$ and $C_{cm1} = 1\,\mu\text{F}$ for the CSC.

The second-stage CM filter capacitors must be designed to limit the current flowing through protective earth to a maximum of 3.5 mA (to avoid nuisance tripping of RCDs) in the worst case operating point. Note that the CM voltage of the AC-AC VSC contains a low-frequency component as a result of third-harmonic injection used in the VSI stage (as a result of space-vector modulation, and at least unavoidable for higher output voltages), see **Fig. 10a**. In contrast, the CSI and the CSR stages both inherently generate a low-frequency component in the respective CM voltage[7] (see **Fig. 10bc**), and the AC-AC CSC's total CM voltage thus contains two different main low-frequency components (third harmonics of the grid and of the motor fundamental frequency), see **Fig. 10d**. Assuming a parasitic capacitance of 1 nF from motor to earth, we find $C_{CM2} = 25\,\text{nF}$ for the VSC and $C_{CM2} = 10\,\text{nF}$ for the CSC. Even though only C_{CM2} on the inverter side is relevant regarding the earth current criteria, we select $C_{cm2} = C_{CM2}$, i.e., follow the paradigm of symmetric filter designs with identical components for rectifier and inverter stages. For the selection of the second-stage CM inductor values, we employ the following worst-case consideration: In the lower part of the EMI frequency range (down to 9 kHz), the grid (LISN) impedance is much lower than the impedance of C_{CM2}, whereas the motor impedance could be much higher (see, e.g., [42]). Therefore, the second-stage CM filter essentially consists of the series connection of L_{cm2} on the rectifier side and L_{CM2} and C_{CM2} on the inverter side. With $f_{c2,CM}$, we thus find $L_{cm2} = L_{CM2} = 1\,\text{mH}$ for the VSC and $L_{cm2} = L_{CM2} = 3.3\,\text{mH}$ for the CSC.

IV. Comparative Evaluation of Passive Component Effort

With the EMI filter components defined in the previous section, it remains to design the VSC's boost inductances and the CSC's DC-link inductance, before then comparing actual volumes and losses of all magnetic components.[8]

The VSC's boost and output inductances (L_{dm1} and L_{DM1}) are designed for a typical peak-to-peak current ripple of $\delta i_{pp} = 40\,\%$ at the nominal operating point as

$$L_b = \frac{1}{2 f_s \delta i_{pp} \sqrt{2} I_{m,n}} \left(\sqrt{\frac{2}{3}} V_{m,n} - \frac{2}{3} \frac{V_{m,n}^2}{V_{dc}} \right) \approx 297\,\mu\text{H}. \quad (14)$$

Similarly, the VSC's total DC-link capacitance follows from an energy-based approach [39] as $C_{dc} \approx 12\,\mu\text{F}$.

The DC-link inductor of the CSC is designed to limit the peak-to-peak current ripple to 20 %.[9] The worst-case DC-link current ripple is evaluated based on the maximum applied peak-to-peak voltage-time area $Vt_{Ldcpp,max}$, whereby the entire motor voltage and motor frequency range is considered[10], resulting in $L_{dc} = 1.3\,\text{mH}$.

The VSC's boost inductors and the CSC's DC-link inductor are designed with a custom Pareto optimization routine [43], considering various core materials (ferrite, iron powder), core shapes (E, ELP and toroidal), and different winding configurations (solid, litz, flat helical, and foil). The first-stage CM inductors L_{cm1} for both, VSC and CSC systems, are also designed with a similar Pareto optimization routine that considers toroidal nanocrystalline cores. Combining all possible

[7]The magnitude depends on the selected modulation scheme; we here consider a modulation scheme with optimized zero-state placement for minimum low-frequency CM voltage generation [14, p. 101ff.].

[8]Note that semiconductor losses imply the same hat sink size, the same number of switches implies similar size of the PCBs, and the overall capacitor volume is found to be significantly lower than that of the magnetics.

[9]A relatively low ripple facilitates operation with a lower DC-link current level while still ensuring a fixed current direction required for current-direction-based four-step commutation sequences.

[10]Since the DC-link current is adjusted according to the operating point as per (4), $Vt_{Ldcpp,max}$ does not depend on the motor current.

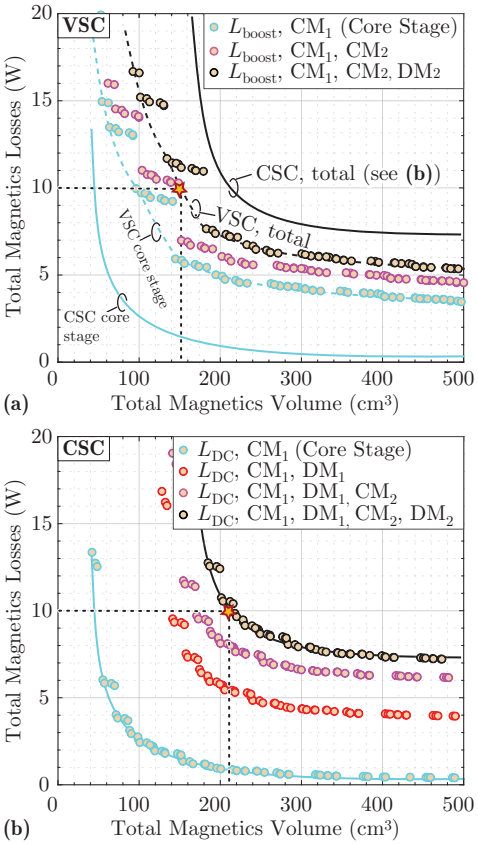

Fig. 11. Loss-vs.-volume Pareto fronts of the magnetic components required for **(a)** the VSC and **(b)** the CSC. Full and symmetric EMI filters (see **Fig. 1**) for the grid and the motor interfaces are considered.

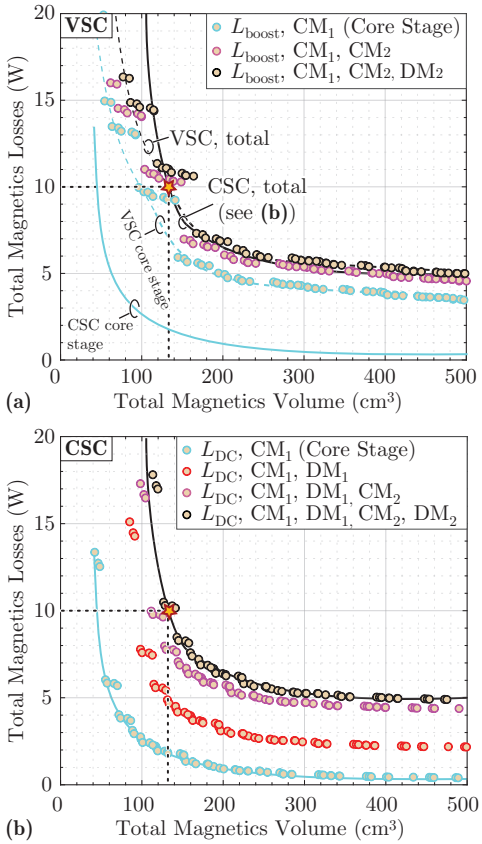

Fig. 12. Loss-vs.-volume Pareto fronts of the magnetic components required for **(a)** the VSC and **(b)** the CSC. Targeting motor-integration, the motor-side DM EMI filter is not necessary and therefore omitted.

Pareto-optimal designs of L_{boost} or L_{DC} with all Pareto-optimal designs of the respective first-stage CM inductors, we obtain a combined loss-vs.-volume Pareto front of the magnetics of the core power stages[11], see **Fig. 11**. Considering only the core power stage, the CSC can be implemented with clearly lower magnetics volume and/or losses compared to a VSC system.

As the remaining inductive components of the EMI filter are mainly subject to low-frequency current stresses, we consider available off-the-shelf components.[12] The corresponding volume and loss contributions are then combined with the Pareto fronts of the main magnetic components to characterize the total effort in terms of magnetic components (see black lines in **Fig. 11**). Thus, considering EMI filters on both, the grid and the motor interface (see **Fig. 1**) for compliance with current and upcoming standards over the full frequency range of 9 kHz to 30 MHz, the VSC achieves overall lower magnetics losses/volume. One reason can be seen in the fact that the CSC's DC-link inductor does not contribute to DM filtering, whereas the VSC's boost inductors do (see **Fig. 6ac**). Therefore, the CSC requires relatively large first-stage DM filter inductors. This, however, could be counteracted by allowing a higher capacitive reactive power consumption that would benefit the CSC more than the VSC, and which is subject to further analysis.

[11]The core power stage comprises all components from C_{dm1} on the grid-side to C_{DM1} on the motor-side, see **Fig. 1**.

[12]VSC DM2: Würth Elektronik 7444011715220; CSC DM1: Würth Elektronik 74437529203221; CSC DM2: Sumida DEP1519BHF-330M.

In order to achieve an overall AC-AC efficiency of 97 % at the nominal operating point, the semiconductor losses leave a budget of about 14 W (see **Fig. 3**). Allocating an assumed 4 W for control electronics, etc., the remaining loss budget of 10 W for all magnetic components together then results in a total magnetics volume of about 155 cm^3 (9.5 in^3) for the VSC and about 210 cm^3 (12.8 in^3) for the CSC, as indicated in **Fig. 11**.

Finally, for an integrated motor-drive system the DM EMI filter on the motor side can be omitted[13], which results in the modified magnetics loss-vs.-volume Pareto fronts shown in **Fig. 12**. These indicate similar effort for both systems, i.e., a total magnetics volume of about 130 cm^3 (8 in^3) for the VSC and for the CSC when again targeting an overall AC-AC efficiency of 97 %.

V. Conclusions

New monolithic bidirectional GaN transistors (140 mΩ, 600 V) enable AC-AC CSCs with similar total chip area as AC-AC VSCs to achieve similar semiconductor AC-AC efficiencies of 98 % for a nominal power of 1.4 kW (nominal motor RMS current of 4 A at nominal motor voltage of 200 V) and a switching frequency of 72 kHz. Furthermore, we find similar requirements regarding the total EMI filter attenuations needed to comply with today's and future (for the frequency range 9 kHz to 150 kHz) EMI limits. We apply these limits

[13]Regarding magnetics, this implies that L_{DM2} of the VSC but L_{DM1} *and* L_{DM2} of the CSC are not needed. Note that the motor is still provided with sinusoidal voltages in both cases.

to both, the grid and the motor interface, with the intent of achieving next-generation plug-and-play motor drive systems. Then, and for a total AC-AC efficiency of 97 %, the total magnetic component volume of the VSC is only about 75 % of the CSC's, as the DC-link inductor does not contribute to the DM attenuation, in contrast to the VSC's boost inductors. Targeting instead a motor integration of the AC-AC converters, the motor-side DM filter stages can be omitted to some extent, and we then find very similar total magnetics volumes for both systems.

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