Power Electronic Systems
Laboratory

Proceedings of the 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016), Glasgow, Scotland, April 19-21, 2016

New Optimum Modulation of Three-Phase ZVS Triangular Current Mode GaN Inverter Ensuring Limited Switching Frequency Variation

M. Kaufmann
A. Tüysüz
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

New optimum modulation of three-phase ZVS triangular current mode GaN inverter ensuring limited switching frequency variation

M. Kaufmann, A. Tüysüz, J. W. Kolar

Power Electronic Systems Laboratory, ETH Zurich, Switzerland
kaufmann@lem.ee.ethz.ch, www.pes.ee.ethz.ch

Keywords: Three-phase inverter, triangular current mode, soft switching, resonant transition switching, common-mode voltage.

Abstract

In three-phase pulse width modulation inverters with an LC output filter, switching losses can be reduced by increasing the current ripple in the inductor until a current zero crossing occurs between the two switching instances of a bridge leg. A disadvantage of this triangular current mode (TCM) operation is the varying switching frequency. This paper presents new modulation methods where the current ripple amplitude is adjusted and a common-mode voltage is introduced in order to limit the switching frequency variation. Moreover, the possibility of increasing the efficiency and minimizing the filter volume are investigated. Numerical optimization results are presented for a 2.5 kW inverter with 400 V DC link voltage as a case study.

1 Introduction

In two-level three-phase pulse width modulation inverters with LC output filters, the switching actions of a bridge leg within one switching period can benefit from a resonant transition if the current ripple in the inductor is increased until a current zero crossing occurs between the two switching instances [1]. This mode of operation is called triangular current mode (TCM), and enables zero-voltage switching (ZVS), which results in lower switching losses [2].

On the other hand, the switching frequency of TCM operation is not fixed as in standard space vector modulation (SVM), and may vary significantly depending on the operating point of the inverter. The large switching frequency variation makes the design of an EMI filter, which might be arranged between inverter and load (e.g. a motor) much more challenging than having a constant switching frequency. Furthermore, delays in measurements and signal processing impose a maximum switching frequency limit that cannot be exceeded in practical applications, which also makes the varying switching frequency an undesirable feature.

One way to decrease the ratio between maximum and minimum switching frequencies is to use two or more interleaved bridge legs per phase with individual filter inductors, and to operate more bridge legs with increasing output currents [3]. However, this approach comes with significant additional hardware effort, partly hindering the filter volume reduction possibility that is enabled by the low-loss (ZVS) application of higher switching frequencies.

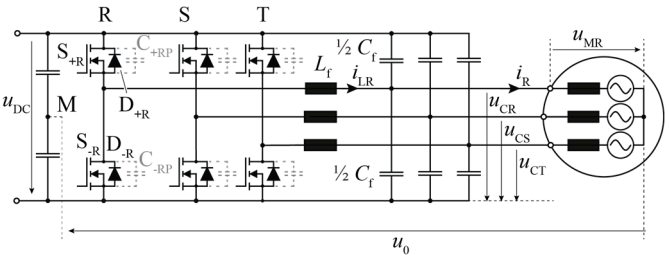

Figure 1. Schematic drawing of a three-phase TCM inverter with the LC output filter and a three-phase machine as load.

This paper discusses an alternative modulation method for three-phase TCM inverters, in which the possibility of utilizing a common-mode (CM) voltage is discussed along with the option of increasing the inductor current ripple amplitude in excess of the minimum ripple required for ZVS, with the goal of limiting the switching frequency variation, the losses, and the filter volume.

In the following section 2, the basic principle of operation of TCM inverters is explained. In section 3, the new modulation techniques are presented and their performances are assessed based on a case study. Finally, a conclusion and an outlook are given in section 4.

2 Two-Level Three-Phase TCM Inverters

2.1 Principle of Operation

Figure 1 shows a two-level three-phase TCM inverter, and Figure 2 (a) depicts the corresponding six different operating phases that occur within a switching period [4]. During interval 1, the upper switch S_+ is conducting and thus, the current i_L increases linearly, given the assumption that the output voltage ripple is negligible. After having turned off S_+, the parasitic output capacitance C_{+P} of S_+ is charged and C_{-P} of S_- is discharged in interval 2 during a resonant transition. Interval 3 starts when C_{-P} is fully discharged and diode D_- starts conducting. Now, switch S_- can be turned on at ZVS. When the current i_L reaches zero, interval 4 begins and it ends by turning S_- off at a desired current level $i_{LS\text{-}off}$. During interval 5, another resonant charging and discharging of the parasitic capacitances

C_{+P} and C_{-P} takes place. After C_{-P} is fully charged, D_+ starts conducting and S_+ can be turned on with ZVS during interval 6. At the zero crossing of i_L, interval 1 starts again.

According to [4], the inductor current waveform can be approximated in a first step with sufficient accuracy using a linear model as in Figure 2 (b), since the duration of the resonant transitions is negligible for practical switching frequencies.

The reverse current i_0 should be large enough such that the energy stored in the inductor suffices to fully discharge and charge the parasitic capacitances of the switches, hence to ensure ZVS. The minimum required i_0 is dependent on the output voltage u_C. Therefore, it varies within an output (fundamental) period even for constant load [4]. A larger i_0 leads to an increase of the conduction losses in the transistors and the inductor. Nevertheless, for a simpler control implementation in practical applications, a constant reverse current $i_{\min}$ can be applied, where $i_{\min}$ is the worst-case (largest) value of i_0 needed within the whole fundamental period.

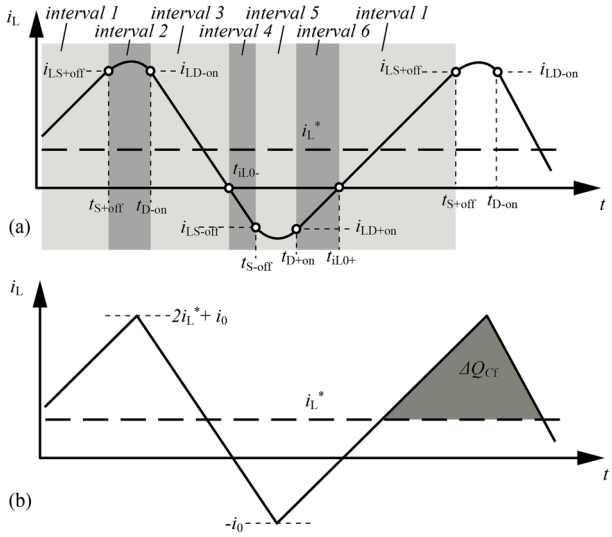

Figure 2. Inductor current waveform and the different intervals within a switching period (a). Linear approximation of the inductor current and the charge ΔQ_{Cf} that determines the output voltage ripple (b).

The upper and lower bounds of the inductor current can be calculated as $i_{L,\mathrm{UB}} = 2i_{\mathrm{L}}^* + i_o$, and $i_{L,\mathrm{LB}} = -i_o$ for a positive short-term average reference value i_{L}^* of the inductor current i_{L}. A current zero crossing detector and precise timers are used in practice rather than high bandwidth current sensing and comparison to upper and lower bounds in order to determine the switching instants, especially in applications with high switching frequencies.

Based on the linear current waveform and with no additional common-mode voltage u_0 applied, the switching frequency of one bridge leg is

$$f_{sX}(\vartheta) = \frac{¼ \cdot u_{\mathrm{DC}}^2 - u_{MX}^2(\vartheta)}{L_f \cdot u_{\mathrm{DC}} \cdot 2 \cdot (|i_{LX}^*(\vartheta)| + i_0)}, \quad (1)$$

where X stands for one of the phases R, S or T, u_{DC} is the DC link voltage, L_{f} is the filter inductance, i_{LX}^* is the desired average inductor current within the considered switching period, u_{MX} is the machine phase voltage, ϑ is the electrical angle within the fundamental period, and i_0 is the aforementioned minimum reverse current $i_{\min}$ required to ensure ZVS.

The root-mean-square (RMS) of the triangular inductor current within one switching cycle can be calculated as

$$i_{\mathrm{L,RMS}} = \sqrt{i_{\mathrm{L}}^{*2} + \frac{1}{12}(2i_{\mathrm{L}}^* + 2i_0)^2}\,. \quad (2)$$

Consequently, the conduction losses in the switches of one bridge leg can be approximated as

$$P_{\mathrm{cond}} = f_{\mathrm{f}} \int_0^{1/f_{\mathrm{f}}} R_{\mathrm{DS,on}} \left(i_{\mathrm{L}}^{*2} + \frac{1}{12}(2i_{\mathrm{L}}^* + 2i_0)^2 \right) \mathrm{d}t, \quad (3)$$

where $R_{\mathrm{DS,on}}$ is the on-state resistance of one switch and f_{f} is the fundamental output frequency. Similarly, the switching losses in a bridge leg can be approximated as

$$P_{\mathrm{sw}} = f_{\mathrm{f}} \int_0^{1/f_{\mathrm{f}}} f_{\mathrm{s}}\, E_{\mathrm{sw}}(i_{\mathrm{sw}})\, \mathrm{d}t, \quad (4)$$

where E_{sw} is the switching energy as a function of the switched current i_{sw}. The inductor current ripple amplitude $\Delta i_L = |i_L^*| + i_0$ leads to a peak-to-peak output voltage ripple

$$\Delta u_{\mathrm{Cf}} = \frac{\Delta Q_{Cf}}{C_{\mathrm{f}}} = \frac{|i_{\mathrm{L}}^*| + i_0}{4\, C_{\mathrm{f}}\, f_{\mathrm{s}}}\,. \quad (5)$$

2.2 Case Study

Today, variable speed drives make up a significant share of the market for low-voltage inverters. Power ratings around 2.5 kW and output frequencies up to 400 Hz are typical for a wide range of applications such as pumps, gantry robots, packaging, conveyor technology and handling belts in various industries [5]-[8]. Therefore, similar specifications are assumed for a case study in this work, as shown in Table 1.

DC link voltage	U_{DC}	400 V
Machine phase voltage (RMS)	u_{MR}	110 V
Machine current (RMS)	i_{R}	8.5 A
Machine fundamental frequency	f_{f}	400 Hz
Power factor	$\cos(\varphi)$	0.92

Table 1. Parameters selected for the case study.

GaN power transistors with a rated blocking voltage of 600 V and $R_{\mathrm{DS,on}} \approx 100$ mΩ (at 100 °C junction temperature) are considered as switches. Soft switching losses are measured using a bridge leg hardware prototype. Details about the switching loss measurement setup and the used gate drive are given in [9]. In this work, the switching energy is approximated as

$$E_{\mathrm{sw}}(i_{\mathrm{sw}}) = E_0 + E_1\, i_{\mathrm{sw}} + E_2 i_{\mathrm{sw}}^2 + E_3 i_{\mathrm{sw}}^3, \quad (6)$$

where i_{sw} is the switched current, yielding

$$P_{\mathrm{sw}} = f_{\mathrm{f}} \int_0^{1/f_{\mathrm{f}}} f_{\mathrm{s}} \left(E_0 + E_1 \left(i_{L,\mathrm{LB}} + i_{L,\mathrm{UB}} \right) + E_2 \left({i_{L,\mathrm{LB}}}^2 + {i_{L,\mathrm{UB}}}^2 \right) + E_3 \left({i_{L,\mathrm{LB}}}^3 + {i_{L,\mathrm{UB}}}^3 \right) \right) \mathrm{d}t, \quad (7)$$

where E_0 = 1.17µJ, E_1 = 0.1µJ/A, E_2 = 0.002 µJ/A^2 and E_3 = 0.0027µJ/A^3.

As can be seen in Equation 1, the filter inductance L_f directly affects the maximum occurring switching frequency. Therefore, the minimum value of L_f is constrained by the maximum switching frequency defined by the delays of the signal processing hardware (FPGA) and the measurement circuitry. Thus, the maximum switching frequency is set to 1 MHz. This results in a minimum filter inductance of 9.5 µH, for the operating conditions of Table 1. Since the filter inductors are contributing significantly to the overall inverter volume, it would be a good design choice to use the minimum allowed inductance value. Once the L_f value is set, the minimum filter capacitance value C_f can be determined easily regarding the maximum allowed output voltage ripple $\Delta u_{C\mathrm{f}}$ at the worst case. When a maximum voltage ripple of $\Delta u = \Delta u_{C\mathrm{f}} / \hat{u}_{\mathrm{MR}} = 5\%$ is set where $\hat{u}_{\mathrm{MR}}$ is the peak fundamental machine phase voltage, a minimum filter capacitance of C_f = 4.7 µF is necessary. Figure 3 depicts the reference inductor current in phase R along with its upper and lower bounds, the time behaviour of the switching frequencies of three bridge legs and the resulting output voltage ripple for L_f = 9.5 µH and C_f = 4.7 µF.

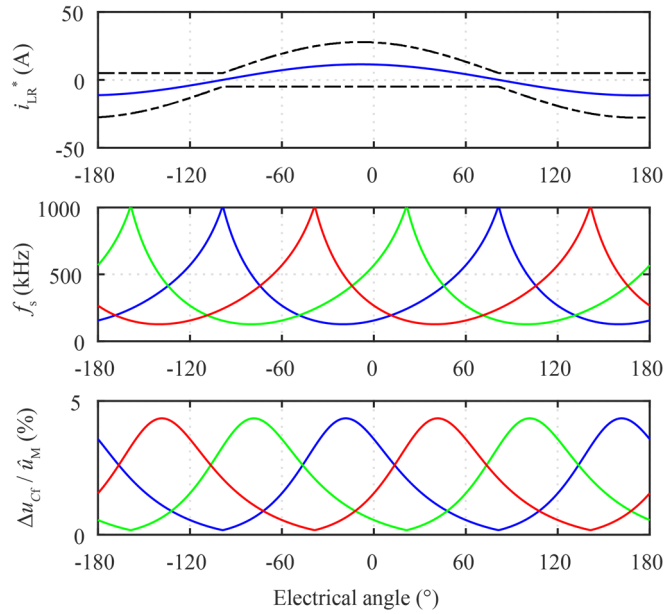

Figure 3. Reference value, upper and lower bound of i_{LR} (top), switching frequencies (middle) and relative output voltage ripples (bottom). Blue, green and red denote phases R, S and T, respectively.

A circuit simulation using GeckoCIRCUITS software [10] is used in order to numerically verify the analysis presented above. Ideal switches with antiparallel ideal diodes and no parasitic capacitances are used and switched using a hysteresis band control of the inductor current resulting in the TCM current waveform. A fixed time step of 5 ns is used for solving the circuit model. The resulting switching frequencies, machine phase voltages and the inductor current in phase R are shown in Figure 4.

Table 2 compares the transistor losses calculated analytically, and the transistor losses calculated based on the current waveforms generated by the numerical circuit simulation, and verifies the analytical models.

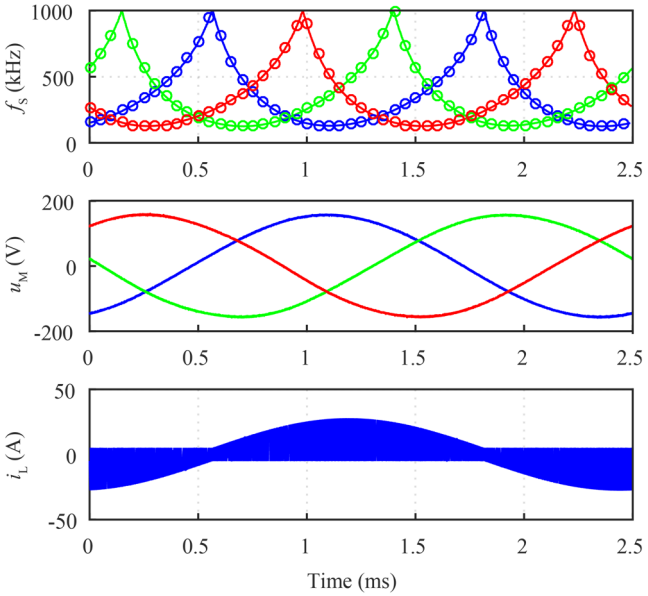

Figure 4. Switching frequencies according to numerical circuit simulation (circles) and Equation 1 (solid lines) (top). Motor phase voltages (middle) and inductor current in phase R (bottom) according to the numerical circuit simulation. Blue, green and red denote phases R, S and T, respectively.

	Analytical (Eq. 3, Eq. 7)	Numerical (GeckoCIRCUITS)
P_{cond}	35.82 W	36.11 W
P_{sw}	22.12 W	22.15 W

Table 2. Calculated transistor losses for the case study.

3 Optimum Modulation

3.1 Degrees of Freedom

In order to limit the switching frequency variation, the switching losses and the filter volume, the common-mode voltage u_0 (cf. Figure 1) can be utilized as well as a reverse current value i_0 that exceeds the value that is needed for ZVS, i.e. $i_0 \geq i_{min}$ [11]. Considering these two degrees of freedom, Equation 1 for the switching frequency transforms into

$$f_{sX}(\vartheta) = \frac{¼ - (m_{\mathrm{MX}}(\vartheta) + m_0(\vartheta))^2}{L_\mathrm{f} \cdot 2 \cdot \left(\left| i_{\mathrm{LX}}^*(\vartheta) \right| + i_{0X}(\vartheta) \right)} \cdot u_{\mathrm{DC}}\,, \quad (8)$$

where $m_{\mathrm{MX}} = u_{\mathrm{MX}}/u_{\mathrm{DC}}$, $m_0 = u_0/u_{\mathrm{DC}}$, $i_0 \geq i_{\mathrm{min}}$ is the reverse inductor current and ϑ is the electrical angle within the fundamental period. $D_X = m_{\mathrm{MX}} + m_0 + ½$ is the duty cycle in phase X. Thus, $|m_{\mathrm{MX}} + m_0| \leq ½$ has to be satisfied for all three phases.

Figure 5 illustrates the relationship between m_0 and the switching frequencies in the three phases, without taking into account the influence of the common mode component of i_L

caused by u_0 on the switching frequency. The reverse current is set to its minimum value i_{min} for all three phases. The boundaries of m_0 for ensuring $0 < D_x < 1$ are denoted by the dashed black lines.

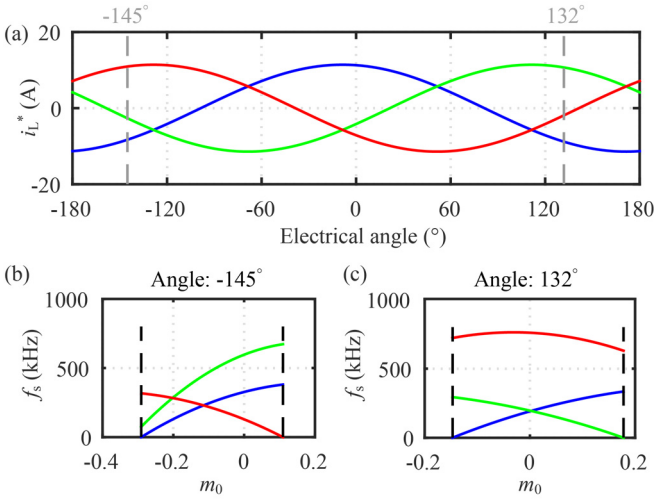

Figure 5. Inductor reference currents i_L^* for $m_0 = 0$ and $i_0 = i_{min}$ (a) and the influence of m_0 on f_s at the angle -145° (b) and 132° (c). Blue, green and red denote phases R, S and T, respectively. The dashed grey lines in (a) indicate the inductor current situation for (b) and (c). The dashed black lines in (b) and (c) denote the boundaries for m_0 due to the duty cycle limitation $0 < D_x < 1$.

3.2 Numerical Optimization

Numerical optimizations are used for finding the optimum i_0 and m_0 values that minimize the switching frequency variation, the losses and the filter volume. In order to do so, the waveforms $i_0(\vartheta)$ and $m_0(\vartheta)$ are parameterized as shown in Figure 6. Parameters $p_1 ... p_6$ define i_{0R} for $-180° < \vartheta < 0$, which is repeated for the other half of the fundamental period. i_{0S} and i_{0T} have the same waveform but are 120° phase-shifted. Parameters $p_7 ... p_{10}$ are describing m_0, which is defined as the sum of a sinusoidal and a triangular function with three times the fundamental frequency and with parameterized amplitudes and phases. Particle swarm optimization is chosen as numerical minimization algorithm. A maximum peak-to-peak output voltage ripple of $\Delta u_{max} = 5\%$, a maximum switching frequency of $f_{s,max} = 1$ MHz, and a limit on the duty cycle of $0.03 < D < 0.97$ are applied as constraints. Moreover, $p_6 \geq i_{min} = 5$ A is enforced to guarantee ZVS, and p_2 is limited to $p_2 \leq 25$ A.

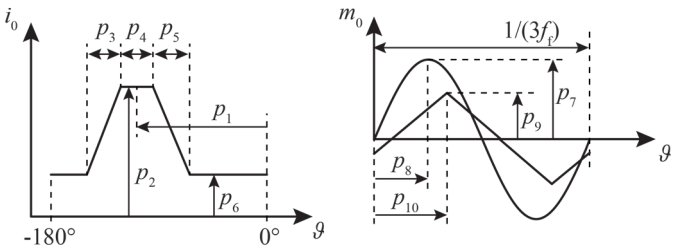

Figure 6. Parameterization of the $i_0(\vartheta)$ and $m_0(\vartheta)$ for numerical optimization.

Figure 7 shows the optimization results when a set of optimum values of i_0 and m_0 is searched with the goal of minimizing the equally weighted sum of the total transistor losses ($P_{cond} + P_{sw}$) and the ratio of maximum and minimum switching frequency within a fundamental period. As can be seen, both a nonzero common-mode voltage and $i_0 \geq i_{min}$ are utilized. As a result, the ratio of the maximum and minimum switching frequency decreases from 7.95 to 2.12. However, the significant increase in i_0 leads to an 8% increase of the conduction losses (from 35.8 W to 38.77 W). Similarly, the switching losses increase by 12%, increasing the overall transistor losses from 58 W to 63.8 W.

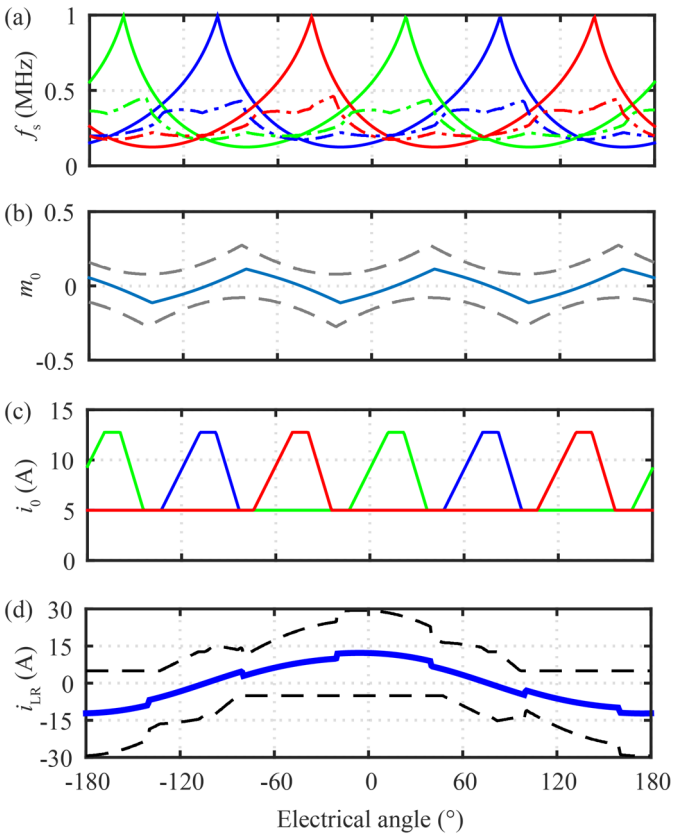

Figure 7. The switching frequency before (solid) and after (dashed) applying the optimized m_0 and i_0 values (a). Boundaries (dashed) and optimum waveform (solid) of the common-mode modulation index m_0 (b). Reverse current profiles (c). Resulting envelope (dashed) and short-term average (solid) of the inductor current in phase R (d). Blue, green and red denote phases R, S and T, respectively. The steps of i_{LR} arise due to the common-mode current $i_{CM} = C_f \cdot du_0/dt = C_f \cdot u_{DC} \cdot dm_0/dt$.

Limiting the switching frequency variation makes the design of a second-stage filter easier, which could be necessary for a grid-tied application of an inverter with strict EMC requirements. Moreover, based on the optimization results shown in Figure 7, the filter inductance L_f can now be made smaller than 9.5 µH to minimize the filter volume without violating the 1 MHz switching frequency limit. On the other hand, when the inverter in TCM operation is used for driving an electric machine, the 5% output voltage ripple limit may be sufficient in terms of output voltage distortion. In this case, i_0 and m_0 can be optimized for increasing the inverter efficiency.

ZVS allows for higher switching frequencies which is beneficial for miniaturization. However, as an intrinsic property of the TCM operation, the flux in the filter inductors L_f varies largely within each switching cycle which increases the core losses and complicates the inductor design.

Figure 8 shows the results of an optimization run where the goal has been set to minimize the inductor core losses, which are approximated as

$$P_{\text{core}} \propto f_{\text{f}} \int_0^{1/f_{\text{f}}} f_{\text{s}}{}^2 (i_{L,\text{UB}} - i_{L,\text{LB}})^3 \, \text{d}t. \tag{9}$$

It can be seen that an increase in i_0 is avoided for obviating additional losses, and a different waveform of common mode voltage is applied, which in turn effects the switching frequency (slightly) and the inductor current waveform. As a result, a 14% decrease in core losses are achieved compared to $u_0 = 0$ and $i_0 = i_{\text{min}}$.

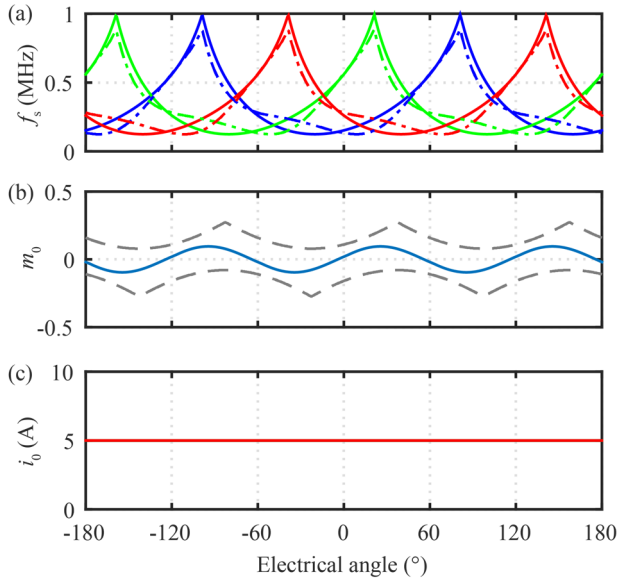

Figure 8. Switching frequency before (solid) and after (dashed) applying the optimized m_0 and i_0 values (a). Boundaries (dashed) and the optimum waveform (solid) of the common-mode modulation index m_0 (b). Reverse current profiles (c). Blue, green and red denote phases R, S and T, respectively.

As explained above, $L_{\text{f}} = 9.5$ µH and $C_{\text{f}} = 4.7$ µF are the minimum filter component values to ensure $f_{\text{s}} < 1$ MHz and $\Delta u < 5\%$ for $i_0 = i_{\text{min}}$ and $m_0 = 0$. On the other hand, previous examples demonstrate that i_0 and m_0 can be used to affect the circuit behaviour significantly. Therefore, in the next example, the filter components L_{f} and C_{f} are also optimized along with i_0 and m_0, with the goal of minimizing the sum of equally weighted total transistor losses and the inductor volume, which is approximated to scale as

$$V_{\text{Lf}} \propto L_{\text{f}} \, i_{L,\text{UB}} \cdot i_{L,RMS} \, , \tag{10}$$

where $i_{\text{L,RMS}}$ denotes the root mean square value of the inductor current. The resulting L_{f} is not much different to 9.5 µH, but C_{f} has increased to 13 µF. As can be seen in Figure 9, the switching frequency is almost unchanged, and i_0 is not modified; however, a common-mode voltage is used in order to shape the inductor current, and its upper and lower boundaries using the superposition of the common mode current through the inductors. The resulting total transistor losses are nearly identical, but a 10.5% decrease is achieved for the inductor volume.

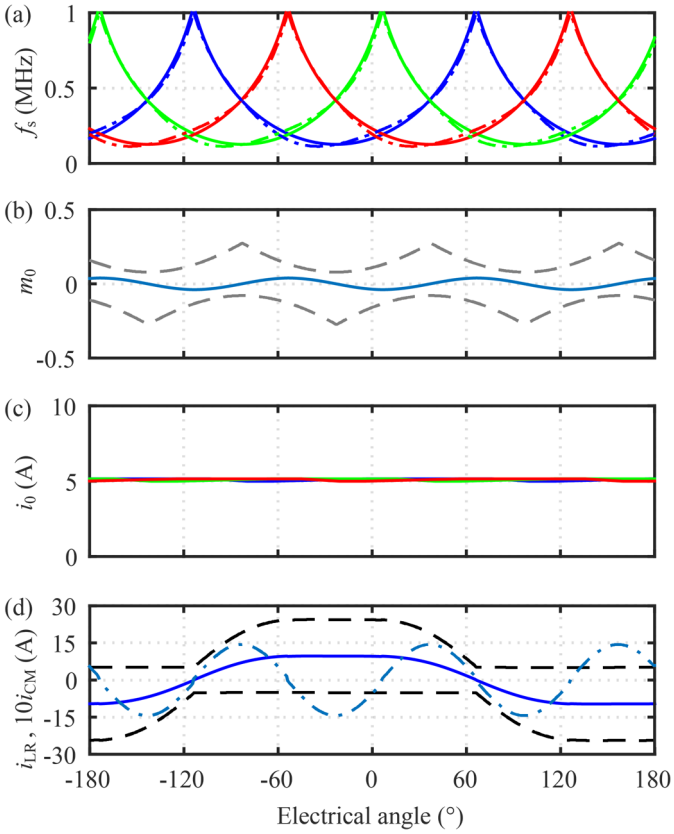

Figure 9. Switching frequency before (solid) and after (dashed) applying the optimized m_0 and i_0 values (a). Boundaries (dashed) and the optimum waveform (solid) of the common-mode modulation index m_0 (b). Reverse current profiles (c). The resulting envelope of the inductor current (dashed) and its average (solid) of phase R as well as the common-mode current i_{CM} multiplied by a factor of 10 (dash-dotted) to illustrate how it reduces the maximum value of i_{LR} (d). Blue, green and red denote phases R, S and T, respectively.

3.3 Intersection Algorithm

The intersection algorithm bases on the contemplation of figures like depicted in Figure 5(b-c). It goes through the following steps to determine m_0 for a given electrical angle:

1. Determine the switching frequencies of the three phases for $m_0 = 0$ and $i_0 = i_{\text{min}}$ and identify the phase with the lowest switching frequency, without loss of generality, e.g. phase T.
2. Calculate for which m_0 phase T has the same switching frequency as phase R or S, i.e. look for the intersections in the m_0-f_{s} plots, cf. Figure 5.
3. Take the m_0 with the smallest absolute value and calculate the switching frequency of phase T for this m_0, subsequently called $f_{\text{s,intersect}}$.

After having determined the m_0 and $f_{\text{s,intersect}}$ values for the whole fundamental period, identify the maximal $f_{\text{s,intersect}}$ and utilize i_0 to limit the maximum switching frequency in all phases over the whole period to this value.

The intersection algorithm yields very similar m_0 references as the numerical optimization (compare Figure 7 and Figure 10). According to the circuit simulation, the peak-to-peak output voltage ripple decreased from 5% to less than 3%, the transistor

losses increased by 28% and the ratio between maximum and minimum switching frequency decreased from 7.95 to 1.84.

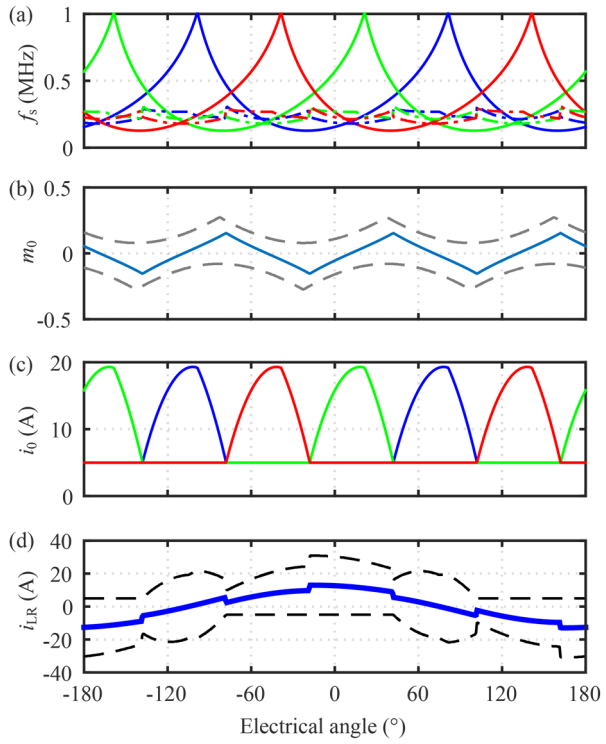

Figure 10. Analytically calculated switching frequency before (solid) and after (dashed) applying the intersection algorithm (a). Boundaries (dashed) and the optimum waveform (solid) of the common-mode modulation index m_0 (b). Reverse current profiles (c) and the resulting envelope of the inductor current (dashed) and its local average (solid) of phase R (d). Blue, green and red denote phases R, S and T, respectively. The steps of i_{LR} arise due to the common-mode current $i_{CM} = C_f \cdot du_0/dt = C_f \cdot u_{DC} \cdot dm_0/dt$.

4 Conclusion and Outlook

Triangular-current mode (TCM) operation may result in higher efficiencies and higher power densities of inverter systems with output filter due to the higher switching frequencies enabled by zero-voltage switching. On the other hand, this mode of operation is characterized by a largely varying switching frequency which is undesired in several applications.

This paper presents new modulation methods for three-phase TCM inverters where the current ripple amplitude and the common-mode voltage are adjusted in order to limit switching frequency variation as well as to increase the efficiency and to minimize the filter volume. Considering 2.5 kW variable speed drive inverter specifications, numerical optimizations are performed with different goals and a reduction of the switching frequency variation by a factor of 4 is demonstrated. Alternatively, the inductor core losses could be decreased by 14% or the filter inductor volume by 10.5%.

A possible challenge in the implementation of the presented methods is the storage and application of the optimum common-mode voltage and reverse current profiles calculated offline. Therefore, an online optimization method, such as perturb and observe, will be considered in the future, and the findings will be verified by measurements.

References

[1] R. Joensson, “A New Switch Circuit for Frequency Inverters”, Proc. of Int. Conf. on Power Conv. and Intelligent Motion (PCIM), 1988, pp. 262-271.

[2] C. Marxgut, J. Biela, J.W. Kolar, “Interleaved Triangular Current Mode (TCM) Resonant Transition, Single Phase PFC Rectifier with High Efficiency and High Power Density”, Proc. of Power Electr. Conf. (IPEC), 2010, pp. 1725-1732.

[3] R. Joensson, “PWM is Obsolete Technology from the ’70s “, Proc. of Int. Conf. on Power Conv. and Intelligent Motion (PCIM), 2009, pp. 390-395.

[4] C. Marxgut, F. Krismer, D. Bortis, J.W. Kolar, “Ultraflat Interleaved Triangular Current Mode (TCM) Single-Phase PFC Rectifier”, IEEE Transactions on Power Electronics, vol. 29, no. 2, 2014, pp. 873-882.

[5] Siemens AG, “SINAMICS: The Complete and Seamless Drive Family for Every Power Rating, Voltage and Performance Level”, online: www.siemens.com/sinamics, retrieved: Jan. 2016.

[6] SEW Eurodrive, “MOVIDRIVE® B Application Inverter, Technical Data”, online: www.sew-eurodrive.de, retrieved: Jan. 2016.

[7] LTI Drives, “CDD3000 Catalogue”, online: www.lti-motion.com, retrieved: Jan. 2016.

[8] Yaskawa, “G7 Drive Flyer”, online: www.yaskawa.com, retrieved: Jan. 2016.

[9] D. Bortis, O. Knecht, D. Neumayr, J.W. Kolar, “Comprehensive Evaluation of GaN GIT in Low- and High-Frequency Bridge Leg Applications”, submitted to the International Power Electronics Conference - ECCE Asia, 2016.

[10] Gecko Simulations AG, online: www.gecko-simulations.com, retrieved: Jan. 2016.

[11] J.W. Kolar, A. Tüysüz, M. Kaufmann, D. Bortis, D. Neumayr, “Steuerverfahren zur Minimierung der EM-Störaussendung und Verluste mehrphasiger AC/DC-Konverter mit TCM-Betrieb der Brückenzweige”, Swiss Patent Application, filed in Aug. 2015.