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EMI Filter Design for a Three-Phase Buck-Boost Y-Inverter VSD with Unshielded Motor Cables Considering IEC 61800-3 Conducted & Radiated Emission Limits

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***Abstract*—The standard converter concept employed in variable speed motor drives is the two-level three-phase Si IGBT voltage source inverter with its switch nodes connected to the motor terminals via shielded cables to avoid excessive high-frequency noise emissions. However, high dv/dt pulses of the inverter pose substantial stresses on the motor, which are further intensified by the ever-faster switching speeds of wide band-gap semiconductors, hence promoting interest in inverters with full-sinewave output filters, which potentially enable the use of inexpensive unshielded motor cables. However, the IEC 61800-3 standard dictates stringent conducted and radiated emission limits on unscreened power interfaces.**

In this work, a DC input and AC output filter structure allowing operation with unshielded cables is derived for a phase-modular $11\,\mathrm{kW}$ buck-boost Y-inverter motor drive system employing $1.2\,\mathrm{kV}$ SiC MOSFETs with a switching frequency of $100\,\mathrm{kHz}$. First, regulations and measurement techniques for conducted and radiated emissions of motor drives are analyzed. Next, the operating principle of the Y-inverter is described and an EMI equivalent circuit is derived, followed by a systematic filter design. Finally, measurements are conducted on an ultra-compact hardware prototype of the converter system with $12\,\mathrm{kW/dm^3}$ ($197\,\mathrm{W/in^3}$) power density, where the results indicate full compliance with the IEC 61800-3 conducted and radiated emission limits for operation with unshielded DC supply and motor cables in a residential area.

***Index Terms*—Variable Speed Drives, Three-Phase Buck-Boost Inverter, Y-Inverter, Electromagnetic Compatibility, DC-Side / AC-Side EMI Filter Design, IEC 61800-3**

I. Introduction

Today, more than two thirds of industry's electric energy consumption is used to power electric motors, contributing approximately $30\,\%$ to the global energy consumption and further growth is forecasted until 2040 [1]. In many applications, Variable Speed Drives (VSDs) allow a reduction of both the energy consumption and the life cycle cost of the overall drive system and are therefore a key technology towards a more sustainable society [2]. However, it is crucial to manage Electromagnetic Interference (EMI) emissions of VSDs [3], where the **IEC 61800-3** [4] is the relevant standard for industrial VSDs and applies both to AC grid connected and DC supplied systems (cf. **Fig. 1**). In industrial applications, there is a clear trend towards DC supply of VSDs [5]–[7], as e.g. power transfer among several drives is possible without loading the AC grid interface. Further, additional infrastructure such as a super capacitor energy storage can be shared among several VSDs [8], and accordingly, in the following a DC supplied system is considered for the analysis.

The Pulse-Width Modulated (PWM) two-level three-phase Silicon Insulated-Gate Bipolar Transistor (Si IGBT) Voltage Source Inverter (VSI), with the motor cable directly connected to the switch nodes of the inverter bridge-legs, is the predominant topology for DC-fed VSDs in industry. Employing shielded cables, the power converter and the motor can be considered as a single unit located in a shielded enclosure, where motor interface EMI emissions are confined and hence are not relevant from a regulatory perspective. Therefore the considered standard dictates – when employing shielded cables – only limits for the conducted grid interface emissions from $150\,\mathrm{kHz}$ to $30\,\mathrm{MHz}$, as well as for the radiated emission of the overall system in the range of $30\,\mathrm{MHz}$ to $1\,\mathrm{GHz}$ as presented in **Fig. 1**.

However, shielded cables are substantially more expensive than regular unshielded cables (up to a factor of three [10]) and also heavier (e.g. $152\,\mathrm{kg/km}$ for the unshielded 4GE-BC50, and $248\,\mathrm{kg/km}$ (+63 %) for the shielded 4GECY-KC50l cable from Belden Inc. ($500\,\mathrm{V}$, $20\,\mathrm{A}$)). In case of moving applications (e.g. in robotics) cables are also subject to repetitive bending and flexing stresses, potentially leading to fatigue and fracture of the cable shield [11]. Further, shielded cables are an obstacle towards non-expert installation of drives, as an improper connection of the cable shield to the converter or motor housing is a major source of error during commissioning of VSDs [12]. Accordingly, the use of unshielded cables would be especially interesting. It is important to highlight that the **IEC 61800-3** does not necessarily dictate the use of shielded cables, but imposes further conducted emission limits on any power interface (e.g. the motor cable or the DC bus) realized with unshielded cables longer than $2\,\mathrm{m}$ for VSDs operating in a residential area (cf. **Fig. 1**).

In case of the standard VSI, the pulse-shaped PWM switch-node voltages are directly applied to the motor cable and accordingly the use of unshielded cables is discouraged due to excessive conducted and radiated emissions [13]. There, the switched voltages with high dv/dt values further cause High-Frequency (HF) motor losses, and add severe motor stresses (i.e. transient overvoltages and reflected waves on long motor cables [14], as well as capacitive bearing currents [15], [16]), ultimately reducing the VSD product

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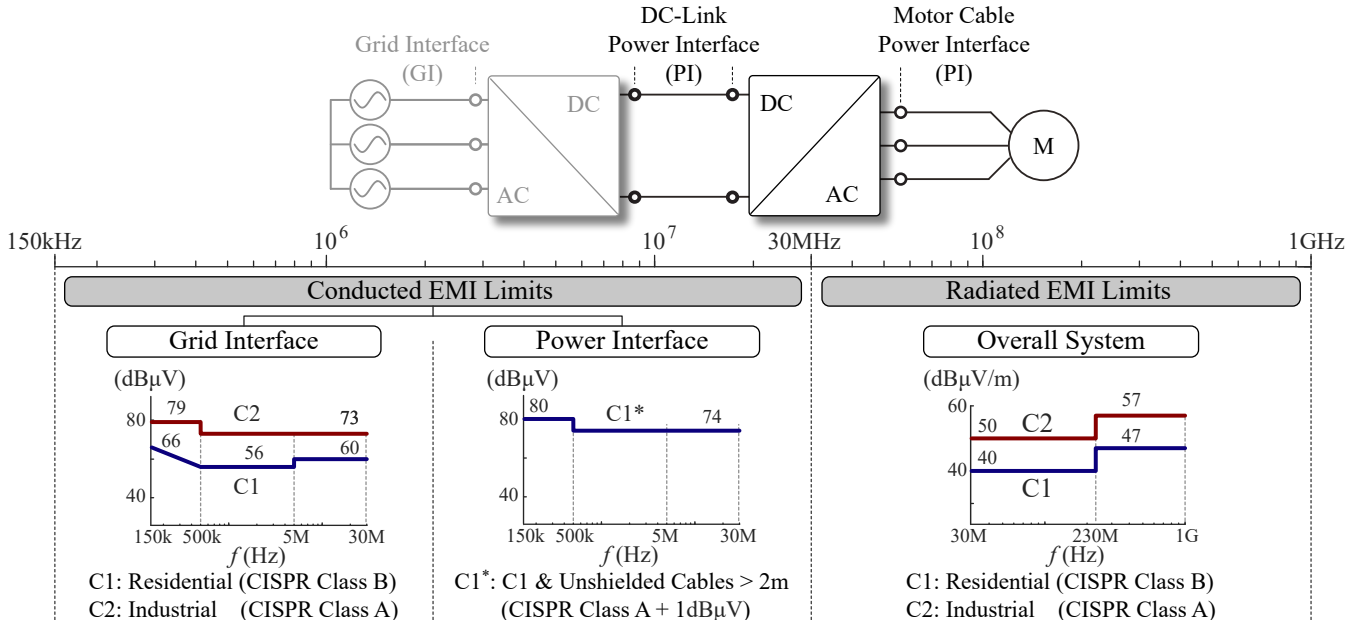

Fig. 1. Conducted and radiated EMI emission limits according to the **IEC 61800-3** [4] for residential (C1) and industrial (C2) applications. Conducted emission limits apply to the frequency band from 150 kHz to 30 MHz, where the grid interface limits are based on the well known *CISPR 11* regulations [9]. When employing long (i.e. $\geq$ 2 m) unshielded cables in residential applications, emission limits also exist for the respective internal power interfaces (i.e. DC bus or motor cable). The overall system further needs to comply with radiated emission limits in the range of 30 MHz to 1 GHz, where the stated limit values are valid for a measurement distance of 3 m.

lifetime. The emergence of ever-faster switching Wide Band-Gap (WBG) semiconductor devices further intensifies this problem [17], [18].

Converters with sinusoidal output voltages (e.g. a VSI with a sinewave filter [19]–[22] attached to the AC terminals) allow reducing motor stresses by filtering out switching-frequency voltage harmonics, where DC-link referenced filters [23]–[26] attenuate simultaneously Differential Mode (DM) and Common Mode (CM) HF noise. There, the high switching frequencies of WBG semiconductors up to 100 kHz allow a very compact realization of the filter and a complete mitigation of audible inverter noise below 20 kHz. Converters employing WBG semiconductors and full-sinewave filters were demonstrated to *increase* the overall system performance compared to Si IGBT inverters with unfiltered PWM waveforms, as the HF motor losses and the semiconductor switching losses can be significantly reduced [27]–[29]. Within this context, the recently introduced phase-modular buck-boost Y-inverter [30]–[32] (cf. **Fig. 2b**) featuring inherently sinusoidal AC output voltages (similar to a Current Source Inverter (CSI)) both above and below the DC-link voltage seems especially attractive, as it allows compatibility with a plurality of nominal DC bus and/or motor voltages. The Y-inverter is therefore considered for the following analysis.

The proliferation of VSDs with sinusoidal output voltages gives rise to the question if – or with what additional amount of filtering effort – such a system could allow operation with long unshielded motor cables. In [10], the impact of several output filter configurations on the conducted EMI emissions up to 30 MHz of a Si IGBT VSD operating with unshielded cables is analyzed, where a DC-link referenced filter structure provided a massive reduction of emission noise level. In [33]–[35] filter design guidelines are provided, considering the less stringent DO160 power interface limits (compared to the **IEC 61800-3** limit values) on the DC side and on the AC side for a standard two-level VSI, where only emissions up to 30 MHz are considered. It was further verified in [36] that radiated emission limits according to the **IEC 61800-3** can be met with a sinewave filter and employing both a 5 m and 75 m long cable. However, so far no comprehensive filter design guidelines for VSD operation with long unshielded cables according to the **IEC 61800-3** including radiated and conducted emissions is available.

In this publication we use prior art in systematic EMI filter design of three-phase Power Factor Correction (PFC) rectifier systems within the scope of an existing 11 kW Y-inverter VSD power stage according to the specifications in **Fig. 2a**. In a first step, in **Sec. II** the basic operating principle of the Y-inverter – a converter with hybrid VSI/CSI emission characteristics – is recapitulated and the impact of modulation and operating point on the HF emissions on DC and AC side is discussed. Subsequently, in **Sec. III** measurement techniques for conducted power interface emissions are presented. An EMI equivalent circuit for the Y-inverter is derived and filter design guidelines are presented. The radiated emission analysis and the related filter design is then conducted in **Sec. IV**, where the resulting electric field strength is estimated based on the converter CM currents. Then, in **Sec. V** the Y-inverter prototype with the derived filter structure on DC and AC side is detailed, and experimental verification of the EMI equivalent circuit and the design considerations is presented. Finally the key findings are summarized in **Sec. VI**.

II. Y-Inverter Topology

Requirements for future DC-fed VSDs include a wide applicability which means that the inverter needs to be capable of matching the DC supply voltage and the motor

voltages for various motor types and supply voltage levels, where sinusoidal output phase voltages allow for low HF motor stresses and losses. Additionally, high efficiency and compactness remain crucial figures of merit, and are especially relevant in mobile applications. In collaboration with the *European Center for Power Electronics* (ECPE [37]), benchmark specifications for an 11 kW VSD were defined for a lighthouse project: A 230 V_{rms} motor (400 V_{rms} line-to-line, nominal stator frequency $f_{ac,nom} = 200$ Hz) is powered from a DC input voltage varying in a wide range of 400 V to 750 V (cf. **Fig. 2a**), hence requiring an inverter system with buck-boost functionality.

The recently introduced phase-modular buck-boost Y-inverter [30]–[32] (the main power circuit is shown in **Fig. 2b**) features all above mentioned requirements and hence is selected for the analysis of operation with unshielded cables.

The operating principle of the Y-inverter is recapitulated within the following two subsections, where the subsequent EMI filter design is conducted for an existing Y-inverter hardware prototype (without explicit EMI filter) capable of covering the operating ranges shown in **Fig. 2a** and featuring a power density of 15 kW/dm^3 (246 W/in^3) and a nominal system efficiency of 98.3 %. Employing a switching frequency of $f_s = 100$ kHz, the prototype system comprises a buck-boost inductor of $L = 85$ µH, an effective AC capacitor of $C = 1.3$ µF, and a DC-link capacitor of $C_{dc} = 12$ µF. The employed Y-inverter hardware prototype is further detailed in **Sec. V**.

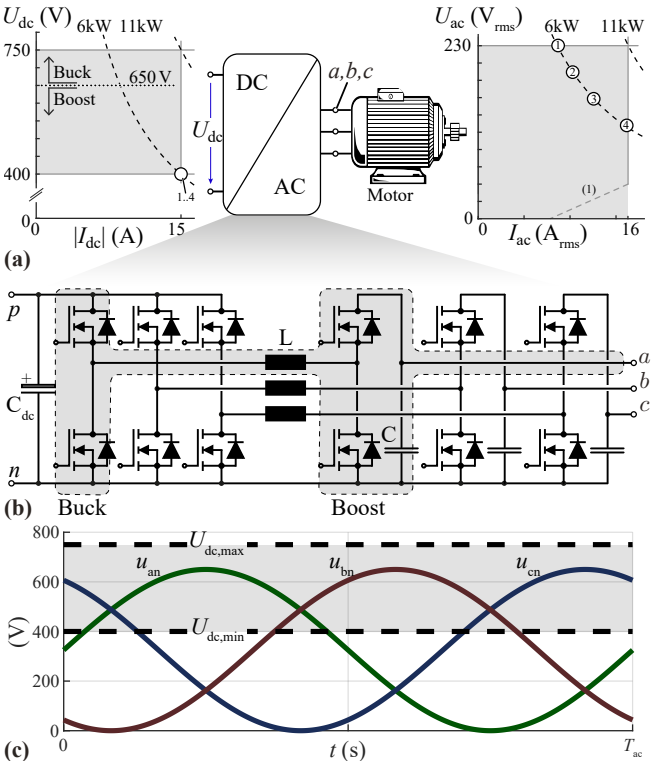

Fig. 2. **(a)** Illustration of the converter DC input and AC output voltage and current range specifications. **(b)** Circuit diagram of the Y-inverter with inherent sinusoidal output voltages; no additional DC/DC converter stage is required for buck-boost capability. **(c)** Y-inverter AC output voltages u_{an},u_{bn},u_{cn} with respect to the negative DC-link rail, as well as maximum and minimum DC input voltage U_{dc} of the converter operating range, clearly illustrating the need for buck-boost capability.
(1) Due to the limited semiconductor thermal capacitance the phase current is further restricted for low output frequencies below 50 Hz.

A. Operating Principle

The three-phase output voltages of the Y-inverter with respect to the negative DC-link rail u_{an},u_{bn},u_{cn} are strictly positive and shown in **Fig. 2c** for standard modulation with a constant offset voltage. This offset voltage is present in all three output phase voltages and hence represents a CM component $u_{CM} = (u_{an} + u_{bn} + u_{cn})/3$ which does not drive a current in an open star point three-phase motor (cf. **Fig. 2a**), and accordingly sinusoidal phase currents i_a,i_b,i_c can be realized [30]. Note that the CM offset voltage u_{CM} is only restricted by the requirement of strictly positive output voltages and can be set such that Discontinuous PWM (DPWM) [38] [30] is achieved as shown in **Fig. 3b**. There, the phase module with the lowest instantaneous output voltage is not switched during one third of the fundamental period T_{ac}, but remains clamped to the negative DC-link rail, reducing the semiconductor switching losses for unity power factor operation by at least one third. Aiming at ultra compact and highly efficient operation, the Y-inverter hardware prototype employed for the filter design analysis operates with DPWM.

Each of the three Y-inverter phase modules consists of a DC/DC buck-boost converter and is controlled independently. Therefore, the modulation is explained here for module a only (for more details refer to [30]), which is highlighted for boost and buck operation in **Fig. 3a**. The modulation strategy aims at single-stage HF energy conversion in each phase module:

- In boost operation (i.e. when $u_{an} > U_{dc}$, cf. **Fig. 3a.i**) the high-side switch of the buck stage is permanently turned on, while the output voltage is controlled by PWM operating the boost stage with a duty cycle d_{Bo}, where the low frequency inductor current $\langle i_L \rangle = i_a/d_{Bo}$ is elevated compared to the phase current (cf. **Fig. 3d**).
- In buck operation (i.e. when $u_{an} \leq U_{dc}$, cf. **Fig. 3a.ii**), the high-side switch of the boost stage is permanently turned on, and the buck stage is PWM operated with a duty cycle d_{Bu} in order to regulate the output voltage, where the low-frequency inductor current is equal to the sinusoidal phase current $\langle i_L \rangle = i_a$ (cf. **Fig. 3d**).

Duty cycles enabling mutually exclusive HF operation of the buck and boost stage can be derived using the instantaneous modulation depth $m(t) = u_{an}(t)/U_{dc}$ (the global modulation index is $M = 2 \cdot \hat{u}_{ac}/U_{dc}$) and are shown in **Fig. 3c**:

$$d_{Bu}(t) = \min(1, m(t)), \quad d_{Bo}(t) = \min(1, 1/m(t)) \quad (1)$$

The HF peak inductor current ripple $\Delta I_{L,pk}$ (cf. **Fig. 3d**) for buck and boost operation (assuming a negligible switching-frequency voltage ripple of the DC-link voltage and the phase output capacitor voltages) is then defined by

$$\Delta I_{L,pk} = \begin{cases} \frac{1}{2}\frac{d_{Bu}(1-d_{Bu})U_{dc}}{f_s L} & \text{(Buck)} \\ \frac{1}{2}\frac{d_{Bo}(1-d_{Bo})u_{an}}{f_s L} & \text{(Boost)} \end{cases}. \quad (2)$$

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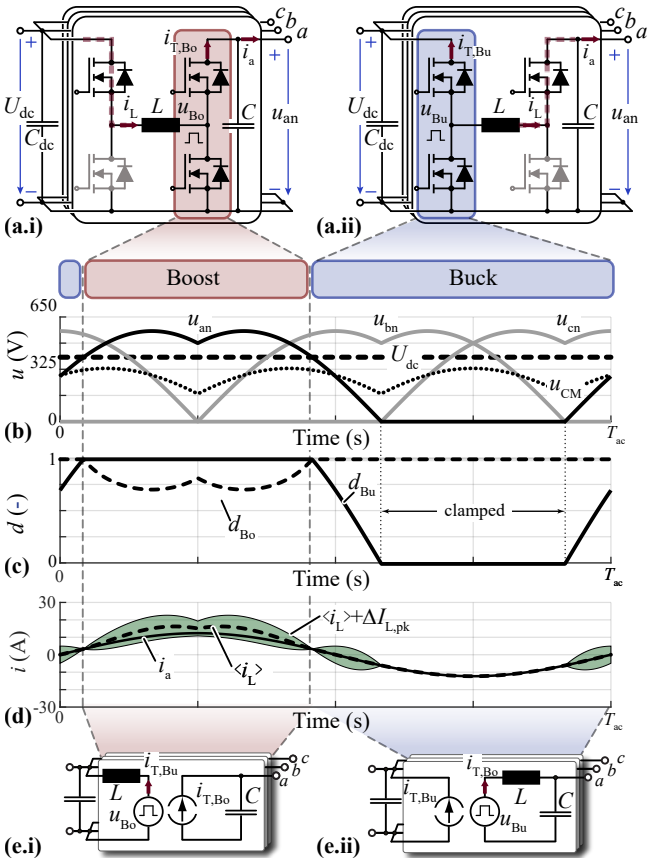

Fig. 3. Operation concept of the Y-inverter highlighted for phase module a in **(a.i)** boost operation (i.e. when $u_{\mathrm{an}} > U_{\mathrm{dc}}$) and **(a.ii)** buck operation (i.e. when $u_{\mathrm{an}} \leq U_{\mathrm{dc}}$). **(b)** DC-link voltage U_{dc} and phase output voltages with respect to the negative DC-link rail u_{an},u_{bn},u_{cn} comprising a time-varying CM offset voltage u_{CM} to enable Discontinuous PWM (DPWM). **(c)** Module a duty cycle of the buck stage d_{Bu} and of the boost stage d_{Bo}. **(d)** Relevant current waveforms of module a including the phase output current i_{a}, low-frequency inductor current $\langle i_{\mathrm{L}} \rangle$ and inductor current i_{L}. **(e)** Equivalent circuit for the time domain HF input and output voltage emissions of the Y-inverter phase module a depending on the operation mode.

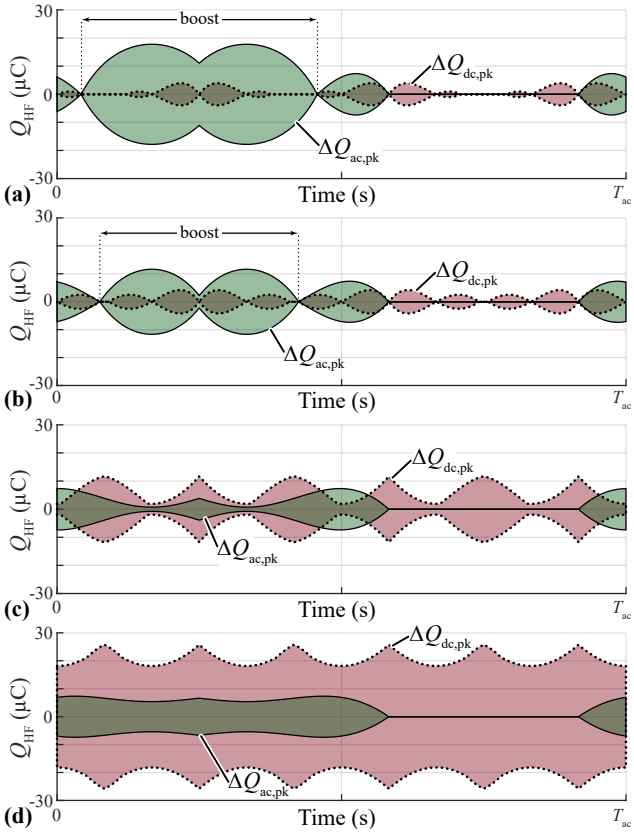

Fig. 4. Calculated peak HF charge variations $Q_{\mathrm{dc,pk}}$ of the DC input capacitor C_{dc} and $Q_{\mathrm{ac,pk}}$ of the AC output capacitor C of phase module a for the Y-inverter operating with DPWM and $U_{\mathrm{dc}} = 400\,\mathrm{V}$, where **(a)-(d)** correspond to the AC operating points ①-④ depicted in **Fig. 2a**. The peak HF voltage ripple on DC and AC capacitor is obtained by dividing $Q_{\mathrm{dc,pk}}$ and $Q_{\mathrm{ac,pk}}$ with its corresponding capacitance C_{dc} and C, respectively. Note that the peak AC charge variation $Q_{\mathrm{ac,pk}}$ depends solely on the operation of the considered phase module, whereas the peak DC charge variation $Q_{\mathrm{dc,pk}}$ depends on the operation of all three modules (cf. **Fig. 3e**).

B. HF Emissions in the Time Domain

As mentioned, the Y-inverter is a hybrid VSI/CSI topology. **Fig. 3e** shows the equivalent circuit for the HF input and output emissions of the Y-inverter phase module a for buck and boost operation. **Fig. 3e.i** shows module a in boost operation (i.e. corresponding to a CSI module [39]), where the switched current in the boost stage high-side semiconductor $i_{\mathrm{T,Bo}}$ is flowing towards the output capacitor C and the boost stage switch-node voltage u_{Bo} causes the HF current ripple on the inductor L which is clamped to the positive DC-link rail and $i_{\mathrm{T,Bu}} = i_{\mathrm{L}}$. **Fig. 3e.ii** highlights module a in buck operation (i.e. corresponding to a VSI module), where the switched current in the buck stage high-side semiconductor $i_{\mathrm{T,Bu}}$ is flowing from the DC-link, while the buck stage switch-node voltage u_{Bu} causes the HF current ripple on the inductor L which is clamped to the upper terminal of the output capacitor C and $i_{\mathrm{T,Bo}} = i_{\mathrm{L}}$. In **Fig. 4a-d**, the calculated peak HF charge variations $Q_{\mathrm{dc,pk}}$ of the DC input capacitor C_{dc} and $Q_{\mathrm{ac,pk}}$ of the Y-inverter phase module a AC output capacitor C are shown for the operation with DPWM, $U_{\mathrm{dc}} = 400\,\mathrm{V}$, and the AC operating points ①-④ depicted in **Fig. 2a** (i.e. with an output power of 6 kW). The switching frequency and buck-boost inductor value are set according to the prototype specifications (i.e. $f_{\mathrm{s}} = 100\,\mathrm{kHz}$, synchronous PWM carriers for all three phase modules and $L = 85\,\mu\mathrm{H}$). The peak HF voltage ripple on the DC capacitor and the AC capacitor is obtained by dividing $Q_{\mathrm{dc,pk}}$ and $Q_{\mathrm{ac,pk}}$ by the corresponding capacitance C_{dc} and C, respectively.

1) AC-side HF Charge Variation: The peak AC charge variation $Q_{\mathrm{ac,pk}}$ depends solely on the operation of the considered phase module (cf. **Fig. 3e**). Hence, assuming a purely sinusoidal phase output current without HF content, $\Delta Q_{\mathrm{ac,pk}}$ is given by the integral of the HF boost high-side semiconductor current $i_{\mathrm{T,Bo}}$:

$$\Delta Q_{\mathrm{ac,pk}} = \begin{cases} \frac{\Delta I_{\mathrm{L,pk}}}{8 f_{\mathrm{s}}} = \frac{d_{\mathrm{Bu}}(1-d_{\mathrm{Bu}})U_{\mathrm{dc}}}{16 f_{\mathrm{s}}^2 L} \leq 13.8\,\mu\mathrm{C} & \text{(Buck)} \\ \frac{1}{2}\frac{(1-d_{\mathrm{Bo}})i_{\mathrm{a}}}{f_{\mathrm{s}}} \leq 17.6\,\mu\mathrm{C} & \text{(Boost)} \end{cases} . \tag{3}$$

For buck operation $\Delta Q_{\mathrm{ac,pk}}$ scales with the peak value $\Delta I_{\mathrm{L,pk}}$ of the triangular inductor current ripple and hence is independent of the phase output current. For a given DC-link voltage, the maximum charge variation results for $d_{\mathrm{Bu}} = 0.5$

and is equal to $7.4\,\mu\mathrm{C}$ for $U_{\mathrm{dc}} = U_{\mathrm{dc,min}} = 400\,\mathrm{V}$ in **Fig. 4a-d**, where up to $13.8\,\mu\mathrm{C}$ result for $U_{\mathrm{dc}} = U_{\mathrm{dc,max}} = 750\,\mathrm{V}$.

In contrast, for boost operation, $\Delta Q_{\mathrm{ac,pk}}$ results due to the square-wave current $i_{\mathrm{T,bo}}$ (cf. **Fig. 3e.i**) and does not depend on the selected inductance value L but scales with the phase current i_{a} (i.e. is load dependent), where the maximum HF charge variation of $17.6\,\mu\mathrm{C}$ results for the maximum boosting effort and nominal power operation at $U_{\mathrm{dc}} = U_{\mathrm{dc,min}} = 400\,\mathrm{V}$ as shown in **Fig. 4a**. Note that (3) assumes that $\Delta I_{\mathrm{L,pk}}$ does not impact $\Delta Q_{\mathrm{ac,pk}}$ in boost operation (i.e. $\Delta I_{\mathrm{L,pk}} < \hat{I}_{\mathrm{ac}} \cdot (1/d_{\mathrm{Bo}} - 1)$), which holds for the prototype specifications and nominal power operation.

2) DC-side HF Charge Variation: In contrast to the AC-side emissions, the peak DC-side charge variation $Q_{\mathrm{dc,pk}}$ depends on the operation of all modules (cf. **Fig. 3e**), where the independent phase modules operate with $120°$ phase-shifted AC output voltages (cf. **Fig. 3b**) and hence the three modules may not work in the same mode (i.e. buck or boost operation) at a given point in time.

Since a phase module in buck operation causes a square-wave current $i_{\mathrm{T,Bu}}$, while a module in boost operation causes a continuous current $i_{\mathrm{T,Bu}}$ (with only a HF ripple $\Delta I_{\mathrm{L,pk}}$) flowing from the DC-link, buck operation can be assumed to dominate the worst case DC-side HF peak charge variation (which is consistent with the operating points considered in **Fig. 4**). Modelling the Y-inverter as a VSI for the DC emissions, $\Delta Q_{\mathrm{dc,pk}}$ can be conservatively approximated with [40]

$$\Delta Q_{\mathrm{dc,pk}} = \frac{1}{8} \frac{\hat{I}_{\mathrm{ac}}}{f_{\mathrm{s}}} \leq 28.3\,\mu\mathrm{C}, \tag{4}$$

i.e. by assuming a switching frequency square-wave current with $50\,\%$ duty cycle and an amplitude of half the phase peak current $0.5 \cdot \hat{I}_{\mathrm{ac}}$, where the maximum charge variation of $28.3\,\mu\mathrm{C}$ results for operation with the maximum AC output current $I_{\mathrm{ac,max}} = 16.3\,\mathrm{A_{rms}}$ (cf. **Fig. 2a**) as displayed in **Fig. 4d**.

III. Conducted EMI Analysis and Filter Design

In order to allow a systematic EMI filter design, (a) the noise emission measurement method needs to be specified, (b) the EMI noise emission equivalent circuit of the selected power converter topology needs to be derived and (c) the required filter attenuation needs to be determined based on the considered emission limits. Accordingly, possible measurement techniques and a setup to evaluate the power interface emissions are discussed in **Sec. III-A**, in **Sec. III-B** an EMI equivalent circuit for the Y-inverter is derived which is used in the filter design procedure in **Sec. III-C** to assess the required DM and CM HF attenuation to comply with the **IEC 61800-3** emission limits.

A. Measurement Method

1) DC Interface: Limiting the DC power interface emissions of basic drive modules (or the grid interface emissions of complete drive modules, cf. **Fig. 1)** is a standard task when designing a VSD and accordingly a vast amount of publications on filter design exists for both VSI and CSI drives [39] [41], where the emissions are recorded using a Line Impedance Stabilization Network (LISN) (referred to as Artificial Mains Network (AMN) in the **IEC 61800-3**). In this work, the DC interface emissions are also evaluated with a LISN serving several purposes: First, the LISN comprises a filter towards the DC source, such that only noise originating from the VSD is recorded. Second, the LISN represents at frequencies larger than $150\,\mathrm{kHz}$ and up to $30\,\mathrm{MHz}$ an almost constant source impedance of $50\,\Omega$ for the attached VSD, and third, the LISN allows to feed the VSD HF emissions into an EMI test receiver.

2) AC (Output) Interface: Employing predominantly shielded cables, the motor-side EMI emissions of a VSD were of less interest in literature (or only within the scope of HF motor stresses and losses). In case of a standard VSI where the unfiltered PWM pulses are directly applied to the motor cable, the resulting HF emissions are several orders of magnitude larger compared to rectifier applications and hence exceed the operation limits of any three-phase LISN [10]. Hence, the **IEC 61800-3** standard suggests the usage of a $1.5\,\mathrm{k}\Omega$ high-impedance voltage probe. (Alternatively, the effectiveness of the filter structure can be assessed by establishing a coupling between the motor cable and the mains input cable during the measurement of the grid interface EMI emissions.) However, there (in contrast to a measurement with a LISN) no clearly defined and constant (over frequency) load impedance exists on the VSD AC terminals, but the load impedance is highly dependent on the employed motor as well as the cable type, length and arrangement [42]. Further, the DM and CM emissions cannot be separated, complicating the filter debugging process in case the emission limits are not met. Alternatively, in [10] the conducted CM EMI emissions were evaluated separately using a capacitive voltage clamp. DM and CM noise splitting was enabled in [43] using a resistive voltage divider, and in [12] [44] based on four current measurements, where the dependency of the load impedance (and hence the measurement results) on the specific setup remains.

Here, the HF emission target given for the AC power interface for operation with unshielded motor cables lies within the range of grid emission limits and employing a three-phase AC LISN is therefore possible. As the LISN decouples the converter from the motor for the relevant frequencies $> 150\,\mathrm{kHz}$, the emission level can also be evaluated using a resistive three-phase load, greatly simplifying the EMI measurement process. Note that the LISN impedance ($\approx 50\,\Omega$ for $f > 150\,\mathrm{kHz}$) aims at approximating the grid impedance, and is not fully representative for the impedance of a motor [45] [46] [3]. Further, in [47]–[49] a large dependency of the EMI emissions on the cable and motor impedance was found for inverters without sine-filter. It is important to mention, that first, also the LISN does not fully represent the complex grid impedance [50] and it was found in [51], that the grid impedance in practice may vary in a wide range from $2\,\Omega$ to $450\,\Omega$ within the conducted emission band, where the selected $50\,\Omega$ LISN impedance is a compromise allowing for clear and reproducible measurement results. Second, when applying a sine-filter, the measured emissions are less dependent on the AC load impedance, compared to the case where the PWM pulses are directly applied to the motor cable [15] [39] [40].

Accordingly, for the filter design a HF impedance of $50\,\Omega$

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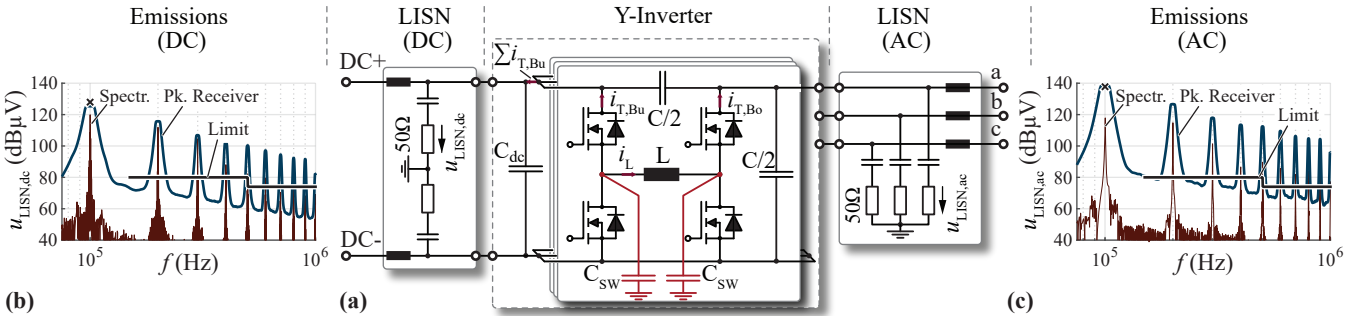

Fig. 5. **(a)** Main power circuit of the Y-inverter with a Line Impedance Stabilization Network (LISN) connected on the DC side and on the AC side. The parasitic switch-node capacitances are highlighted in red. The simulated voltage spectrum (red), the resulting peak detector signal (blue), as well as the **IEC 61800-3** C1 power interface emission limits (black) on DC side and on the AC side are shown in **(b)** and **(c)**, respectively.

(i.e. the presence of a LISN) is assumed, and in a first step in **Sec. V-A1** the experimental emission measurements are conducted employing a LISN and a resistive three-phase load. Then, in a second step in **Sec. V-A2** the emissions are evaluated with a high-impedance voltage probe when the converter is driving a motor, where the close matching of the results supports the selected measurement strategy.

B. Y-Inverter EMI Equivalent Circuit

The main power circuit of the Y-inverter attached to a (simplified) LISN on both input (DC) and output (AC) side is shown in **Fig. 5a**. There, the AC output capacitor of each phase module is equally referenced to the positive and negative DC-link rail in order to reduce the capacitance variation of the employed non-linear capacitors (as is discussed in more detail in **Sec. III-C**), and the parasitic switch-node capacitances C_{SW} are highlighted in red. The simulated emission spectrum and the peak detector signal [52] on the DC side and the AC side are also displayed in **Fig. 5b** and **Fig. 5c**, respectively, for the specifications of the existing Y-inverter hardware prototype (i.e. operation with DPWM, $f_{\mathrm{s}} = 100\,\mathrm{kHz}$, $C_{\mathrm{dc}} = 12\,\mu\mathrm{F}$, $L = 85\,\mu\mathrm{H}$ and $C = 1.3\,\mu\mathrm{F}$) and the operating point depicted in **Fig. 4a** ($U_{\mathrm{dc}} = 400\,\mathrm{V}$, $U_{\mathrm{ac}} = 230\,\mathrm{V_{rms}}$ (i.e. modulation index $M = 1.6$) and nominal output power of $6\,\mathrm{kW}$).

The knowledge of the relevant emission mechanisms of the employed power converter topology is crucial for the conducted EMI filter design process, where an abundance of publications on emission mechanisms for three-phase voltage source (i.e. boost-type) PWM rectifiers [53]–[56] and current source (i.e. buck-type) PWM rectifiers [57]–[59] exists (note that a bidirectional boost-type PWM rectifier corresponds to a buck-type PWM inverter and vice versa). As discussed in **Sec. II**, the Y-inverter is a hybrid VSI (i.e. buck-type) and CSI (i.e. boost-type) inverter topology, where the independent phase modules may work in different modes for a given point in time (cf. **Fig. 3**), and so far no EMI equivalent circuit has been presented for the Y-inverter in literature. A detailed derivation of the Y-inverter EMI equivalent circuit is performed in the following, allowing to quantify the conducted EMI emissions. This information is then used in **Sec. III-C** to determine the required DM and CM filter attenuation for DC and AC side.

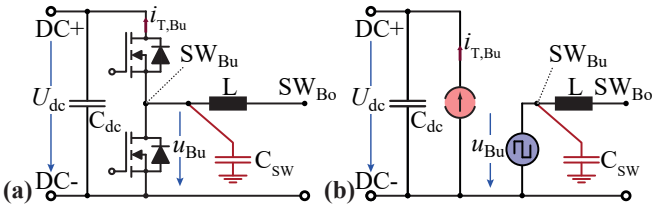

Fig. 6. **(a)** Single Y-inverter buck stage half-bridge, and **(b)** voltage and current source based equivalent circuit, where the half-bridge represents a current source ($i_{\mathrm{T,Bu}}$) towards the input terminals DC^+ and DC^-, and a voltage source (u_{Bu}) towards the switch-node terminal $\mathrm{SW_{Bu}}$ (with a parasitic capacitance C_{SW} to PE). This modelling approach is also applicable to the boost stage half-bridges.

As highlighted in **Fig. 6**, a single half-bridge of the Y-inverter buck stage represents a current source $i_{\mathrm{T,Bu}}$ towards the input terminals DC^+ and DC^-, and a voltage source u_{Bu} towards the switch-node terminal $\mathrm{SW_{Bu}}$ (a half-bridge of the boost stage can be modelled analogously).

Employing this modelling approach to the buck stage and boost stage half-bridges of the main Y-inverter power circuit from **Fig. 5a**, the equivalent circuit shown in **Fig. 7a** results. Further, **Fig. 7b** illustrates the power circuit from **Fig. 7a** with a separate DM/CM representation of the voltage and current sources: The buck stage voltages u_{Bu} of the modules a, b, c are split into a single CM voltage $u_{\mathrm{CM,Bu}} = 1/3 \sum u_{\mathrm{Bu}}$ and three DM voltages $u_{\mathrm{DM,Bu}}$ (e.g. $u_{\mathrm{DM,Bu,a}} = u_{\mathrm{Bu,a}} - u_{\mathrm{CM,Bu}}$, with $\sum u_{\mathrm{DM,Bu}} = 0$), and the same DM/CM splitting is also performed for the boost stage voltages u_{Bo}. Similarly, each of the boost stage currents $i_{\mathrm{T,Bo}}$ is represented by a CM current $i_{\mathrm{T,Bo,CM}} = 1/3 \sum i_{\mathrm{T,Bo}}$ and a parallel DM current $i_{\mathrm{T,Bo,DM}}$ (e.g. $i_{\mathrm{T,Bo,DM,a}} = i_{\mathrm{T,Bo,a}} - i_{\mathrm{T,Bo,CM}}$, with $\sum i_{\mathrm{DM}} = 0$). The DM/CM current splitting is also applied to the buck stage currents, where the buck DM currents cancel out in the DC-link rails and are hence irrelevant for the EMI emission formation. Accordingly, only the buck CM current $\sum i_{\mathrm{T,Bu}}$ is shown in the equivalent circuit in **Fig. 7b**, which allows now to identify the relevant EMI emission sources and paths.

1) DC-Side DM Emissions: **Fig. 8a** shows the DM part of the simulated DC-side voltage spectrum presented in **Fig. 5b**, and **Fig. 8b** illustrates the relevant emission sources and paths. There, the buck CM currents $\sum i_{\mathrm{T,Bu}}$ close through the DC-link capacitor and the $\mathrm{DC}^{+/-}$ referenced AC-side

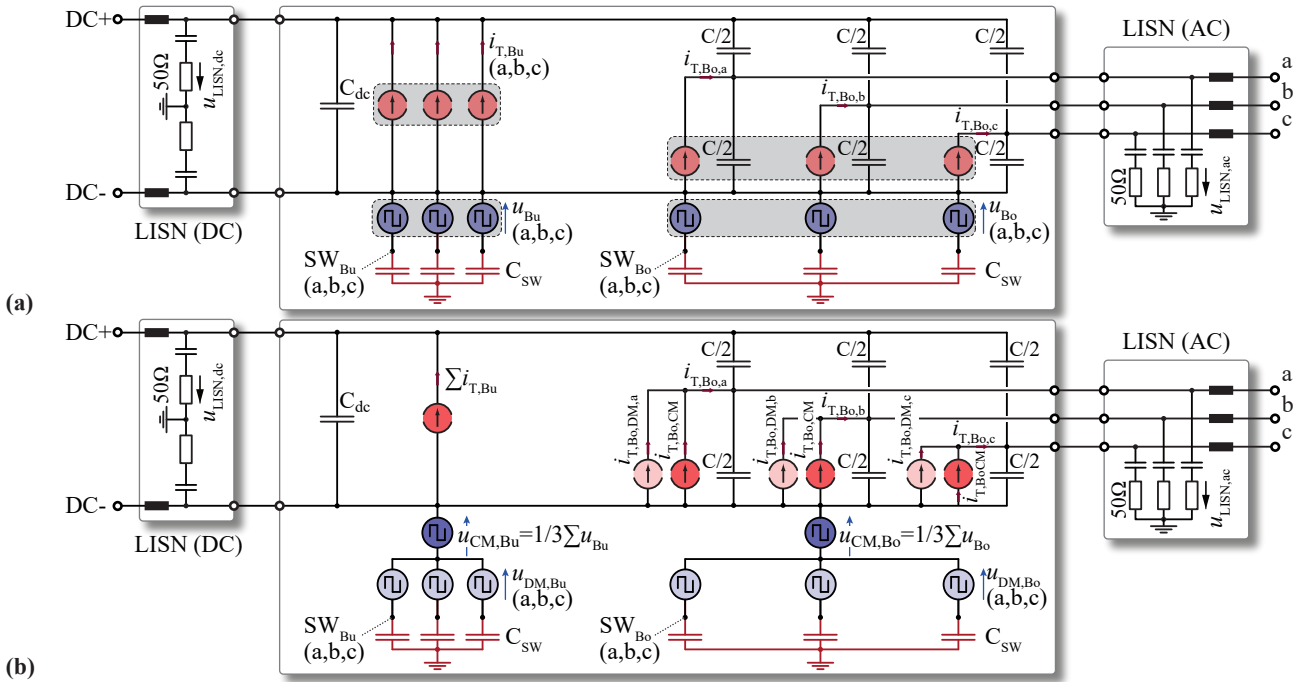

Fig. 7. (a) Y-inverter main power circuit from **Fig. 5a** with the buck stage and boost stage half-bridges modelled according to **Fig. 6**. **(b)** Y-inverter power circuit with a separate DM/CM representation of the voltage and current sources. Since the buck DM currents cancel out in the DC-link rails only the buck CM current $\sum i_{\mathrm{T,Bu}}$ is shown.

filter capacitors $3C/2$ (cf. **Fig. 7b**). Given the symmetric AC-side filter structure, the two nodes labelled with $(*)$ remain at the same potential, such that no current is flowing through the AC LISN and no DM/CM conversion takes place (the impact of the parasitic capacitances C_{SW} to PE is neglected here). Moreover, approximately half the boost CM current $1/2\sum i_{\mathrm{T,Bo}}$ closes through the positive DC-link rail if $C_{\mathrm{dc}} >> 3C/2$ (i.e. the voltage drop across C_{dc} can be neglected).

The currents closing through the DC-link capacitor cause a HF voltage variation $u_{\mathrm{C,dc,HF}}$ [60], which is also applied to the series connection of the two DC LISN resistors with opposite sign, hence representing a DM emission.

As the $50\,\Omega$ LISN resistors are large compared to a capacitor in the µF range for frequencies $\geq 150\,\mathrm{kHz}$, they do not impact the resulting HF voltage variation on DC-link capacitor C_{dc} (the same also holds for the output capacitors C). Further, the impedance of the $250\,\mathrm{nF}$ LISN capacitors is $< 10\%$ of the $50\,\Omega$ LISN resistors for frequencies $\geq 150\,\mathrm{kHz}$ and accordingly, the resulting DM emissions can be approximated with

$$\hat{u}_{\mathrm{DM,dc}} = \frac{1}{2}\hat{u}_{\mathrm{C,dc,HF}}, \tag{5}$$

i.e. the DM emissions reduced by $6\,\mathrm{dB}$ compared to $\hat{u}_{\mathrm{C,dc,HF}}$.

Fig. 8c presents a simplified DC-side DM equivalent circuit where the impact of $1/2\sum i_{\mathrm{T,Bo}}$ and the path through $3C/2$ on the DC-side DM emissions is neglected. As discussed in **Sec. II-B1**, the HF current fed into the positive DC-link rail $i_{\mathrm{T,Bu}}$ is a square-wave current in buck and solely a triangular HF current ripple in boost operation. Accordingly, buck operation is assumed to dominate the DC-side peak voltage ripple. For switching frequencies below the regulated conducted emissions band (i.e. $f_{\mathrm{s}} < 150\,\mathrm{kHz}$), this is further accentuated by the fact that the frequency spectrum of a triangular HF current $i_{\mathrm{T,Bu}}$ in boost operation shows a decay of approximately $-40\,\mathrm{dB/dec}$ (i.e. with $1/f^2$), whereas the spectrum of the square-wave current $i_{\mathrm{T,Bu}}$ in buck operation decays only with $-20\,\mathrm{dB/dec}$ (i.e. with $1/f$) [61]. In [61] it is further suggested to conservatively assign the resulting HF peak charge variation $\Delta Q_{\mathrm{dc,pk}}$ according to (4) to a single switching-frequency current component in the frequency domain, and assuming a decay of the current spectrum according to the current waveform (i.e. here $-20\,\mathrm{dB/dec}$ for a square-wave signal). Hence, the DC-side DM emission formation of the Y-inverter in the frequency domain can be approximated with

$$\hat{u}_{\mathrm{C,dc,HF}}(nf_{\mathrm{s}}) = \frac{1}{2\pi n f_{\mathrm{s}} C_{\mathrm{dc}}} \frac{2\pi f_{\mathrm{s}} \Delta Q_{\mathrm{dc,pk}}}{n}, \tag{6}$$

where $n = 1, 2, 3, \ldots$ represents the switching frequency harmonics at nf_{s}. The estimated peak DM emissions using (5) and (6) of $\hat{u}_{\mathrm{DM,dc}}(100\,\mathrm{kHz}) = 116\,\mathrm{dB\mu V}$ for the considered operation point are represented by a cross in **Fig. 8a** and nicely matches the simulated peak emissions, where $\hat{x}(f)[\mathrm{dB\mu V}] = 20\log_{10}(\frac{\hat{x}(f)}{1\,\mu\mathrm{V}\sqrt{2}})$.

2) AC-Side (Output) Emissions: As presented in **Fig. 7b**, both DM and CM components of the AC-side currents $i_{\mathrm{T,Bo}}$ are relevant for the emission formation. Again, the frequency spectrum of $i_{\mathrm{T,Bo}}$ can be approximated with the peak charge variation $\Delta Q_{\mathrm{ac,pk}}$ (3) as

$$\hat{i}_{\mathrm{T,Bo}}(nf_{\mathrm{s}}) = \frac{2\pi f_{\mathrm{s}} \Delta Q_{\mathrm{ac,pk}}}{n^k}, \tag{7}$$

where the current spectrum decays with $k = 2$ in buck operation (triangular current, decaying with $-40\,\mathrm{dB/dec}$) and $k = 1$ in boost operation (square-wave current, decaying with $-20\,\mathrm{dB/dec}$) [61]. For the given converter specifications, the maximum $\Delta Q_{\mathrm{ac,pk}}$ occurs in boost operation.

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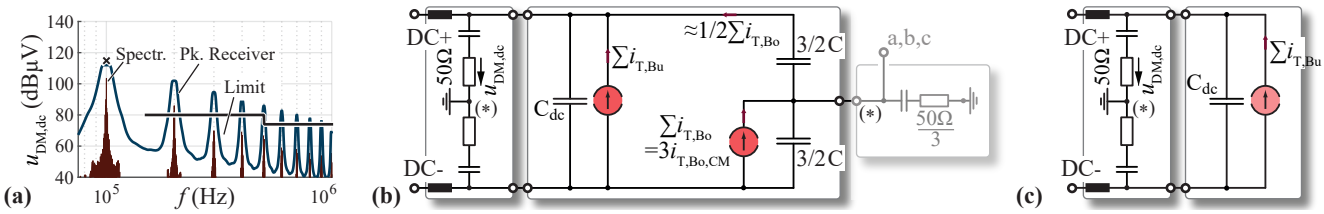

Fig. 8. DC-side DM emission equivalent circuit: **(a)** Simulated DM voltage spectrum, **(b)** relevant emission sources and paths, and **(c)** simplified equivalent circuit.

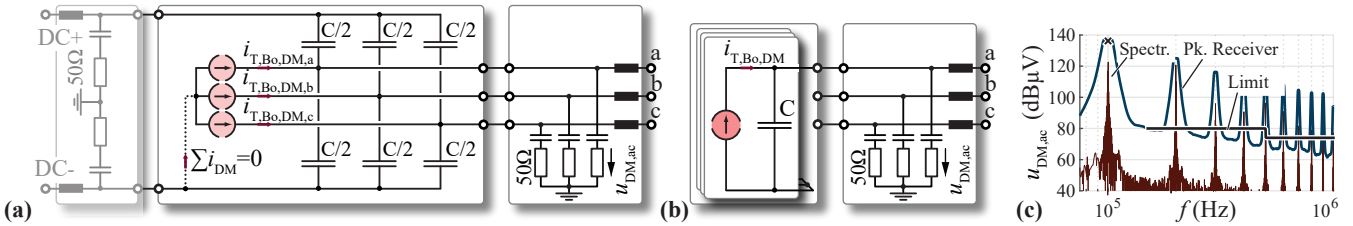

Fig. 9. AC-side DM emission equivalent circuit: **(a)** Relevant emission sources and paths, **(b)** simplified equivalent circuit, and **(c)** simulated DM voltage spectrum.

Hence the frequency spectrum of the DM and CM currents can be approximated assuming two modules in buck operation and with negligible HF currents (e.g. $\hat{i}_{\mathrm{T,Bo,b}} \approx \hat{i}_{\mathrm{T,Bo,c}} \approx 0$), while the remaining module in boost operation dominates the HF emissions (e.g. $i_{\mathrm{T,Bo,a}} = \hat{i}_{\mathrm{T,Bo}}$), such that

$$\hat{i}_{\mathrm{T,Bo,CM}}(nf_{\mathrm{s}}) = \frac{1}{3}\sum_{a,b,c}\hat{i}_{\mathrm{T,Bo}}(nf_{\mathrm{s}}) \approx \frac{1}{3}\hat{i}_{\mathrm{T,Bo}}(nf_{\mathrm{s}}), \quad (8)$$

$$\hat{i}_{\mathrm{T,Bo,DM}}(nf_{\mathrm{s}}) = \hat{i}_{\mathrm{T,Bo}} - \hat{i}_{\mathrm{T,Bo,CM}} \approx \frac{2}{3}\hat{i}_{\mathrm{T,Bo}}(nf_{\mathrm{s}}). \quad (9)$$

Hence, the DM and CM currents are reduced by ≈4 dB (i.e. scaled by 2/3) and ≈10 dB (i.e. scaled by 1/3), respectively, compared to $\hat{i}_{\mathrm{T,Bo}}$.

The boost stage DM currents $i_{\mathrm{T,Bo,DM}}$ shown in **Fig. 7b** can equally close through $C/2$ via DC^+ and DC^- and thereby cause HF DM voltages on the AC output terminals, as highlighted in **Fig. 9a**. Hence, the simplified AC-side DM equivalent circuit in **Fig. 9b** comprises per phase module a total capacitance C and (neglecting the impact of the LISN on the HF voltage variation on C) the AC-side DM emissions are defined by

$$\hat{u}_{\mathrm{DM,ac}}(nf_{\mathrm{s}}) = \hat{u}_{\mathrm{C,HF,DM}}(nf_{\mathrm{s}}) = \frac{\hat{i}_{\mathrm{T,Bo,DM}}(nf_{\mathrm{s}})}{2\pi nf_{\mathrm{s}}C}. \quad (10)$$

The estimated peak DM emissions $\hat{u}_{\mathrm{DM,ac}}(100\,\mathrm{kHz}) = 136\,\mathrm{dB\mu V}$ for the considered operation point are represented by a cross in **Fig. 9c** and nicely match the simulated peak emissions. Note, that for identical parasitic capacitances C_{SW} in all three modules (cf. **Fig. 7b**), the buck stage $u_{\mathrm{DM,Bu}}$ and boost stage DM voltages $u_{\mathrm{DM,Bo}}$ cause no current through the DC- and AC-side LISN resistors and are therefore not shown in **Fig. 9a** and **Fig. 9b**.

Finally, the relevant emission sources and paths for CM emissions is shown in **Fig. 10a**. With $C_{\mathrm{dc}} >> 3C/2$, approximately half the boost stage CM current $1/2\sum i_{\mathrm{T,Bo}}$ returns via the positive DC-link rail (cf. **Fig. 7b**), and hence the boost CM current path comprises a total capacitance $3C$ (the positive and negative DC-link rails are represented here as a single rail $\mathrm{DC}^{+/-}$). Further, the buck $u_{\mathrm{CM,Bu}}$ and boost stage CM voltage $u_{\mathrm{CM,Bo}}$ connect to PE via $3 \cdot C_{\mathrm{SW}}$.

Here, in a first step, the emissions due to the CM current $\sum i_{\mathrm{T,Bo}}$ are assessed, and the emissions resulting due to the buck stage CM voltage $u_{\mathrm{CM,Bu}}$ as well as the boost stage CM voltage $u_{\mathrm{CM,Bo}}$ are discussed in the next subsection. The AC capacitor $3C$ CM HF voltage spectrum $\hat{u}_{\mathrm{C,HF,CM}}$ is defined by $\sum \hat{i}_{\mathrm{T,Bo}} = 3\hat{i}_{\mathrm{T,Bo,CM}}$ (8)

$$\hat{u}_{\mathrm{C,HF,CM}}(nf_{\mathrm{s}}) = \frac{\sum \hat{i}_{\mathrm{T,Bo}}(nf_{\mathrm{s}})}{2\pi nf_{\mathrm{s}}3C} = \frac{\hat{i}_{\mathrm{T,Bo,CM}}(nf_{\mathrm{s}})}{2\pi nf_{\mathrm{s}}C}, \quad (11)$$

resulting to $\hat{u}_{\mathrm{C,HF,CM}}(100\,\mathrm{kHz}) = 130\,\mathrm{dB\mu V}$ for the considered operation point. This voltage is applied to the series connection of the AC and DC LISN forming a voltage divider (cf. dotted line in **Fig. 10a**) with

$$\hat{u}_{\mathrm{CM,dc}}(nf_{\mathrm{s}}) = 0.6 \cdot \hat{u}_{\mathrm{C,HF,CM}}(nf_{\mathrm{s}}) \quad (12)$$

$$\hat{u}_{\mathrm{CM,ac}}(nf_{\mathrm{s}}) = 0.4 \cdot \hat{u}_{\mathrm{C,HF,CM}}(nf_{\mathrm{s}}). \quad (13)$$

Hence, the recorded LISN CM voltages $\hat{u}_{\mathrm{CM,dc}}$ and $\hat{u}_{\mathrm{CM,ac}}$ are reduced by ≈4 dB and ≈8 dB, respectively, compared to $\hat{u}_{\mathrm{C,HF,CM}}$ and the expected CM emissions are given by $\hat{u}_{\mathrm{CM,dc}}(100\,\mathrm{kHz}) = 126\,\mathrm{dB\mu V}$ (cf. **Fig. 10b**) and $\hat{u}_{\mathrm{CM,ac}}(100\,\mathrm{kHz}) = 123\,\mathrm{dB\mu V}$ (cf. **Fig. 10c**), again matching the simulated emissions.

3) Additional Common Mode Emissions: The Y-inverter emission mechanisms discussed so far can be considered modulation imposed, as they can easily be calculated for given converter specifications and operating point using the equations from **Sec. II**. Further, since the impedance of capacitors in the µF range above 100 kHz is much smaller than the 50 Ω LISN resistors, the filter capacitors of the Y-inverter depicted in **Fig. 5a** are not substantially loaded when attaching a LISN and hence the recorded emission spectrum should not change notably if e.g. the emissions are measured on a resistance higher than 50 Ω or if the measurement is conducted with a high-impedance voltage probe (cf. **Fig. 17b**) when the Y-inverter is driving a motor.

An additional emission path not yet discussed originates

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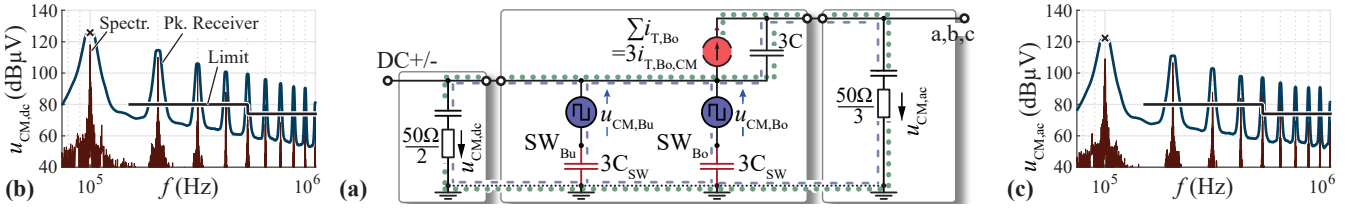

Fig. 10. **(a)** CM equivalent circuit of the Y-inverter and simulated voltage spectrum on **(b)** DC side and **(c)** AC side.

from the parasitic capacitances C_{SW} of the switch nodes of buck and boost stages to PE (cf. **Fig. 7b**, **Fig. 10a**) existing in a practical converter realization. The total parasitic capacitance $6 \cdot C_{\mathrm{SW}}$ provides a current path for the total HF CM switch-node voltage $1/2(u_{\mathrm{Bu,CM}} + u_{\mathrm{Bo,CM}}) = 1/6 \sum (u_{\mathrm{Bu}} + u_{\mathrm{Bo}})$ to PE (dashed line in **Fig. 10a**), where AC and DC LISN form a parallel return path to the DC-link rail DC$^{+/-}$ (i.e. DC and AC side show the same emission level). As the capacitance C_{SW} is not part of the Y-inverter main power circuit, this additional source of emissions is referred to as parasitically imposed.

The CM component of the switch-node voltages in the frequency domain can be approximated conservatively with

$$1/6 \sum (u_{\mathrm{Bu}} + u_{\mathrm{Bo}})(nf_{\mathrm{s}}) \approx \frac{2}{n\pi} \frac{k_{\mathrm{a}}}{6} u_{\mathrm{SW,max}}, \qquad (14)$$

by assuming a square-wave switched voltage with an amplitude of $1/2 \cdot u_{\mathrm{SW,max}}$ and a duty cycle of 50 %, with $u_{\mathrm{SW,max}} = \max(U_{\mathrm{dc}}, 2\hat{U}_{\mathrm{ac}})$ the maximum switched voltage for a given operation point, and $k_{\mathrm{a}}/6$ as scaling factor representing the number of HF operated half-bridges relative to the total number of six half-bridges (i.e. $k_{\mathrm{a}} = 3$ for PWM and $k_{\mathrm{a}} = 2$ for DPWM). The recorded CM voltage on DC and AC LISN due to the switch-node parasitic capacitance C_{SW} can be approximated with

$$\hat{u}_{\mathrm{CM,par}}(nf_{\mathrm{s}}) \approx \frac{2}{n\pi} \frac{k_{\mathrm{a}}}{6} \frac{u_{\mathrm{SW,max}}}{Z_{6\cdot\mathrm{C,SW}}(nf_{\mathrm{s}})} R_{\mathrm{DC,AC}}, \qquad (15)$$

where $R_{\mathrm{DC,AC}} = 10\,\Omega$ is the parallel resistance of DC and AC LISN, and $Z_{6\cdot\mathrm{C,SW}}$ the impedance of the total parasitic capacitance $6 \cdot C_{\mathrm{SW}}$. The parasitic switch-node capacitance C_{SW} is typically very small and a value of $C_{\mathrm{SW}} = 20\,\mathrm{pF}$ was measured for the converter prototype with floating heat sinks. Hence, for the considered operating point an emission level of $\hat{u}_{\mathrm{CM,par}}(100\,\mathrm{kHz}) = 99\,\mathrm{dB\mu V}$ results on DC and AC side of the Y-inverter, which is more than 20 dB below the modulation imposed CM emissions, thus in this case the impact on the overall CM emissions shown in **Fig. 10b** and **Fig. 10c** is small.

However, it is important to highlight that $|Z_{6\cdot\mathrm{C,SW}}(100\,\mathrm{kHz})| = 13\,\mathrm{k\Omega} >> R_{\mathrm{DC,AC}}$, and hence $Z_{6\cdot\mathrm{C,SW}}$ dominates the total impedance of the current path represented by the dashed line in **Fig. 10a** up to frequencies in the range of 10 MHz. Hence, the parasitically imposed emissions $\hat{u}_{\mathrm{CM,par}}$ according to (15) scale approximately linearly with $R_{\mathrm{DC,AC}}$ and are (in contrast to the modulation imposed emissions) not independent of the source and load impedance. Further, $\hat{u}_{\mathrm{CM,par}}$ remains constant over frequency (as long as $|Z_{6\cdot\mathrm{C,SW}}(f)| >> R_{\mathrm{DC,AC}}$) as both the emission source (i.e. the switched CM voltage) and the impedance of the parasitic capacitance decay linearly with frequency, and $\hat{u}_{\mathrm{CM,par}}$ might become relevant for higher frequencies. Last, note that a DC-link referenced filter for combined DM/CM attenuation is not effective for the parasitically imposed emissions, as the filter inductors are bypassed via the filter capacitors providing a low impedance return path to the DC-link rails (cf. **Fig. 10a**). Accordingly, (at least) one filter stage on the DC and on the AC side needs to separately attenuate CM and DM noise, where the CM filter comprises Y2 safety capacitors to PE, such that the impact of the source and load impedance on the recorded emissions on DC and AC side is again minimized.

TABLE I
WORST CASE EMISSIONS AND REQUIRED ATTENUATIONS

	$\hat{u}(100\,\mathrm{kHz})[dB\mu V]$	$\hat{u}(200\,\mathrm{kHz})[dB\mu V]$	$A_{\mathrm{req}}[dB]$
DC_{DM}	121	109	**39**
DC_{CM}	126	114	**44**
AC_{DM}	136	124	**54**
AC_{CM}	123	111	**41**
par_{CM}	102	102	**38**

In summary, the overall expected emission level (given by the sum of the discussed emission mechanisms) of the DC LISN $\hat{u}_{\mathrm{LISN,dc}}(100\,\mathrm{kHz}) = 128\,\mathrm{dB\mu V}$ and the AC LISN $\hat{u}_{\mathrm{LISN,ac}}(100\,\mathrm{kHz}) = 138\,\mathrm{dB\mu V}$ is shown in **Fig. 5b** and **Fig. 5c**, respectively, again closely matching the simulated peak emissions.

C. EMI Filter Design

As defined, the goal of the filter design is the compliance with the **IEC-61800-3** conducted power interface emission limits for residential applications with long unshielded cables (cf. **Fig. 1**). Hence, for a DC-fed VSD the emissions on the DC and on the AC side of the Y-inverter have to be attenuated below $80\,\mathrm{dB\mu V}$ (i.e. $10\,\mathrm{mV}$) from $150\,\mathrm{kHz}$ to $500\,\mathrm{kHz}$, and below $74\,\mathrm{dB\mu V}$ from $500\,\mathrm{kHz}$ to $30\,\mathrm{MHz}$.

With the emission mechanisms and equations for a simplified emission estimation derived and verified by means of a circuit simulation in **Sec. III-B**, the goal of this section is to assess the minimum required filter attenuation to comply with the above summarized power interface emission limits and to find a suitable filter structure.

The required attenuation is defined by the design frequency $f_{\mathrm{D}} = n_{\mathrm{D}} f_{\mathrm{s}}$ [61] given by the first regulated switching frequency harmonic

$$n_{\mathrm{D}} = ceil(\frac{150\,\mathrm{kHz}}{f_{\mathrm{s}}}). \qquad (16)$$

Here, the design frequency results to $f_{\mathrm{D}} = 200\,\mathrm{kHz}$ (i.e. the second switching frequency harmonic). The filter design

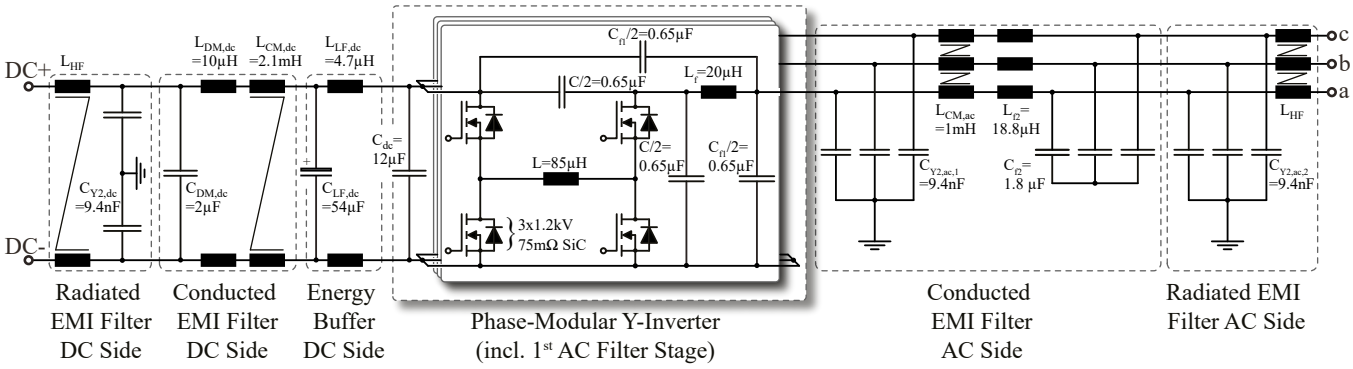

Fig. 11. Schematic circuit with the main power components of the Y-inverter prototype and the EMI filter on DC and AC side. Details on the employed components are given in **Table II**.

TABLE II
Y-INVERTER VSD PROTOTYPE MAIN POWER COMPONENTS.

Component	Nom. value	Details
Semiconductors	$f_\mathrm{s} = 100\,\mathrm{kHz}$	3 x Cree SiC C3M0075120J 75 mΩ 1.2 kV,
AC inductors	$L = 85\,\mu\mathrm{H}$	2 x TDK EELP 43 Ferrite Core (N97), 5.4 mm air gap, 20 turns of 625 x 71 µm litz wire
	$L_\mathrm{f1} = 20\,\mu\mathrm{H}$	2 x Würth Elektronik WE-HCI 10 µH, 21 A, 3.4 mΩ
	$L_\mathrm{f2} = 18.8\,\mu\mathrm{H}$	4 x Bourns Inc. SRP1265C-4R7M 4.7 µH, 20 A, 9.5 mΩ
	$L_\mathrm{CM,ac} = 1\,\mathrm{mH}$	(at 200 kHz) VAC T60006-L2030-W423 (VITROPERM 500 F), 10 turns of 1.4 mm solid wire
DC inductors	$L_\mathrm{LF,dc} = 4.7\,\mu\mathrm{H}$	1 x Vishay IHLP6767DZER4R7M01 4.7 µH, 27 A, 11.2 mΩ
	$L_\mathrm{CM,dc} = 2.1\,\mathrm{mH}$	(at 200 kHz) VAC T60006-L2025-W380 (VITROPERM 500 F), 13 turns of 1 mm solid wire
	$L_\mathrm{DM,dc} = 10\,\mu\mathrm{H}$	1 x Vishay IHLP6767GZER100M01 10 µH, 25 A, 12 mΩ
HF inductors	$L_\mathrm{HF} = 340\,\mathrm{nH}$	(at 30 MHz) Fair-Rite 1 x 5952020801, 2 x 5952020601, NiZn (Fair-Rite 52) plug-on core
DC capacitors	$C_\mathrm{dc,LF} = 48\,\mu\mathrm{F}$	12 x Chemi-Con ALUM 18 µF, 450 V (2 in series)
	$C_\mathrm{dc,HF} = 12\,\mu\mathrm{F}$	48 x TDK Ceralink 0.25 µF, 900 V
	$C_\mathrm{DM,dc} = 2\,\mu\mathrm{F}$	8 x TDK Ceralink 0.25 µF, 900 V
AC capacitors	$C = C_\mathrm{f1} = 1.3\,\mu\mathrm{F}$	6 x Syfer X7R, 0.47 µF, 1 kV referenced evenly to positive and negative DC-link rails (C and C_f1 represent the min. capacitance values for the considered converter specifications)
	$C_\mathrm{f2} = 1.8\,\mu\mathrm{F}$	8 x KEMET C0G, 0.22 µF, 500 V
PE capacitors	$C_\mathrm{Y2} = 9.4\,\mathrm{nF}$	2 x Johanson-Dielectrics Y2 safety certified MLCC, X7R 4.7 nF, 250 V
Controller	-	TMS320C2834X

target is to attenuate the DM and CM noise below the emission limit of 80 dBµV considering an additional margin of 10 dB (to account for component tolerances) and 6 dB (to account for the worst case summation of DM and CM noise) to

$$\hat{u}_\mathrm{max}(f_\mathrm{D}) = 80\,\mathrm{dB\mu V} - 10\,\mathrm{dB} - 6\,\mathrm{dB} = 64\,\mathrm{dB\mu V}. \quad (17)$$

The worst case emission levels on DC and AC side for $f_\mathrm{s} = 100\,\mathrm{kHz}$ and $f_\mathrm{D} = 200\,\mathrm{kHz}$, as well as the corresponding required filter attenuations A_req according to (17) are summarized in **Table I**. There, the worst case DC-side DM noise (DC_DM) is given for operation with the maximum AC phase current of $I_\mathrm{ac,max} = 16.3\,\mathrm{A_{rms}}$ and unity power factor operation. The remaining modulation imposed worst case emissions on the AC side ($AC_\mathrm{DM}, AC_\mathrm{CM}$) and on the DC side ($DC_\mathrm{CM}$) result for the operating point considered in **Sec. III-B** with maximum boosting effort and nominal output power, while the maximum parasitically imposed emissions (par_CM) result for operation with the maximum DC-link voltage $U_\mathrm{dc} = U_\mathrm{dc,max} = 750\,\mathrm{V}$ (cf. **Fig. 2a**).

In the following, a suitable filter structure for DC and AC side of the Y-inverter prototype is derived, where the HF attenuation A of an m stage LC-filter can be approximated with [62]

$$A(f) = \frac{1}{(2\pi f)^{2m}} \frac{1}{\prod_{v=1}^{m} C_\mathrm{f,v} \prod_{v=1}^{m} L_\mathrm{f,v}}\,, \quad (18)$$

where a minimum filter volume results for a realization of the stages with identical component values [63].

1) AC-Side Filter: Employing ceramic capacitors allows for a highly compact filter realization [64], where the sum of the employed capacitance values located on the AC side of the Y-inverter are limited in order to avoid excessive conduction losses due to the capacitive reactive currents. Here, a reactive current limit of 20 % nominal AC output current for operation with 6 kW output power was selected, resulting in

$$\sum C \leq \frac{20\,\%\, I_\mathrm{ac,nom}}{2\pi f_\mathrm{ac,max} U_\mathrm{ac,max}} \approx 6\,\mu\mathrm{F}. \quad (19)$$

To achieve the desired DM attenuation of ≈60 dB (cf. **Table I**) the AC filter is realized as a two-stage LC filter (i.e. with 30 dB attenuation each), where the first stage is DC-link referenced to simultaneously attenuate DM and CM noise (cf. **Fig. 11**). There, C_f1 is realized as the output filter capacitor C of the existing prototype by referenc-

ing three $1\,\mathrm{kV}$ $0.47\,\mu\mathrm{F}$ X7R capacitors (cf. **Table II**) to the positive and negative DC-link rail, such that the non-linear capacitance variation over the fundamental period is reduced [65] [26] and a minimum capacitance value of $min(C) = min(C_{\mathrm{f1}}) = 1.3\,\mu\mathrm{F}$ results. To achieve the desired attenuation of $30\,\mathrm{dB}$ per stage $L_{\mathrm{f1}} = 20\,\mu\mathrm{H}$ is selected according to (18). Note that (in contrast to the buck-boost inductor L) the HF losses in subsequent filter inductors are very small, and hence a compact realization with commercial flat-wire inductors is possible.

As discussed in **Sec. III-B**, DM and CM noise are attenuated separately in the second filter stage, where linear $500\,\mathrm{V}$ C0G ceramic capacitors are employed for the realization of the DM $C_{\mathrm{f2}} = 1.8\,\mu\mathrm{F}$, in order to avoid the high capacitance variation and losses resulting when using X7R capacitors in an open star point DM filter [64]. The second filter stage DM inductance is also set to $L_{\mathrm{f2}} = 18.8\,\mu\mathrm{H}$, where a different commercial inductor is selected to achieve a good form factor (cf. **Table II**).

The second stage CM filter consists of a CM choke and Y2 safety capacitors to PE, where the latter are subject to a ground current limit given by the usage of Residual-Current Devices (RCDs): As the Y-inverter prototype employs DPWM, the low-frequency AC terminal CM voltage u_{CM} (cf. **Fig. 3b**) is time varying and contains frequency components at multiples of the triple fundamental frequency $3 \cdot f_{\mathrm{ac}}$. Neglecting the impedance of the inductive components, u_{CM} is applied to the series connection of the PE capacitances of DC and AC side (cf. **Fig. 10a**), causing a low-frequency PE current I_{PE}. Assuming as a worst case a very large PE capacitance of the DC-bus, I_{PE} is only limited by the total AC-side PE capacitance $\sum C_{\mathrm{PE}}$, and the (RMS) PE current results equal to

$$\begin{aligned} I_{\mathrm{PE}} &= \sqrt{\frac{1}{T_{\mathrm{ac}}} \int_0^{T_{\mathrm{ac}}} (\frac{\mathrm{d}\, u_{\mathrm{CM}}(t)}{\mathrm{d}\, t} \sum C_{\mathrm{PE}})^2 \,\mathrm{d}\, t} \\ &= \sqrt{\frac{1}{2} - \frac{3\sqrt{3}}{8\pi}}\; 2\pi f_{\mathrm{ac}} \hat{U}_{\mathrm{ac}} \sum C_{\mathrm{PE}} \ . \end{aligned} \tag{20}$$

The goal is to design the CM filter such that $I_{\mathrm{PE}} < 15\,\mathrm{mA_{rms}}$ (i.e. $50\,\%$ of a $30\,\mathrm{mA_{rms}}$ RCD) for the maximum AC frequency $f_{\mathrm{ac}} = f_{\mathrm{ac,max}} = 200\,\mathrm{Hz}$ and voltage $\hat{U}_{\mathrm{ac}} = \hat{U}_{\mathrm{ac,max}} = 325\,\mathrm{V_{pk}}$. Note, that motor and motor cable also contribute to $\sum C_{\mathrm{PE}}$, where here a motor PE capacitance up to $10\,\mathrm{nF}$ [3], and a motor cable PE capacitance up to $15\,\mathrm{nF}$ (corresponding to an unshielded cable with $150\,\mathrm{pF/m}$ of $100\,\mathrm{m}$ length) is considered for the filter design, and hence according to (20) up to $60\,\mathrm{nF}$ PE capacitance (i.e. $20\,\mathrm{nF}$ per phase module) can be employed.

It is important to mention that the Y-inverter prototype employing DPWM may not be attached simultaneously to a LISN on DC and AC side (as illustrated in **Fig. 5a**) during the emission evaluation in **Sec. V-A**: A LISN comprises a total PE capacitance in the range of $10\,\mu\mathrm{F}$ (due to the line side filter), which also contributes to $\sum C_{\mathrm{PE}}$ and causing according to (20) massive PE currents $> 1\,\mathrm{A}$, leading hence to saturation of the employed CM chokes. Accordingly, in a practical setup the AC LISN is only connected when measuring the AC-side emissions, and the DC LISN only when measuring the DC-side emissions.

This maximum PE capacitance of $20\,\mathrm{nF}$ is equally distributed on both side of the AC-side CM choke $L_{\mathrm{CM,ac}}$ (cf. **Fig. 11**): $C_{\mathrm{Y2,ac,1}} = 10\,\mathrm{nF}$ is located in front of the CM choke $L_{\mathrm{CM,ac}}$ to provide a low impedance return path to the DC-link rails for parasitically imposed emissions (cf. **Fig. 10a**), and $C_{\mathrm{Y2,ac,2}} = 10\,\mathrm{nF}$ is located after the CM choke $L_{\mathrm{CM,ac}}$ to form an LC filter for modulation imposed CM emissions, where $C_{\mathrm{Y2,ac,2}}$ is also part of the radiated emissions filter discussed in **Sec. IV-B**. Note that the low impedance return path for parasitically imposed emissions is typically formed by connecting PE capacitors to the DC-link rails, which were in case of the considered converter prototype not directly accessible due to the integrated DC energy buffer (cf. **Fig. 11**). The required filter attenuation of $38\,\mathrm{dB}$ (cf. **Table I**) for parasitically imposed CM emissions is achieved according to (18) by employing a CM choke with $L_{\mathrm{CM,ac}} = 1\,\mathrm{mH}$, which is realized with a high permeability nanocrystalline magnetic core (cf. **Table II**, note that the core shows a frequency dependent permeability, where $L_{\mathrm{CM,ac}} = 1\,\mathrm{mH}$ results for the design frequency $f_{\mathrm{D}} = 200\,\mathrm{kHz}$).

2) DC-Side Filter: As mentioned, the converter prototype comprises an electrolytic capacitor energy buffer $C_{\mathrm{LF,dc}} = 54\,\mu\mathrm{F}$ to stabilize the DC-link voltage in case of variations of the current supplied by an upstream converter, where two small inductors $L_{\mathrm{LF,dc}} = 5\,\mu\mathrm{H}$ limit the switching frequency currents in $C_{\mathrm{LF,dc}}$ to avoid excessive capacitor losses (cf. **Fig. 11**). Note that according to (18), the DM filter formed by $C_{\mathrm{LF,dc}}$ and $2 \cdot L_{\mathrm{LF,dc}}$ provides an attenuation of close to $60\,\mathrm{dB}$, exceeding the DC-side DM filter demand according to **Table I**. However, due to the high series resistance and low self-resonance frequency of electrolytic capacitors, the attenuation provided by the DC energy buffer is not considered in the filter design, and an additional filter stage is added with $2 \cdot L_{\mathrm{DM,dc}} = 10\,\mu\mathrm{H}$ and $C_{\mathrm{DM,dc}} = 2\,\mu\mathrm{F}$, where $C_{\mathrm{DM,dc}}$ is realized with the same CeraLink ceramic capacitors employed in $C_{\mathrm{dc,HF}}$ such that a high self-resonance frequency results. As found in **Sec. V-A**, the electrolytic capacitors employed in $C_{\mathrm{LF,dc}}$ still provide some attenuation above $150\,\mathrm{kHz}$ yielding a very low emission level at the design frequency $f_{\mathrm{D}} = 200\,\mathrm{kHz}$ with a margin above $20\,\mathrm{dB}$, and the HF DC DM filter could eventually employ lower component values.

Finally, the DC-side CM filter consists of a CM choke $L_{\mathrm{CM,dc}} = 2.1\,\mathrm{mH}$ (consisting of a high permeability nanocrystalline magnetic core, cf. **Table II**) forming a second order CL filter for parasitically imposed emissions with $C_{\mathrm{Y2,ac,1}}$ and providing a series attenuation with the DC LISN for modulation imposed emissions.

IV. Radiated EMI Analysis and Filter Design

In contrast to the conducted emission limits applying to each power interface individually, the radiated emission limits concern the overall converter system and have to be complied with for the complete VSD independently of the power interface realization, where employing shielded cables reduces radiated emissions [13]. Again, the measurement method for the experimental verification is discussed in **Sec. IV-A** and subsequently the required attenuation and

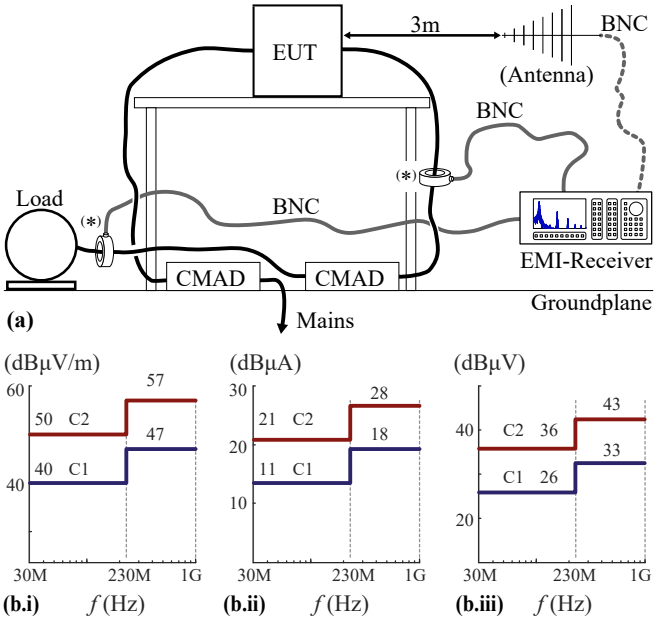

Fig. 12. **(a)** Illustration of the measurement setup for radiated emissions according to **IEC 61800-3** [4], where all cables connected to the Equipment Under Test (EUT) are individually HF terminated with a Common Mode Absorption Device (CMAD) and the emission level is sensed with an antenna.
(*) Alternatively, the radiated emissions can be calculated based on a measurement with a high-bandwidth current probe (e.g. F-33-1) [66]. **(b.i) IEC 61800-3** E-field limits for a measurement distance of $3\,\mathrm{m}$, translated into a **(b.ii)** CM current and **(b.iii)** test receiver voltage reading limit for a current probe with $6.3\,\Omega$ transfer impedance.

realization of the radiated EMI filter is derived in **Sec. IV-B**.

A. Measurement Method (Radiated EMI)

The test setup for the radiated EMI emission measurement according to **IEC 61800-3** is illustrated in **Fig. 12a**, where an electromagnetically quiet environment (i.e. an Open-Area Test Site (OATS) or a Semi-Anechoic Chamber (SAC)) is required. The Equipment Under Test (EUT) is located on a wooden table and the cables are HF terminated with a Common Mode Absorption Device (CMAD), such that a reproducible setup with an effective cable length of approximately $1.5\,\mathrm{m}$ results and the radiated emissions are then measured with an antenna in $3\,\mathrm{m}$ distance.

Since measurements in complying test sites (i.e. OATS or SAC) are time consuming and expensive, a popular pre-compliance method bases on the measurement of the cable HF CM currents (recorded with a clamp-on current probe, cf. **Fig. 12a**), which is less susceptible to background EMI noise. It was shown in [67] [68] that radiated emissions due to CM currents can greatly exceed those caused by DM currents, and in [66] the CM currents $i_{\mathrm{CM,rad}}$ **not** returning in the cable are identified as the dominant source of radiation, hence allowing to quantify the radiated emissions based upon a measurement of the conducted CM current $i_{\mathrm{CM,rad}}$ (cf. **Fig. 13**). For a given frequency f (and hence wavelength $\lambda = c_0/f$, where c_0 is the speed of light in free space) and cable length l_{cable}, the electric field E in function of the CM current $i_{\mathrm{CM,rad}}$ and measured at a distance r can be described as [66]

$$E = \begin{cases} \frac{\mu_0 \cdot f \cdot l_{\mathrm{cable}} \cdot i_{\mathrm{CM,rad}}}{r}, & \frac{\lambda}{4} \leq l_{\mathrm{cable}} \\ \frac{\mu_0 \cdot \frac{c_0}{4} \cdot i_{\mathrm{CM,rad}}}{r}, & \frac{\lambda}{4} > l_{\mathrm{cable}}. \end{cases} \tag{21}$$

Accordingly, the **IEC 61800-3** E-field limits displayed in **Fig. 12b.i**. can be translated with (21) into corresponding CM currents **Fig. 12b.ii**, yielding a maximum value of $11\,\mathrm{dB\mu A}$ (i.e. $3.5\,\mu\mathrm{A}$) for residential applications (C1).

Ref. [66] recommends the **Fischer FCC F-33-1** clamp-on current probe with a frequency range up to $250\,\mathrm{MHz}$, which is also employed here for the radiated EMI evaluation. The maximum reading of an EMI test receiver when measuring the CM currents with the **FCC F-33-1** showing a transfer impedance of approximately $6.3\,\Omega$ is given in **Fig. 12b.iii**, where an emission level up to $26\,\mathrm{dB\mu V}$ (i.e. $20\,\mu\mathrm{V}$) can be tolerated.

This method was also employed within the field of VSDs in [69], where a successful verification measurement with an antenna in a SAC was conducted. Accordingly, the subsequent filter design process in **Sec. IV-B** as well as the experimental verification of the radiated emission level in **Sec. V** bases on the measurement of the CM current $i_{\mathrm{CM,rad}}$.

B. Radiated EMI Filter Design

According to the **IEC 61800-3**, the resulting E-field for residential applications has to be attenuated below $40\,\mathrm{dB\mu V/m}$ from $30\,\mathrm{MHz}$ to $230\,\mathrm{MHz}$, and $47\,\mathrm{dB\mu V/m}$ from $230\,\mathrm{MHz}$ to $1\,\mathrm{GHz}$. Generally, it is hard to assess the filtering demand for radiated emissions, as the main power components experience self-resonance below $30\,\mathrm{MHz}$ [70], while the dominant conducted emission mechanisms (cf. **Sec. III-B** greatly decay up to $30\,\mathrm{MHz}$ and less deterministic emission phenomena become relevant.

The radiated EMI filter design approach presented here bases on the fact that at the boundary of conducted and radiated EMI emission limits (i.e. at $30\,\mathrm{MHz}$) the emissions are measured with the LISN and the current clamp. **Fig. 13a** illustrates the measurement with a LISN (the phase currents i_{a},i_{b},i_{c} are separated into low-frequency $i_{\mathrm{a,LF}}$,$i_{\mathrm{b,LF}}$,$i_{\mathrm{c,LF}}$ and HF currents $i_{\mathrm{a,HF}}$,$i_{\mathrm{b,HF}}$,$i_{\mathrm{c,HF}}$), where the measured HF CM current $i_{\mathrm{meas,LISN}}$ evaluates to

$$\begin{aligned} i_{\mathrm{meas,LISN}} &= (i_{\mathrm{a,HF}} + i_{\mathrm{b,HF}} + i_{\mathrm{c,HF}})/3 \\ &= (i_{\mathrm{CM,rad}} + i_{\mathrm{CM,HF}})/3 \end{aligned} \tag{22}$$

and contains both the CM current returning through the cable $i_{\mathrm{CM,HF}}$ as well as $i_{\mathrm{CM,rad}}$. In contrast, **Fig. 13c** highlights the measurement with the high-bandwidth current clamp, where the measured HF CM current $i_{\mathrm{meas,CC}}$ is given by

$$\begin{aligned} i_{\mathrm{meas,CC}} &= (i_{\mathrm{a,HF}} + i_{\mathrm{b,HF}} + i_{\mathrm{c,HF}}) - i_{\mathrm{CM,HF}} \\ &= i_{\mathrm{CM,rad}} \quad . \end{aligned} \tag{23}$$

Assuming $i_{\mathrm{CM,HF}}$ and $i_{\mathrm{CM,rad}}$ to be in phase, $i_{\mathrm{CM,rad}} \leq 3 \cdot i_{\mathrm{meas,LISN}}$ holds. Considering now conservatively that $i_{\mathrm{meas,LISN}} = i_{\mathrm{CM,rad}}/3$ (i.e. $i_{\mathrm{CM,HF}} = 0\,\mathrm{A}$ and no CM current returning through the cable), the CM current limit of $11\,\mathrm{dB\mu A}$ corresponding to the C1 radiated emission limits displayed in **Fig. 12b** translates to $35\,\mathrm{dB\mu V}$ measured at

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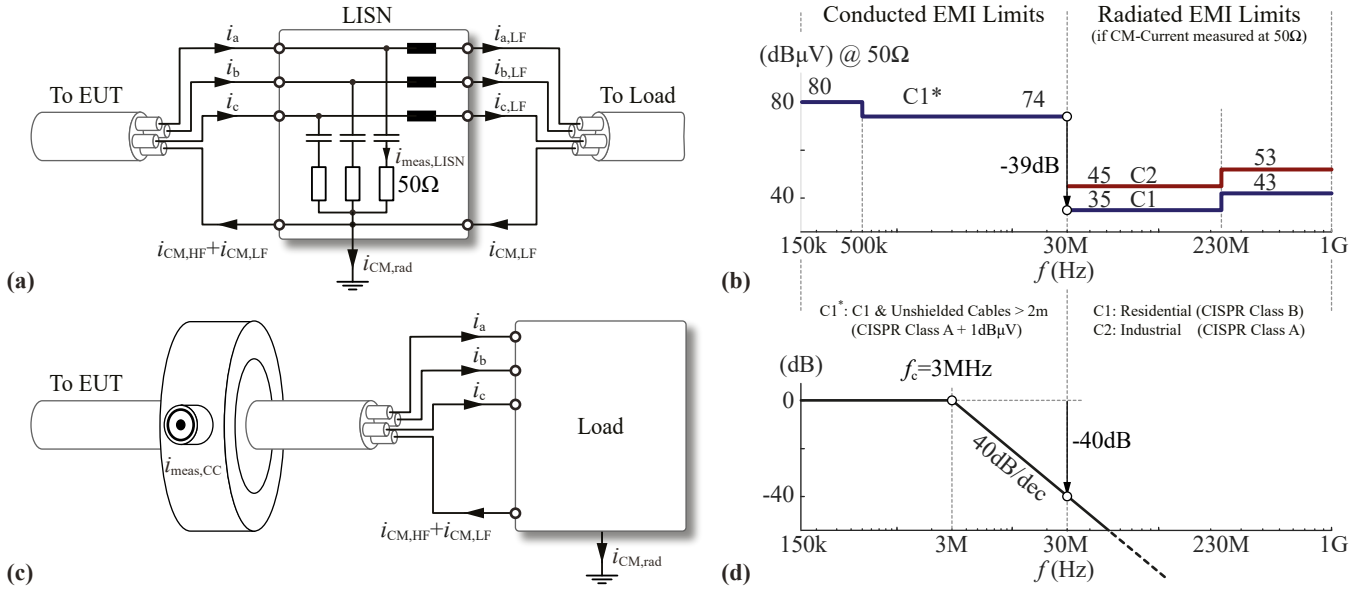

Fig. 13. CM-current measurement with **(a)** a LISN (where the phase currents i_{a},i_{b},i_{c} are separated into low-frequency $i_{\mathrm{a,LF}}$,$i_{\mathrm{b,LF}}$,$i_{\mathrm{c,LF}}$ and HF $i_{\mathrm{a,HF}}$,$i_{\mathrm{b,HF}}$,$i_{\mathrm{c,HF}}$ currents) and **(c)** a current clamp (where only the CM current $i_{\mathrm{CM,rad}}$ **not** returning through the cable is measured). Translating the current limits for radiated emissions from **Fig. 12(b.ii)** to a voltage measurement at $50\,\Omega$, the voltage limits above $30\,\mathrm{MHz}$ shown in **(b)** result. **(d)** Illustration of the radiated EMI filter design process to compensate for the more stringent CM current limit above $30\,\mathrm{MHz}$ according to **(b)**.

one of the $50\,\Omega$ LISN resistors and hence a step of $-39\,\mathrm{dB}$ compared to the C1 conducted emission limits results at $30\,\mathrm{MHz}$ in **Fig. 13b**.

Assuming conducted CM emissions equal to the limit value of $74\,\mathrm{dB\mu V}$ at $30\,\mathrm{MHz}$ without any dedicated radiated EMI filter measures, an additional second-order filter (i.e. showing a HF attenuation of $-40\,\mathrm{dB/dec}$ according to (18)) with corner frequency $f_{\mathrm{c}} = 3\,\mathrm{MHz}$ as illustrated in **Fig. 13d** is required to comply at $30\,\mathrm{MHz}$ with the $39\,\mathrm{dB}$ lower C1 radiated emission limits.

As mentioned, the radiated emission limits apply above typical self-resonance frequencies of power filter components. Accordingly dedicated HF filtering components need to be employed, where a proper HF layout of the radiated emission filter is crucial. The selected filter topology is a CL filter, where the safety capacitors of the conducted EMI filter $3 \cdot C_{\mathrm{Y2,ac,2}} = 30\,\mathrm{nF}$ (cf. **Sec. III-C**,**Fig. 11**) with a low impedance connection to the PE plane in the converter are part of the radiated EMI filter. To avoid capacitive coupling between the CM choke windings, (single-turn) NiZn-Ferrite plug-on cores (Fair-rite 52 material) with a HF attenuation up to $1\,\mathrm{GHz}$ are employed. The CM choke consists of one $35\,\mathrm{mm}$ core with $AL = 283\,\mathrm{nH}$ and two stacked $21\,\mathrm{mm}$ cores with $AL = 151\,\mathrm{nH}$ each, yielding a total inductance of $585\,\mathrm{nH}$ (decays to $340\,\mathrm{nH}$ at $30\,\mathrm{MHz}$) for the single-turn plug-on choke realization (cf. **Table II**), providing hence the desired filter attenuation at $30\,\mathrm{MHz}$ with a margin of $10\,\mathrm{dB}$.

An identical filter realization is employed for the DC side and the AC side of the Y-inverter prototype and finally, in **Fig. 11**, the schematic circuit and component values of the Y-inverter prototype with the conducted and radiated EMI filter stages is shown.

V. Experimental EMI Measurements

The $11\,\mathrm{kW}$ Y-inverter prototype including the first AC output filter stage is shown in **Fig. 14a**, where a volume of $740\,\mathrm{cm^3}$ corresponds to a power density of $15\,\mathrm{kW/dm^3}$ ($246\,\mathrm{W/in^3}$).

The Y-inverter with the designed filter attached on DC and AC side according to **Fig. 11** complying with the **IEC 61800-3** C1 conducted and radiated emission limits for operation with long unshielded cables is depicted in **Fig. 14b**, where a power density of $12\,\mathrm{kW/dm^3}$ ($197\,\mathrm{W/in^3}$) results (DC and AC filter board contribute each a volume of $74\,\mathrm{cm^3}$, hence increasing the total volume by $20\,\%$).

To avoid noise coupling from the converter directly to the cables (i.e. bypassing the converter filter), and to create a reproducible measurement setup, the Y-inverter prototype is placed in a metallic EMI enclosure emulating a housing as shown in **Fig. 14c**. Note that the enclosure was designed as a general test environment for converters, and for an industrial product a case closely fitting the converter would be preferable to maximize the system power density. Unshielded cables leave the case on both the DC side (three conductor cable for $\mathrm{DC^+}$,$\mathrm{DC^-}$ and PE) and the AC side (four conductor cable for a,b,c and PE), whereas the cables inside the housing are shielded to avoid near-field coupling [71]. The casing cooling recesses show a diameter $d = 10\,\mathrm{mm} < \lambda/20$ at $1\,\mathrm{GHz}$ such that EMI noise is confined [66].

A. Conducted EMI Measurements

In the following, emission results recorded for several operating points with the maximum boosting effort (i.e. $U_{\mathrm{dc}} = U_{\mathrm{dc,min}} = 400\,\mathrm{V}$, cf. **Fig. 2a**) are presented in order to verify the Y-inverter HF emission mechanisms derived

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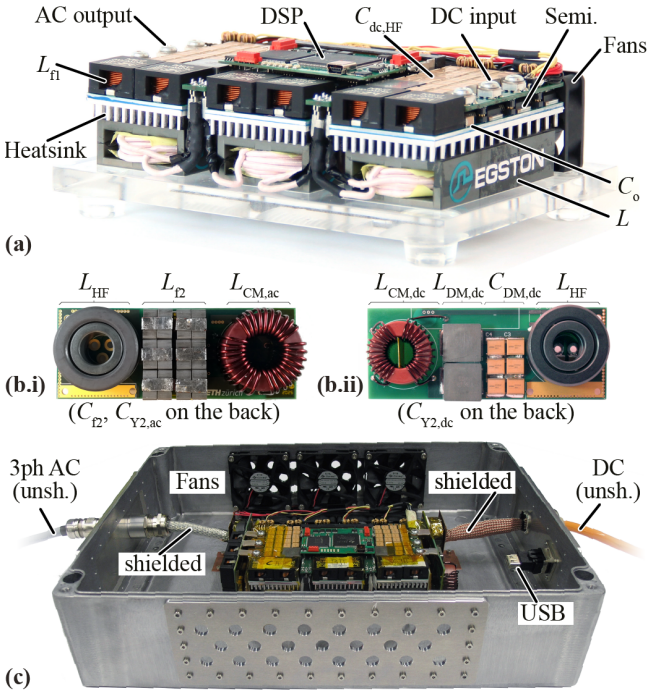

Fig. 14. (a) Y-inverter hardware prototype including the first AC filter stage (160x110x42mm^3 = 6.3x4.3x1.7in^3, $\rho = 15\,\mathrm{kW/dm^3} = 246\,\mathrm{W/in^3}$) and the additional filter boards for **(b.i)** AC side and **(b.ii)** DC side (110x42x16mm^3 = 4.3x1.7x0.6in^3). Component designators refer to **Fig. 11** and **Table II**. **(c)** Prototype with the mounted filter boards ($\rho = 12\,\mathrm{kW/dm^3} = 197\,\mathrm{W/in^3}$) placed in a shielded EMI enclosure to emulate a converter housing. Note that the motor and DC cable inside the enclosure are shielded to avoid coupling of noise from the converter, while the cables leaving the EMI enclosure are unshielded.

in **Sec. III-B** as well as the selected filter structure from **Sec. III-C**. For this reason, the switching frequency emissions at 100 kHz (located below the **IEC 61800-3** regulated band for conducted emissions starting at 150 kHz) are also shown, where emissions above the limit value of 80 dBµV result, and a 20 dB attenuator was employed on the input of the test receiver to avoid overloading the intermediate frequency amplifier (cf. [57]).

All EMI measurements are recorded using the R&S ESPI-3 test receiver, where the peak detector (9 kHz receiver bandwidth, 10 ms measurement time and 4 kHz steps) is employed to reduce the measurement time. Note that the **IEC 61800-3** limit values depicted in **Fig. 1** refer to a measurement with the slow quasi-peak detector, which generally yields readings lower or equal to the peak detector. Hence employing the peak detector is conservative, and also indicates compliance for quasi-peak detector measurements. In a first step, the converter is tested extensively with a resistive three-phase load in **Sec. V-A1**, where the emissions are recorded using a LISN on the DC input and AC output side for various operating points. There, the impact of output power, modulation index and modulation strategy is assessed. Subsequently, in **Sec. V-A2** the converter emissions are evaluated while powering a three-phase induction machine, where a close matching with the results obtained with a LISN is reported. The measured AC emissions presented in the following are recorded for phase a, where the remaining two phases show similar emission levels.

1) Measurements with LISN: A LISN is attached to the converter on the DC side (R&S NNLK8122, single-phase, up to 1 kV) or the AC side (R&S ESH2-Z5, three-phase, up to 250 $\mathrm{V_{rms}}$). As discussed in **Sec. III-A**, when using a LISN on the AC side, the employed load is decoupled from the converter for high frequencies $> 150\,\mathrm{kHz}$ and hence has negligible impact on the recorded emissions. Accordingly, for the following experiments a resistive three-phase load is employed, greatly simplifying the measurement process.

In **Fig. 15**, the impact of the modulation index M on the Y-inverter DC-side and AC-side emissions is investigated and compared against the **IEC 61800-3** C1 power interface limits. The converter is operated with DPWM, an input voltage of $U_{\mathrm{dc}} = 400\,\mathrm{V}$ and a constant resistive three-phase load with $R = 26\,\Omega$. Increasing modulation depth values M (with increasing output power) are employed starting from $M = 0.4$, where $M = 1.6$ corresponds to $U_{\mathrm{ac}} = 230\,\mathrm{V_{rms}}$ and the nominal output power of 6 kW. The thin lines in **Fig. 15** represent the spectrum obtained by the EMI receiver peak detector, while the thick dashed lines connecting the respective emission peak values (occurring at multiples of the switching frequency) have no regulatory implications but serve to distinguish between the different measurement points more clearly.

As can be noted in **Fig. 15a**, the DC-side emissions at the switching frequency increase with increasing modulation index and output power from 81 dBµV at $M = 0.4$ ($P = 0.2\,\mathrm{kW}$) to 85 dBµV at $M = 0.8$ (P=1.0 kW), which is in accordance with the discussed DC-side EMI emission mechanism in III-B, where the DM emissions scale with the switched phase currents. Accordingly, the DC-side emissions drop to 79 dBµV at $M = 1.2$ ($P = 2.2\,\mathrm{kW}$), when the phase modules partially are operating in boost operation, and a continuous current is drawn from the DC-link by the boosting module. Then, at $M = 1.6$ ($P = 6\,\mathrm{kW}$) the emissions increase again with the elevated phase currents and reach the maximum value of 90 dBµV. It can be noted that for all considered operating points, the second switching frequency harmonic component at $f_{\mathrm{D}} = 2 \cdot f_{\mathrm{s}} = 200\,\mathrm{kHz}$ is clearly below the limit value of 80 dBµV by a margin of more than 20 dB, while the emissions slightly increase again at 300 kHz. This is contradictory to the simulated noise shown in **Fig. 5b** which is continuously decreasing with frequency. Both the high margin to the limit value at $f_{\mathrm{D}} = 200\,\mathrm{kHz}$ as well as the noise increase at 300 kHz shown in **Fig. 15a** can be explained by the fact that the employed electrolytic capacitors $C_{\mathrm{dc,LF}}$ are conservatively considered ineffective at $f_{\mathrm{D}} = 200\,\mathrm{kHz}$ in the filter design process in **Sec. III-C2**, which is a too conservative assumption. Then, at 300 kHz the attenuation provided by $C_{\mathrm{dc,LF}}$ is reduced (the self-resonance frequency is exceeded), resulting in elevated emissions compared to 200 kHz. Also, although the emissions do not continuously drop with increasing frequency, as in the case of an ideal filter realization without self-resonance of components, the recorded values remain below the respective limit in the complete conducted EMI band up to 30 MHz.

A similar trend can be observed for the AC side in **Fig. 15b**, where the switching frequency EMI emissions

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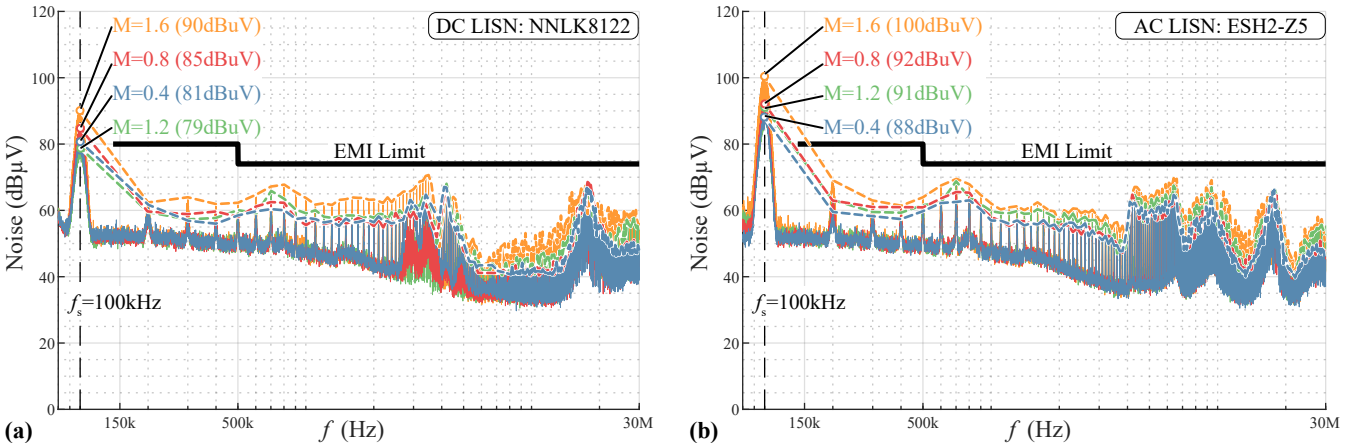

Fig. 15. Conducted EMI noise measurement results employing a LISN at **(a)** the DC input side and **(b)** the AC output side of the Y-inverter compared against the **IEC 61800-3** C1 power interface limits. The converter is operated with DPWM, an input voltage of $U_{\mathrm{dc}} = 400\,\mathrm{V}$ and a constant resistive three-phase load with $R = 26\,\Omega$. Several modulation depth values M are employed, where $M = 1.6$ corresponds to $U_{\mathrm{ac}} = 230\,\mathrm{V_{rms}}$ and the nominal power of 6 kW. The thin lines represent the spectrum obtained by the EMI receiver (peak detector, 9 kHz receiver bandwidth, 10 ms measurement time and 4 kHz steps), while the thick dashed lines connecting the respective emission peak values have no regulatory implications but serve to distinguish between the different measurement points more clearly.

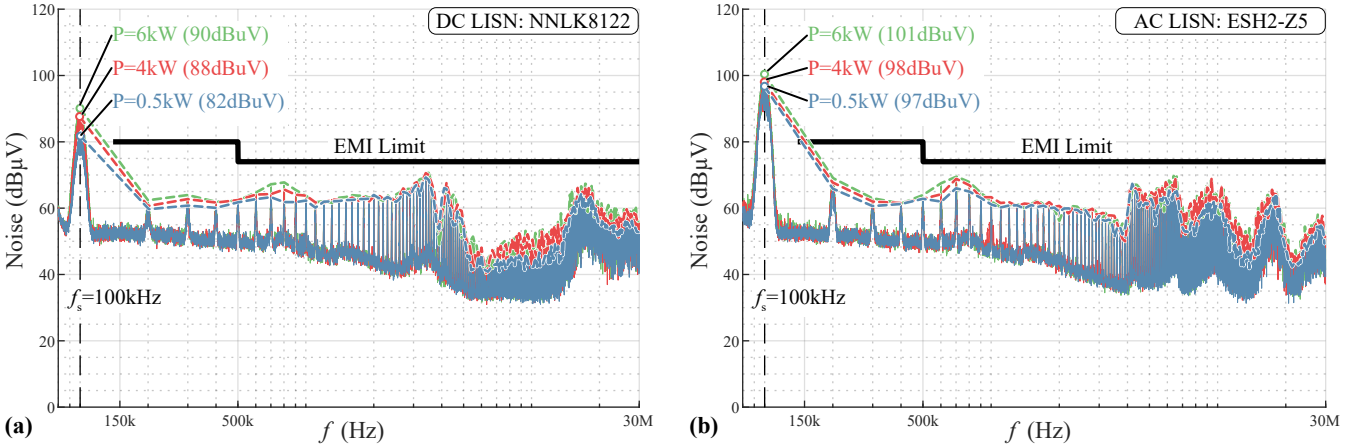

Fig. 16. Conducted EMI noise measurement results employing a LISN at **(a)** the DC input side and **(b)** the AC output side of the Y-inverter. The converter is operated with DPWM, an input voltage of $U_{\mathrm{dc}} = 400\,\mathrm{V}$ and a constant modulation depth $M = 1.6$ ($U_{\mathrm{ac}} = 230\,\mathrm{V_{rms}}$), while the resistive three-phase load is gradually decreased down to $R = 26\,\Omega$ (corresponding to the nominal power of 6 kW).

increase from 88 dBµV at $M = 0.4$, to 92 dBµV at $M = 0.8$, which corresponds to the emission behaviour of a voltage-source inverter with maximum emissions occurring, with $d_{\mathrm{Bu}} = 0.5$. When approaching boost operation, the emissions remain constant or even slightly decay and 91 dBµV result at $M = 1.2$ (the employed DPWM operation further reduces the maximum output voltage with respect to the negative DC-link rail $u_{\mathrm{an,max}}$ by approximately 15 %, such that a mild boosting effort results for $M = 1.2$). With increasing boosting effort (and output power), the *power dependent* current-source type emissions become the dominant emission mechanism, where up to 100 dBµV result (i.e. an increase of 9 dB or a factor of 3) at the operating point with $M = 1.6$ and nominal power of $P = 6\,\mathrm{kW}$. As for the DC side, the AC-side results are consistent with the emission model derived in **Sec. III-B**, where the recorded spectrum remains despite the non-ideal filter realization (i.e. employing filter components with self-resonance above a certain frequency) constantly below the relevant limits. Note that the dashed line for $M = 1.6$ crossing the emission limit line between 100 kHz and 200 kHz does not indicate exceeding the emission limits, as this line solely interconnects the emissions peaks for illustration purposes. In fact the emissions at $f_{\mathrm{D}} = 200\,\mathrm{kHz}$ comply with the emission limits with the desired margin of 10 dB.

It is worth mentioning that when operating the converter with sinusoidal PWM instead of DPWM, the boosting effort and accordingly also the low-frequency inductor current $\langle i_{\mathrm{L}} \rangle$ is increased and for the operating point with $M = 1.6$ shown in **Fig. 15b** 100 kHz AC-side emissions elevated by 10 dB were recorded.

To isolate the impact of the converter output power on the emissions, **Fig. 16** shows emission measurements for a constant modulation depth $M = 1.6$ (corresponding to $U_{\mathrm{ac}} = 230\,\mathrm{V_{rms}}$ with $U_{\mathrm{dc}} = 400\,\mathrm{V}$) and a varying resistive AC load. There, a continuous increase in emissions with output power can be observed for the DC side and the AC side. Note that for low power, the power independent voltage source emission mechanism dominates the switching-frequency noise, while the emissions increase by approximately a factor of 1.5 (3.5 dB) when increasing the output power from 4 kW to 6 kW.

2) Measurements with Motor: With the filter design and EMI equivalent circuit verified using LISNs and a resistive

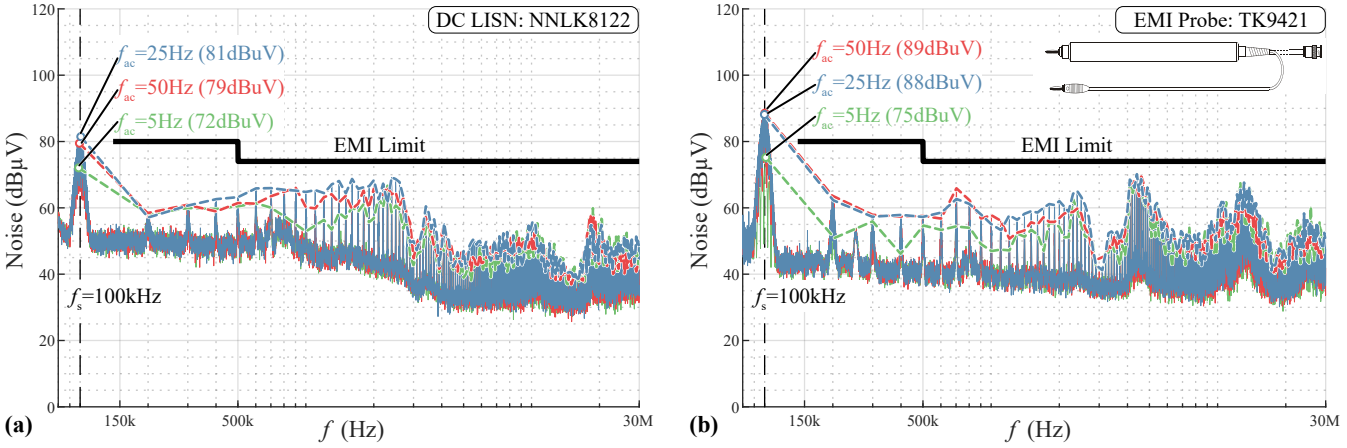

Fig. 17. Conducted EMI noise measurement results at **(a)** the DC input side and **(b)** the AC output side of the Y-inverter driving an induction machine (Bartholdi HAC-145 S 08, 330 $\mathrm{V_{rms}}$ (line-to-line), 2 kW, 2880 rpm nominal speed) in no-load condition. The emissions are measured using a LISN on the DC side, and the Schwarzbeck TK9421 high-impedance voltage probe on the AC side. The converter is operated with DPWM and an input voltage of $U_{\mathrm{dc}} = 400\,\mathrm{V}$.

load, the question remains, whether the Y-inverter prototype also complies with the emission limits when driving a motor. Accordingly, the converter emissions were measured while driving an induction machine (Bartholdi HAC-145 S 08, 330 $\mathrm{V_{rms}}$ (line-to-line), 2 kW, 2880 rpm nominal speed) in no-load condition through an unshielded cable of 5 m length (the motor was not directly grounded, but attached to PE through the cable). The Y-inverter is again operated with DPWM and an input voltage of $U_{\mathrm{dc}} = 400\,\mathrm{V}$. Open-loop V/f control is employed, where the nominal motor voltage $U_{\mathrm{ac}} = 191\,\mathrm{V_{rms}}$ (line-to-neutral, i.e. $M = 1.35$) corresponds to a stator frequency of 50 Hz. The emissions are measured using a LISN on the DC side, and the Schwarzbeck TK9421 high-impedance voltage probe (attached to the motor terminal a) on the AC side.

The resulting EMI emissions for increasing stator frequency (and motor speed as well as AC voltage) can be observed for the DC side and the AC side in **Fig. 17a** and **b**, respectively. The resulting motor phase current for a very low stator frequency $f_{\mathrm{ac}} = 5\,\mathrm{Hz}$ is $I_{\mathrm{ac}} = 1.8\,\mathrm{A_{rms}}$ (apparent output power $S = 0.1\,\mathrm{kW}$), then increases and remains constant at $I_{\mathrm{ac}} = 3.0\,\mathrm{A_{rms}}$ for $f_{\mathrm{ac}} = 25\,\mathrm{Hz}$ ($S = 0.9\,\mathrm{kW}$) and $f_{\mathrm{ac}} = 50\,\mathrm{Hz}$ ($S = 1.7\,\mathrm{kW}$). Again, the DC-side emissions at the switching frequency depicted in **Fig. 17a** increase in buck operation with the increasing phase current from 72 dBµV at $f_{\mathrm{ac}} = 5\,\mathrm{Hz}$, to 81 dBµV at $f_{\mathrm{ac}} = 25\,\mathrm{Hz}$, and then slightly drop to 79 dBµV when reaching boost operation at $f_{\mathrm{ac}} = 50\,\mathrm{Hz}$ with $M = 1.35$. Note that the switching frequency component in **Fig. 17a** is reduced compared to the values shown in **Fig. 15a**, which is due to the reduced phase currents dominating the EMI emissions around 100 kHz. However, the emissions above 200 kHz are only mildly power dependent and the DC-side emissions obtained when driving a motor greatly resemble those obtained for a resistive AC load in **Fig. 15a**.

The AC-side emissions recorded with the Schwarzbeck TK9421 high-impedance voltage probe are shown in **Fig. 17b**, where $f_{\mathrm{ac}} = 5\,\mathrm{Hz}$ (i.e. $M = 0.14$) and $f_{\mathrm{ac}} = 25\,\mathrm{Hz}$ (i.e. $M = 0.68$) correspond to buck operation and hence voltage-source emission mechanism, where the emissions increase up to a buck duty cycle of $d_{\mathrm{Bu}} = 0.5$ and are approximately independent of the output power. Hence the switching frequency emissions for $f_{\mathrm{ac}} = 25\,\mathrm{Hz}$ and $M = 0.68$ of 88 dBµV are close to the emission peaks obtained for operation with a LISN and resistive load depicted in **Fig. 15b** with $M = 0.4$ and $M = 0.8$. Due to the low apparent power and phase current, the EMI emissions only increase marginally to 89 dBµV when further increasing the stator frequency to $f_{\mathrm{ac}} = 50\,\mathrm{Hz}$ with $M = 1.35$ (i.e. with nominal motor voltage of $U_{\mathrm{ac}} = 191\,\mathrm{V_{rms}}$).

Similar to the DC side, the AC-side switching-frequency noise for operation with a motor shown in **Fig. 17b** is reduced compared to **Fig. 15b** due to the reduced phase currents and the lower maximum boosting effort (limited by the motor voltage rating), while the emissions above 200 kHz match with good accuracy, hence supporting the selected filter verification process where first in-detail pre-compliance testing is conducted with a LISN and a resistive AC load.

Industrial drives typically contain a display where speed and/or torque reference can be set. In case of the Y-inverter prototype driving the induction motor, the stator frequency reference of the DSP controller was set via communication through a USB cable, where the measurements presented in **Fig. 17** were obtained using an optical USB cable. It is important to mention that in the MHz range, auxiliary or communication cables leaving the converter housing may become the predominant source of EMI noise: In case of employing a standard USB cable instead of a fiber-optic USB cable for the operating point with a stator frequency of $f_{\mathrm{ac}} = 50\,\mathrm{Hz}$ depicted in **Fig. 17a**, DC-side emissions elevated by up to 20 dB could be observed above 10 MHz.

B. Radiated EMI Measurements

As discussed in **Sec. IV-A**, the radiated emissions of the converter prototype are assessed using the **Fischer FCC F-33-1** clamp-on current probe with a frequency range up to 250 MHz, where the ESPI test receiver employs a receiver bandwith of 120 kHz, and the limit values presented in **Fig. 12b.iii** corresponding to the **IEC 61800-3** C1 radiated emissions limits are considered.

The test setup is according to **Fig. 12a** with CMADs HF terminating the unshielded DC supply and AC motor cable on the floor, such that the measurement can be considered independent of the AC load and the DC source. Accordingly, the experiment is again conducted with a $26\,\Omega$ resistive three-phase load.

The resulting HF noise above $30\,\mathrm{MHz}$ is shown in **Fig. 18**, where a first measurement was conducted on the AC side with the prototype itself and the DC supply turned off. There a substantial noise floor with readings up to $16\,\mathrm{dB\mu V}$ (i.e. only a margin of $10\,\mathrm{dB}$ remains to the emission limit value!) results as the unshielded cables act as antenna and pick up e.g. radio broadcast signals.

Operating the converter again with $U_{\mathrm{dc}} = 400\,\mathrm{V}$, $M = 1.6$ ($U_{\mathrm{ac}} = 230\,\mathrm{V_{rms}}$) and $6\,\mathrm{kW}$ output power, the resulting CM currents not returning through the cables on the unshielded DC and AC interface are measured, where values up to $23\,\mathrm{dB\mu V}$ are recorded. Hence the measurement results imply compliance with the calculated C1 radiated emission up to $250\,\mathrm{MHz}$. According to [66], most CM cable radiation occurs below $250\,\mathrm{MHz}$, where above $230\,\mathrm{MHz}$ the C1 radiated emission limits are further relaxed by $7\,\mathrm{dB}$. Also, the recorded emissions (up to $23\,\mathrm{dB\mu V}$) do not peak at the boundary of the current probe frequency range, but decay towards the noise floor when approaching $250\,\mathrm{MHz}$. In summary, the measurement results can be considered as a strong indication towards full compliance with the **IEC 61800-3** C1 radiated EMI limits, where only a measurement with an antenna in a certified test site could finally prove full conformity.

We would like to highlight, that at $250\,\mathrm{MHz}$ the wavelength is approximately $1.2\,\mathrm{m}$, such that even short cables become efficient antennas [66]. Accordingly, a short disconnected cable for an external auxiliary supply leaving the converter housing caused the recorded emissions to exceed the limit values in an initial measurement.

VI. Conclusion

Employing unshielded cables in VSD applications allows a more flexible, lightweight and cheaper system realization compared to shielded cables, where the **IEC 61800-3** dictates stringent conducted and radiated EMI emission limits on unshielded power interfaces.

As research described in literature so far investigated the impact of several filter structures on the EMI emissions of a VSD, no comprehensive filter design guidelines including conducted and radiated EMI emissions for operation with unshielded cables are available in publications. In this paper, we provide an overview on suitable measurement techniques for power interfaces EMI emissions of DC-fed VSDs, and a complying filter structure for conducted and radiated emissions is derived for an existing $11\,\mathrm{kW}$ buck-boost Y-inverter motor drive prototype. Within this context, an EMI equivalent circuit is derived and verified for the Y-inverter showing hybrid VSI/CSI emission characteristics. Experimental measurements support the filter design process and indicate full compliance for operation with unshielded DC and AC cables according to the **IEC 61800-3**, where the ultra-compact prototype system features a power density of $12\,\mathrm{kW/dm^3}$ ($197\,\mathrm{W/in^3}$).

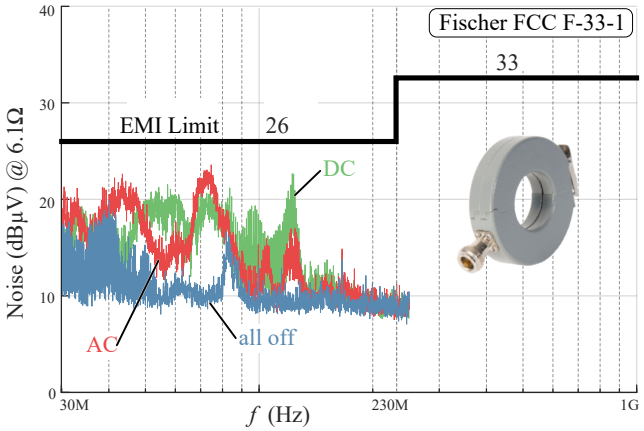

Fig. 18. Pre-compliance measurement to assess the radiated EMI emissions: The **Fischer FCC F-33-1** clamp-on current probe with a frequency range up to $250\,\mathrm{MHz}$ is employed to measure CM currents not returning through the DC supply or AC motor cable and the limit values corresponding to the **IEC 61800-3** C1 radiated emission limits are derived as discussed in **Sec. IV-A** (cf. **Fig. 12**). Measured currents $i_{\mathrm{CM,rad}}$ (reading in $\mathrm{dB\mu V}$) are shown for the AC interface when the converter prototype and the DC supply are turned off, as well as for both DC and AC interface at the nominal operating point ($U_{\mathrm{dc}} = 400\,\mathrm{V}$, $U_{\mathrm{ac}} = 230\,\mathrm{V_{rms}}$, $f_{\mathrm{ac}} = 50\,\mathrm{Hz}$, $P = 6\,\mathrm{kW}$).

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References

[1] "World energy outlook 2017," *International Energy Agency (IEA)*, Nov. 2017. [Online]. Available: https://www.iea.org/reports/world-energy-outlook-2017

[2] "Energy efficiency - motors and drives infographics (3AUA0000182864)," *ABB*, Dec. 2018. [Online]. Available: https://library.abb.com

[3] J. Luszcz, *High Frequency Conducted Emission in AC Motor Drives Fed By Frequency Converters: Sources and Propagation Paths*. Wiley, 2018.

[4] *IEC 61800-3: Adjustable speed electrical power drive systems - part 3: EMC requirements and specific test methods*, International Electrotechnical Commission (IEC) Std., 2017.

[5] F. J. T. E. Ferreira and A. T. de Almeida, "Reducing energy costs in electric-motor-driven systems: Savings through output power reduction and energy regeneration," *IEEE Industry Applications Magazine*, vol. 24, no. 1, pp. 84–97, Aug. 2018.

[6] S. Puls, J. Hegerfeld, J. Austermann, and H. Borcherding, "Transient overvoltage protection solutions for drive inverters operating on an open industrial DC grid," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)*, July 2020, pp. 1–8.

[7] D. Meike and I. Rankis, "New type of power converter for common-ground DC bus sharing to increase the energy efficiency in drive systems," in *Proc. of the IEEE International Energy Conference and Exhibition (ENERGYCON)*, Sept. 2012, pp. 225–230.

[8] J. O. Krah, N. Sieweke, C. Klarenbach, M. Hoeltgen, and D. Langhals, "Smart supercapacitor based DC-link extension for drives offers UPS capability and acts as an energy efficient line regeneration replacement," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)*, May 2016, pp. 1–8.

[9] *C.I.S.P.R., Industrial, Scientific and Medical (ISM) Radio-Frequency Equipment - Electromagnetic Disturbance Characteristics - Limits and Methods of Measurement - Publication 11*, IEC International Special Committee on Radio Interference Std., 2015.

[10] N. Hanigovszki, J. Landkildehus, G. Spiazzi, and F. Blaabjerg, "An EMC evaluation of the use of unshielded motor cables in AC adjustable speed drive applications," *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 273–281, Jan. 2006.

[11] W. L. Gore & Associates, Inc., *Tech Note: Understanding Cable Stress and Failure in High Flex Applications*. [Online]. Available: https://www.gore.com/resources/tech-note-understanding-cable-stress-and-failure-high-flex-applications

[12] J. Dobusch, D. Kuebrich, T. Duerbaum, and F. Diepold, "Implementation of current based three-phase CM/DM noise separation on the drive side," in *Proc. of the IEEE International Symposium on Electromagnetic Compatibility (EMC EUROPE)*, Aug. 2018, pp. 220–225.

[13] E. J. Bulington, S. Abney, and G. L. Skibinski, "Cable alternatives for PWM AC drive applications," in *Proc. of the IEEE IAS Petroleum and Chemical Technical Conference (PCIC)*, Sept. 1999, pp. 247–259.

[14] L. A. Saunders, G. L. Skibinski, S. T. Evon, and D. L. Kempkes, "Riding the reflected wave - IGBT drive technology demands new motor and cable considerations," in *Proc. of the IEEE IAS Petroleum and Chemical Industry Technical Conference (PCIC)*, Sept. 1996, pp. 75–84.

[15] S. Chen, T. A. Lipo, and D. Fitzgerald, "Modeling of motor bearing currents in PWM inverter drives," *IEEE Transactions on Industry Applications*, vol. 32, no. 6, pp. 1365–1370, Nov. 1996.

[16] J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski, "Effect of PWM inverters on AC motor bearing currents and shaft voltages," *IEEE Transactions on Industry Applications*, vol. 32, no. 2, pp. 250–259, Mar. 1996.

[17] M. Fuerst and M. Bakran, "An advanced filtering method for partial discharge measurement in the presence of high dv/dt," in *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)*, May 2019, pp. 1–7.

[18] B. Zhang and S. Wang, "A survey of EMI research in power electronics systems with wide-bandgap semiconductor devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 626–643, Nov. 2020.

[19] P. T. Finlayson, "Output filters for PWM drives with induction motors," *IEEE Industry Applications Magazine*, vol. 4, no. 1, pp. 46–52, Jan. 1998.

[20] J. K. Steinke, "Use of an LC filter to achieve a motor-friendly performance of the PWM voltage source inverter," *IEEE Transactions on Energy Conversion*, vol. 14, no. 3, pp. 649–654, Sept. 1999.

[21] N. Hanigovszki, J. Landkildehus, and F. Blaabjerg, "Output filters for AC adjustable speed drives," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2007, pp. 236–242.

[22] J. Guzinski, H. Abu-Rub, and P. Strankowski, *Variable Speed AC Drives with Inverter Output Filters*. John Wiley & Sons, 2015.

[23] D. Rendusara and P. Enjeti, "New inverter output filter configuration reduces common mode and differential mode dv/dt at the motor terminals in PWM drive systems," in *Proc. of the IEEE Power Electronics Specialists Conference (PESC)*, vol. 2, June 1997, pp. 1269–1275 vol.2.

[24] D. A. Rendusara and P. N. Enjeti, "An improved inverter output filter configuration reduces common and differential modes dv/dt at the motor terminals in PWM drive systems," *IEEE Transactions on Power Electronics*, vol. 13, no. 6, pp. 1135–1143, Nov. 1998.

[25] H. Akagi and T. Shimizu, "Attenuation of conducted EMI emissions from an inverter-driven motor," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 282–290, Jan. 2008.

[26] F. Maislinger, H. Ertl, G. Stojcic, C. Lagler, and F. Holzner, "Design of a 100 kHz wide bandgap inverter for motor applications with active damped sine wave filter," *The Journal of Engineering*, no. 17, pp. 3766–3771, Apr. 2019.

[27] K. Shirabe, M. Swamy, J. K. Kang, M. Hisatsune, Y. Wu, D. Kebort, and J. Honea, "Advantages of high frequency PWM in AC motor drive applications," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Sept. 2012, pp. 2977–2984.

[28] M. M. Swamy, J. Kang, and K. Shirabe, "Power loss, system efficiency, and leakage current comparison between Si IGBT VFD and SiC FET VFD with various filtering options," *IEEE Transactions on Industry Applications*, vol. 51, no. 5, pp. 3858–3866, Apr. 2015.

[29] N. Mukherjee, J. Fuerst, F. Diepold, and F. A. Vega, "900 V GaN-based sine-wave inverters for three-phase industrial applications," in *Proc. of the International Conference on Power Electronics, Machines and Drives (PEMD)*, vol. 2019, no. 17, Apr. 2019, pp. 3754–3759.

[30] M. Antivachis, D. Bortis, L. Schrittwieser, and J. W. Kolar, "Novel buck-boost inverter topology for fuel-cell powered drive systems," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2018.

[31] M. Antivachis, D. Bortis, D. Menzi, and J. W. Kolar, "Comparative evaluation of y-inverter against three-phase two-stage buck-boost DC-AC converter systems," in *Proc. of the IEEE International Power Electronics Conference (IPEC - ECCE Asia)*, May 2018, pp. 181–189.

[32] M. Antivachis, N. Kleynhans, and J. W. Kolar, "Three-phase sinusoidal output buck-boost GaN y-inverter for advanced variable speed AC drives," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, early access, Sept. 2020.

[33] H. Bishnoi, P. Mattavelli, R. P. Burgos, and D. Boroyevich, "EMI filter design of DC-fed motor-drives using behavioral EMI models," in *Proc. of the IEEE European Conference on Power Electronics and Applications (EPE ECCE Europe)*, Sept. 2015, pp. 1–10.

[34] X. Zhang, D. Boroyevich, P. Mattavelli, J. Xue, and F. Wang, "EMI filter design and optimization for both AC and DC side in a DC-fed motor drive system," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2013, pp. 597–603.

[35] C. Jettanasen and A. Ngaopitakkul, "Minimization of common-mode conducted noise in PWM inverter-fed AC motor drive systems using optimized passive EMI filter," in *Proc. of the International Multi-Conference of Engineers and Computer Scientists (IMECS)*, vol. 2, Mar. 2010, pp. 1249–1252.

[36] F. Maislinger, H. Ertl, G. Stojcic, and F. Holzner, "Efficiency and motor-performance improvement using WBG-inverters with observer-based actively damped LC-sine wave filters," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)*. VDE, May 2019, pp. 1–9.

[37] "European Center for Power Electronics e.V. (ECPE)," www.ecpe.org.

[38] K. Taniguchi, Y. Ogino, and H. Irie, "PWM technique for power MOSFET inverter," *IEEE Transactions on Power Electronics*, vol. 3, no. 3, pp. 328–334, July 1988.

[39] H. Dai, T. M. Jahns, R. A. Torres, D. Han, and B. Sarlioglu, "Comparative evaluation of conducted common-mode EMI in voltage-source and current-source inverters using wide-bandgap switches," in *Proc. of the IEEE Transportation Electrification Conference and Expo (ITEC)*, June 2018, pp. 788–794.

[40] M. Antivachis, P. Niklaus, D. Bortis, and J. W. Kolar, "Input / output EMI filter design for three-phase ultra-high speed motor drive GaN inverter stage," *IEEE CPSS Transactions on Power Electronics and Applications*, to be published.

[41] H. Bishnoi, P. Mattavelli, R. Burgos, and D. Boroyevich, "EMI behavioral models of DC-fed three-phase motor drive systems," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4633–4645, Oct. 2014.

[42] M. Moreau, N. Idir, and P. Le Moigne, "Modeling of conducted EMI in adjustable speed drives," *IEEE Transactions on Electromagnetic Compatibility*, vol. 51, no. 3, pp. 665–672, July 2009.

[43] J. Dobusch, P. Konarski, D. Kuebrich, and T. Duerbaum, "Implementation of voltage based three-phase CM/DM noise separation on the drive side," in *Proc. of the IEEE European Conference on Power Electronics and Applications (EPE ECCE Europe)*, Sept. 2018, pp. 1–9.

[44] G. Grandi, D. Casadei, and U. Reggiani, "Common- and differential-mode HF current components in AC motors supplied by voltage source inverters," *IEEE Transactions on Power Electronics*, vol. 19, no. 1, pp. 16–24, Jan. 2004.

[45] J. Luszcz, "Motor cable as an origin of supplementary conducted EMI emission of ASD," in *Proc. of the IEEE European Conference on Power Electronics and Applications (EPE ECCE Europe)*, Sept. 2009, pp. 1–7.

[46] ——, "Motor cable effect on the converter fed AC motor common mode current," in *Proc. of the IEEE International Conference-Workshop Compatibility and Power Electronics (CPE)*, June 2011, pp. 445–450.

[47] B. Revol, J. Roudet, J. Schanen, and P. Loizelet, "EMI study of three-phase inverter-fed motor drives," *IEEE Transactions on Industry Applications*, vol. 47, no. 1, pp. 223–231, Nov. 2011.

[48] V. D. Santos, N. Roux, B. Revol, B. Sareni, B. Cougo, and J. Carayon, "Unshielded cable modeling for conducted emissions issues in electrical power drive systems," in *Proc. of the IEEE International Symposium on Electromagnetic Compatibility (EMC EUROPE)*, Sept. 2017, pp. 1–6.

[49] B. Cougo, H. H. Sathler, R. Riva, V. D. Santos, N. Roux, and B. Sareni, "Characterization of low-inductance sic module with integrated capacitors for aircraft applications requiring low losses and low emi issues," *IEEE Transactions on Power Electronics*, July 2021.

[50] C. M. Lundmark, E. O. A. Larsson, and M. H. J. Bollen, "Unintended consequences of limiting high-frequency emission by small end-user equipment," in *Proc. of the IEEE Power Engineering Society (PES) General Meeting*, vol. 6, June 2006.

[51] J. R. Nicholson and J. A. Malack, "RF impedance of power lines and line impedance stabilization networks in conducted interference measurements," *IEEE Transactions on Electromagnetic Compatibility*, vol. EMC-15, no. 2, pp. 84–86, May 1973.

[52] M. L. Heldwein, "EMC filtering of three-phase PWM converters," Ph.D. dissertation, ETH Zurich, 2008.

[53] M. Hartmann, H. Ertl, and J. W. Kolar, "EMI filter design for a 1 MHz , 10 kW three-phase/level PWM rectifier," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1192–1204, Apr. 2011.

[54] R. Zhang, X. Wu, and T. Wang, "Analysis of common mode EMI for three-phase voltage source converters," in *Proc. of the IEEE Power Electronics Specialist Conference (PESC)*, vol. 4, June 2003, pp. 1510–1515.

[55] D. O. Boillat, F. Krismer, and J. W. Kolar, "EMI filter volume minimization of a three-phase, three-level T-type PWM converter system," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2473–2480, Apr. 2017.

[56] A. Mallik, W. Ding, and A. Khaligh, "A comprehensive design approach to an EMI filter for a 6-kW three-phase boost power factor correction rectifier in avionics vehicular systems," *IEEE Transactions on Vehicular Technology*, vol. 66, no. 4, pp. 2942–2951, Apr. 2017.

[57] T. Nussbaumer, M. L. Heldwein, and J. W. Kolar, "Differential mode input filter design for a three-phase buck-type PWM rectifier based on modeling of the EMC test receiver," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1649–1661, Oct. 2006.

[58] M. L. Heldwein, T. Nussbaumer, and J. W. Kolar, "Common mode modelling and filter design for a three-phase buck-type pulse width modulated rectifier system," *IET Power Electronics*, vol. 3, no. 2, pp. 209–218, Mar. 2010.

[59] K. Basu, A. K. Sahoo, V. Chandrasekaran, and N. Mohan, "Grid-side AC line filter design of a current source rectifier with analytical estimation of input current ripple," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6394–6405, Dec. 2014.

[60] L. Ran, S. Gokani, J. Clare, K. J. Bradley, and C. Christopoulos, "Conducted electromagnetic emissions in induction motor drive systems. I. Time domain analysis and identification of dominant modes," *IEEE Transactions on Power Electronics*, vol. 13, no. 4, pp. 757–767, July 1998.

[61] K. Raggl, T. Nussbaumer, and J. W. Kolar, "Guideline for a simplified differential-mode EMI filter design," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 3, pp. 1031–1040, Mar. 2010.

[62] A. Nagel and R. W. De Doncker, "Systematic design of EMI-filters for power converters," in *Proc. of the IEEE Industry Applications Society (IAS) Annual Meeting*, vol. 4, Oct. 2000, pp. 2523–2525 vol.4.

[63] M. L. Heldwein and J. W. Kolar, "Design of minimum volume EMC input filters for an ultra compact three-phase PWM rectifier," in *Proc. of the Brazilian Power Electronic Conference (COBEP)*, Sept. 2007, pp. 454–461.

[64] D. Menzi, D. Bortis, G. Zulauf, M. Heller, and J. W. Kolar, "Novel iGSE-C loss modeling of X7R ceramic capacitors," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13 367–13 383, Dec. 2020.

[65] F. Maislinger, H. Ertl, G. Stojcic, and L. Siplika, "Performance of a two-stage actively damped LC filter for GaN/SiC motor inverters," in *Proc. of the IEEE International Power Electronics and Motion Control Conference (PEMC)*, Aug. 2018, pp. 177–183.

[66] H. W. Ott, *Electromagnetic Compatibility Engineering*. John Wiley & Sons, 2011.

[67] C. R. Paul and D. R. Bush, "Radiated emissions from common-mode currents," in *Proc. of the IEEE International Symposium on Electromagnetic Compatibility*, Aug. 1987, pp. 1–7.

[68] C. R. Paul, "A comparison of the contributions of common-mode and differential-mode currents in radiated emissions," *IEEE Transactions on Electromagnetic Compatibility*, vol. 31, no. 2, pp. 189–193, May 1989.

[69] Z. Vrankovic, G. L. Skibinski, and C. Winterhalter, "Novel double clamp methodology to reduce shielded cable radiated emissions initiated by electronic device switching," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Sept. 2015, pp. 4351–4360.

[70] Shuo Wang, F. C. Lee, D. Y. Chen, and W. G. Odendaal, "Effects of parasitic parameters on EMI filter performance," *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 869–877, May 2004.

[71] R. Wang, H. F. Blanchette, M. Mu, D. Boroyevich, and P. Mattavelli, "Influence of high-frequency near-field coupling between magnetic components on EMI filter design," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4568–4579, Jan. 2013.

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