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***Abstract*—On-Board Chargers (OBCs) comprising an ac-dc front-end and a subsequent isolated dc-dc converter stage represent a crucial component of Electric Vehicles (EVs), and must be able to charge the EV battery from both, a three-phase mains and a single-phase mains. Further, a lightweight and compact realization of the OBC is key in mobile applications. This requirement for high gravimetric and volumetric power density is often hindered by the large (electrolytic) dc-link capacitor required to buffer the power pulsation at twice the mains frequency in single-phase operation, which can be omitted by employing an active Power Pulsation Buffer (PPB) circuit allowing to minimize the overall capacitor volume. This paper proposes a novel Smart-dc-Link (S-Link) concept which improves the OBC performance by utilizing the active PPB circuitry also in three-phase operation. There, the S-Link facilitates a six-pulse dc-link voltage variation enabling a substantial switching loss reduction in the ac-dc converter front-end, while advantageously the dc output voltage can be kept constant.**

***Index Terms*—On-Board Chargers, Power Pulsation Buffer, S-Link, Series Stacked Power Buffer, Series Voltage Injection, 1/3-Modulation**

I. Introduction

Mass adoption of Electric Vehicles (EVs) is currently taking place [1] with the On-Board Charger (OBC) representing a vital piece of equipment [2]. OBCs are required to feature high efficiency, high gravimetric and volumetric power densities [2], as well as bidirectional power flow capability for feeding power back to the grid in vehicle-to-grid (V2G) applications [2], [3]. Further, the OBC should allow operation with a three-phase mains or single-phase mains such that the EV battery can be charged independent of the available grid infrastructure. In this paper, a novel Smart-dc-Link (S-Link) concept (see **Fig. 1**) is proposed, which allows to improve the performance of OBCs in both, three-phase and single-phase operation. The S-Link concept is derived and detailed in **Section II** and **Section III** discusses design guidelines for the main energy buffering components. Then, **Section IV** presents the corresponding closed-loop control structure and verifies the concept with detailed circuit simulations.

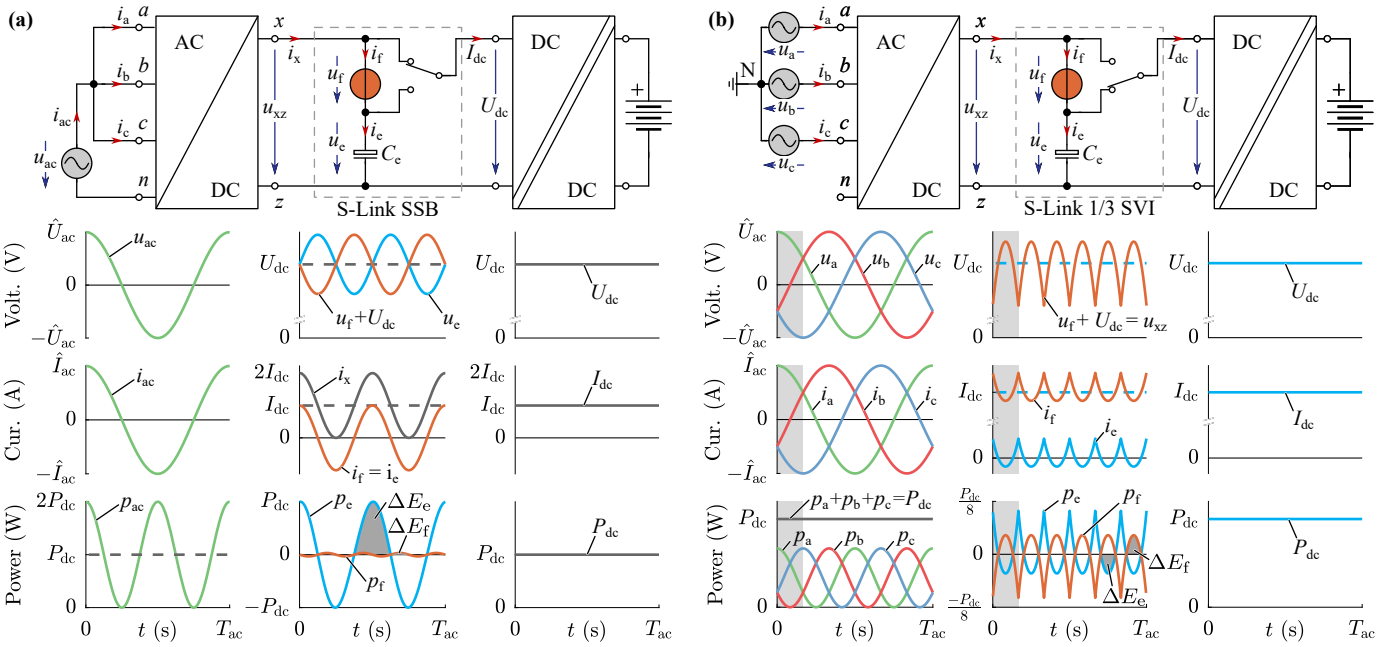

Fig. 1. Proposed On-Board Charger (OBC) concept comprising a PFC ac-dc front-end, a Smart-dc-Link (S-Link) and an isolated dc-dc converter for operation in **(a)** a single-phase and **(b)** a three-phase grid. The shown characteristic voltage, current, and power waveforms do not include switching-frequency components.

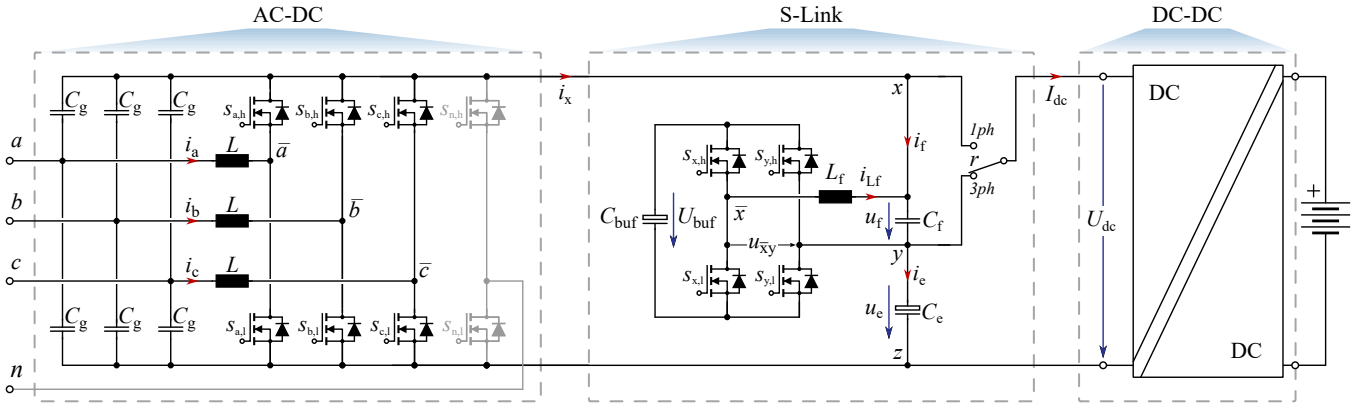

Fig. 2. Main power circuit of the proposed S-Link OBC comprising a PFC ac-dc front-end, a Smart-dc-Link (S-Link) and an isolated dc-dc converter. The circuit is configured for three-phase operation; the unfolder bridge-leg needed for single-phase operation is shown in gray.

II. Operating Principle

Fig. 1 depicts the proposed OBC concept comprising a Power Factor Correction (PFC) ac-dc front-end, an S-Link circuit (represented here by a voltage source u_f, a series capacitor C_e and a selector switch) and an isolated dc-dc converter (providing galvanic insulation), which operates in a single-phase or a three-phase grid (the detailed power circuit structure is highlighted in **Fig. 2**). The corresponding Low-Frequency (LF; i.e., switching-frequency components are not shown) voltage, current and power waveforms highlight the basic S-Link operating principle, whereby unity-power-factor operation and lossless power conversion is assumed. **Tab. I** lists the considered system specifications.

A. Single-Phase Configuration

In single-phase operation (**Fig. 1a**), the three ac-dc front-end terminals a, b, c are parallel-connected to the grid (modelled by an ideal voltage source u_ac) and equally share the grid current i_ac, i.e., $i_\mathrm{a} = i_\mathrm{b} = i_\mathrm{c} = i_\mathrm{ac}/3$, to realize a single-phase nominal power capability that is almost as high as the rated power in three-phase operation [4]–[6]. The main converter waveforms within a mains period $T_\mathrm{ac} = 1/f_\mathrm{ac}$ are highlighted in **Fig. 1a**. The grid input power p_ac comprises (for unity-power-factor operation) the inherent twice-mains frequency power pulsation on top of the average power that equals the (constant) output power P_dc. This power pulsation is typically buffered by large dc-link capacitors, imposing a significant penalty on the OBC power density [7]. In contrast, active Power Pulsation Buffers (PPBs) [7] allow to mitigate or drastically reduce the bulky dc-link capacitors. Therefore, for single-phase operation, the S-Link is configured such that it acts as a Series Stacked Buffer (SSB) [8]–[10]: The major part of the power pulsation is absorbed by the bulk capacitor C_e, which processes the power p_e. Here, a comparably small C_e can be selected and a thus comparably large fluctuation of the voltage u_e is accepted, because the S-Link injects an ac voltage u_f compensating the fluctuation of u_e such that the input voltage $U_\mathrm{dc} = u_\mathrm{xz} = u_\mathrm{e} + u_\mathrm{f}$ of the isolated dc-dc converter (drawing constant current I_dc and power P_dc) advantageously remains constant during a mains period T_ac.

Table I
Considered System Specifications.

Description	3-Phase Grid	1-Phase Grid
Grid volt.[1]	$U_\mathrm{ac} = 230\,\mathrm{V_{RMS}}$	$U_\mathrm{ac} = 240\,\mathrm{V_{RMS}}$
Grid curr.	$I_\mathrm{ac} = 9.6\,\mathrm{A_{RMS}}$	$I_\mathrm{ac} = 24\,\mathrm{A_{RMS}}$
Grid freq.	$f_\mathrm{ac} = 50\,\mathrm{Hz}$	$f_\mathrm{ac} = 60\,\mathrm{Hz}$
dc curr.	$I_\mathrm{dc} = 12.3\,\mathrm{A}$	$I_\mathrm{dc} = 10.8\,\mathrm{A}$
dc power	$P_\mathrm{dc} = 6.6\,\mathrm{kW}$	$P_\mathrm{dc} = 5.8\,\mathrm{kW}$

[1]line-to-neutral voltage

B. Three-Phase Configuration

In three-phase operation (**Fig. 1b**) the terminals a, b, c are connected to the three grid phases (voltage sources $u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}$). To maximize the efficiency of the ac-dc front-end, a six-pulse-shaped (envelope of the maximum line-to-line voltage absolute values) dc-link voltage u_xz can be introduced, thereby enabling 1/3-modulation [11]–[13]: At any given point in time, only one out of the three bridge-legs switches at high-frequency while the other two bridge-legs (connected to the grid phases with the maximum and minimum instantaneous grid voltages, respectively) clamp the grid terminals to the positive x and negative z dc-link rail, respectively. Thus, the switching losses of the ac-dc front-end can be reduced by more than 66% [12], [13]. Typically, this six-pulse variation of u_xz has to be realized by the downstream dc-dc converter [13], which has two main disadvantages: First, the dc-dc converter stage faces a time-varying input voltage, decreasing the conversion efficiency. Second, the dc-dc converter is involved in the grid current regulation and thus an *integrated* synergetic control of the ac-dc front-end and the dc-dc converter (which, in addition, requires a correspondingly high (input) voltage control bandwidth) is needed. In combination, this prevents the use of standard, off-the-shelve dc-dc converter modules, which is undesirable, e.g., regarding economies of scale.

As the grid input power $p_\mathrm{a} + p_\mathrm{b} + p_\mathrm{c} = P_\mathrm{dc}$ is ideally constant, no PPB is required in three-phase operation. However, the S-Link can be reconfigured to act as a Series Voltage Injection (SVI) circuit that realizes the six-pulse variation of the ac-dc front-end dc-side voltage u_xz (which again does not comprise

a dc voltage component). Advantageously, the ac-dc front-end can then operate with 1/3-modulation while the isolated dc-dc converter still faces a constant input voltage U_{dc} and thus can be controlled independently of the ac-dc front-end. This enables the use of a standard high-efficiency off-the-shelve dc-dc converter.

C. Main S-Link Power Circuit

The main power circuit of the considered S-Link OBC realization is depicted in **Fig. 2**: The PFC ac-dc front-end (shown without Electromagnetic Interference (EMI) filter) comprises three standard two-level bridge-legs (alternatively, also multi-level flying capacitor bridge-legs could be employed to minimize the volume of the boost inductors L [14], [15]). Further, an additional LF unfolder half-bridge connects to the grid neutral n in single-phase operation (it is disconnected/disabled for three-phase operation), enabling single-phase totem-pole PFC operation with almost the same rated power as in three-phase mode [5]. For the realization of the S-Link voltage source u_{f}, an H-bridge circuit (with the dc-side LF energy storage capacitor C_{buf} and the power semiconductors $s_{\mathrm{x,h}}$, $s_{\mathrm{x,l}}$, $s_{\mathrm{y,h}}$ and $s_{\mathrm{y,l}}$) and a second-order $L_{\mathrm{f}}C_{\mathrm{f}}$ output filter is utilized. Last, the isolated dc-dc converter (not further detailed here, as a standard off-the-shelve system could be employed) is connected by a relay r to the lower terminal y ($r = 3ph$ and $U_{\mathrm{dc}} = u_{\mathrm{e}}$ for three-phase operation) or the upper terminal x ($r = 1ph$ and $U_{\mathrm{dc}} = u_{\mathrm{xz}}$ for single-phase operation) of the S-link output filter capacitor C_{f}.

III. S-Link Design Guidelines

The goal of this section is to provide basic design guidelines for the identification of suitable S-Link parameters, i.e., the buffer capacitor value C_{buf} and voltage U_{buf}, the S-Link power semiconductor voltage rating U_{R}, and the bulk capacitor value C_{e}.

Typically, in a single-phase-only application the selected voltage range of u_{f} of an SSB [8]–[10] represents a degree of freedom for the system design, which impacts the tolerable voltage fluctuation of the bulk capacitor voltage u_{e} (and hence defines the minimally required value of C_{e}), as well as the required SSB energy storage capability (buffer capacitor value C_{buf}, voltage U_{buf}, and the rated voltage U_{R} of the S-Link power semiconductors) and hence can be used to optimize the overall SSB volume and losses.

Here, the design process is different, as the three-phase operation with 1/3-modulation defines a (minimum) voltage range of u_{f} (i.e., output voltage capability of the S-Link) and a step-by-step design guideline is provided in the following. Again, unity-power-factor operation and lossless power conversion is assumed, and only the LF voltage and current waveforms are considered to allow the derivation of simple analytic expressions. Furthermore, the impact of the S-Link filtering elements on the LF converter waveforms is neglected (i.e., zero LF current through $C_{\mathrm{f}} \ll C_{\mathrm{e}}, C_{\mathrm{buf}}$ as its impedance $|Z_{\mathrm{Cf}}(f_{\mathrm{ac}})|$ is large, and zero LF voltage across L_{f} as its impedance $|Z_{\mathrm{Lf}}(f_{\mathrm{ac}})|$ is low at the grid frequency level f_{ac}).

A. Three-Phase Configuration

The three-phase grid input voltage and current of phase $j \in \{a, b, c\}$ is defined by

$$\begin{aligned} u_{\mathrm{j}}(t) &= \hat{U}_{\mathrm{ac}} \cos\left(2\pi f_{\mathrm{ac}} t - \phi_{\mathrm{j}}\right) \\ i_{\mathrm{j}}(t) &= \hat{I}_{\mathrm{ac}} \cos\left(2\pi f_{\mathrm{ac}} t - \phi_{\mathrm{j}}\right), \end{aligned} \tag{1}$$

with the phase angles $\phi_{\mathrm{j}} = \{0, \frac{-2\pi}{3}, \frac{-4\pi}{3}\}$ and the output power resulting to $P_{\mathrm{dc}} = \frac{3}{2}\hat{U}_{\mathrm{ac}}\hat{I}_{\mathrm{ac}} = 6.6\,\mathrm{kW}$ according to **Tab. I**.

In 1/3-modulation, the output voltage u_{xz} of the ac-dc front-end converter follows the maximum line-to-line voltage [11]–[13]. Due to the repetitive six-pulse voltage pattern, it is sufficient to consider a time interval $t \in [0, T_{\mathrm{ac}}/6]$ (the specific simplifications valid for this first, representative sector are highlighted with (*) in the following equations) where the voltage u_{xz} is defined by the phase a and c line-to-line voltage $u_{\mathrm{a,c}}(t) = u_{\mathrm{a}}(t) - u_{\mathrm{c}}(t)$ and the corresponding dc-link current i_{x} is given by

$$\begin{aligned} u_{\mathrm{xz}}(t) &= \max(u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}) - \min(u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}) \\ &\overset{(*)}{=} u_{\mathrm{a,c}}(t) = \sqrt{3}\hat{U}_{\mathrm{ac}} \sin\left(2\pi f_{\mathrm{ac}} t + \frac{\pi}{3}\right), \\ i_{\mathrm{x}}(t) &= \frac{P_{\mathrm{dc}}}{u_{\mathrm{xz}}(t)} \overset{(*)}{=} \frac{P_{\mathrm{dc}}}{\sqrt{3}\hat{U}_{\mathrm{ac}} \sin\left(2\pi f_{\mathrm{ac}} t + \frac{\pi}{3}\right)}, \end{aligned} \tag{2}$$

resulting in $u_{\mathrm{xz}} \in [488\,\mathrm{V}, 563\,\mathrm{V}]$ with an average value $\bar{u}_{\mathrm{xz}} = U_{\mathrm{dc}} = \frac{3}{\pi}\sqrt{3}\hat{U}_{\mathrm{ac}} = 538\,\mathrm{V}$, and in $i_{\mathrm{x}} \in [11.7\,\mathrm{A}, 13.5\,\mathrm{A}]$ with an average value $\bar{i}_{\mathrm{x}} = I_{\mathrm{dc}} = 12.3\,\mathrm{A}$.

1) Buffer Capacitor C_{buf} Energy Requirement: The task of the S-Link circuit in three-phase operation is (in first approximation) to realize the six-pulse variation of the ac front-end voltage u_{xz} on top of the average value $\bar{u}_{\mathrm{xz}}$ as

$$\begin{aligned} u_{\mathrm{f}}(t) &= u_{\mathrm{xz}}(t) - \bar{u}_{\mathrm{xz}} \\ &\overset{(*)}{=} \sqrt{3}\hat{U}_{\mathrm{ac}}(\sin\left(2\pi f_{\mathrm{ac}} t + \frac{\pi}{3}\right) - \frac{3}{\pi}), \end{aligned} \tag{3}$$

with $u_{\mathrm{f}} \in [-50\,\mathrm{V}, 25\,\mathrm{V}]$ and zero average value $\bar{u}_{\mathrm{f}} = 0$. Neglecting the LF current flowing through the capacitor C_{f} (used for high-frequency (HF) filtering only) the S-Link input current is defined by $i_{\mathrm{f}}(t) = i_{\mathrm{x}}(t)$ according to (2) such that the instantaneous power $p_{\mathrm{f}}(t)$ (see **Fig. 1b**) can be approximated with

$$p_{\mathrm{f}}(t) = u_{\mathrm{f}}(t) i_{\mathrm{f}}(t) \overset{(*)}{=} P_{\mathrm{dc}} \frac{\sin\left(2\pi f_{\mathrm{ac}} t + \frac{\pi}{3}\right) - \frac{3}{\pi}}{\sin\left(2\pi f_{\mathrm{ac}} t + \frac{\pi}{3}\right)}, \tag{4}$$

resulting in $p_{\mathrm{f}} \in [-677\,\mathrm{W}, 298\,\mathrm{W}]$ and a non-zero average value $\bar{p}_{\mathrm{f}} = -12\,\mathrm{W}$ (even though $\bar{u}_{\mathrm{f}} = 0$, both, u_{f} and i_{f} contain higher-order harmonics; the convolution thus results in this small dc power component). Note that the average power can be reduced to $\bar{p}_{\mathrm{f}} = 0$ by injecting a small average voltage $\bar{u}_{\mathrm{f}} \approx 1\,\mathrm{V}$ and the regulation of the average buffer power intake $\bar{p}_{\mathrm{f}}$ will be discussed in more detail in **Section IV** and $\bar{p}_{\mathrm{f}} = 0$ is considered in the following step. Last, the energy variation of the S-Link buffer capacitor C_{buf} is defined by $E_{\mathrm{buf}}(t) = \int p_{\mathrm{f}}(t)\,\mathrm{d}t$, with the minimum energy storage requirement $\Delta E_{\mathrm{buf}} = \max(E_{\mathrm{buf}}(t)) - \min(E_{\mathrm{buf}}(t))$=406 mJ for the considered specifications in **Tab. I**.

2) Buffer Capacitor C_{buf} Voltage and Capacitance Value: In practice, the energy stored in the buffer capacitor C_{buf} cannot be fully utilized, as the S-Link duty cycle

$$d_{\bar{\mathrm{x}}\mathrm{y}}(t) = \frac{u_{\mathrm{f}}(t)}{U_{\mathrm{buf}}(t)} \tag{5}$$

needs to be maintained in the linear range of $d_{\bar{\mathrm{x}}\mathrm{y}} \in [-1, 1]$ and a sufficient duty cycle margin (here selected as $|d_{\bar{\mathrm{x}}\mathrm{y}}| \leq d_{\mathrm{lim}} = 0.6$, i.e., 40% margin) has to be considered to assure grid current controllability in case of transients. Further, to enable the use of high-performance GaN MOSFETs with rated voltage $U_{\mathrm{R}} = 150\,\mathrm{V}$ in the S-Link H-bridge switching stage with a 1/3 U_{R} blocking voltage margin, the maximum buffer voltage has to be limited to values $U_{\mathrm{buf,max}} \leq 2/3U_{\mathrm{R}} = 100\,\mathrm{V}$.

For defined values of $U_{\mathrm{buf,max}}$ and C_{buf}, the resulting buffer voltage-swing $\Delta U_{\mathrm{buf}} = U_{\mathrm{buf,max}} - U_{\mathrm{buf,min}}$ is directly defined by the energy storage requirement $\Delta E_{\mathrm{buf}} = \frac{1}{2}C_{\mathrm{buf}}(U^2_{\mathrm{buf,max}} - U^2_{\mathrm{buf,min}}) = 406\,\mathrm{mJ}$. The three-phase S-Link operation is, however, well conditioned in a sense that the minimum buffer voltage $U_{\mathrm{buf,min}}$ occurs in the close vicinity of the S-Link output voltage u_{f} zero crossing (see **Fig. 1**). With the S-Link duty cycle $d_{\bar{\mathrm{x}}\mathrm{y}}$ according to (5) being a function of the buffer voltage $U_{\mathrm{buf}}(t)$ the analytic expression for the minimally required buffer capacitor value C_{buf} to maintain the desired duty cycle limitation $d_{\mathrm{lim}} = 0.6$ becomes excessively complex. Hence, the buffer voltage U_{buf} and the resulting duty cycle $d_{\bar{\mathrm{x}}\mathrm{y}}$ is calculated iteratively in Matlab, decreasing the values of C_{buf} until the maximum value of $d_{\bar{\mathrm{x}}\mathrm{y}}(t)$ equals $d_{\mathrm{lim}} = 0.6$ as highlighted in **Fig. 3a**; $C_{\mathrm{buf}} = 135\,\mu\mathrm{F}$ results as minimum value. The buffer capacitor utilization can be defined as

$$\xi_{\mathrm{buf}} = \Delta E_{\mathrm{buf}}/(\frac{1}{2}C_{\mathrm{buf}}U^2_{\mathrm{buf,max}}), \tag{6}$$

and results here to $\xi_{\mathrm{buf}} = 60\%$. Note that by reducing the duty cycle margin to 30% (i.e., $d_{\mathrm{lim}} = 0.7$, depicted in **Fig. 3a**), the buffer capacitor could be decreased to $C_{\mathrm{buf}} = 83\,\mu\mathrm{F}$. However, there the remaining energy at the buffer voltage minimum $U_{\mathrm{buf,min}}$ is critically low (utilization of $\xi_{\mathrm{buf}} = 98\%$) and hence $C_{\mathrm{buf}} = 135\,\mu\mathrm{F}$ ($d_{\mathrm{lim}} = 0.6$) is considered in the following.

Here, the bulk capacitor C_{e} serves as the current return path for the ac component of the S-Link current $i_{\mathrm{f}} = i_{\mathrm{x}}$, i.e., $i_{\mathrm{e}}(t) = i_{\mathrm{x}}(t) - \bar{i}_{\mathrm{x}}$, and buffers an energy $\Delta E_{\mathrm{e}} = \Delta E_{\mathrm{buf}} = 406\,\mathrm{mJ}$ (see **Fig. 6b**). For a required maximum peak-to-peak voltage fluctuation of, e.g., $\Delta U_{\mathrm{e}} = 10\,\mathrm{V} = \Delta E_{\mathrm{e}}/(C_{\mathrm{e}}U_{\mathrm{dc}})$ a small series capacitor value $C_{\mathrm{e,min,1}} = 75\,\mu\mathrm{F}$ is sufficient in three-phase operation and the minimum capacitor value C_{e} is dominated by the storage requirement in *single-phase* operation.

B. Single-Phase Configuration

The single-phase grid voltage and current are defined by

$$\begin{aligned} u_{\mathrm{ac}}(t) &= \hat{U}_{\mathrm{ac}}\cos(2\pi f_{\mathrm{ac}}t), \\ i_{\mathrm{ac}}(t) &= \hat{I}_{\mathrm{ac}}\cos(2\pi f_{\mathrm{ac}}t), \end{aligned} \tag{7}$$

with the output power resulting to $P_{\mathrm{dc}} = \frac{1}{2}\hat{U}_{\mathrm{ac}}\hat{I}_{\mathrm{ac}} = 5.8\,\mathrm{kW}$ according to **Tab. I**.

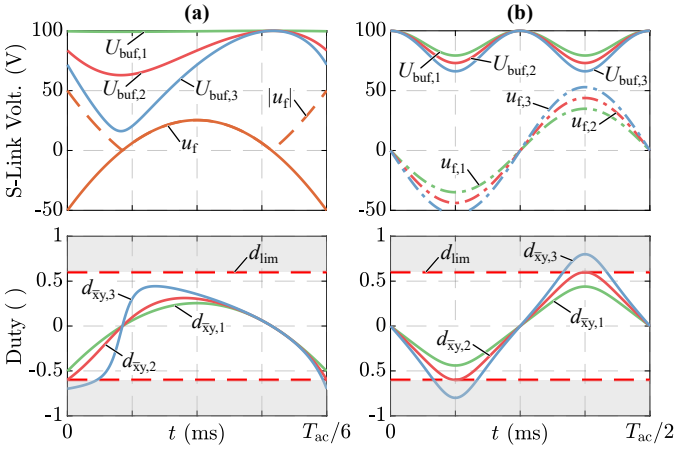

Fig. 3. **(a)** Simulated S-Link waveforms in three-phase operation within one sixth of a mains period $T_{\mathrm{ac}}/6$ for a constant maximum buffer voltage $U_{\mathrm{buf,max}} = 100\,\mathrm{V}$ and for decreasing buffer capacitor values $C_{\mathrm{buf},1} \to \infty$, $C_{\mathrm{buf},2} = 135\,\mu\mathrm{F}$ (the minimally required C_{buf} to limit $d_{\bar{\mathrm{x}}\mathrm{y}} \leq d_{\mathrm{lim}} = 0.6$), and $C_{\mathrm{buf},3} = 83\,\mu\mathrm{F}$. **(b)** Simulated S-Link waveforms in single-phase operation within one half mains period $T_{\mathrm{ac}}/2$ for a constant buffer capacitor value $C_{\mathrm{buf}} = 135\,\mu\mathrm{F}$ and a maximum buffer voltage $U_{\mathrm{buf,max}} = 100\,\mathrm{V}$, and for decreasing values of the bulk capacitor $C_{\mathrm{e},1} = 410\,\mu\mathrm{F}$, $C_{\mathrm{e},2} = 326\,\mu\mathrm{F}$, and $C_{\mathrm{e},3} = 270\,\mu\mathrm{F}$. The displayed waveforms represent the buffer capacitor voltage U_{buf}, the output voltage u_{f} (as well as the corresponding absolute value $|u_{\mathrm{f}}|$) and the duty cycle $d_{\bar{\mathrm{x}}\mathrm{y}}$. Note that in (a) the S-Link power p_{f} is independent of the selected value C_{buf} (as long as the desired voltage u_{f} can be generated) whereas in (b) the S-Link voltage u_{f} (and hence also the S-Link power p_{f}) increases with decreasing values of C_{e}.

1) Bulk Capacitor C_{e} Value: With the buffer capacitor $C_{\mathrm{buf}} = 135\,\mu\mathrm{F}$ and maximum voltage $U_{\mathrm{buf,max}} = 100\,\mathrm{V}$ defined, the bulk capacitance C_{e} has to be selected such that the S-Link buffering capabilities are not exceeded. In single-phase operation the grid input power pulsates with twice the mains frequency $f_{\mathrm{ac}} = 60\,\mathrm{Hz}$ and the ac-dc front-end current i_{x} and the S-Link current $i_{\mathrm{f}} = i_{\mathrm{e}}$ are defined as

$$\begin{aligned} i_{\mathrm{x}}(t) &= I_{\mathrm{dc}}(1 + \cos(4\pi f_{\mathrm{ac}}t)), \\ i_{\mathrm{f}}(t) &= i_{\mathrm{e}}(t) = i_{\mathrm{x}}(t) - I_{\mathrm{dc}} = I_{\mathrm{dc}}\cos(4\pi f_{\mathrm{ac}}t), \end{aligned} \tag{8}$$

i.e., with the S-Link SSB [8]–[10] processing the grid power pulsation. The resulting voltage fluctuation of the bulk capacitor voltage u_{e} and the S-Link voltage u_{f} are hence given by

$$\begin{aligned} u_{\mathrm{e}}(t) &= U_{\mathrm{dc}} + I_{\mathrm{dc}}\frac{\sin(4\pi f_{\mathrm{ac}}t)}{4\pi f_{\mathrm{ac}} \cdot C_{\mathrm{e}}}, \\ u_{\mathrm{f}}(t) &= U_{\mathrm{dc}} - u_{\mathrm{e}}(t) = -I_{\mathrm{dc}}\frac{\sin(4\pi f_{\mathrm{ac}}t)}{4\pi f_{\mathrm{ac}} \cdot C_{\mathrm{e}}}, \end{aligned} \tag{9}$$

with the voltage fluctuation of $u_{\mathrm{f}}(t)$ scaling proportional to the inverse of the bulk capacitor C_{e} value, thereby assuring a constant dc voltage $U_{\mathrm{dc}} = u_{\mathrm{xz}}$ in the ac-dc front-end and the isolated dc-dc converter. Hence, with (8) and (9) the instantaneous S-Link power p_{f} results to

$$p_{\mathrm{f}}(t) = u_{\mathrm{f}}(t) \cdot i_{\mathrm{f}}(t) = -I^2_{\mathrm{dc}}\frac{\sin(8\pi f_{\mathrm{ac}}t)}{8\pi f_{\mathrm{ac}} \cdot C_{\mathrm{e}}}, \tag{10}$$

varying with four times the grid frequency f_{ac}. Integration yields the minimum buffer capacitor energy storage requirement

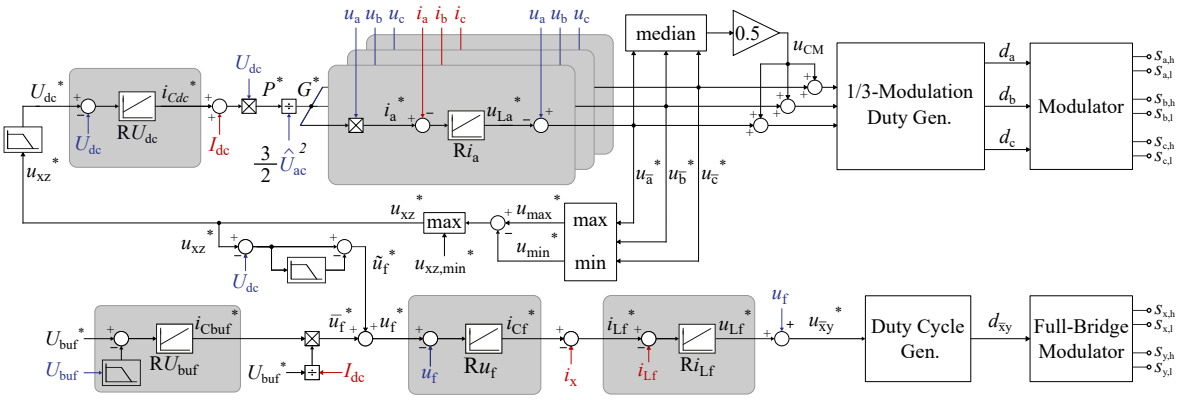

Fig. 4. Cascaded control structure of the proposed S-Link OBC for operation in a three-phase grid.

ΔE_{buf} as

$$\Delta E_{\mathrm{buf}} = \frac{I_{\mathrm{dc}}^2}{32\pi^2 f_{\mathrm{ac}}^2 \cdot C_{\mathrm{e}}}. \tag{11}$$

with ΔE_{buf} scaling with the inverse of the bulk capacitor C_{e} value. For a defined maximum buffer voltage $U_{\mathrm{buf,max}}$, the buffer capacitor energy results to

$$E_{\mathrm{buf}}(t) = \frac{1}{2} C_{\mathrm{buf}} U_{\mathrm{buf,max}}^2 + \frac{1}{2}\Delta E_{\mathrm{buf}}(\cos(8\pi f_{\mathrm{ac}} t) - 1) \tag{12}$$

which can be used to derived the time-varying buffer voltage $U_{\mathrm{buf}}(t) = \sqrt{2E_{\mathrm{Cbuf}}(t)/C_{\mathrm{buf}}}$ and **Fig. 3b** highlights simulated buffer voltage waveforms for several values of the bulk capacitor C_{e}. Note that here – in contrast to three-phase operation – the maximum value of the S-Link output voltage u_{f} is reached at the same point in time as the minimum value of the buffer voltage U_{buf}. Further, simple analytic expressions exist for $u_{\mathrm{f}}(t)$ and $U_{\mathrm{buf}}(t)$ such that the equation for the maximum tolerable value d_{lim} of the duty cycle $d_{\bar{\mathrm{x}}\mathrm{y}}$ according to (5) can be solved for the minimally required bulk capacitor value C_{e},

$$C_{\mathrm{e,min,2}} = \frac{P_{\mathrm{dc}}\sqrt{64\,\pi^2\,\mathrm{C_{buf}}^2\,U_{\mathrm{buf,max}}^2\,{U_{\mathrm{dc}}}^2\,f_{\mathrm{ac}}^2 + {\mathrm{P_{dc}}}^2\,{d_{\mathrm{lim}}}^2} + \mathrm{P_{dc}}^2\,d_{\mathrm{lim}}}{32\,\mathrm{C_{buf}}\,U_{\mathrm{buf,max}}^2\,{U_{\mathrm{dc}}}^2\,d_{\mathrm{lim}}\,f_{\mathrm{ac}}^2\,\pi^2} \tag{13}$$

resulting to $C_{\mathrm{e,min,2}} = 326\,\mu\mathrm{F}$ for the considered specifications in **Tab. I** and a 40% S-Link duty cycle margin. Note that, e.g., for a 20% S-Link duty cycle margin, C_{e} could be reduced to $270\,\mu\mathrm{F}$.

Aiming at a compact realization of the S-Link bulk capacitor C_{e}, high-performance electrolytic capacitors, e.g., $600\,\mathrm{V}$ / $82\,\mu\mathrm{F}$ B43541A8826M060 from TDK are considered here which, however, exhibit a $120\,\mathrm{Hz}$ ripple current limit of $1.6\,\mathrm{A_{RMS}}$ (i.e, $20\,\mathrm{mA_{RMS}}/\mu\mathrm{F}$), imposing a further limit for the minimally viable bulk capacitor value C_{e}. The resulting bulk capacitor RMS current stress results from (8) to $I_{\mathrm{e}} = I_{\mathrm{dc}}/\sqrt{2} = 7.6\,\mathrm{A_{RMS}}$ which translates into a minimum capacitor value of $C_{\mathrm{e,min,3}} = 384\,\mu\mathrm{F}$. Hence, C_{e} is selected to $C_{\mathrm{e}} = \max(C_{\mathrm{e,min,1}}, C_{\mathrm{e,min,2}}, C_{\mathrm{e,min,3}}) = 384\,\mu\mathrm{F}$, i.e., is limited by the ripple current limit of today's electrolytic capacitor technology, and can be realized by 5 parallel $82\,\mu\mathrm{F}$ capacitors resulting in a boxed volume of $110\,\mathrm{cm}^3$.

TABLE II
CONSIDERED S-LINK PARAMETERS.

f_{sw} [kHz]	C_{g} [nF]	L [µH]	$f_{\mathrm{sw,SLink}}$ [kHz]	L_{f} [µH]	C_{f} [µF]	C_{buf} [µF]	C_{e} [µF]
96	150	250	288	9.6	5	155	410

It is worth highlighting that in case of a traditional converter system without S-Link (i.e., the entire single-phase power pulsation is covered by the dc-link capacitor) a $2.9\,\mathrm{mF}$ capacitor would be required to limit the peak-to-peak dc-link voltage fluctuation to $10\,\mathrm{V}$, corresponding to a boxed volume of $770\,\mathrm{cm}^3$.

IV. CONTROL

In a next step, the S-Link concept and the derived design guidelines are verified by means of closed-loop circuit simulations in PLECS and this section derives the required control concepts. The employed component values are summarized in **Tab. II**. Note that C_{buf} was slightly increased to $155\,\mu\mathrm{F}$ to provide sufficient buffering capacity when also considering a small dc-link capacitor in the ac-dc front-end (required for HF filtering and to provide a low inductance commutation loop) which also has to be charged and discharged by the S-Link in three-phase operation. The S-Link power semiconductors operate with a high switching frequency $f_{\mathrm{sw,SLink}} = 288\,\mathrm{kHz}$ (with 180° phase-shifted Pulsewidth Modulation (PWM) carriers for the two bridge-legs realizing an effective switching frequency doubling to $576\,\mathrm{kHz}$) allowing for a high control bandwidth and for small filter components $L_{\mathrm{f}} = 9.6\,\mu\mathrm{H}$ and $C_{\mathrm{f}} = 5\,\mu\mathrm{F}$; in contrast, the PFC ac-dc front-end employs a lower switching frequency $f_{\mathrm{sw}} = 96\,\mathrm{kHz}$.

A. Three-Phase Operation

Fig. 4 presents the cascaded closed-loop control structure of the S-Link OBC in three-phase configuration. There, the dc-link voltage regulator RU_{dc} defines a grid conductivity reference $G^* = \hat{I}_{\mathrm{ac}}^*/\hat{U}_{\mathrm{ac}}$, which is translated into sinusoidal grid current references with the desired amplitude and in phase

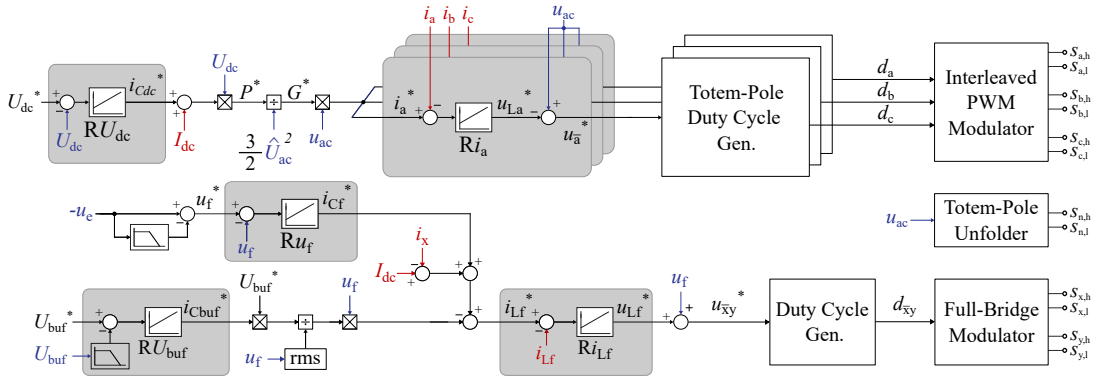

Fig. 5. Cascaded control structure of the proposed S-Link OBC for operation in a single-phase grid.

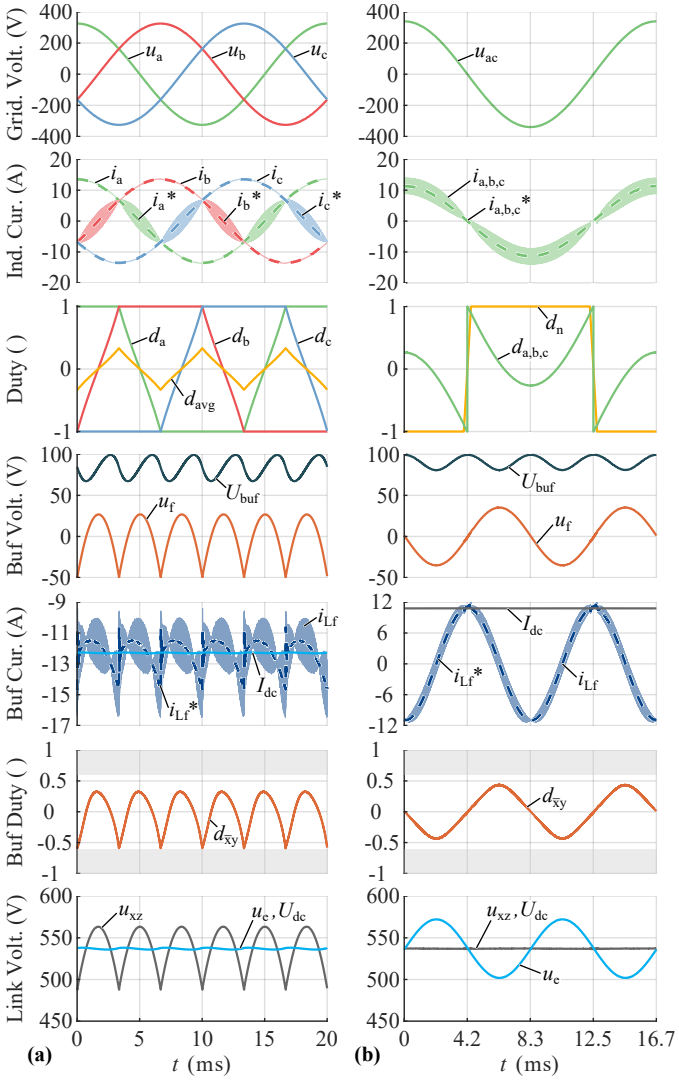

Fig. 6. Main S-Link OBC converter waveforms simulated in PLECS for **(a)** three-phase and **(b)** single-phase operation.

with the respective grid voltages. The grid currents are then tracked synergetically (i.e., with 1/3 modulation where the phase with the instantaneously maximum and minimum grid voltage are not switched) by the ac-dc front-end and the S-Link injection circuit: The grid current controllers Ri_{a},Ri_{b},Ri_{c} define a time-varying voltage reference $\tilde{u}_{\mathrm{f}}$ required to shape the grid currents, which is then tracked by the underlying S-Link voltage Ru_{f} and current Ri_{Lf} controller, where appropriate feedforward terms are used. Note that an additional voltage regulator RU_{buf} assures that the average buffer voltage U^*_{buf} is maintained by injecting an LF buffer voltage reference $\bar{u}^*_{\mathrm{f}}$ into the S-Link output voltage reference, which results in a net power consumption (to compensate the S-Link component losses) within the time period $T_{\mathrm{ac}}/6$.

Fig. 6a presents the simulated S-Link OBC waveforms in a three-phase grid with a line-to-neutral voltage $U_{\mathrm{ac}} = 230\,\mathrm{V_{RMS}}$, a dc-link voltage $U_{\mathrm{dc}} = 538\,\mathrm{V}$ and the nominal output power of $P_{\mathrm{dc}} = 6.6\,\mathrm{kW}$. In three-phase operation (**Fig. 6a**) only one of the three ac-dc front-end bridge-legs switches at HF (as can be observed from the duty cycles), and due to the dc-link-referenced filter capacitors C_{g} (see **Fig. 2**) no HF current ripple occurs in the clamped phases. Sinusoidal grid currents are enabled by the S-Link injecting the six-pulse voltage variation u_{f}, resulting in a power pulsation in the S-Link. Despite the associated fluctuation of the buffer capacitor voltage U_{buf}, the S-Link duty cycle $d_{\bar{\mathrm{x}}\mathrm{y}}$ remains within the desired band of $d_{\bar{\mathrm{x}}\mathrm{y}} \in [-0.6, 0.6]$ and the maximum buffer voltage constraint of $U_{\mathrm{buf}} \leq 100\,\mathrm{V}$ is respected.

B. Single-Phase Operation

Fig. 5 presents the cascaded closed-loop control structure of the S-Link OBC in single-phase configuration. In contrast to the three-phase operation, all phases of the ac-dc front-end are parallel-connected (with 120° phase-shifted PWM carriers for interleaved operation with a reduced HF filtering demand). The totem-pole unfolder is now active and connects the grid neutral n to either the positive or the negative dc-link rail (based on the polarity of the grid voltage u_{ac}) to enable the generation of bipolar voltages. The S-Link acts now as a compensating SSB with the ac fluctuation of the bulk capacitor voltage u_{e} fed as a reference signal into the S-Link output voltage regulator Ru_{f}.

Fig. 6b presents the simulated S-Link OBC waveforms in a single-phase grid with a line-to-neutral voltage $U_{\mathrm{ac}} = 240\,\mathrm{V_{RMS}}$, a dc-link voltage $U_{\mathrm{dc}} = 540\,\mathrm{V}$ and the nominal

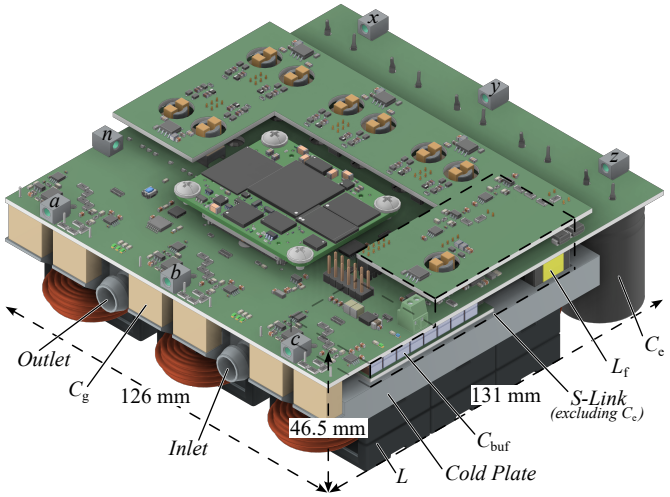

Fig. 7. 3D CAD rendering of a 6.6 kW S-Link OBC (not including the isolated dc-dc converter) according to **Tab. I**; the employed circuit parameters are listed in **Tab. II**. The system dimensions are $126 \times 131 \times 46.5\,\mathrm{mm}^3$, resulting in a volumetric power density of $8.6\,\mathrm{kW/dm^3}$ ($140\,\mathrm{W/in^3}$).

output power of $P_{\mathrm{dc}} = 5.8\,\mathrm{kW}$. Despite the pulsating single-phase input power leading to a large variation in the bulk capacitor voltage u_{e}, the input voltage of the dc-dc converter $U_{\mathrm{dc}} = u_{\mathrm{xz}}$ remains ideally constant. The fluctuation of the buffer voltage U_{buf} is reduced compared to three-phase operation, and its average value $\bar{U}_{\mathrm{buf}}$ could be reduced to decrease the hard-switching losses of the S-Link power semiconductors while maintaining the desired duty cycle $d_{\bar{\mathrm{xy}}}$ margin.

V. Conclusion

An On-Board Charger (OBC) must be able to charge Electric Vehicle (EV) batteries from both, a three-phase mains and a single-phase mains, and compact and lightweight converter realizations are required. This paper proposes the novel Smart-dc-Link (S-Link) concept, which improves the OBC performance by enabling higher conversion efficiencies and allowing to reduce the dc-link capacitor value and/or volume. The concept is systematically derived, and design guidelines for the sizing of the main S-Link energy storage components are provided. Further, the required cascaded control concepts for single-phase and three-phase operation are elaborated and the S-Link concept is verified by means of circuit simulations in PLECS. A 6.6 kW S-Link OBC prototype featuring a power density of $8.6\,\mathrm{kW/dm^3}$ is currently under development, and a 3D CAD rendering of the system is depicted in **Fig. 7**.

References

[1] K. Anastasiadou and N. Gavanas, "State-of-the-art review of the key factors affecting electric vehicle adoption by consumers," *Energies*, vol. 15, no. 24, p. 9409, Dec. 2022.

[2] M. Shahjalal, T. Shams, M. N. Tasnim, M. R. Ahmed, M. Ahsan, and J. Haider, "A critical review on charging technologies of electric vehicles," *Energies*, vol. 15, no. 21, p. 8239, Nov. 2022.

[3] J. Yuan, L. Dorn-Gomba, A. D. Callegaro, J. Reimers, and A. Emadi, "A review of bidirectional on-board chargers for electric vehicles," *IEEE Access*, vol. 9, pp. 51 501–51 518, 2021.

[4] M. Hagemeyer, P. Wallmeier, F. Schafmeister, and J. Böcker, "Comparison of unidirectional three- and four-wire-based boost PFC-rectifier topologies for non-isolated three-phase EV on-board chargers under common-mode aspects," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Phoenix, AZ, USA, Jun. 2021, pp. 569–576.

[5] P. Papamanolis, D. Bortis, F. Krismer, D. Menzi, and J. W. Kolar, "New EV battery charger PFC rectifier front-end allowing full power delivery in 3-phase and 1-phase operation," *Electronics*, vol. 10, no. 17, p. 2069, Aug. 2021.

[6] B. Strothmann, G. Book, F. Schafmeister, and J. Böcker, "Single-phase operation of common-mode-free bidirectional three-phase PFC-rectifier for non-isolated EV charger with minimized DC-link," in *Proc. Power Convers. Intelligent Motion Conf. (PCIM Europe)*, Nuremberg, Germany, May 2021.

[7] D. Neumayr, D. Bortis, and J. W. Kolar, "Ultra-compact power pulsation buffer for single-phase DC/AC converter systems," in *Proc. IEEE Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia)*, Hefei, China, May 2016, pp. 2732–2741.

[8] S. Qin, Y. Lei, C. Barth, W.-C. Liu, and R. C. N. Pilawa-Podgurski, "Architecture and control of a high energy density buffer for power pulsation decoupling in grid-interfaced applications," in *Proc. IEEE Workshop Control Modeling Power Electron. (COMPEL)*, Vancouver, Canada, Jul. 2015.

[9] ——, "A high-efficiency high energy density buffer architecture for power pulsation decoupling in grid-interfaced converters," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE USA)*, Montreal, Canada, Sep. 2015, pp. 149–157.

[10] Z. Liao, N. C. Brooks, and R. C. Pilawa-Podgurski, "Design constraints for series-stacked energy decoupling buffers in single-phase converters," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7305–7308, Sep. 2018.

[11] K. Rigbers, P. Lürkens, M. Wendt, S. Schröder, U. Böke, and R. W. De Doncker, "High-efficient soft-switching converter for three-phase grid connections of renewable energy systems," in *Proc. Int. Conf. Power Electron. Drives Syst. (PEDS)*, Kuala Lumpur, Malaysia, Nov. 2005, pp. 246–250.

[12] M. Antivachis, J. Azurza Anderson, D. Bortis, and J. W. Kolar, "Analysis of a synergetically controlled two-stage three-phase DC/AC buck-boost converter," *CPSS Trans. Power Electron. Appl.*, vol. 5, no. 1, pp. 34–53, Mar. 2020.

[13] J. Azurza Anderson, M. Haider, D. Bortis, J. W. Kolar, M. Kasper, and G. Deboy, "New synergetic control of a 20kW isolated Vienna rectifier front-end EV battery charger," in *Proc. IEEE Workshop Control Modeling Power Electron. (COMPEL)*, Toronto, Canada, Jun. 2019.

[14] T. Meynard and H. Foch, "Multi-level choppers for high voltage applications," *EPE Journal*, vol. 2, no. 1, pp. 45–50, Jan. 1992.

[15] Y. Lei, C. Barth, S. Qin, W. C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. Pilawa-Podgurski, "A 2-kW single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8570–8581, Nov. 2017.