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Comparative Evaluation of Three-Phase-Unfolder-Based MVAC-LVDC Solid-State Transformers

Jonas Huber [1], Uwe Drofenik[2], Francisco Canales[3], Johann W. Kolar [1]

[1] ETH Zurich, Switzerland
[2] TU Wien, Austria
[3] ABB Switzerland Ltd., Switzerland

Corresponding author: Jonas Huber, huber@lem.ee.ethz.ch
Speaker: Jonas Huber, huber@lem.ee.ethz.ch

Abstract

Solid-state transformers (SSTs) for MVac-LVdc conversion, e.g., in future high-power EV charging stations, should feature low conversion losses and low complexity. Therefore, topologies based on a three-phase unfolder, i.e., a six-pulse rectifier, which thus eliminate PFC rectifier input stages and instead rely on modular dc-dc isolation stages for sinusoidal input current shaping, are of high interest. This paper discusses state-of-the-art and new topologies in this category, explains the operating principles of the systems, and, finally, provides a comparative evaluation of the SST topologies concerning realization effort, component stresses, and general complexity.

1 Introduction

Solid-state transformers (SSTs) have been proposed for various applications like traction and future smart grids or dc distribution systems [1], [2]. In particular, SSTs are also considered for supplying low-voltage dc (LVdc) loads from the medium-voltage ac (MVac) three-phase mains, e.g., high-power EV charging stations [3]–[5], datacenters [6], or electrolyzers [7], where in all cases mostly unidirectional power flow is required.

To handle the MV input, SSTs typically employ input-series output-parallel (ISOP) arrangements of converter cells, e.g., in the per-phase branches of the well-known cascaded H-bridge (CHB) structure [8]. There, each cell contains an active ac-dc PFC rectifier stage and a downstream isolated dc-dc converter. Even if realized with only unidirectional power flow capability [9], the complexity is relatively high and each branch processes a single-phase power flow with a correspondingly large fluctuation at twice the mains frequency.

In contrast, this paper discusses SST topologies with a three-phase unfolder stage at the MVac input, i.e., a six-pulse (B6) rectifier [3], [4], [10]–[13]. Compared to fully phase-modular approaches like the CHB system, the unfolder stage improves the operating conditions of the converter branches that are arranged on the dc side and not directly connected to the MVac grid.[1] The then unipolar (but pulsating) input voltages facilitate the direct application of isolated dc-dc converter cells without ac-dc stages and the processed power is roughly constant.

Thus, **Section 2** summarizes the known B6-bridge-based MVac-LVdc SST topologies shown in **Fig. 1** and **Section 3** introduces the new topologies from **Fig. 2**. **Section 4** provides a high-level comparative evaluation of all topologies and **Section 5** concludes the paper.

2 State-of-the-Art Topologies

For each considered topology, we introduce an idealized equivalent circuit, which is useful for explaining the operating principles and facilitates the derivation of straightforward yet meaningful indicators for realization efforts and component stresses. In the equivalent circuits (see, e.g., **Fig. 3**), controlled current sources model the output branches (OBs), i.e., the ISOP configuration of isolated dc-dc converters that deliver power to the LVdc load, and the injection branches (IBs), i.e., the series connections of half-bridge cells (HBCs) or full-bridge cells

[1] Note that there is a structural but not operational similarity to “controlled transition bridge” converters [14]. Further, there are topologies that integrate a B6 rectifier with a non-modular isolation stage, but these are limited in power rating due to discontinuous input currents [5].

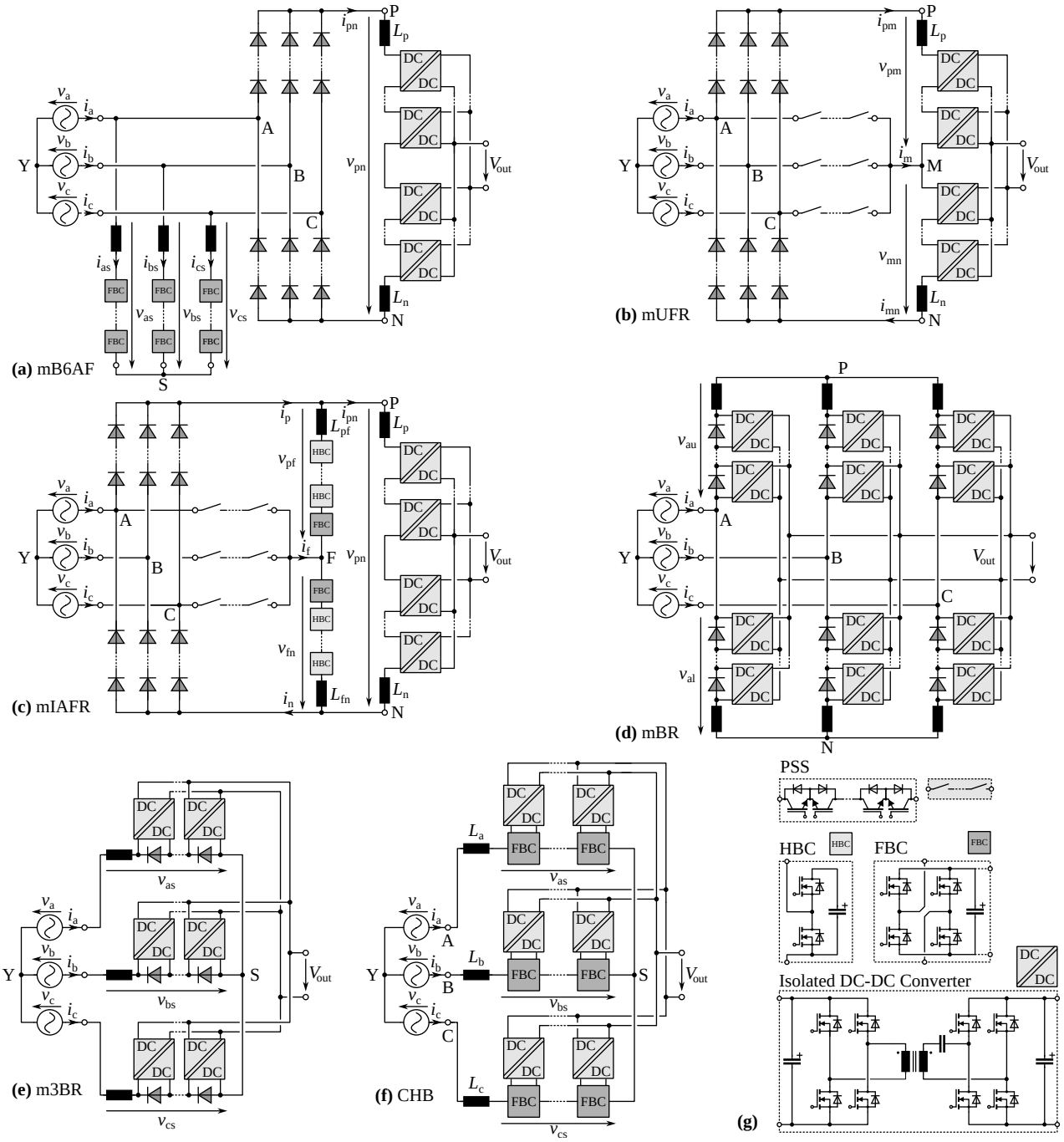

Fig. 1: State-of-the-art MVac-LVdc SST topologies discussed in **Section 2**. **(a)** mB6AF; **(b)** mUFR [15]; **(c)** mIAFR [3], [10]; **(d)** mBR [4], [11]; **(e)** mB3R [12], [13]. **(f)** CHB (for reference). **(g)** Legend.

(FBCs) that only process reactive power. Simple control block diagrams explain the generation of the OB and IB current or voltage references from an exemplary reference power flow, $P^* = 1\,\mathrm{MW}$, and for ohmic mains behavior achieved by using the reference conductance $G^* = P^*/V_\mathrm{g}^2$ ($V_\mathrm{g} = 10\,\mathrm{kV}$ is the MVac mains line-to-line rms voltage) to obtain phase current references that are proportional to the phase voltages. Further, the mains voltages define the B6 rectifier switching state such that always the phase with the maximum voltage is connected to the dc-side terminal P and the phase with the minimum voltage to N. It is thus useful to define a mapping of the phase voltages (and currents) v_a, v_b, and v_c to v_max, v_mid, and v_min such that $v_\mathrm{max} > v_\mathrm{mid} > v_\mathrm{min}$; the mapping changes in each 60 °-wide sector of the mains period.

2.1 mB6AF: B6 Rectifier with Active Filter

The mB6AF (**Fig. 1a** and **Fig. 3**) features a B6 rectifier, one OB that operates from the characteristic

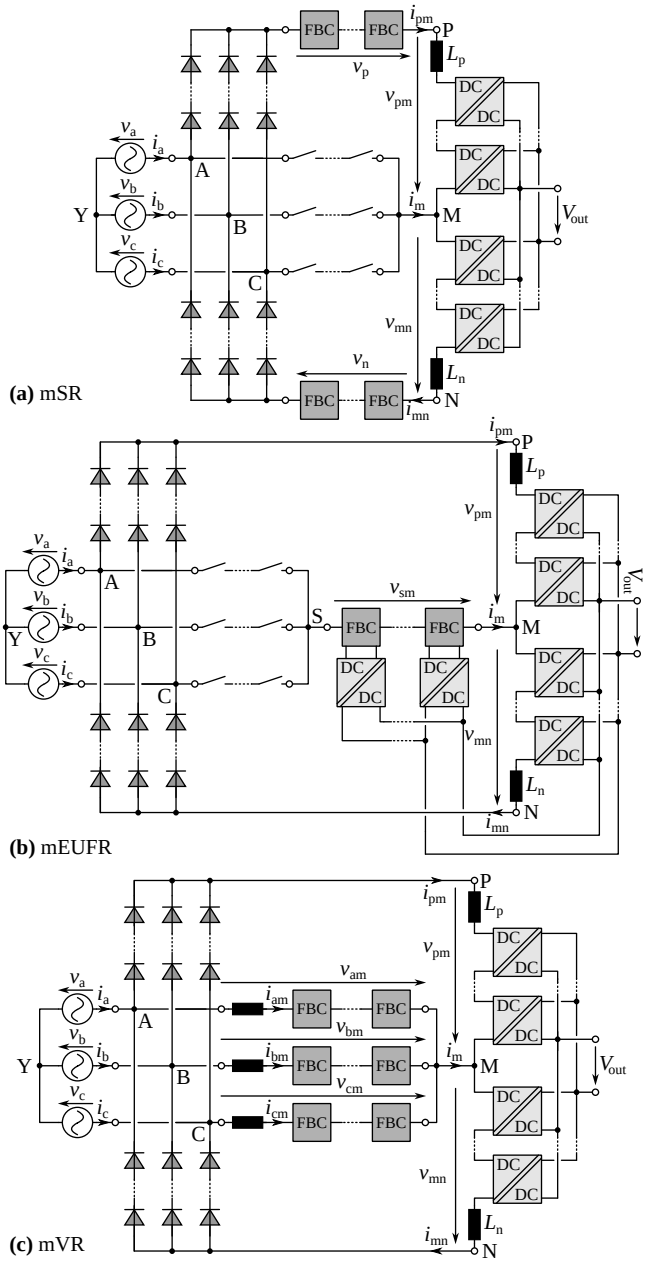

Fig. 2: Proposed MVac-LVdc SST topologies discussed in **Section 3.** **(a)** mSR; **(b)** mEFUR; **(c)** mVR.

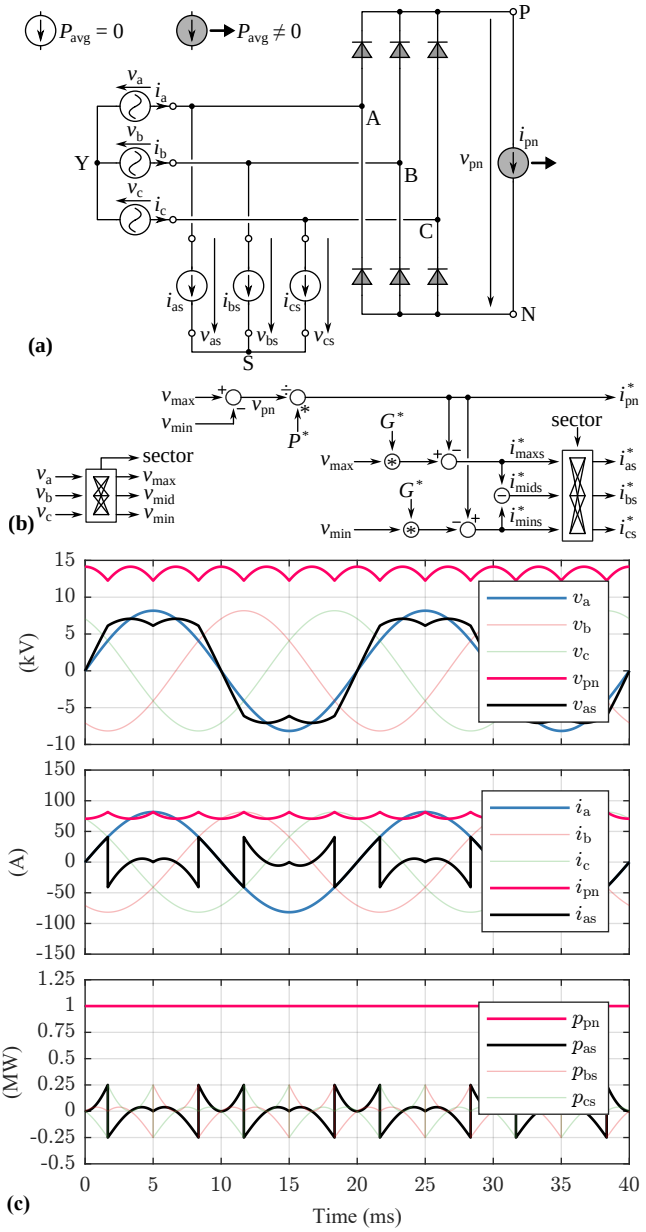

Fig. 3: mB6AF (see **Fig. 1a**). **(a)** Idealized equivalent circuit, **(b)** generation of OB and IB current references, and **(c)** simulated key waveforms.

six-pulse-shaped dc-side voltage $v_{\rm pn} = v_{\rm max} - v_{\rm min}$, and an ac-side active filter (AF) consisting of three IBs with FBCs.[2] Controlling the OB input current to $i^*_{\rm pn} = P^*/v_{\rm pn}$ results in constant power flow P^*. The IB current references are calculated such that the AF compensates harmonic distortions (i.e., the average power processed by the IBs is zero) of the diode rectifier with impressed output current $i_{\rm pn}$, resulting in sinusoidal phase currents and ohmic mains behavior.

[2]Note that a local, slow control loop regulates the average value of the floating FBC dc capacitor voltage, compensating losses.

2.2 mUFR: Modular Unfolder Rectifier

The mUFR shown in **Fig. 1b** and in **Fig. 4** is a direct extension of the non-modular LV variant proposed in [15] to MV applications. In contrast to the mB6AF, the mUFR features two OBs and a thus formed node M. There is no AF (no IBs), but three four-quadrant phase-selector switches (PSSs) can connect one phase terminal at a time to M. The OB currents $i_{\rm pm}$ and $i_{\rm mn}$ directly define the max. and min. phase currents, respectively, and the PSSs route the current $i_{\rm m} = i_{\rm mn} - i_{\rm pm}$ to the mid phase. Whereas thus sinusoidal mains currents result, the two OB input voltages $v_{\rm pm}$ and $v_{\rm mn}$ vary widely be-

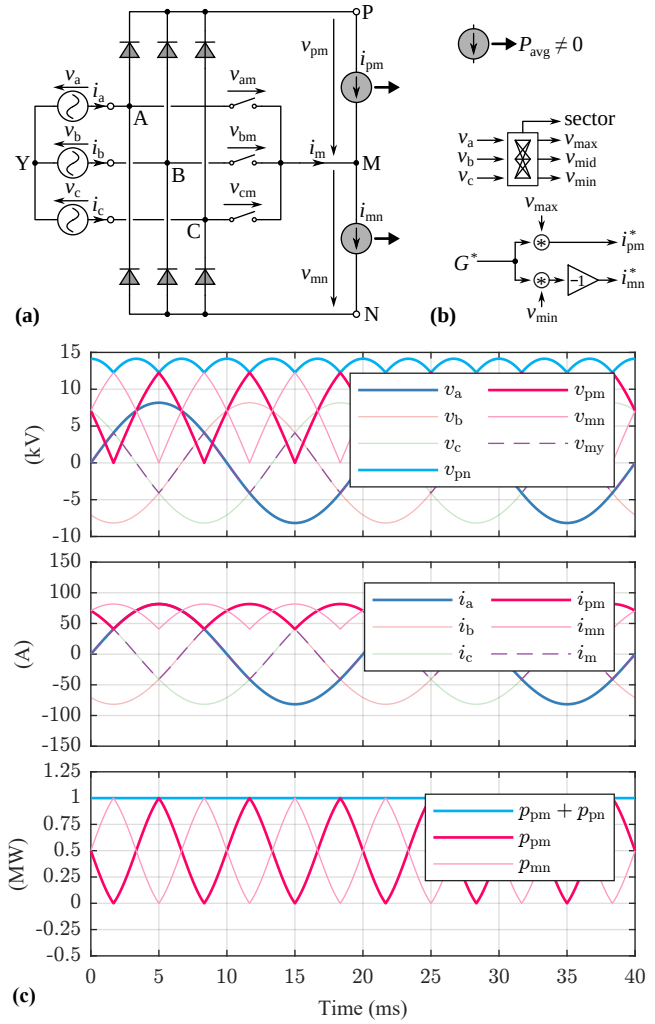

Fig. 4: mUFR (see **Fig. 1b**). **(a)** Idealized equivalent circuit, **(b)** generation of OB and IB current references, and **(c)** simulated key waveforms.

tween 0 V and $\sqrt{3/2}V_{\mathrm{g}}$, and each OB processes power fluctuating between zero and the total output power.

2.3 mIAFR: Modular Integrated Active Filter Rectifier

The mIAFR (see **Fig. 1** and **Fig. 5a**) has been proposed in [10] and then analyzed in [3]; it is a modularized MV version of the well-known LV IAF rectifier [16], [17]. In essence, the ac-side AF of the mB6AF is moved to the dc-side, leaving the operation of the OB with $i^*_{\mathrm{pn}} = P^*/v_{\mathrm{pn}}$ unchanged. However, three PSSs and two IBs suffice for implementing the AF functionality by injecting a current that is proportional to v_{mid} into the mid phase. The IB voltages v_{pf} and v_{fn} are always positive and therefore the IBs employ HBCs only.[3] The IB voltages and

[3]Note that practical realizations require one FBC in each IB to compensate inductive voltage drops [3], [10].

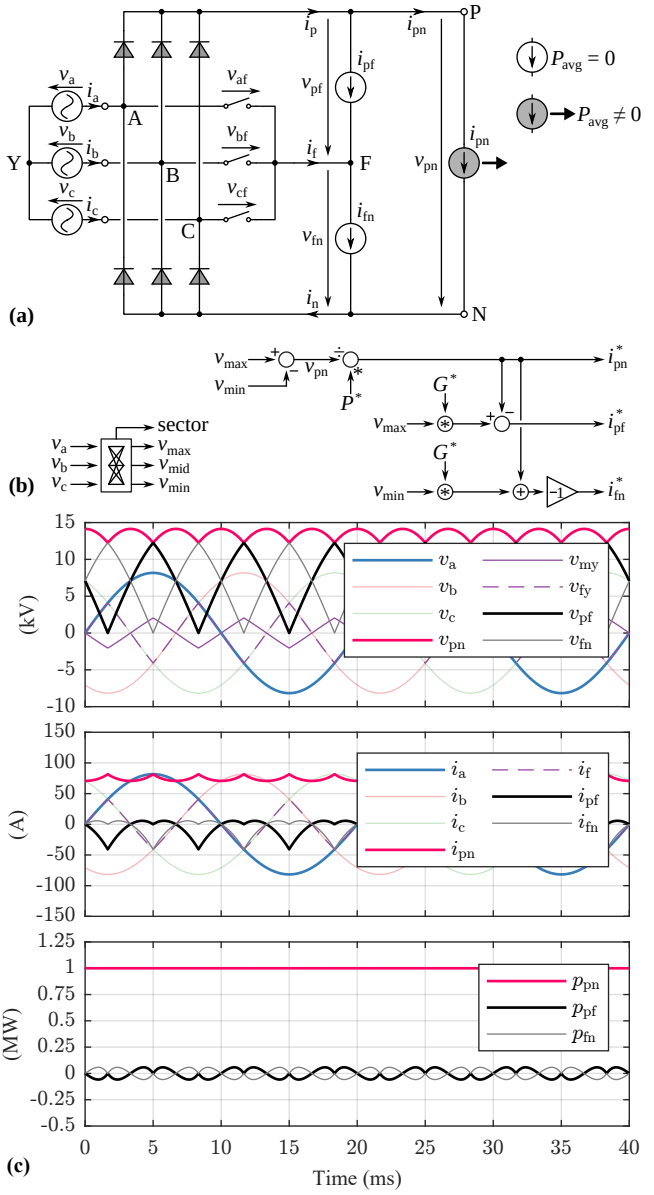

Fig. 5: mIAFR (see **Fig. 1c**). **(a)** Idealized equivalent circuit, **(b)** generation of OB and IB current references, and **(c)** simulated key waveforms.

the processed phase current i_{mid}, advantageously, result in relatively low IB peak power and low power fluctuation. On the other hand, v_{pf} and v_{fn} vary between zero and $\sqrt{3/2}V_{\mathrm{g}}$ (as the mUFR OB voltages discussed in **Section 2.2**) and hence *each* IB requires almost as many converter cells as the OB.

2.4 mBR: Modularized Bridge Rectifier

An alternative way of utilizing a B6 rectifier has been proposed in [4] and analyzed in [11]: The mBR shown in **Fig. 1d** and in **Fig. 6** uses the voltages across blocking rectifier diodes as unipolar supply voltages for isolated dc-dc converters connected in parallel to the diodes; i.e., the OBs are integrated into the B6 rectifier, which, advanta-

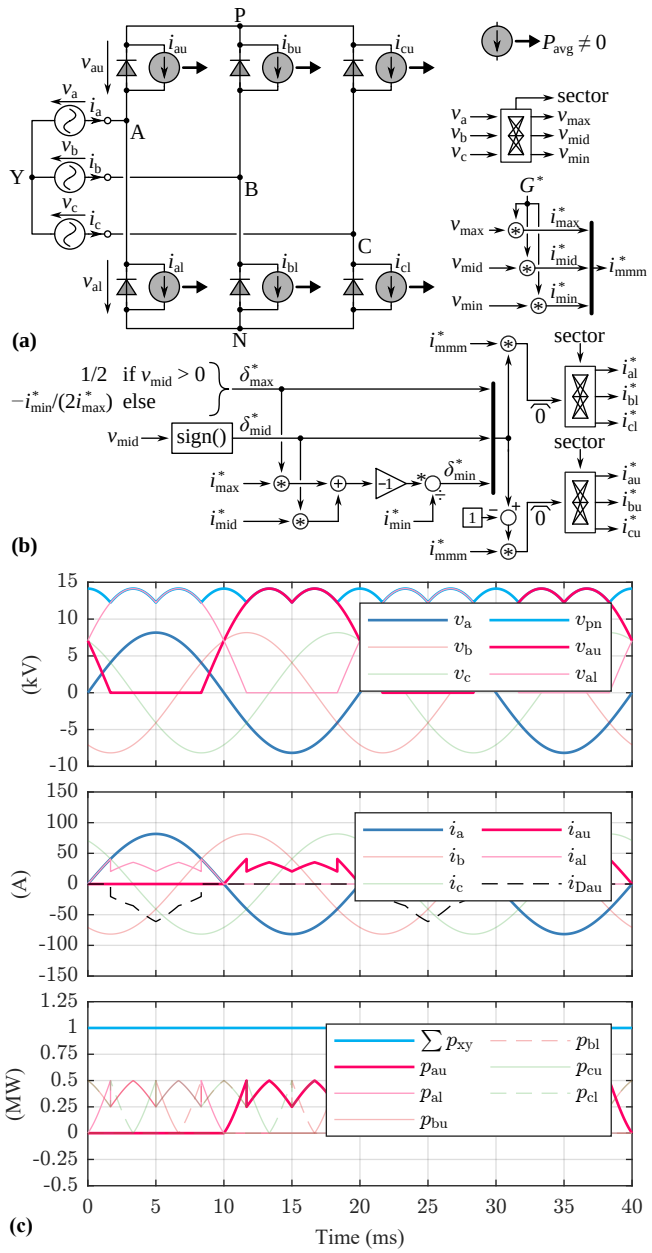

Fig. 6: mBR (see **Fig. 1d**). **(a)** Idealized equivalent circuit, **(b)** generation of OB and IB current references, and **(c)** simulated key waveforms.

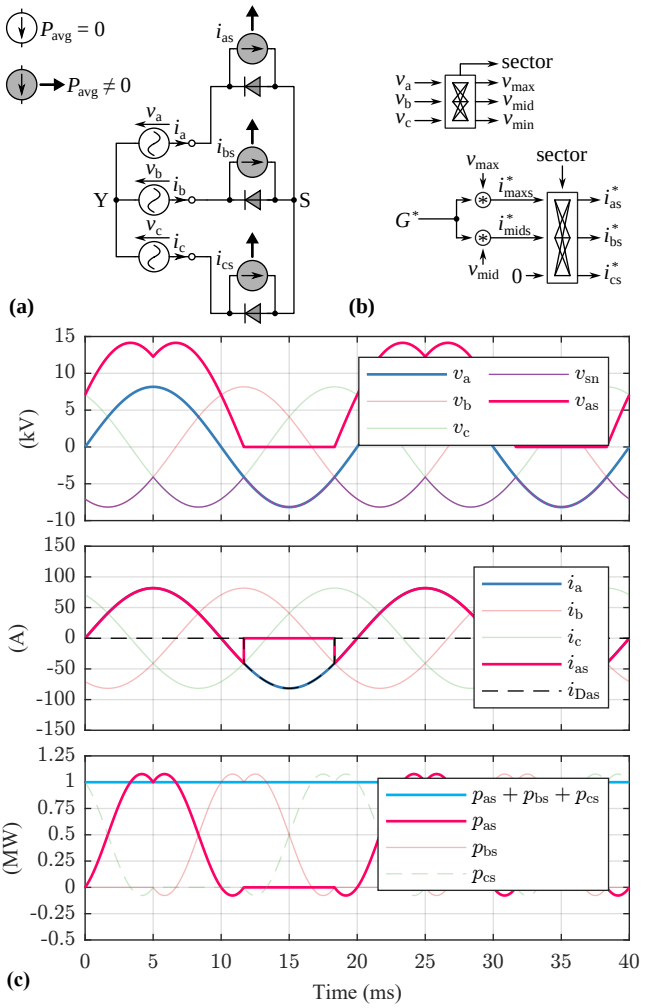

Fig. 7: mB3R (see **Fig. 1e**). **(a)** Idealized equivalent circuit, **(b)** generation of OB and IB current references, and **(c)** simulated key waveforms.

geously, ensures defined voltage sharing among the series-connected diodes. Still, the mains voltages define the conduction state of the B6 bridge and thus which OBs have a non-zero input voltage needed for drawing power. Specifically, the lower diode of the max. phase, the upper diode of the min. phase, and both diodes of the mid phase are blocking. The direction of the mid phase current defines whether the upper or the lower OB should impress this current and thus deliver power to the output, i.e., $\delta^*_{\mathrm{mid}} = \mathrm{sign}(v_{\mathrm{mid}}) = \pm 1$ with δ denoting the share of the respective phase current provided by the respective lower OB. In contrast, δ^*_{max} and δ^*_{min} are degrees of freedom (coupled by Kirchhoff's current law in the nodes P and N) that allow optimization of the OB stresses [11]; here, δ^*_{max} and δ^*_{min} are selected such that the two active OBs (lower OB of the max. phase and upper OB of the min. phase) process equal power. Note that the resulting currents in the conducting diodes are non-zero but lower than in normal B6 operation. However, all 6 OBs must be rated for an input voltage of $v_{\mathrm{pn}} = v_{\mathrm{max}} - v_{\mathrm{min}}$, i.e., the line-to-line voltage magnitude, and at any given time, only 3 out of the 6 OBs deliver power to the load.

2.5 mB3R: Modularized B3 Rectifier

Similarly, the mB3R proposed in [12], [13] and shown in **Fig. 1e** and in **Fig. 7** employs a reduced B3 rectifier with isolated dc-dc converters connected in parallel to the diodes. Essentially, a single diode replaces the ac-dc converter stage used in conventional CHB-based SSTs (see **Sec-**

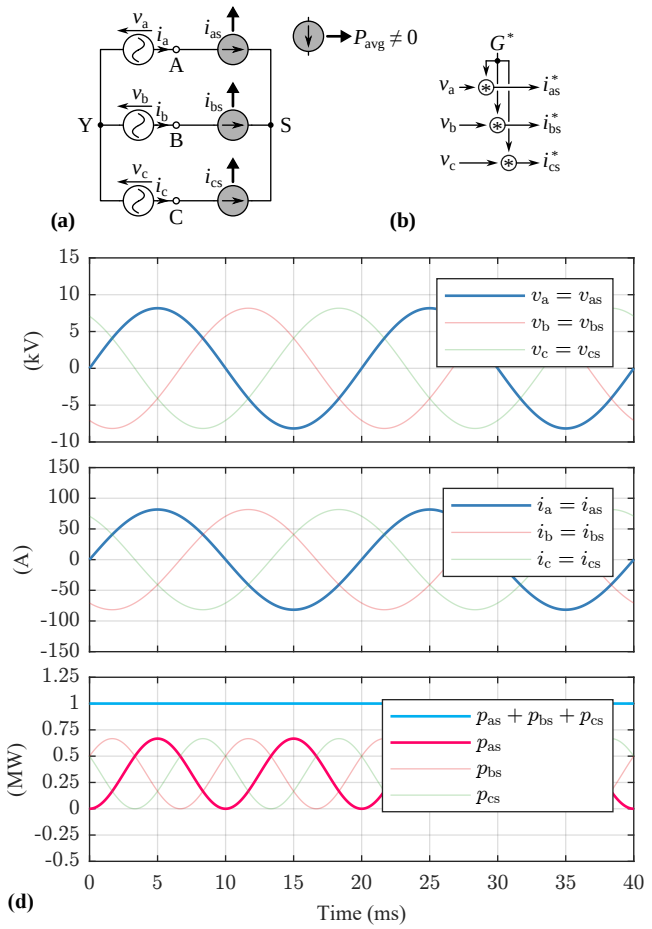

Fig. 8: CHB (see **Fig. 1f**). **(a)** Idealized equivalent circuit, **(b)** generation of OB and IB current references, and **(c)** simulated key waveforms.

tion 2.6), which comes at the price of large fluctuations of the voltage and power processed by the OBs.

2.6 CHB: Cascaded H-Bridge SST

For completeness, **Fig. 1f** and **Fig. 8** show the well-known CHB-based SST structure mentioned in the introduction. Unlike in the other topologies, the OBs process ac input voltages and currents, i.e., each cell consists of an ac-dc converter stage (i.e., an FBC) and an isolated dc-dc converter. Being a fully phase-modular system, each OB processes power that shows the characteristic twice-mains frequency fluctuation of single-phase systems.[4]

3 Proposed Topologies

This section introduces further MVac-LVdc SST topologies based on a B6 rectifier input stage.

[4]Alternatively, the power fluctuation could be buffered on the cells' MV side in correspondingly large capacitors.

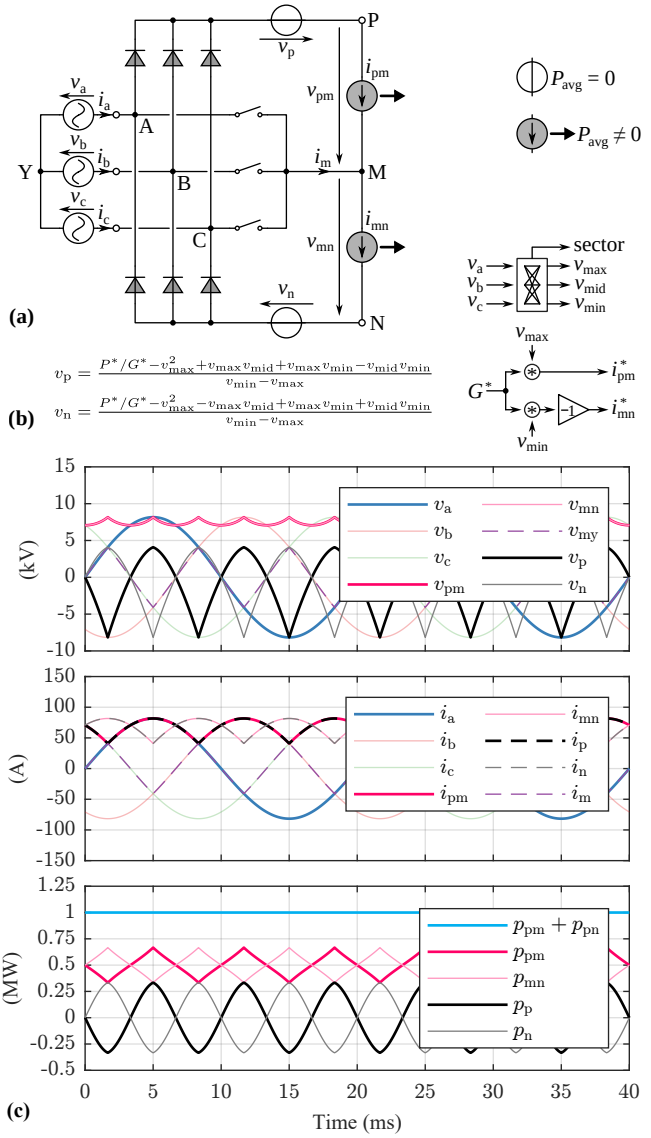

Fig. 9: mSR (see **Fig. 2a**). **(a)** Idealized equivalent circuit, **(b)** generation of OB and IB current references, and **(c)** simulated key waveforms.

3.1 mSR: Modular Swiss Rectifier

The proposed mSR shown in **Fig. 2a** and in **Fig. 9** follows from the mIAFR using duality considerations: whereas the mIAFR employs current-source-type IBs connected in parallel to the OB, the mSR uses voltage-source-type IBs connected in series to two OBs. The OBs form the dc midpoint M to which the PSS network connects. Structurally, the mSR is a modular extension of the LV Swiss rectifier [17]. As in the mUFR (see **Section 2.2**), the two OBs directly define the phase currents $i_{\max}$ and $i_{\min}$. Connecting the mid phase via the PSSs to M implies large voltages between the B6 bridge's dc terminals and M, which the mSR IBs provide (in contrast to the mUFR, where the OBs are subject to these voltage variations). Specifically, the selected

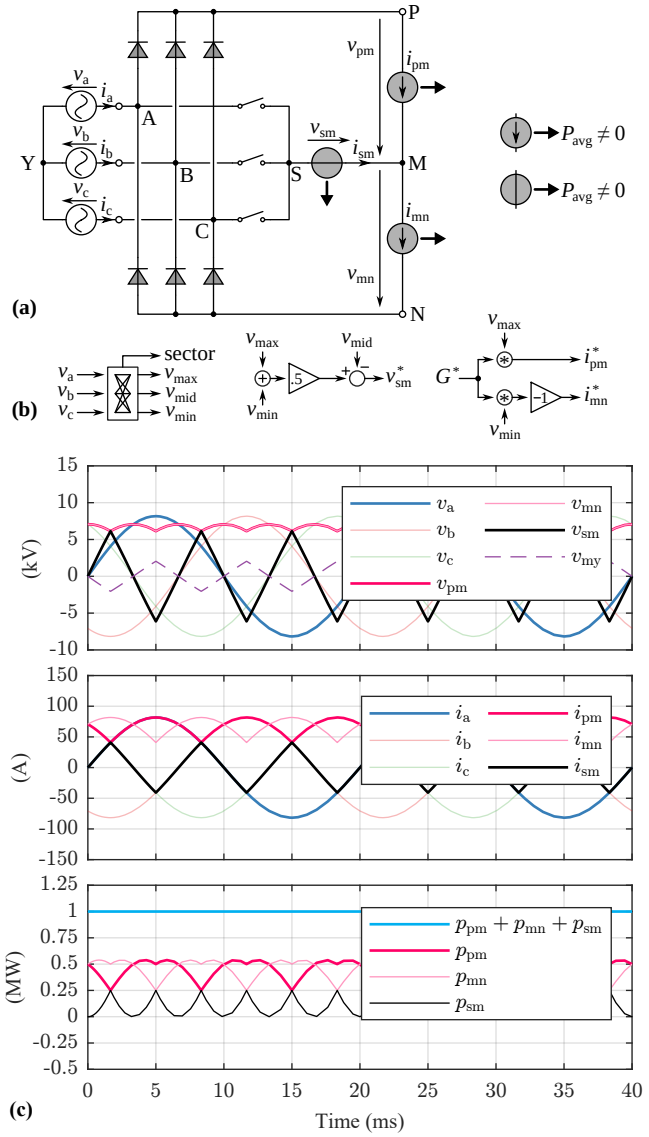

Fig. 10: mEUFR (see **Fig. 2b**). **(a)** Idealized equivalent circuit, **(b)** generation of OB and IB current references, and **(c)** simulated key waveforms.

IB voltage references v_{p}^* and v_{n}^* ensure equal and almost constant OB voltages ($v_{\mathrm{pn}} = v_{\mathrm{mn}}$).[5] However, v_{p}^* and v_{n}^* are ac voltages and hence the IBs must be realized with FBCs. As the IBs reside in the main dc current path (in series to the OBs), they process high power fluctuations, which implies relatively large energy buffering requirements.

3.2 mEUFR: Modular Extended Unfolder Rectifier

The mEUFR shown in **Fig. 2b** and in **Fig. 10** combines the mSR's two IBs into a single voltage-source-type IB connected between the dc midpoint M and the star-point S of the PSS network. The two OBs again directly impress the currents of the max. and the min. phase. The IB voltage reference v_{sm}^* follows from the requirement $v_{\mathrm{pm}} = v_{\mathrm{mn}}$, which implies $v_{\mathrm{my}} = 0.5(v_{\mathrm{max}} + v_{\mathrm{min}})$. However, the IB processes a non-zero average power, i.e., it's FBCs must be connected to isolated dc-dc converters, essentially forming a third OB that contributes to the total output power.

[5] Alternatively, equal power processed by the two OBs (i.e., $p_{\mathrm{pm}} = p_{\mathrm{mn}}$) could be achieved at the price of increased voltage requirements for the OBs and the IBs.

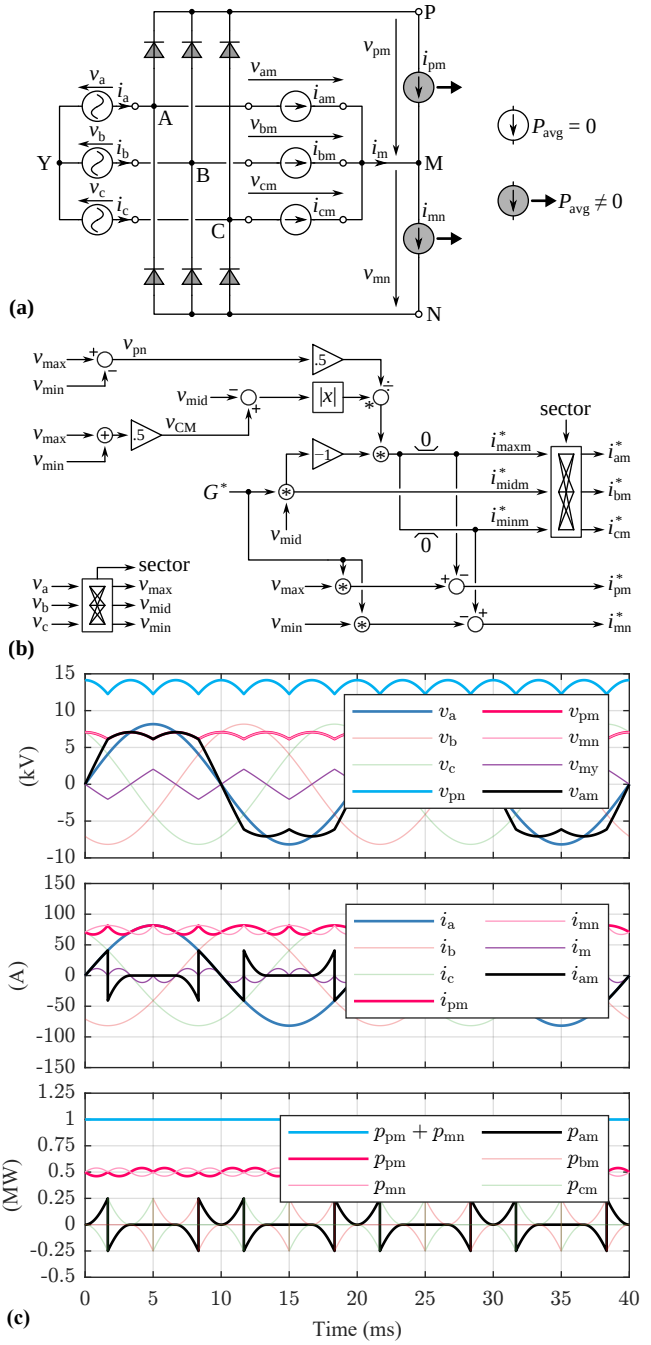

Fig. 11: mVR (see **Fig. 2c**). **(a)** Idealized equivalent circuit, **(b)** generation of OB and IB current references, and **(c)** simulated key waveforms.

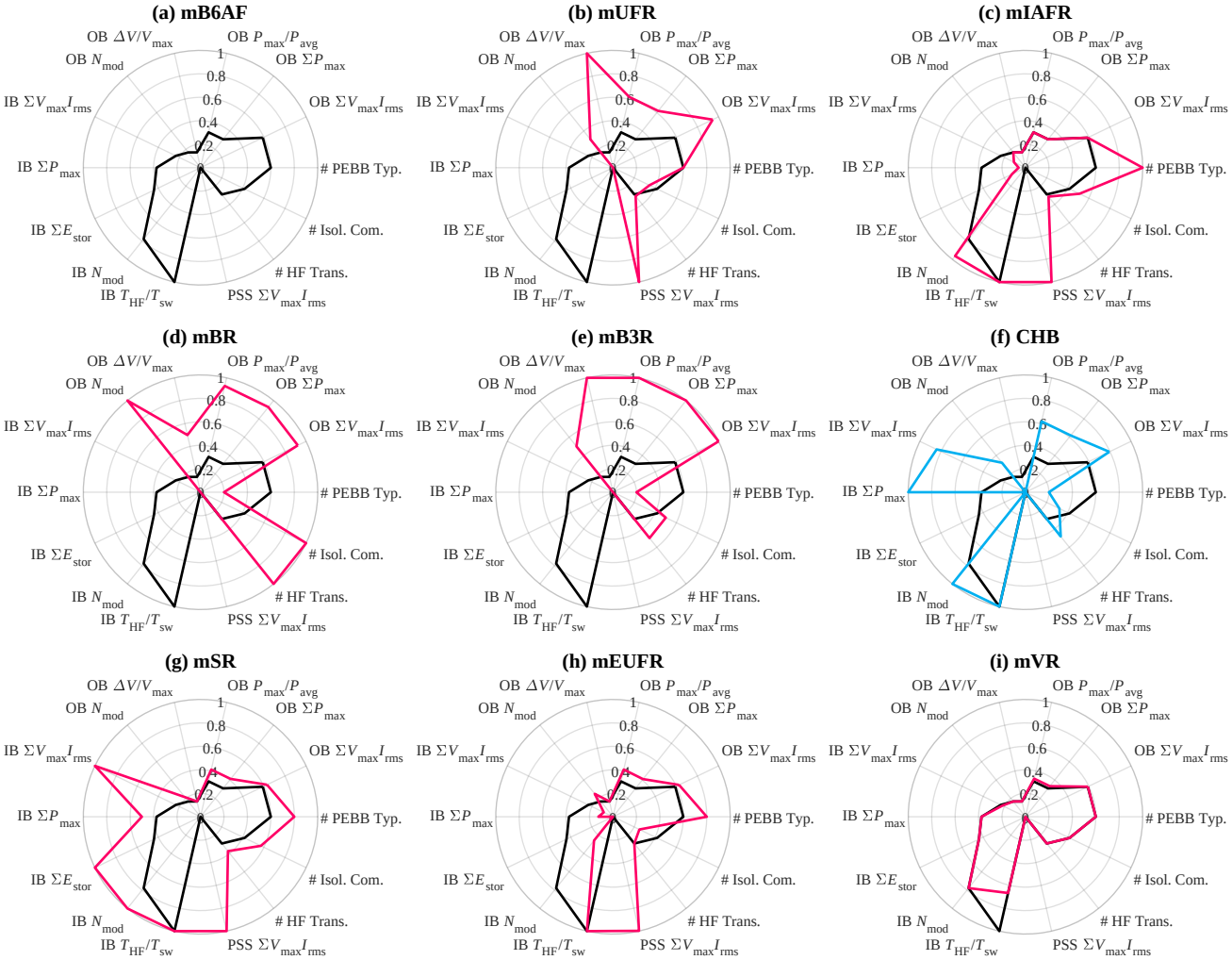

Fig. 12: Comparative evaluation. Smaller values indicated more favorable characteristics and the values on each axis are normalized to the respective maximum amongst all topologies; **Fig. 13** provides absolute values.

3.3 mVR: Modular Vienna Rectifier

Connecting the star-point S formed by the three IBs of the mB6AF (see **Section 2.1**) to a dc midpoint M formed by two OBs, the mVR topology shown in **Fig. 2c** and in **Fig. 11** results; the name follows from the close structural similarity to the LV Vienna Rectifier (VR) [18]. Inspired by an advantageous operating mode of LV VRs using pre-shaped dc-side voltages [19], the operating mode of the mVR ensures that only two out of the three IBs operate with high-frequency (HF) switching at any given time ("2/3-PWM"): **Fig. 11c** confirms that always one IB operates with zero current, i.e., all transistors of the FBCs can be turned off, avoiding switching losses. The price to pay is a minor fluctuation in the powers p_{pm} and p_{mn} processed by the OBs.

4 Comparative Evaluation

Based on the idealized equivalent circuits and considering exemplary specifications (10-kV line-to-line rms grid voltage, 1-MW output power, 1700-V transistors with 70% blocking voltage utilization, nominal maximum modulation index $M = 0.85$, 10% peak-to-peak IB capacitor LF voltage ripple), key indicators for realization efforts and component stresses of all discussed topologies are compared in **Fig. 12** and **Fig. 13**; the mB6AF is considered as a baseline: $\sum V_{\mathrm{max}} I_{\mathrm{rms}}$ represents the total installed converter power, i.e., isolated dc-dc converters for OBs, HBCs or FBCs (considering a factor 2 over HBCs) for the IBs. Similarly, $\sum P_{\mathrm{max}}$ is the sum of the peak power processed by the OBs or IBs, $P_{\mathrm{max}}/P_{\mathrm{avg}}$ quantifies the utilization of the OBs, and $\Delta V/V_{\mathrm{max}}$ characterizes the input voltage range of the dc-dc converters. N_{mod} gives the number of converter modules; for OBs, this corresponds to the number of medium-frequency transformers (MFTs) providing the galvanic separation between the MV and the LV side. $\sum E_{\mathrm{stor}}$ is the stored capacitive energy (not considering small capacitors

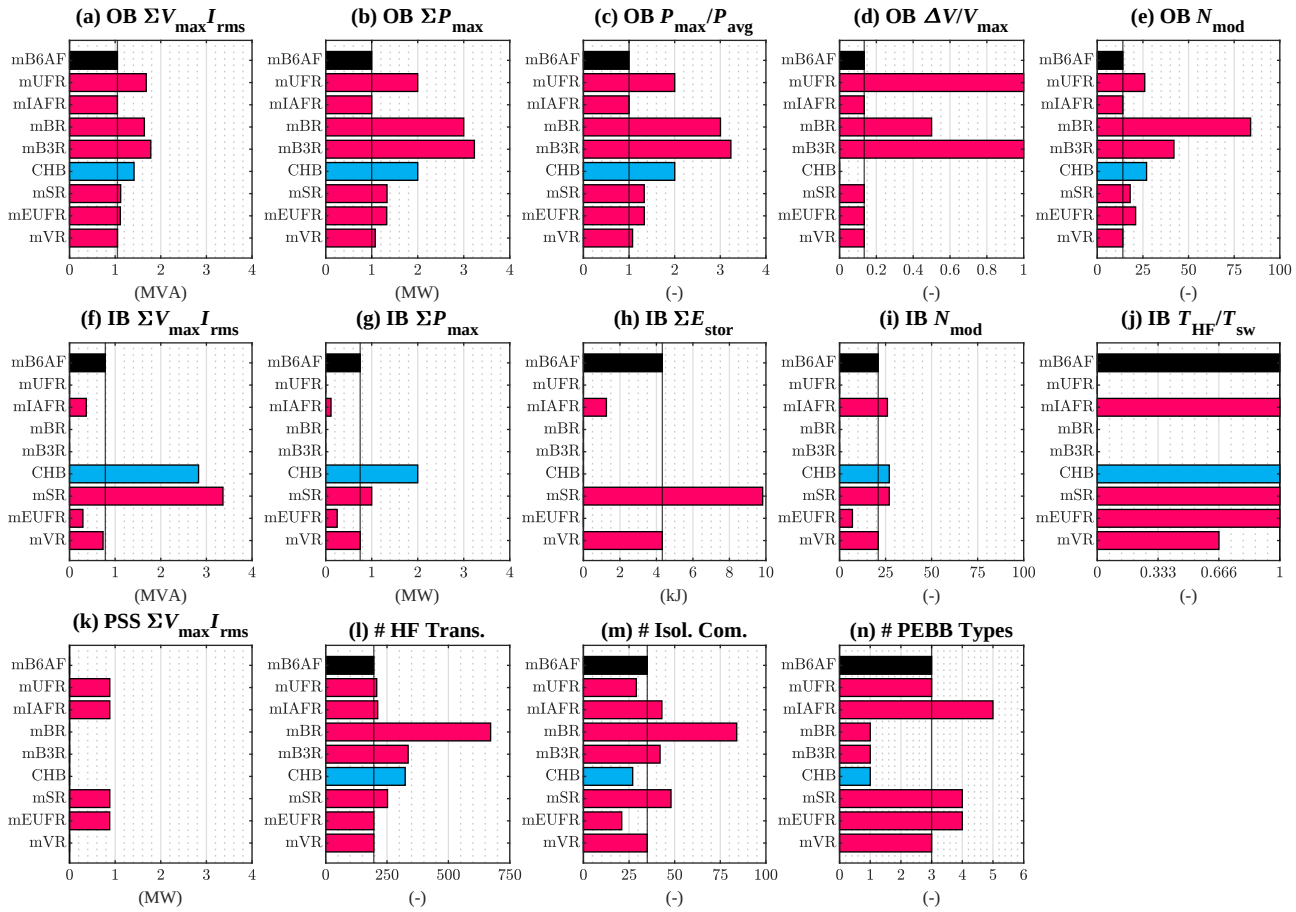

Fig. 13: Absolute values for the performance indicators used in the comparative evaluation from **Fig. 12** for 1-MW output power, 10-kV grid (line-to-line rms), 1700-V transistors (70% blocking voltage utilization), nominal maximum modulation index $M = 0.85$, and 10% peak-to-peak IB capacitor LF voltage ripple.

used solely for HF ripple filtering), and $T_{\mathrm{HF}}/T_{\mathrm{sw}}$ is the time share during which the IB converter cells switch with HF. Finally, the number of HF-operated transistors (i.e., excluding the PSSs that could be realized with elements of higher blocking voltage and slow switching speeds like 6.5-kV IGBTs), the number of isolated communication links between a central controller and the converter cells, and the number of different power-electronic building block (PEBB) types are given.

Interestingly, the conventional/baseline mB6AF performs very favorably in most dimensions. If PSSs are accepted (despite the potential issues with static and transient voltage sharing among series-connected devices), the mIAFR with the AF moved to the dc side is an interesting alternative; the mEUFR features overall fewer converter modules but requires two types of dc-dc converters with different power ratings. The mBR, the mB3R, and also the standard CHB solution[6] are highly modular (only one PEBB type), but suffer from relatively low utilization of the installed power electronics. The mSR does not show advantages, mostly because the IBs process the full dc-side current. Finally, the mVR shows very similar performance as the baseline mB6AF, but the "2/3-PWM" operating method reduces the switching losses of the IBs while introducing only a marginal fluctuation of the power processed by the OBs. Note that for many topologies, certain implementation variants and simplifications are conceivable; for example, replacing and/or complementing the diodes of the B6 bridge by anti-parallel switches (e.g., IGBTs, thyristors) facilitates bidirectional power flow.

5 Conclusion & Outlook

This paper provides an overview on existing and new three-phase-unfolder-based MVac-LVdc SST topologies. Based on idealized equivalent circuits, we explain the basic operating principles and provide a first comparative evaluation considering key

[6]The ac-dc stages in the converter cells are treated as IBs with FBCs.

indicators for the realization efforts, component stresses, and complexity. All in all, some (in particular, the mB6AF, the mIAFR, and the mVR) MVac-LVdc SSTs based on robust three-phase unfolder stages (B6 rectifiers) are interesting alternatives to fully modular systems, especially for high-power applications with (mostly) unidirectional power flow, e.g., for future high-power EV charging stations. Further research should extend the comparative evaluation to SST topologies with a single MFT like [20] and hybrid concepts based on low-frequency transformers as discussed in [6], e.g., employing 12-pulse rectifiers and active filters. Also, the cost aspect should be considered, whereby concepts requiring only one type of PEBB (like the mBR) might benefit from economies of scale.

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