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EMI Filter Design for the Integrated Dual Three-Phase Active Bridge (D3AB) PFC Rectifier

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***Abstract*—A Dual Three-Phase Active Bridge (D3AB) Power Factor Correction (PFC) rectifier features two dc ports: one on the primary side, which is not isolated from the mains, and a second, galvanically isolated dc port on the secondary side. A model for calculating the conducted Electromagnetic Interference (EMI) noise of a $7.5\,\mathrm{kW}$ D3AB PFC rectifier operating from a $400\,\mathrm{V_{rms}}$ line-to-line mains and generating dc output voltages of $V_{\mathrm{dc},1} = 800\,\mathrm{V}$ and $V_{\mathrm{dc},2} = 400\,\mathrm{V}$ is presented in this paper. The EMI model takes into account the implications of the power levels provided at the primary-side and secondary-side dc ports, P_1 and P_2, respectively, on the conducted EMI noise and is used to design an EMI filter for a hardware prototype of the D3AB converter topology that is volume-optimized for the considered specifications. The designed filter has a volume of $0.17\,\mathrm{dm^3} = 10.4\,\mathrm{in^3}$ ($0.09\,\mathrm{dm^3} = 5.5\,\mathrm{in^3}$ for the Differential Mode (DM) filter and $0.08\,\mathrm{dm^3} = 4.9\,\mathrm{in^3}$ for the Common Mode (CM) filter part). As part of the experimental verification of the model, the conducted EMI noise of the hardware prototype is measured under two different workload scenarios, i.e., $P_1 = 4\,\mathrm{kW}$, $P_2 = 2.5\,\mathrm{kW}$ and $P_1 = 0$, $P_2 = 6.5\,\mathrm{kW}$. Measurements show that the level of conducted EMI noise increases with increasing load on the secondary side, which is consistent with the predictions of the noise model. The complete hardware prototype achieves sinusoidal mains currents with a Power Factor (PF) of $\lambda = 0.994$ and a Total Harmonic Distortion (THD) of currents lower than $5.6\,\%$ at the considered loads and complies with the CISPR 11 class A Quasi-Peak (QP) conducted EMI limit.**

I. Introduction

A three-phase PFC rectifier system which features two independent dc ports (cf. **Fig. 1**), as, e.g., required for directly supplying a high power drive system ($5\,\mathrm{kW}$, $800\,\mathrm{V}$) and a galvanically isolated dc distribution system powering auxiliaries ($2.5\,\mathrm{kW}$, $400\,\mathrm{V}$) is investigated in this paper. Galvanic isolation enables a flexible design of the grounding concept intended for the dc distribution network, which is beneficial, e.g., to achieve low fault currents in case of a line-to-ground fault [1]. **Table I** summarizes the main specifications of the considered rectifier system.

Typically, series connection of three-phase PFC rectifier and galvanically isolated dc–dc converter is used to realize this type of converter system, with the dc voltage output of the three-phase rectifier being used for supplying high power loads and the dc–dc converter. A literature search reveals a large number of different solutions for this realization, both with unidirectional (e.g. [2]) and bidirectional power flow (e.g. [3]–[5]). Connecting several converter stages in series, though, has the disadvantage that the entire output power must be processed by the rectifier stage. Accordingly, numerous single-stage concepts are presented in the literature which realize both, rectification and galvanic isolation. However, many concepts, such as the topologies based on the Swiss rectifier [6]–[8] and the matrix converter [9]–[11], are unsuitable for the task at hand because they only provide isolated ports.

TABLE I. Converter specification.

Ac line voltage (phase-to-neutral, RMS)	$V_{\mathrm{ac1,rms}} = 230\,\mathrm{V}$
Ac line frequency	$f_1 = 50\,\mathrm{Hz}$
Primary-side dc link voltage	$V_{\mathrm{dc},1} = 800\,\mathrm{V}$
Secondary-side dc link voltage	$V_{\mathrm{dc},2} = 400\,\mathrm{V}$
Maximum total power	$P_1 + P_2 = 7.5\,\mathrm{kW}$
Primary-side power	$P_1 = 5\,\mathrm{kW}$
Secondary-side power	$P_2 = 2.5\,\mathrm{kW}$

Integrated converter topologies with two dc ports are commonly derived from a combination of the above-mentioned series connection of a three-phase rectifier and a dc–dc converter, where the rectifier stage is usually implemented as a two-level six-switch Voltage Source Converter (VSC) with line-side input inductors, which allows bidirectional power flow. In these circuit topologies, the three-phase VSC also serves as the High-Frequency (HF) ac source for the HF transformer. Examples in this regard are described in [12]–[14], i.e., the combinations of three-phase VSC and single-phase LLC resonant converter, three-phase VSC and three-phase LLC resonant converter, and three-phase VSC and three-phase Dual Active Bridge (DAB) converter, respectively. In addition, also more exotic circuit topologies are described; for example, [15] explains a rectifier with unidirectional power flow that requires only two controllable power switches. This topology, though, has the disadvantage of discontinuous currents in the line-side input inductors. Furthermore, only the voltage present at one of the two dc ports can be controlled (the remaining voltage varies depending on the load). In contrast, [16] describes a nine-switch topology which allows operation with continuous currents in the line-side inductors and independent regulation of the voltages at the two dc ports. However, in addition to the higher number of semiconductor switches, this topology requires a comparably high dc link voltage.

A common property of the circuit topologies mentioned so far is that the line-side input inductors of the three-phase VSC and the HF transformers of the dc–dc converter are stand-alone components. Thus, the HF voltage components applied to the input inductors, which could be utilized for galvanically isolated power transfer, remain unused. Accordingly, in a further step of integration, the HF transformers of the dc–dc converter can be integrated into the input inductors by adding extra

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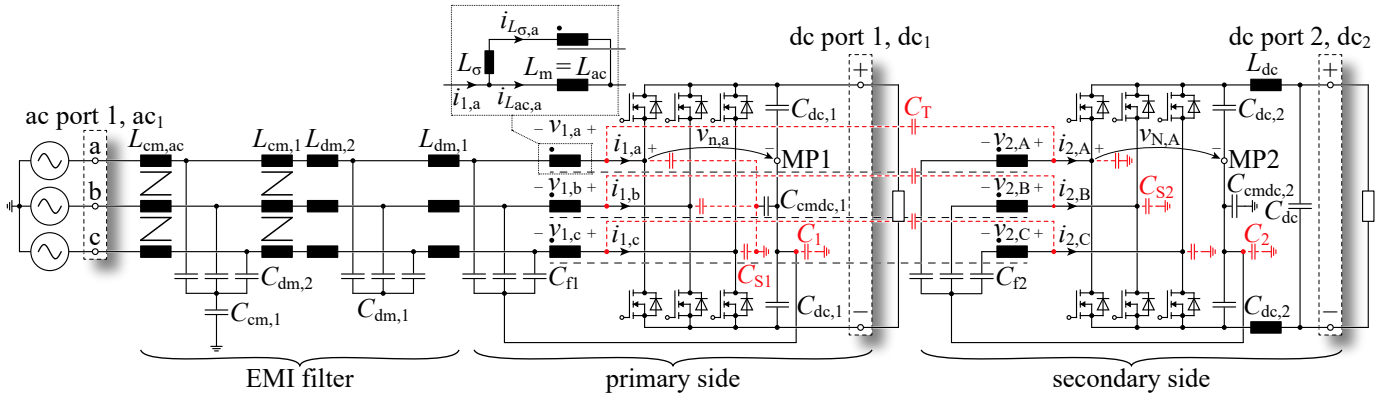

Fig. 1. Topology of the Dual Three-Phase Active Bridge (D3AB) Power Factor Correction (PFC) rectifier shown with EMI filter on ac port 1 (ac_1). The parasitic capacitances between the switching nodes and earth, the dc link mid-points and earth, and between the primary-side and secondary-side coils of the coupled boost inductors (transformers) are shown in red color.

windings to the inductors as described in [17], [18]. In a direct comparison of the circuits presented there, the Dual Three-Phase Active Bridge Converter (D3ABC) topology (cf. Fig. 1) proposed and basically described in [18] concerning modulation and operational behavior, advantageously has a lower need for independently controlled semiconductor switches (12 instead of 24), which motivates a further investigation.

This paper focuses on the analysis of conducted Electromagnetic Interference (EMI) in the D3ABC. The main aim is to derive an EMI model that provides insights into the origins of the EMI noise at the primary-side ac port (ac_1), taking the dependencies on the values of the converter components as well as the loads connected to the two dc ports into account. Furthermore, the derived EMI model should be suitable for filter optimization. In this regard, e.g., a converter optimization according to [18] can be complemented by the optimization of the EMI filter. **Section II** describes the derivation of a simplified equivalent circuit, which enables a comprehensible explanation of the converter's operating principle. **Section III** details the modeling of the EMI noise sources and the derivation of the electrical networks that describe the main propagation paths of conducted EMI noise. In this context, a model is developed that can be meaningfully used even during the design phase of the converter, when only few measurement data are available. On the basis of this modeling, **Section IV** describes the design of an EMI filter that is volume-optimized for the considered specifications, i.e., for defined limitations of conducted EMI and defined safety margins for Differential Mode (DM) and Common Mode (CM) EMI noise. Finally, **Section V** discusses the results of the experimental verification for two selected workload scenarios. A volume-optimized prototype of the D3ABC with a total power density of $4.1\,\mathrm{kW/dm^3} = 67.4\,\mathrm{kW/in^3}$ is used for the experimental verification. Measurement results of the conducted EMI noise show that the realized converter complies with the Quasi-Peak (QP) limit defined in CISPR 11 class A for operation according to Table I.

II. Operating Principle

Due to the highly integrated character of the D3ABC topology, an overall analysis of the entire system would be relatively complex. However, this is not required, because the D3ABC can be separated into different functional parts, which allows a substantial simplification of the analysis. That separation is explained in this section and comprises the steps listed below.

1) The decoupling of the three-phase system into *three independent single-phase circuits* (**Section II-A**).
2) The separation into *ac–dc operation without galvanic isolation*, i.e., on the primary side and on the secondary side, and *dc–dc operation with galvanic isolation* between the primary-side and secondary-side dc ports (**Section II-B**).

A. Independent single-phase circuits

With the assumption of symmetric line voltages, defined as

$$v_{\mathrm{ac,a,b,c}}(t) = V_{\mathrm{ac1,peak}} \sin\left(2\pi f_1 t + \theta_{\mathrm{a,b,c}}\right), \quad (1)$$

$$V_{\mathrm{ac1,peak}} = \sqrt{2} V_{\mathrm{ac1,rms}}, \;\; \theta_{\mathrm{a,b,c}} \in \{0°, 120°, 240°\}, \quad (2)$$

line frequency f_1, and a modulation without Low-Frequency (LF) CM voltage (e.g., third harmonic injection), the mid-point of the primary-side dc link, MP1, is on the same potential as the line star point. Furthermore, the D3ABC topology employs no CM filter inductors directly in series to the coupled boost inductors (L_{ac}, L_σ in Fig. 1).[1] For these reasons, the three phases of the D3ABC without EMI filter, i.e., the parts of the circuit depicted in Fig. 1 that are marked with the curly braces referring to *primary side* and *secondary side*, can be separated into three single-phase circuits as shown in **Fig. 2(a)** where MP1 is connected to the line star point. There, the single complex impedance Z_{EMI} approximates the impedance of the EMI filter between the converter and the mains. The voltage source, v_{ac}, refers to one of the three phase voltages of the mains.

B. Separation of ac–dc and dc-dc operation

In a first step, it needs to be analyzed whether the power conversion between ac port 1 and dc port 1 (referred to

[1] Only the CM inductors of the EMI filter introduce couplings between the phases. However, the first filter stage, which is composed of three coupled boost inductors (L_{ac}, L_σ) and the three filter capacitors (C_{f1}) features large DM and CM attenuations of 70 dB and 44 dB, respectively. Therefore, the implications of these couplings on the main converter waveforms, e.g., the currents in the boost inductors, can be neglected.

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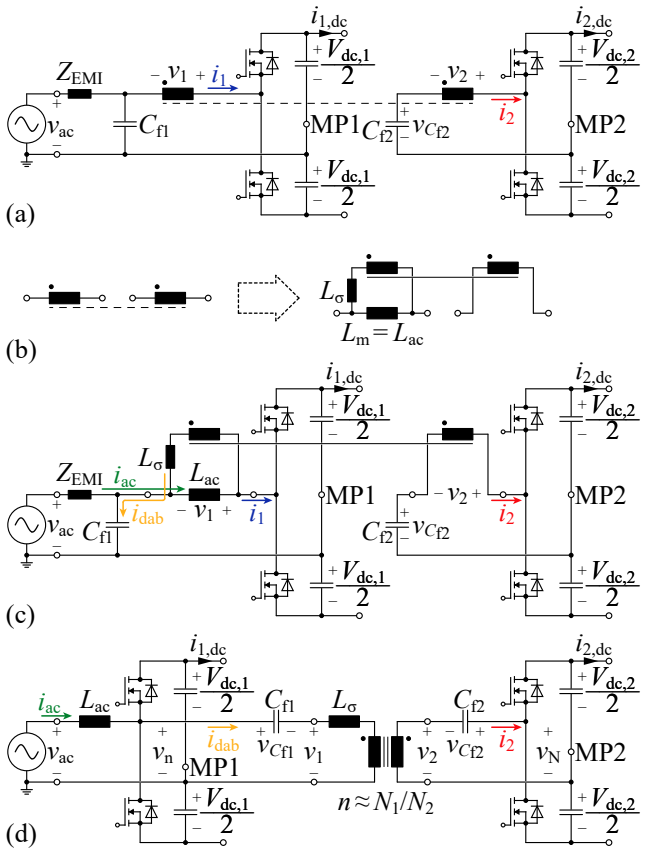

Fig. 2. Derivation of the single-phase equivalent circuit with decoupled circuits for ac_1–dc_1 and dc_1-dc_2 operations: (a) single phase of the D3ABC depicted in Fig. 1; (b) equivalent circuit of the transformer; (c) circuit of (a) with the transformer being replaced according to (b); (d) final equivalent circuit with separated junctions for the LF and HF components of the input current at the switching node of the considered primary-side half-bridge.

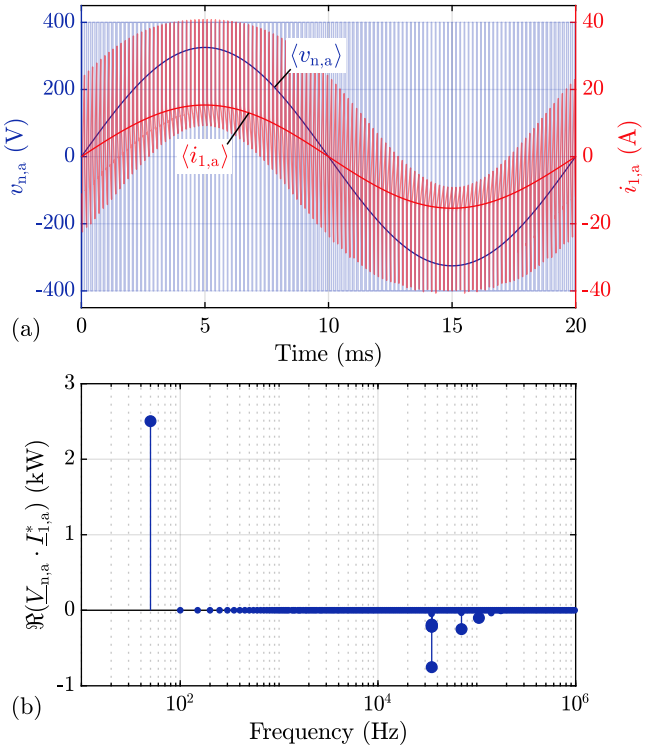

Fig. 3. (a) Waveforms of $v_n(t)$ and $i_1(t)$, defined in the single-phase circuit of Fig. 2(a), over a line period of 20 ms. For the purpose of illustration, the waveforms have been determined for a reduced switching frequency of $f_s = 6\,\text{kHz}$. The shown sinusoidal characteristics, $\langle v_{n,a} \rangle$ and $\langle i_{1,a} \rangle$, refer to the local average values of the instantaneous values of $v_n(t)$ and $i_1(t)$. (b) Spectrum of the active power at the switching node of the primary-side half-bridge of a single phase, for a switching frequency of $f_s = 35\,\text{kHz}$. The waveforms and the spectrum are calculated for the ac–dc operation described in [18] with the voltages and the mains frequency specified in Table I, an output power of $P_2 = 7.5\,\text{kW}$ at dc_2, $2\pi f_s L_{ac} \approx 29.5\,\Omega$, $2\pi f_s L_\sigma \approx 19.6\,\Omega$, and $n = 2.6$.

as ac_1–dc_1 operation) and the power conversion between dc port 1 and dc port 2 (dc_1–dc_2 operation) can be considered separately. For this purpose, the spectrum of the active power at the switching node of the single-phase equivalent circuit depicted in Fig. 2(a), $P_1(f)$, is analyzed for a typical operating condition. The calculation of $P_1(f)$ for a given frequency f requires the phasor of the voltage, $\underline{V}_n(f)$, and the complex conjugated phasor of the current, $\underline{I}_1^*(f)$, at the switching node,

$$P_1(f) = \Re\left[\underline{V}_n(f)\underline{I}_1^*(f)\right]. \tag{3}$$

These phasors are determined from the corresponding time-domain waveforms. **Fig. 3(a)** shows example waveforms for v_n and i_1, which have been calculated for the ac_1–dc_2 operation as described in [18] with a switching frequency of $f_s = 6\,\text{kHz}$ (low switching frequency for the purpose of illustration). The calculation uses the voltages and frequency specified in Table I, an output power of $7.5\,\text{kW}$ at port dc_2, $2\pi f_s L_{ac} \approx 29.5\,\Omega$, $2\pi f_s L_\sigma \approx 19.6\,\Omega$, and $n = 2.6$. Sinusoidal lines in Fig. 3(a) correspond to the local average values over one switching period. The local average value of v_n is calculated by integration of the instantaneous value,

$$\frac{1}{T_s}\int_t^{t+T_s} v_n(\tau)\,\mathrm{d}\tau = \langle v_n \rangle_{T_s}(t) = \langle v_n \rangle, \tag{4}$$

and $\langle i_1 \rangle$ is calculated in the same way. Local average values $\langle v_n \rangle$ and $\langle i_1 \rangle$ highlight the LF components below switching frequency in the waveforms and illustrate that only a component at line frequency, $f_1 = 50\,\text{Hz}$, is present.

Fig. 3(b) depicts the spectrum of the power in one phase calculated with (3), using the same settings as in Fig. 3(b), except for a higher switching frequency of 35 kHz. According to this result, the power transfer can be separated into a LF part at $f = 50\,\text{Hz}$ with positive power (primary-side half-bridge consumes energy) and a HF part for $f \geq 35\,\text{kHz}$ with negative power (primary-side half-bridge provides energy). The LF part of the spectrum, illustrated with the local average values $\langle v_{n,a} \rangle$ and $\langle i_{1,a} \rangle$ in Fig. 3(a), refers to a three-phase PFC rectifier operation without galvanic isolation from ac_1 to dc_1. The HF part of the spectrum achieves dc–dc power conversion with galvanic isolation from dc_1 to dc_2.

According to this result, a separation of the analysis for the ac_1–dc_1 and the dc_1–dc_2 operation is feasible, provided that f_s is several orders of magnitude higher than the line frequency f_1 at ac_1. Therefore, the single-phase equivalent circuit is further modified, to clearly reveal this separation. In a first step, the coupled boost inductor (which can be considered like a transformer), is replaced by the equivalent circuit shown in **Fig. 2(b)**. This circuit consists of a magnetizing inductance

L_m, a stray inductance L_σ, and an ideal HF transformer with a given turns ratio,

$$n \approx N_1/N_2. \tag{5}$$

The circuit resulting after this replacement is shown in **Fig. 2(c)**. In a final step, the paths for the LF current i_ac and the HF current i_dab, highlighted in Fig. 2(c), are separated. This final step is based on the results obtained for the frequency spectrum of the power depicted in Fig. 3(b) and denotes an approximation that is only valid if the assumptions listed below are met.

1) At line frequency of, e.g., $f_1 = 50\,\mathrm{Hz}$, it is assumed that the capacitances C_f1 and C_f2 and the capacitances in the EMI filter feature comparably high impedances and can be approximated by open circuits. Furthermore, all inductances feature very low impedances and can be replaced by short circuits in a first approximation. Based on these considerations, the LF component of i_ac passes through the line voltage source, v_ac, the magnetizing inductance, $L_\mathrm{m} = L_\mathrm{ac}$, and the half-bridge.
2) With regard to HF voltage and current components, it is assumed that the impedance of C_f1 is much lower than the impedances of Z_EMI and L_ac. Accordingly, the HF current i_dab is mainly conducted from the switching node of the primary-side half-bridge through the transformer (the secondary-side dc link capacitance $C_\mathrm{dc,2}$ and filter capacitance C_f2), the stray inductance L_σ, and the filter capacitance C_f1.[2]

Consequently, the junction connecting Z_EMI, C_f1, L_ac, and L_σ can be split into two junctions: the first junction connects Z_EMI to L_ac and the second junction connects L_σ to C_f1. Furthermore, the Z_EMI value is usually much lower than the impedance of L_ac and can be neglected. With this, the equivalent circuit depicted in **Fig. 2(d)** results, which is similar to the circuit described in [19], [20]. The derived circuit allows to separately analyze the conversion mechanisms that are relevant for the operation as rectifier (ac_1–dc_1) and isolated dc–dc converter (dc_1–dc_2). In addition, this figure points out that the magnetizing inductance, L_m, acts as boost inductance, L_ac, for ac_1–dc_1 operation.

1) Ac-dc conversion without isolation: According to Fig. 3, the local average values of v_n and i_1 are approximately sinusoidal with a frequency equal to the line frequency. Since Z_EMI and L_ac can be approximated by a short circuit at line frequency, the local average values of the voltages across this components are negligible,

$$\langle v_{Z\mathrm{emi}} \rangle \approx 0, \quad \langle v_{L\mathrm{ac}} \rangle \approx 0. \tag{6}$$

For this reason, the voltage across the filter capacitor C_f1 is approximately equal to the line voltage. Furthermore, the primary-side half-bridge must be controlled such that the local average voltage at the switching node, $\langle v_\mathrm{n} \rangle$, is approximately equal to the voltage across C_f1,

$$\langle v_\mathrm{n} \rangle = \left(D_1 - \frac{1}{2} \right) V_\mathrm{dc,1} \approx v_{C\mathrm{f1}} \approx v_\mathrm{ac}. \tag{7}$$

[2]For simplicity, the triangular HF current in the boost inductance L_ac is neglected in this section, since it does not transfer active power.

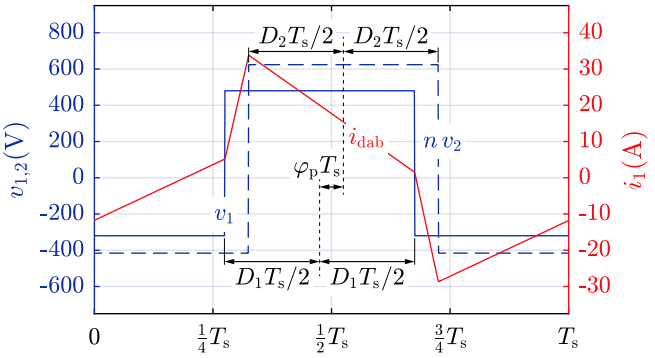

Fig. 4. Definitions of D_1, D_2, and load angle φ_p, illustrated based on waveforms that have been calculated for one switching period, T_s, with $2\pi f_\mathrm{s} L_\sigma \approx 19.6\,\Omega$, $n = 2.6$, $V_\mathrm{dc,1} = 800\,\mathrm{V}$, $V_\mathrm{dc,2} = 400\,\mathrm{V}$, $\varphi_\mathrm{p} = 18\,°$, and $D_1 = D_2 = 0.4$.

Based on (1), (2), and (7), the duty cycles of the three primary-side half-bridges result,

$$D_\mathrm{1,a,b,c}(t) \approx \frac{1}{2}\left[1 + m_1 \sin\left(2\pi f_1 t + \theta_\mathrm{a,b,c}\right)\right], \tag{8}$$

using the modulation index $m_1 = 2V_\mathrm{ac1,peak}/V_\mathrm{dc,1}$. A controller slightly adjusts the duty cycles of (8) in order to achieve PFC rectifier operation with defined active and reactive power levels on the primary side as it is known for PFC rectifiers.

2) Dc-dc conversion with isolation: The converter's dc–dc part represents a DAB converter with primary-side and secondary-side half-bridge circuits (e.g., as proposed in [21]). Due to (8), each primary-side half-bridge is operated with a time-varying duty cycle to achieve PFC rectifier operation. Furthermore, the basic modulation scheme of the D3ABC uses same duty-cycles, $D_1 = D_2 = D$, and same switching frequency, f_s, for the primary-side and secondary-side half-bridges.

According to Fig. 2(d), the difference between the voltage at the switching node of the primary-side half-bridge, v_n, and the filter capacitance $v_{C\mathrm{f1}}$ is applied to the primary side of the transformer,

$$v_1 = v_\mathrm{n} - v_{C\mathrm{f1}}. \tag{9}$$

The same applies to the secondary side,

$$v_2 = v_\mathrm{N} - v_{C\mathrm{f2}}. \tag{10}$$

where $v_{C\mathrm{f2}}$ is determined similar to the primary side, i.e., the voltage across the secondary-side filter capacitor C_f2 is approximately equal to the LF component of the voltage at the switching node of the secondary-side half-bridge,

$$v_{C\mathrm{f2}} \approx \langle v_\mathrm{N} \rangle = \left(D_2 - \frac{1}{2} \right) V_\mathrm{dc,2}, \tag{11}$$

in order to prevent saturation of the transformer. The difference between v_1 and $n\,v_2$ is applied to the transformer's stray inductance, L_σ, and causes a change of the inductor current, i_dab. The HF phase shift, φ_p, between the rectangular transformer voltages $v_1(t)$ and $v_2(t)$, as defined in **Fig. 4**, is used to control the power transferred between dc_1 and dc_2 [18],

$$P_\mathrm{dc1-dc2} = \frac{nV_\mathrm{dc,1}V_\mathrm{dc,2}}{2f_\mathrm{s}L_\sigma}\varphi_\mathrm{p}\left(2D(1-D) - |\varphi_\mathrm{p}|\right). \tag{12}$$

III. Noise Model of the D3ABC

An EMI model that can be used in the design phase is typically a mixture of physical and behavioral component models,[3] as presented, for example, in [25]–[27]. Procedures described therein propose the identification of the main sources of EMI noise, separation into DM and CM EMI noise components, and identification of main propagation paths of DM and CM EMI noise. Depending on availability, the parameterization of the model can be based on data sheet values, simulations, or measured data. Based on this, the additional attenuation of DM and CM EMI noise required to comply with EMI regulations can be determined. The required attenuation enables the design of a suitable EMI filter, which is typically optimized based on a certain cost function, e.g., minimum filter volume, while meeting certain constraints (e.g., maximum current ripple and maximum reactive power at line frequency) [28]–[30].

In the following, a complete EMI noise model of the D3ABC, i.e., valid for DM and CM EMI noise, is determined. This is used in a subsequent step to derive the DM and CM EMI noise models in **Section III-A** and **Section III-B**, respectively.

The six half-bridges represent the EMI noise source of the D3ABC topology. Based on the assumption of constant dc link voltages, each half-bridge can be replaced by a voltage source with a rectangular output voltage waveform similar to the voltage at the switching node of the half-bridge shown in Fig. 3(a). i.e., $v_{\mathrm{n,a}}$, $v_{\mathrm{n,b}}$, and $v_{\mathrm{n,c}}$ on the primary side and $v_{\mathrm{N,A}}$, $v_{\mathrm{N,B}}$, and $v_{\mathrm{N,C}}$ on the secondary side. These voltages are further divided into two CM voltage sources,

$$\begin{aligned} v_{\mathrm{cm},1} &= \frac{v_{\mathrm{n,a}} + v_{\mathrm{n,b}} + v_{\mathrm{n,c}}}{3}, \\ v_{\mathrm{cm},2} &= \frac{v_{\mathrm{N,A}} + v_{\mathrm{N,B}} + v_{\mathrm{N,C}}}{3}, \end{aligned} \tag{13}$$

for primary side and secondary side, respectively, and six DM voltage sources,

$$\begin{aligned} v_{\mathrm{dm},1,\mathrm{a,b,c}} &= v_{\mathrm{n,a,b,c}} - v_{\mathrm{cm},1}, \\ v_{\mathrm{dm},2,\mathrm{A,B,C}} &= v_{\mathrm{N,A,B,C}} - v_{\mathrm{cm},2}. \end{aligned} \tag{14}$$

At this point it is to be noted that the three primary-side half-bridges and the three secondary-side half-bridges are operated with interleaving, i.e., the carrier signals of the PWM units are phase-shifted to each other by $120\,°$.[4] Waveforms for the primary side DM and CM voltages, $v_{\mathrm{dm},1}$ and $v_{\mathrm{cm},1}$, calculated according to Section III-C and the respective local average values $\langle v_{\mathrm{dm},1,\mathrm{a}} \rangle$ and $\langle v_{\mathrm{cm},1} \rangle$ are shown in **Fig. 5(a)** (using a low switching frequency of $6\,\mathrm{kHz}$ for the purpose of illustration). The average value of $\langle v_{\mathrm{cm},1} \rangle$ is zero, i.e., no LF CM voltage is injected with this modulation scheme. The spectra of these voltages (for $f_{\mathrm{s}} = 35\,\mathrm{kHz}$) are shown in **Fig. 5(b)**.[5]

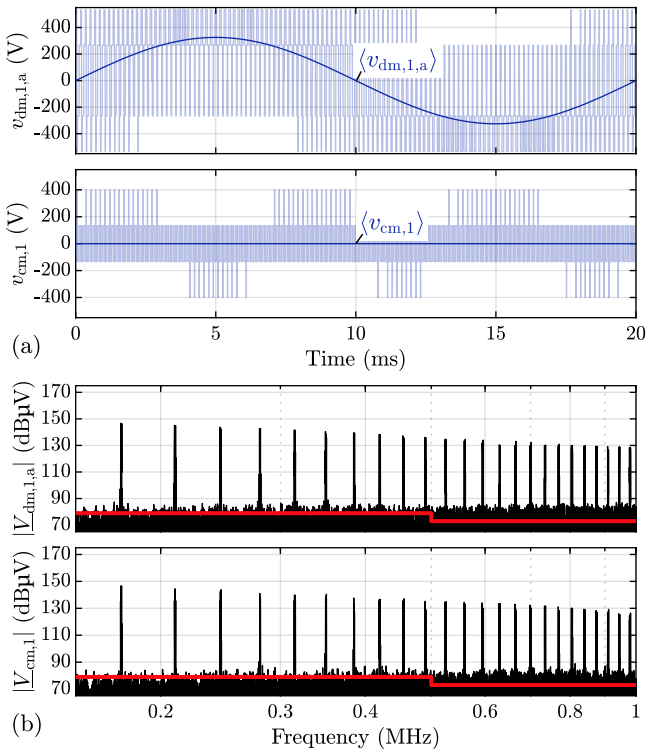

Fig. 5. Illustration of the DM and CM voltage components: (a) in time domain for a switching frequency of $6\,\mathrm{kHz}$ (low switching frequency for the purpose of illustration) and (b) in frequency domain for a switching frequency of $35\,\mathrm{kHz}$ and for the operating conditions specified in Table I.

Replacing the half-bridges in Fig. 1 by the voltage sources that model the CM and DM voltage components defined in (13) and (14) and omitting the EMI filter components (i.e., the EMI filter, $C_{\mathrm{cmdc},1}$, and $C_{\mathrm{cmdc},2}$) results in the circuit depicted in **Fig. 6**. The EMI filter is not part of Fig. 6, since the EMI noise models derived in this Section are the basis for the EMI filter design in Section IV. In order to characterize the HF EMI noise with a defined line impedance, a three-phase ac LISN is placed between the converter and the three-phase ac line. According to [31], the simplified network of the LISN consists of three inductors, three capacitors, and three resistors, i.e., $3\times50\,\mathrm{uH}$, $3\times250\,\mathrm{nF}$, and $3\times50\,\Omega$, respectively, as shown in Fig. 6. The line voltage sources are approximated by short circuits with regard to HF EMI noise.

The red capacitor symbols with dashed connecting lines in Fig. 6 represent the considered parasitic coupling capacitances of the physically largest components in the circuit (transformers and semiconductors with heat sink). Due to the sizes of these components, it is expected that their parasitic couplings are considerably high and therefore become relevant already at the first spectral component of the EMI noise that enters the regulated EMI frequency band, i.e., at $f = 175\,\mathrm{kHz}$. Since it

[3] Behavioral models are parameterized on the basis of measured data and allow accurate predictions of conducted EMI [22]–[24]. However, the necessity of having comprehensive measurement data is in contradiction to the initial situation of a converter development, during which usable measurement data is only available to a limited extent. In contrast, physical models are based on component-specific physical interrelationships and hence rely, e.g., on material data and component geometries. Such models, though, are often highly simplified and therefore less accurate than behavioral models.

[4] With this, the CM voltage component at $f = f_{\mathrm{s}}$ is reduced by $11.5\,\mathrm{dB}$ (at the cost of an increase of the DM component at $f = f_{\mathrm{s}}$ by $6.8\,\mathrm{dB}$). This significantly reduces parasitic ringing that may occur in the CM equivalent circuit (derived in Section III-B and depicted in Fig. 8(c)) at $f = f_{\mathrm{s}}$ due to the relatively small dc link capacitances, $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$, cf. Table II in Section IV.

[5] Compared to the primary side, the secondary-side voltages have the same shape and a different amplitude (the secondary-side dc link voltage is half of the primary-side dc link voltage) and are phase-shifted by the HF phase-shift, φ_{p}.

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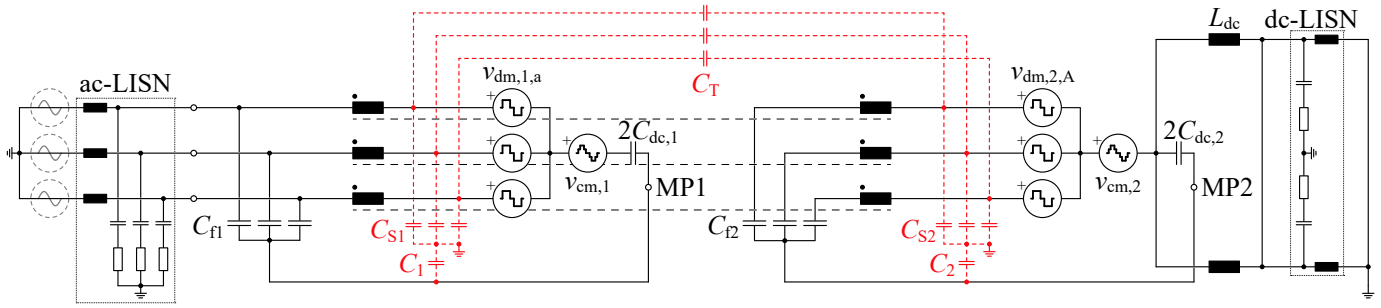

Fig. 6. The D3ABC topology (without EMI filter part) with the half-bridges being replaced by voltage sources that model DM and CM EMI noise components with respect to port ac_1. A three-phase ac-Line Impedance Stabilization Network (LISN) and a dc-LISN are connected to the ports ac_1 and dc_2, respectively, to define the terminating impedances at these ports.

is found that the self-resonance frequencies of all components are above $175\,\mathrm{kHz}$ (the lowest self-resonance frequency results for C_{f1} with a resonance frequency of $350\,\mathrm{kHz}$), the modeling of self-resonances of converter components was omitted for the sake of clarity.

The HF properties of the loads connected to dc_1 and dc_2, e.g., characterized by parasitic inductances in series to each load or parasitic capacitances to Protective Earth (PE), have an impact on the EMI noise at ac_1. However, load characteristics depend on the application and their HF properties are a priori unknown. For this reason, loads are replaced by suitable substitutes in order to facilitate a complete (terminated) EMI noise model. With regard to the DM EMI noise at each dc port, parasitic resonances between the load and the dc link would lead to a significant increase in conducted EMI. For the analysis, it is therefore assumed that dc-LISN networks[6] are inserted between the respective dc link capacitors and the connected loads, such that resonances between the dc links and the loads can be excluded. In the context of CM EMI noise, it is mainly the parasitic earth capacitances of the load that have an impact on the conducted EMI. A detailed analysis reveals highest levels of EMI noise at ac_1 if the primary-side dc load has no parasitic capacitance to PE. This is achieved by placing a CM filter inductor between dc_1 and the dc-LISN. The high impedance value of the CM filter inductor (ideally) acts as an open circuit at HF and therefore the load connected to dc_1 is omitted in Fig. 6. On the secondary side, the worst-case is found to be present if the load features a large capacitance to PE which is clarified as part of the explanation of the CM EMI model in Section III-B. There it becomes apparent that the effective CM impedance of the dc-LISN is low enough to be considered as worst-case load scenario. It is to be noted that the presented model is intended for the design of the ac-side EMI filter and therefore, the dc-side DM EMI noise sources of the model, such as described in [32], are not included.

Due to the rectangular waveform characteristics of the DM and CM noise voltages, the corresponding amplitude spectra feature envelopes that decrease with $-20\,\mathrm{dB/dec}$. Therefore, the EMI noise levels for frequencies close to $150\,\mathrm{kHz}$ are most relevant for the design of the EMI filter, given that the switching frequency is below the frequency range that is regulated for EMI ($f \in [150\,\mathrm{kHz},\ 30\,\mathrm{MHz}]$). As a final note, the derived models are expected to be useful up to a frequency of approximately $1\,\mathrm{MHz}$ and attenuations of up to approximately $100\,\mathrm{dB}$. The limitation related to damping is based on the fact that also very weak coupling between a filter node where high ac excitations are present (i.e., toward the switching stage) and a filter node with very low ac excitations (toward the grid) substantially increases the ac excitation at the grid-side node of the filter. Such coupling could be reduced by further improving the filter layout, e.g., by using a placement of the filter components that is similar to the schematic diagram of the filter (with this, the input-side and output-side filter components are located far from each other). However, in view of the need for a high power density, this typically is not possible in industrial designs, for which reason a certain reduction in filter attenuation is accepted.

[6]Fig. 6 depicts the network of the dc-LISN, which consists of two inductors ($50\,\mu\mathrm{H}$ each), two capacitors ($470\,\mathrm{nF}$ each), and two resistors ($50\,\Omega$ each).

A. DM EMI model of the D3ABC

To isolate the DM EMI noise component from the CM components, the CM voltage sources are set to zero, $v_{\mathrm{cm},1} = v_{\mathrm{cm},2} = 0$. Furthermore, a symmetric three-phase system is assumed and all component tolerances are neglected. Therefore, no CM voltage components can occur in the circuit and the noise levels in all three phases, a, b, and c, are the same. Accordingly, it is sufficient to analyze a single phase, e.g., phase a. Due to the absence of CM voltage components, the electric potentials at the star-points of the DM noise voltage sources, $v_{\mathrm{dm},1,\mathrm{a,b,c}}$ and $v_{\mathrm{dm},2,\mathrm{A,B,C}}$, and at the star-points formed by C_{f1}, C_{S1}, C_{f2}, and C_{S2} are all equal. For this reason, voltages across C_1, C_2, $2C_{\mathrm{dc},1}$, and $2C_{\mathrm{dc},2}$ are zero, i.e., these components can be replaced by short circuits, and the dc inductors, L_{dc}, as well as the dc-LISN can be neglected. Finally, each real transformer in Fig. 6 is replaced by the circuit in Fig. 2(b), which results in the single-phase equivalent circuit shown in **Fig. 7(a)**.

As indicated in Fig. 7(a), the total DM EMI noise, $v_{\mathrm{dm,t}}$, that is applied to the LISN is equal to the voltage ripple across C_{f1}, which depends on the capacitor current. The capacitor current is composed of the currents through L_σ and L_{ac}, i.e., $i_{\mathrm{dm,dab}}$ and $i_{\mathrm{dm,bst}}$, respectively. For a meaningful design of C_{f1} and C_{f2}, which implies that the resonance frequency of L_σ, C_{f1}, and C_{f2} is below the switching frequency, it can be assumed that $v_{\mathrm{dm,t}} \ll v_{\mathrm{dm},1}$ and $v_{\mathrm{dm,t}} \ll v_{\mathrm{dm},2}$ apply. Therefore, the feedback of $v_{\mathrm{dm,t}}$ on the currents $i_{\mathrm{dm,dab}}$ and

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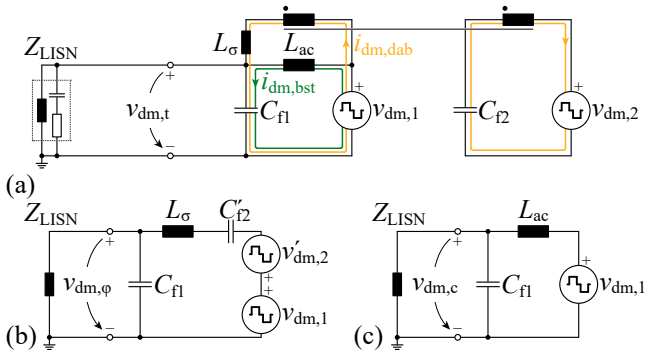

Fig. 7. Equivalent circuit for modeling the DM EMI part of the D3ABC: (a) total DM EMI model; (b) partial model related to the load-dependent DM EMI noise component; (c) partial model for calculating the load-independent DM EMI noise component.

$i_{\mathrm{dm,bst}}$ is negligible and the implications of the two currents on $v_{\mathrm{dm,t}}$ can be analyzed separately.

Following the path of the current $i_{\mathrm{dm,dab}}$, i.e., L_{ac} is left open, reveals the circuit shown in **Fig. 7(b)**. There, the primary-side referred values of the secondary-side filter capacitor, $C'_{\mathrm{f2}} = C_{\mathrm{f2}}/n^2$, and the secondary-side DM voltage source, $v'_{\mathrm{dm,2}} = n\,v_{\mathrm{dm,2}}$, are connected in series to the primary-side DM voltage source, $v_{\mathrm{dm,1}}$. It is to be noted that the total voltage across $v_{\mathrm{dm,1}}$ and $v'_{\mathrm{dm,2}}$ is equal to the voltage difference $v_{\mathrm{dm,1}} - v'_{\mathrm{dm,2}}$. Accordingly, $v_{\mathrm{dm,1}} - v'_{\mathrm{dm,2}} \approx 0$ results for zero HF phase shift, $|\varphi_{\mathrm{p}}|$, between $v_{\mathrm{dm,1}}$ and $v'_{\mathrm{dm,2}}$ if $V_{\mathrm{dc,1}} = nV_{\mathrm{dc,2}}$ applies. In this case, $i_{\mathrm{dm,dab}}$ is zero. With increasing value of $|\varphi_{\mathrm{p}}|$, i.e., increasing power transfer between dc_1 and dc_2, cf. (12), the voltage applied to L_σ, $v_{\mathrm{dm,1}} - v'_{\mathrm{dm,2}}$, and, with this, $i_{\mathrm{dm,dab}}$ increase. As a consequence, the EMI noise component, $v_{\mathrm{dm},\varphi}$ in Fig. 7(b), increases if the secondary-side load increases.

Following the path of the current $i_{\mathrm{dm,bst}}$ gives the circuit shown in **Fig. 7(c)**. This current features a triangular shape that is typical for VSCs. The HF components of $v_{\mathrm{dm,1}}$ are mainly defined by the line voltage and the dc link voltage and are practically independent of the load. For this reason, the related EMI noise component, $v_{\mathrm{dm,c}}$, is also independent of the load (assuming constant inductance L_{ac}).

The total DM EMI noise is obtained by means of superposition,

$$v_{\mathrm{dm,t}} = v_{\mathrm{dm},\varphi} + v_{\mathrm{dm,c}}. \tag{15}$$

B. CM EMI model of the D3ABC

For the analysis of the CM equivalent circuit of the converter's EMI model, the DM voltage sources in Fig. 6 are set to zero, $v_{\mathrm{dm,1,a,b,c}} = v_{\mathrm{dm,2,A,B,C}} = 0$. Consequently, the three primary-side phases of the D3ABC can be considered to be connected parallel to each other and the same applies to the three phases of the secondary side. As for the analysis conducted for DM EMI noise, a symmetric three-phase system is assumed, with all component tolerances being neglected. With this, the circuit shown in **Fig. 8(a)** results for the D3ABC without EMI filter. In a subsequent step, the transformer is replaced by the equivalent circuit shown in Fig. 2(b), which leads to the network depicted in **Fig. 8(b)**.

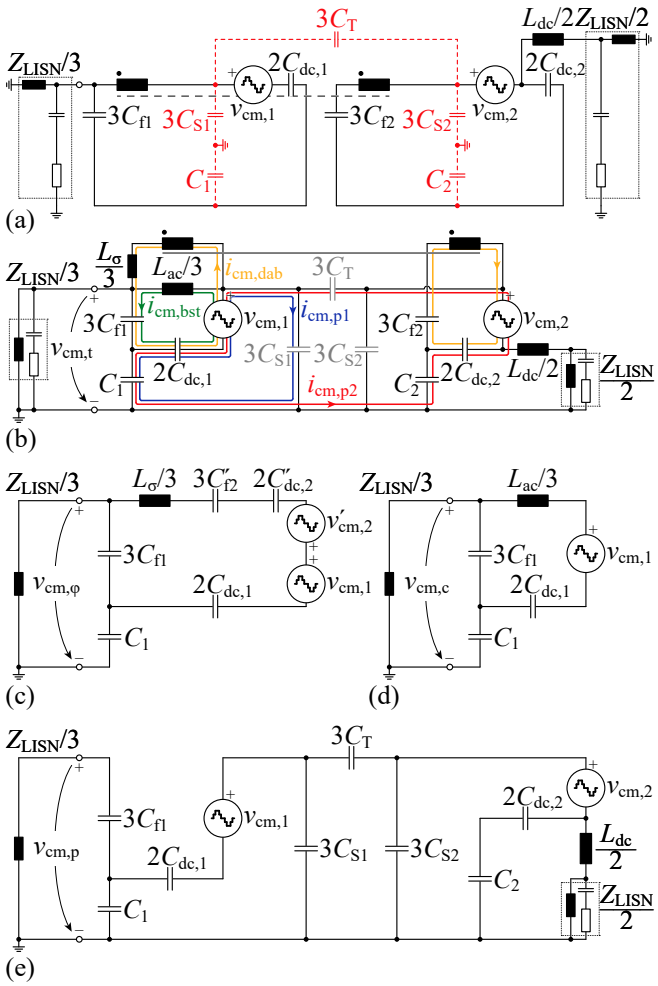

Fig. 8. Equivalent circuit for modeling the CM EMI part of the D3ABC: (a) total CM EMI model; (b) total CM EMI model with the transformer being replaced by the equivalent circuit depicted in Fig. 2(b); (c) partial model related to the load-dependent CM EMI noise component; (d) partial model for calculating the load-independent CM EMI noise component that is generated by the primary-side CM EMI noise voltage source; (e) partial model related to the CM EMI noise voltage that arises due to the parasitic capacitances C_{S1}, C_{S2}, and C_{T}.

The total CM EMI noise voltage at the LISN, $v_{\mathrm{cm,t}}$, is the sum of the CM EMI noise voltages across $3C_{\mathrm{f1}}$ and C_1. Accordingly, $v_{\mathrm{cm,t}}$ depends on the CM EMI noise currents in the capacitors $3C_{\mathrm{f1}}$ and C_1. In the presented analysis, these capacitor currents are split into the four partial currents marked in Fig. 8(b): $i_{\mathrm{cm,dab}}$, $i_{\mathrm{cm,bst}}$, $i_{\mathrm{cm,p1}}$, and $i_{\mathrm{cm,p2}}$. The implications of these currents on $v_{\mathrm{cm,t}}$ are detailed in the following. It should be noted that $v_{\mathrm{cm,t}} \ll v_{\mathrm{cm,1}}$ and $v_{\mathrm{cm,t}} \ll v_{\mathrm{cm,2}}$ is assumed. Accordingly, the feedback of $v_{\mathrm{cm,t}}$ on $i_{\mathrm{cm,dab}}$, $i_{\mathrm{cm,bst}}$, $i_{\mathrm{cm,p1}}$, and $i_{\mathrm{cm,p2}}$ is negligible and each of the four partial currents can be analyzed separately.

Following the path of the current $i_{\mathrm{cm,dab}}$, i.e., $L_{\mathrm{ac}}/3$, $3C_{\mathrm{S1}}$, $3C_{\mathrm{S2}}$, and $3C_{\mathrm{T}}$ are left open, reveals the circuit shown in **Fig. 8(c)**, which is similar to Fig. 7(b) except for the dc link capacitances, $2C_{\mathrm{dc,1}}$ and $2C'_{\mathrm{dc,2}} = 2C_{\mathrm{dc,2}}/n^2$, and the parasitic capacitance C_1.[7] At the ac-side interface, marked with $v_{\mathrm{cm},\varphi}$, the parasitic capacitance C_1 is in series with the

[7]On the secondary side, a parallel path to $C_{\mathrm{dc,2}}$ exists, through C_2, $Z_{\mathrm{LISN}}/2$, and $L_{\mathrm{dc}}/2$, but the current in this parallel path is negligible.

remaining circuit. The rms value of $i_{\mathrm{cm,dab}}$ increases with the HF phase shift, $|\varphi_{\mathrm{p}}|$, and, accordingly, the operating power of the isolated dc–dc part of the D3ABC is increased. For this reason, $v_{\mathrm{cm},\varphi}$ increases as the load on the secondary side increases.

Following the path of the current $i_{\mathrm{cm,bst}}$, i.e., $L_\sigma/3$, $3C_{\mathrm{S1}}$, $3C_{\mathrm{S2}}$, and $3C_{\mathrm{T}}$ are left open, gives the circuit shown in **Fig. 8(d)** that corresponds to the DM circuit in Fig. 7(c), except for the additional dc link capacitance, $2C_{\mathrm{dc1}}$, and the capacitance C_1, which appears at the input of the network and in series to the remaining circuit. Since $v_{\mathrm{cm},1}$ does not depend on the load, and assuming that $L_{\mathrm{ac}}/3$ is constant, the partial CM EMI noise voltage $v_{\mathrm{cm,c}}$ does not depend on the load either.

Finally, the circuit shown in **Fig. 8(e)** results if $L_\sigma/3$ and $L_{\mathrm{ac}}/3$ are left open. With this approximation, the filter capacitance C_{f1} is in series to the remaining circuit. Mainly the primary-side CM voltage source $v_{\mathrm{cm},1}$ contributes to the formation of $v_{\mathrm{cm,p}}$, by means of the current $i_{\mathrm{cm,p1}}$, which primarily flows through the series connected capacitors $2C_{\mathrm{dc1}}$, $\approx 3(C_{\mathrm{S1}}+C_{\mathrm{T}})$, and C_1. The current $i_{\mathrm{cm,p2}}$ that is generated by the secondary-side CM voltage source $v_{\mathrm{cm},2}$ is comparably small and, consequently, the HF phase shift, φ_{p}, has a minor impact on $v_{\mathrm{cm,p}}$. A respective circuit simulation of the investigated D3ABC reveals that $v_{\mathrm{cm,p}}$ increases by less than $3\,\mathrm{dB}$ at $175\,\mathrm{kHz}$ if the output power at port dc_1 is decreased from $4\,\mathrm{kW}$ to 0 and, at the same time, the output power at port dc_2 is increased from $2.5\,\mathrm{kW}$ to $6.5\,\mathrm{kW}$ (these power values stem from the example workload scenarios 1 and 2 defined in **Section V-D**).

It is worth noting that, according to the equivalent circuit in Fig. 8(e), the value of $i_{\mathrm{cm,p2}}$ increases as the CM impedance of the load connected to the secondary-side dc port, represented here by Z_{LISN}, decreases. Accordingly, the highest value for $i_{\mathrm{cm,p2}}$ results if Z_{LISN} is replaced by a short circuit. However, in terms of a worst-case estimation, it is sufficient if Z_{LISN} is much smaller than the impedance of $3C_{\mathrm{S2}}$. According to Section IV-A, C_{S2} has an estimated value of $200\,\mathrm{pF}$ for the hardware investigated in this work. Thus, in the considered frequency range of $150\,\mathrm{kHz} < f < 1\,\mathrm{MHz}$, the impedance of $3C_{\mathrm{S2}}$ is between $1.8\,\mathrm{k\Omega}$ and $270\,\Omega$, which is more than a factor of 10 larger than $Z_{\mathrm{LISN}}/2 = 25\,\Omega$. Consequently, the CM impedance of the dc-LISN sufficiently represents the worst case in the considered case.

The total CM EMI noise is obtained by means of superposition,

$$v_{\mathrm{cm,t}} = v_{\mathrm{cm},\varphi} + v_{\mathrm{cm,c}} + v_{\mathrm{cm,p}}. \tag{16}$$

C. Verification of the EMI models

To verify the derived EMI models, the spectra of the DM and CM noise calculated with the EMI models, i.e., without EMI filter, have been compared to the DM and CM noise spectra obtained from circuit simulations of the converter. The characterization of the DM and CM noise sources of the EMI models is a three-step process, which has been realized with MATLAB. First, the time-domain waveforms of the voltages at the six switching nodes over a mains period are calculated based on the duty cycles and the HF phase shift defined by (8) and (12), for the operating conditions listed in Table I. In a subsequent step, the waveforms of the DM and CM voltages, i.e., $v_{\mathrm{dm},1}(t)$, $v_{\mathrm{cm},1}(t)$, $v_{\mathrm{dm},2}(t)$, and $v_{\mathrm{cm},2}(t)$, are calculated, as shown in Fig. 5(a) for the primary-side DM and CM voltages. Finally, the corresponding spectra, e.g., depicted in Fig. 5(b), are determined. With this, the noise voltages at the mains-side interface of the converter, $v_{\mathrm{dm,t}}(t)$ in Fig. 7(a) and $v_{\mathrm{cm,t}}(t)$ in Fig. 8(b), are determined by superposition.[8]

In order to determine the expected upper and lower boundaries of the noise voltage measured by a CISPR-compliant QP detector, the spectra of $v_{\mathrm{dm,t}}(t)$ and $v_{\mathrm{cm,t}}(t)$, i.e., $V_{\mathrm{dm,rms}}(f)$ and $V_{\mathrm{cm,rms}}(f)$, are post-processed by estimating the minimum and maximum QP signal levels as proposed in [31] for a defined receiver bandwidth of $RBW = 9\,\mathrm{kHz}$. The estimation of the minimum QP signal level (in the following referred to as *Min* estimate) of the DM voltage at the LISN (in $\mathrm{dB\mu V}$) can be calculated with

$$V_{\mathrm{dm,min}}(f) = 20\,\mathrm{dB\mu V}\log_{10}\left(\frac{1}{1\,\mu\mathrm{V}}\sqrt{\sum_{\xi=f-\frac{RBW}{2}}^{\xi=f+\frac{RBW}{2}} V_{\mathrm{dm,rms}}(\xi)^2}\right), \tag{17}$$

which represents an equal spectral power within RBW. In a similar way, [31] proposes an estimation of the maximum QP signal level (in the following referred to as *Max* estimate) calculated with

$$V_{\mathrm{dm,max}}(f) = 20\,\mathrm{dB\mu V}\log_{10}\left(\frac{1}{1\,\mu\mathrm{V}}\sum_{\xi=f-\frac{RBW}{2}}^{\xi=f+\frac{RBW}{2}} V_{\mathrm{dm,rms}}(\xi)\right). \tag{18}$$

The same expression can be used to evaluate the *Min*/*Max* estimates of the CM noise components. The lower and upper solid lines in **Fig. 9(a,b)** represent the calculated results for these boundaries.[9]

For comparison, a circuit simulation of the converter was performed using the operating conditions and component values listed in Table I, Table II, and Table III. From the results of the simulation, the spectra and the *Min*/*Max* estimates were calculated (shown as dotted lines in Fig. 9(a,b)). It can be seen in Fig. 9(a,b) that the calculated and simulated *Min* estimates of the DM and CM EMI noises at the harmonics of the switching frequency agree well. **Fig. 9(c)** shows the absolute deviations at those harmonics that are less than $2.5\,\mathrm{dB}$ over the entire frequency range considered. The discrepancies in case of the *Max* estimates for both DM and CM EMI noise are largely related to the fact that the calculations of the waveforms of the voltages at the switching nodes assume a constant dc link voltage without ripple. The simulation considers the voltage ripple, leading to sidebands with higher amplitudes, which mainly increase the results of the *Max* estimates.

[8] In anticipation of the findings of Section IV, the EMI models are parameterized using the values listed in Table II and Table III for the converter components and parasitic capacitances for these calculations.

[9] Due to the symmetry of the simulated circuit, the DM components of all phases are identical. Therefore, only the spectrum of phase a is shown.

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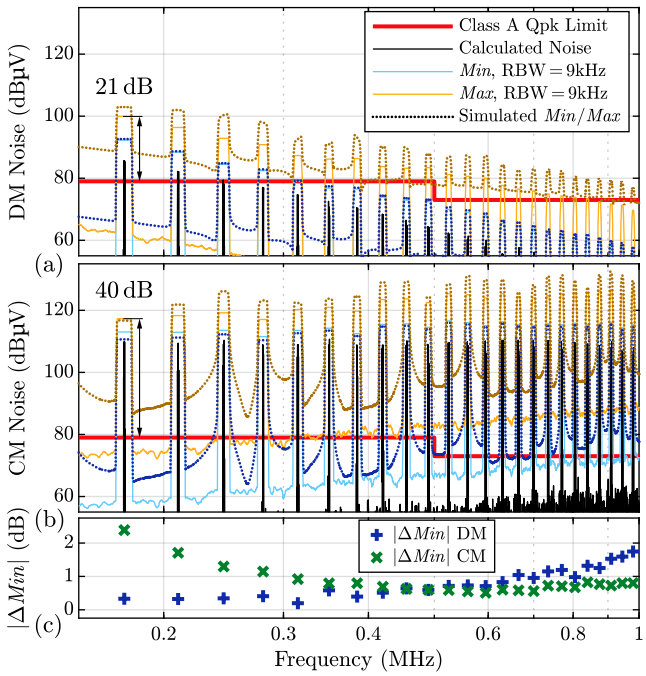

Fig. 9. Resultant EMI noise voltages at the LISN for the converter without EMI filter calculated by applying the DM and CM voltages shown in Fig. 5(b) to the equivalent circuits in Fig. 7 and Fig. 8: (a) DM, (b) CM. The solid black curves depict the calculated voltage spectra, and the lightblue and orange curves represent the *Min*/*Max* estimates determined with (17) and (18), respectively. The solid and dotted curves result if the voltages at the six switching nodes of the D3AB are calculated numerically with MATLAB and simulated with a circuit simulator, respectively. (c) Shows the difference of the *Min* estimates between calculated and simulated noise at the harmonics of the switching frequency.

IV. EMI Filter Design

This section describes the design of an EMI filter for a given prototype of the D3ABC topology using the EMI noise models of Section III. The power stage of the prototype has been optimized by means of an η–ρ-Pareto optimization as described in [18] in a preceding step. The separation between the EMI filter and the power stage is made according to the converter parts marked with curly braces in Fig. 1, i.e., all components between the port ac_1 and $L_{\mathrm{dm},1}$ (including $L_{\mathrm{dm},1}$) are part of the EMI filter, and all remaining components belong to the main converter part. This kind of separation is motivated by the fact that besides L_{ac} and L_σ, also the filter capacitors C_{f1} are subject to relatively large rms currents. For this reason, these passive components substantially contribute to the total converter volume and need to be included in the η–ρ-Pareto optimization of the D3ABC. For the sake of brevity, the design of the main converter part is not outlined further in this paper. However, it is noted that it was found during a refinement step of the converter optimization that the resonance frequencies of the resonant circuits shown in Fig. 7(b,c) and Fig. 8(c,d), e.g., formed by the series connection of $3C_{\mathrm{f1}}$, $2C_{\mathrm{dc},1}$, $3C'_{\mathrm{f2}}$, $2C'_{\mathrm{dc},2}$, and $L_\sigma/3$ in Fig. 8(c), can be close to the switching frequency. In this regard, the network depicted in Fig. 8(c) turned out to be most critical. Therefore, the original optimization procedure was extended by a boundary condition related to the selection of C_{f1}, $C_{\mathrm{dc},1}$, C_{f2}, $C_{\mathrm{dc},2}$, and L_σ that limits the resonance frequency of this network to less than half of the switching frequency,

$$C_{\mathrm{r}} = \frac{1}{\frac{1}{3C_{\mathrm{f1}}} + \frac{1}{2C_{\mathrm{dc},1}} + \frac{n^2}{3C_{\mathrm{f2}}} + \frac{n^2}{2C_{\mathrm{dc},2}}}, \tag{19}$$

$$f_{\mathrm{r},\sigma} = \frac{1}{2\pi\sqrt{\frac{L_\sigma}{3}\,C_{\mathrm{r}}}} < \frac{f_{\mathrm{s}}}{2}. \tag{20}$$

Table II lists the resulting converter parameters and component values. With these values, $f_{\mathrm{r},\sigma} = 15.3\,\mathrm{kHz} < \frac{35\,\mathrm{kHz}}{2}$ applies.

TABLE II. Main component values of the D3ABC ($\Delta I_{L_{\mathrm{ac,pkpk}}}$ is the maximum peak-to-peak change of the inductor current within one switching period and $I_{\mathrm{m,pk}}$ is the amplitude of the mains current).

Ripple ratio	$r = \frac{\Delta I_{L_{\mathrm{ac,pkpk}}}}{I_{\mathrm{m,pk}}} = 260\,\%$
Switching frequency	$f_{\mathrm{s}} = 35\,\mathrm{kHz}$
Ac inductance	$L_{\mathrm{ac}} = 3 \times 134\,\mu\mathrm{H}$
Transformer turns ratio	$n = 2.6$
Stray inductance	$L_\sigma = 3 \times 88\,\mu\mathrm{H}$
Primary-side dc link capacitor	$C_{\mathrm{dc},1} = 2 \times 12\,\mu\mathrm{F}$
Secondary-side dc link capacitor	$C_{\mathrm{dc},2} = 2 \times 37\,\mu\mathrm{F}$
Secondary-side dc filter inductor	$L_{\mathrm{dc}} = 2 \times 14.7\,\mu\mathrm{H}$
Primary-side filter capacitor	$C_{\mathrm{f1}} = 3 \times 10\,\mu\mathrm{F}$
Secondary-side filter capacitor	$C_{\mathrm{f2}} = 3 \times 21.5\,\mu\mathrm{F}$

Prior to the design of the EMI filter, the spectra of the EMI noise voltages that appear at the LISN without EMI filter part, cf. Fig. 6, are analyzed in a first step in **Section IV-A** in order to determine the required attenuation characteristics of the EMI filter. Thereafter, the design of the EMI filter is described in **Section IV-B** and **Section IV-C** for the DM and CM parts of the EMI filter, respectively. The EMI filter is designed to comply to the CISPR class A QP limit for $P_1 = 5\,\mathrm{kW}$ at the port dc_1 and $P_2 = 2.5\,\mathrm{kW}$ at dc_2 as described in **Section I**.

A. EMI noise voltages without EMI filter part

In order to enable the estimation of the spectra of the DM and CM voltage components at the LISN without EMI filter, the values of the parasitic capacitances C_{S1}, C_{S2}, C_1, C_2, and C_{T} must first be estimated.

The parasitic capacitances from the switching nodes to PE, C_{S1} and C_{S2}, are partly determined by the metal areas on the back of the low-side transistors, since all MOSFETs are mounted on a conductive heat sink that is connected to PE, and partly due to the parasitic capacitances between the high-side gate driver and PE. A respective estimation reveals $C_{\mathrm{S1}} \approx C_{\mathrm{S2}} \approx 200\,\mathrm{pF}$.

With regard to the parasitic capacitances that are present between the midpoints of the dc links and PE, C_1 and C_2, it is assumed that these capacitances are mainly due to the high-side transistors and the low-side gate drivers. However, compared to C_{S1} and C_{S2}, the low-side gate drivers of each side of the converter (primary and secondary) share a common supply, which reduces the value of the parasitic capacitances. Accordingly, a value of approximately $450\,\mathrm{pF}$ has been determined for C_1 and C_2.

Finally, the parasitic capacitance of each coupled inductor / transformer is estimated based on ideal plate capacitor approximations. For this, the overlapping areas between the coils of the primary side and the secondary side are approximated

TABLE III. Estimated values of the parasitic capacitances.

Primary-side switch-node capacitances	$3 \times C_{\mathrm{S1}} = 3 \times 200\,\mathrm{pF}$
Secondary-side switch-node capacitances	$3 \times C_{\mathrm{S2}} = 3 \times 200\,\mathrm{pF}$
Primary-side parasitic dc link capacitance	$C_1 = 450\,\mathrm{pF}$
Secondary-side parasitic dc link capacitance	$C_2 = 450\,\mathrm{pF}$
Parasitic transformer capacitances	$3 \times C_{\mathrm{T}} = 3 \times 100\,\mathrm{pF}$

by a first plate capacitor, $C_{\mathrm{T},12}$. The areas between the coils and the magnetic core are approximated by two further plate capacitors, $C_{\mathrm{T},1\mathrm{c}}$ and $C_{\mathrm{T},2\mathrm{c}}$, for primary side and secondary side, respectively. These two capacitors are connected in series with the impedance of the magnetic core material. With respect to this impedance, reference [33] reveals a measured conductivity $\sigma \geq 0.5\,\mathrm{S/m}$ for the ferrite core material 3C95, i.e., a material that is similar to the core material used in this paper (N95). Furthermore, it is found that the conductivity increases for increasing frequency. A similar result was obtained for the measured impedance characteristic of another related ferrite material (N87) in [34]. There, the measurements show a decrease in impedance with increasing frequency throughout the entire frequency range between $100\,\mathrm{kHz}$ and $50\,\mathrm{MHz}$. A comparison of the impedances of the parasitic capacitances and the resistance of the core at the relevant frequency of $175\,\mathrm{kHz}$ reveals that the impedance of the core can be neglected. Thus, the total parasitic capacitance, C_{T}, is calculated with

$$C_{\mathrm{T}} = C_{\mathrm{T},12} + \frac{C_{\mathrm{T},1\mathrm{c}} C_{\mathrm{T},2\mathrm{c}}}{C_{\mathrm{T},1\mathrm{c}} + C_{\mathrm{T},2\mathrm{c}}}, \tag{21}$$

i.e., $C_{\mathrm{T},12}$ is connected in parallel to the series connection of $C_{\mathrm{T},1\mathrm{c}}$ and $C_{\mathrm{T},2\mathrm{c}}$. **Table III** lists the values estimated for C_{S1}, C_{S2}, C_1, C_2, and C_{T}.

The values of the *Max* estimates for the DM and CM EMI noise determined in Section III-C and shown in Fig. 9 serve as a basis to define the required attenuations of the DM and CM parts of the EMI filter. It can be seen that the 5$^{\mathrm{th}}$ harmonic of the switching frequency, at $5f_{\mathrm{s}} = 175\,\mathrm{kHz}$, is the first harmonic component that enters the EMI frequency range defined by the CISPR regulation.

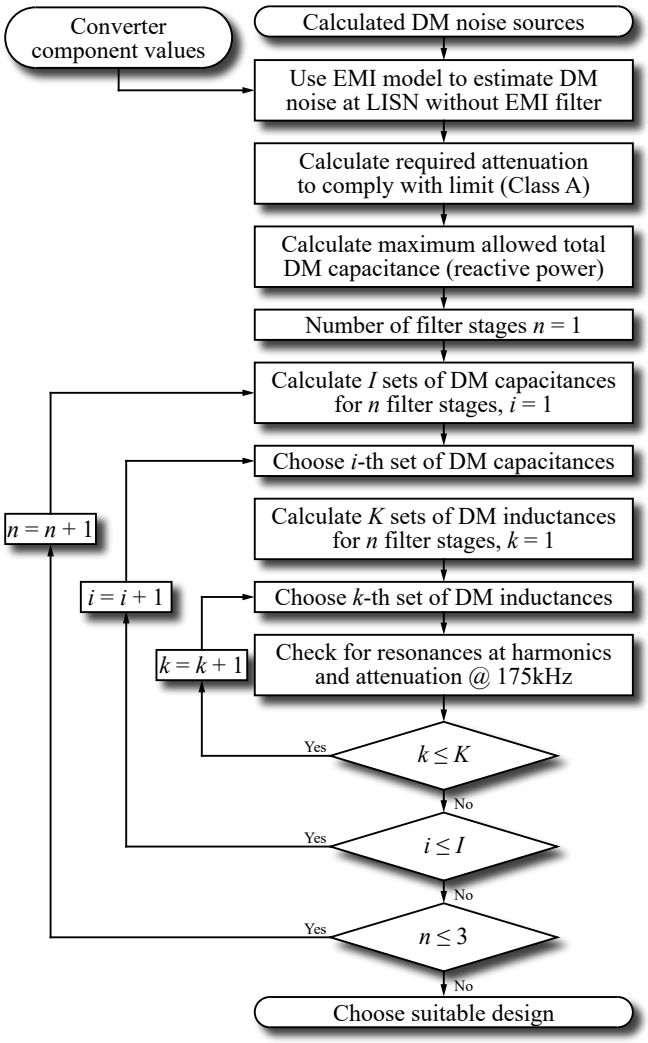

Fig. 10. Step by step illustration of the DM EMI filter design process. For the CM filter, the process is very similar, with the following differences: the maximum CM capacitance is limited by the maximum permissible line-frequency current on PE, the last filter stage has no CM capacitance, and the values of the CM filter capacitances, $C_{\mathrm{cmdc},1}$ and $C_{\mathrm{cmdc},2}$, must also be iterated.

B. DM filter design

Fig. 10 depicts the flow chart of the DM EMI filter design procedure, revealing the individual design steps in simplified form. According to the spectrum of the *Max* estimate depicted in Fig. 9(a), the highest attenuation of $21\,\mathrm{dB}$ is required at the lowest frequency that is relevant for the EMI filter, $f \approx 5f_{\mathrm{s}} = 175\,\mathrm{kHz}$. Therefore, the EMI filter is designed with respect to this requirement. However, the required attenuation at $175\,\mathrm{kHz}$ is increased by $6\,\mathrm{dB}$, to $27\,\mathrm{dB}$, in order to take into account an eventual increase of the EMI noise voltage due to superimposed CM noise voltage components.

In a first step, a single L–C filter stage was considered. However, to achieve the required attenuation, the resonance frequency of this filter stage would need to be equal to $33\,\mathrm{kHz}$, which is very close to the switching frequency and leads to a HF rms current of more than $5\,\mathrm{A}$ at $35\,\mathrm{kHz}$. A significant reduction of this HF current, e.g., to less than $1\,\mathrm{A}$, could only be achieved by substantially increasing the filter inductance and / or capacitance, but this leads to an intolerable increase of the filter volume and / or the reactive power consumption at mains frequency.

For these reasons, the two-stage $L_{\mathrm{dm},1}$–$C_{\mathrm{dm},1}$–$L_{\mathrm{dm},2}$–$C_{\mathrm{dm},2}$ filter structure depicted in **Fig. 11(a)** has been considered in a second step. The resonance frequencies of this network are greater than the switching frequency to allow a small filter volume. In order to prevent resonant amplifications at the harmonics of the switching frequency, a forbidden frequency range was defined around the frequencies of the harmonic components of the EMI noise voltages,

$$f_{\mathrm{forbidden}} \in \left[k f_{\mathrm{s}} - \frac{\Delta f}{2},\ k f_{\mathrm{s}} + \frac{\Delta f}{2} \right], \qquad k \in \mathbb{N}, \tag{22}$$

where it was found that $\Delta f = 6\,\mathrm{kHz}$ enables sufficiently low HF rms currents in the filter inductors. Furthermore, the compact off-the-shelf inductors that are used to realize $L_{\mathrm{dm},1}$ and $L_{\mathrm{dm},2}$ are subject to partial saturation (i.e., their inductances drop with increasing current; the considered peak value of the ac current is $I_{\mathrm{ac,peak}} = 16.4\,\mathrm{A}$). For this reason, the resonance

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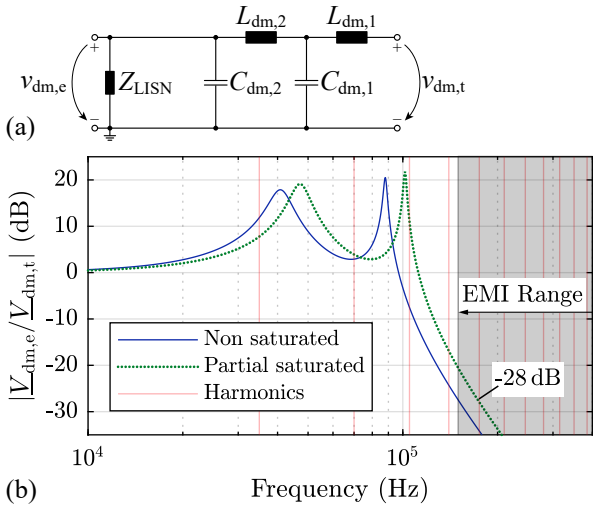

Fig. 11. (a) Implemented DM EMI filter circuit and (b) input-to-output TFs for non-saturated and partially saturated DM inductors (the inductance decreases with increasing current and reaches its minimum at the peak value of the ac current, $I_{\mathrm{ac,peak}} = 16.4\,\mathrm{A}$, Z_{LISN} is approximated with a $50\,\Omega$ resistor).

frequencies of the filter depend on the instantaneous values of the phase currents, which must be taken into account when evaluating (22). Accordingly, the optimization of the EMI filter with respect to minimum filter volume is not straightforward and has been conducted by means of an exhaustive search over a range of possible component values.

This exhaustive search considers a set of initial inductances,

$$L_{\mathrm{dm},1}, L_{\mathrm{dm},2} \in \{3.3,\ 6.8,\ 8.2,\ 10,\ 12,\ 22\}\,\mu\mathrm{H}, \qquad (23)$$

and a set of corresponding reduced inductances (to take partial saturation at $I_{\mathrm{ac,peak}} = 16.4\,\mathrm{A}$ into account),

$$L_{\mathrm{dm},1,\mathrm{min}}, L_{\mathrm{dm},2,\mathrm{min}} \in \{3.2,\ 5.0,\ 6.1,\ 8,\ 9,\ 16.5\}\,\mu\mathrm{H}. \quad (24)$$

For each of the capacitances, $C_{\mathrm{dm},1}$ and $C_{\mathrm{dm},2}$, one ceramic capacitor with $56\,\mathrm{nF}$ in parallel to one or two film capacitors with

$$C \in \{100,\ 120,\ 150,\ 220,\ 330,\ 470\}\,\mathrm{nF} \qquad (25)$$

is considered. **Table IV** lists the component values that result for the optimized EMI filter and **Fig. 11(b)** depicts the Transfer Functions (TFs) of the two-stage filter for unsaturated and partially saturated inductors. The vertical red lines in Fig. 11(b) indicate the harmonics of the switching frequency for $f_{\mathrm{s}} = 35\,\mathrm{kHz}$. The filter achieves an attenuation of at least $28\,\mathrm{dB}$ at a frequency of $5\,f_{\mathrm{s}} = 175\,\mathrm{kHz}$. Furthermore, according to the results of a circuit simulation, the total rms value of all spectral current components with frequencies greater than the line frequency, $f > 50\,\mathrm{Hz}$, is less than $800\,\mathrm{mA}$ in both DM filter inductors, $L_{\mathrm{dm},1}$ and $L_{\mathrm{dm},2}$. Thus, the HF currents in the inductors are much smaller than for the single-stage solution.

Since the second resonance frequency of the DM EMI filter is at $102\,\mathrm{kHz}$, which is close to the third harmonic of the EMI noise at $f = 3 \times 35\,\mathrm{kHz} = 105\,\mathrm{kHz}$, the sidebands of the DM EMI noise at $102\,\mathrm{kHz}$ have been examined more closely in a circuit simulation. The simulation reveals that the maximum amplitudes of the DM EMI noise in the region at $102\,\mathrm{kHz}$ are $30\,\mathrm{dB}$ less than the peak at $105\,\mathrm{kHz}$. In addition, the equivalent series resistances of $L_{\mathrm{dm},1}$ and $L_{\mathrm{dm},2}$ at $105\,\mathrm{kHz}$ are approximately equal to $1\,\Omega$ for each inductor (determined by measuring the impedances of the components), which provides further attenuation of the resonance and consequently leads to a negligible increase in current due to the second resonance frequency of the DM EMI filter.

TABLE IV. Component values of the volume-optimized EMI filter.

DM filter inductance 1	$3 \times L_{\mathrm{dm},1} = 3 \times 12\,\mu\mathrm{H}$
DM filter capacitance 1	$3 \times C_{\mathrm{dm},1} = 3 \times 526\,\mathrm{nF}$
DM filter inductance 2	$3 \times L_{\mathrm{dm},2} = 3 \times 22\,\mu\mathrm{H}$
DM filter capacitance 2	$3 \times C_{\mathrm{dm},2} = 3 \times 356\,\mathrm{nF}$
CM filter inductance 1	$L_{\mathrm{cm},1} = 522\,\mu\mathrm{H}$
CM filter capacitance 1	$C_{\mathrm{cm},1} = 290\,\mathrm{nF}$
Ac-side CM filter inductance	$L_{\mathrm{cm,ac}} = 147\,\mu\mathrm{H}$
Primary-side dc link CM filter cap.	$C_{\mathrm{cmdc},1} = 82\,\mathrm{nF}$
Secondary-side dc link CM filter cap.	$C_{\mathrm{cmdc},2} = 19\,\mathrm{nF}$

C. CM filter design

According to Fig. 9(b), the *Max* estimate of the CM EMI noise voltage slightly increases for increasing frequency. However, this increase will already be more than compensated for with a 2nd-order filter, since the filter's attenuation characteristic is $-40\,\mathrm{dB/decade}$. For this reason, the CM part of the EMI filter must provide an attenuation of $40\,\mathrm{dB}$ at $5\,f_{\mathrm{s}} = 175\,\mathrm{kHz}$ to meet the given limit. This attenuation is increased by $6\,\mathrm{dB}$ to ensure that the total EMI noise voltage, i.e., the superposition of its DM and CM voltage components, does not exceed the given limit and, in addition to this, by $10\,\mathrm{dB}$ to account for component tolerances and uncertainties in the estimations of the parasitic capacitances. With this, a required attenuation of $56\,\mathrm{dB}$ at $175\,\mathrm{kHz}$ results.

The considered CM part of the EMI filter is a third-order $L_{\mathrm{cm},1}$–$C_{\mathrm{cm},1}$–$L_{\mathrm{cm},2}$ filter structure,[10] which is integrated into the previously determined DM part of the EMI filter according to Fig. 1, i.e., $L_{\mathrm{cm},1}$ is connected in series to the three DM filter inductors $L_{\mathrm{dm},2}$, the CM filter capacitor is inserted between the star point formed by the three DM filter capacitors $C_{\mathrm{dm},2}$ and PE, and $L_{\mathrm{cm},2}$ is inserted at the mains-side input of the EMI filter. In addition, CM filter capacitances, $C_{\mathrm{cmdc},1}$ and $C_{\mathrm{cmdc},2}$, are included between the midpoints of the primary-side and secondary-side dc links and PE as shown in Fig. 1. **Fig. 12(a)** depicts the CM equivalent circuit of the EMI filter (without $C_{\mathrm{cmdc},1}$ and $C_{\mathrm{cmdc},2}$, since these capacitors are in parallel to C_1 and C_2, cf. Fig. 1).

Now that the attenuation characteristic and the structure of the CM part of the EMI filter are defined, the component values need to be determined such that minimum filter volume results. In this regard, the stringent limitation of the maximum permissible line-frequency current on PE to a rms value of $3.5\,\mathrm{mA}$ confines the maximum allowable capacitances of the CM EMI filter capacitors to relatively small values. In a considered worst-case scenario, with an assumed line voltage imbalance of $6\,\%$ (according to IEC 60939-3) and capacitance tolerances of $\pm 10\,\%$ (for both the DM and CM EMI filter

[10] In the course of the design of the CM part of the EMI filter, four different filter structures were considered, starting from a 2nd-order structure ($L_{\mathrm{cm},1}$–$C_{\mathrm{cm},1}$) to a 5th-order structure ($L_{\mathrm{cm},1}$–$C_{\mathrm{cm},1}$–$L_{\mathrm{cm},2}$–$C_{\mathrm{cm},2}$–$L_{\mathrm{cm},3}$), with the 3rd-order filter structure achieving the lowest total volume.

capacitors), a maximum allowable value for the sum of the CM EMI filter capacitances, $C_{\mathrm{cmdc},1} + C_{\mathrm{cm},1}$, of $C_{\mathrm{cm},\Sigma} = 399\,\mathrm{nF}$ is determined using the procedure described in [35].

The selection of suitable component values is conducted in the context of an exhaustive search. In a first step, $C_{\mathrm{cm},\Sigma}$ is distributed to $C_{\mathrm{cmdc},1}$ and $C_{\mathrm{cm},1}$ using five discrete values,

$$C_{\mathrm{cmdc},1} = \{0,\, 20\,\%,\, 40\,\%,\, 60\,\%,\, 80\,\%\}\, C_{\mathrm{cm},\Sigma}, \tag{26}$$

$$C_{\mathrm{cm},1} = C_{\mathrm{cm},\Sigma} - C_{\mathrm{cmdc},1}, \tag{27}$$

which, together with the required filter attenuation at $f = 175\,\mathrm{kHz}$, defines the maximum value of the inductance $L_{\mathrm{cm},1,\mathrm{max}}$. Based on this result, $L_{\mathrm{cm},1}$ is chosen using five discrete values,

$$L_{\mathrm{cm},1} = \{20\,\%,\, 40\,\%,\, 60\,\%,\, 80\,\%,\, 100\,\%\}\, L_{\mathrm{cm},1,\mathrm{max}}, \tag{28}$$

and $L_{\mathrm{cm,ac}}$ is calculated with the remaining required filter attenuation at $f = 175\,\mathrm{kHz}$. With this, 25 different designs result for the CM EMI filter, which have been evaluated with regard to the expected volume. The capacitor volumes are estimated with

$$V_{C,\mathrm{cm}} = p_0 + p_1 C, \tag{29}$$

using $p_0 = 1.2 \times 10^{-6}\,\mathrm{m}^3$ and $p_1 = 24\,\mathrm{m}^3\mathrm{F}^{-1}$ (referring to the F881 series of metallized polypropylene film capacitors manufactured by Kemet). Each inductor is optimized in terms of minimum volume, using a specifically implemented optimization procedure that is based on a scalable model of a 3-phase CM EMI inductor with toroidal core.[11] Nanocrystalline material is used for the cores of the CM EMI filter inductors and the three coils are made of solid copper wire. It is to be noted that the optimization method returns capacitors and core dimensions that are not directly available, since the optimization is based on scalable models. Therefore, the most suitable capacitors and cores have to be selected manually in a final step. Table IV lists the final component values.

Fig. 12(b) depicts the frequency response of the EMI filter with respect to CM disturbances and for constant values of the CM EMI filter inductances.[12] At $f = 175\,\mathrm{kHz}$, the first filter stage, composed of $L_{\mathrm{cm},1}$ and $C_{\mathrm{cm},1}$, provides an attenuation of $\approx 40\,\mathrm{dB}$ and the second stage ($L_{\mathrm{cm,ac}}$ and ac-LISN) $\approx 23\,\mathrm{dB}$. The filter capacitors $C_{\mathrm{cmdc},1}$ and $C_{\mathrm{cmdc},2}$ have a negative effect on the attenuation at $f = 175\,\mathrm{kHz}$ and require an additional attenuation of $5\,\mathrm{dB}$. This is due to the fact that $C_{\mathrm{cmdc},1}$ and $C_{\mathrm{cmdc},2}$ attenuate the CM EMI voltage component caused by the currents $i_{\mathrm{cm,p1}}$ and $i_{\mathrm{cm,p2}}$, but not the voltage components that are due to the currents $i_{\mathrm{cm,bst}}$ and $i_{\mathrm{cm,dab}}$, cf. Fig. 8. Accordingly, $C_{\mathrm{cmdc},1}$ and $C_{\mathrm{cmdc},2}$ become mainly effective at high frequencies where the CM EMI noise currents $i_{\mathrm{cm,bst}}$ and $i_{\mathrm{cm,dab}}$ in Fig. 8(b) are well attenuated by the second-order filter structures $L_\sigma/3$–$3C_{\mathrm{f1}}$ and $L_{\mathrm{ac}}/3$–$3C_{\mathrm{f1}}$, respectively. At 1 MHz, for example, inserting $C_{\mathrm{cmdc},1}$ and $C_{\mathrm{cmdc},2}$ increases the CM attenuation by $20\,\mathrm{dB}$.

As a result, the EMI filter achieves a CM attenuation of $58\,\mathrm{dB}$ at $f = 175\,\mathrm{kHz}$. Compared to the required attenuation of $56\,\mathrm{dB}$ determined at the beginning of this subsection, the total attenuation is $2\,\mathrm{dB}$ higher, which is related to the final step of the design of the CM part of the EMI filter, where suitable capacitors and cores have to be selected manually. In this regard, each component value resulting from the optimization is between a smaller and a larger available component. To be on the safe side, the larger component was always chosen for the realization.

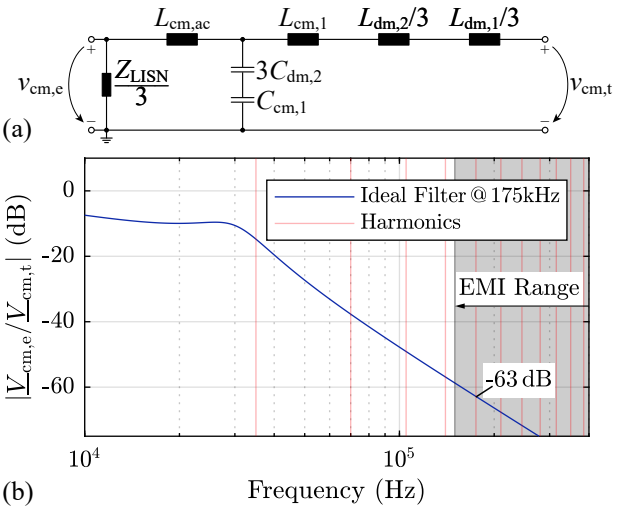

Fig. 12. (a) Implemented CM EMI filter circuit and (b) input-to-output TF of the CM EMI filter for the component values listed in Table IV ($Z_{\mathrm{LISN}}/3$ is approximated with a $16.7\,\Omega$ resistor).

V. Measurements

This section presents a verification of the EMI noise calculated with the EMI models derived in Section III using measurement results. In this regard, **Section V-A** presents the realized hardware demonstrator, **Section V-B** describes the measurements of the DM and CM TFs of the EMI propagation paths and the realized EMI filter, and **Section V-C** shows measured waveforms of the ac-side phase voltages and phase currents to confirm the converter's capability, when operating as a PFC rectifier at the considered power levels. Finally, Section V-D presents the results of EMI measurements and provides a comparison with the calculated EMI noise.

A. Hardware

Fig. 13(a) depicts the realized hardware demonstrator of the D3ABC that features a total rated power of $7.5\,\mathrm{kW}$. The converter is designed to be operated as a bidirectional three-phase PFC rectifier, with the line connected to the port ac_1 and the various dc loads connected to ports dc_1 and dc_2. The outer dimensions of the converter including the EMI filter are $150\,\mathrm{mm} \times 240\,\mathrm{mm} \times 54\,\mathrm{mm} = 5.91\,\mathrm{in} \times 9.45\,\mathrm{in} \times 2.13\,\mathrm{in}$

[11] A simplified model is used to determine the inductance value and the current densities in the coils. The optimization procedure ensures that the inductance value of the resulting design does not fall below the required inductance value given a permeability of $27\,\mathrm{mH/m}$ and the current densities in the coils remain below the maximum permissible current density of $10\,\mathrm{A/mm^2}$ given a fill factor of 0.5. Since the CM voltage after the first stage is already low (e.g., $120\,\mathrm{dB\mu V}$ at $175\,\mathrm{kHz}$, cf. Fig. 9(b)), possible saturation of the inductance cores is neglected.

[12] The permeability of nanocrystalline magnetic core material and, thus, the inductances of the CM filter inductors decrease for increasing frequency. The attenuation characteristic evaluated in the optimization and depicted in Fig. 12(b) was calculated for the inductances present at $f = 175\,\mathrm{kHz}$.

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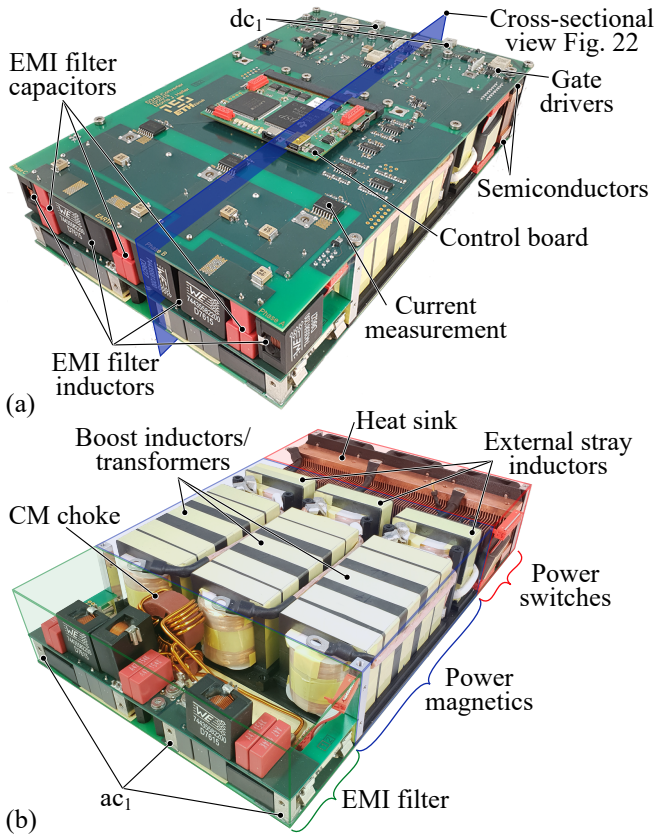

Fig. 13. Hardware demonstrator of a D3ABC with 7.5 kW total power. The outer dimensions are 150 mm × 240 mm × 54 mm = 5.91 in × 9.45 in × 2.13 in (width × depth × height). (a) The upper PCB contains control board, current sensors, and primary-side power semiconductors with their gate drivers. (b) Without upper PCB, the arrangement of the EMI filter, the boost inductors (transformers), the stray inductors, and the heat sinks for the power semiconductors are visible (from front to back). Dc port 2 is not visible on these pictures. The blue plane shows the location of the cross-sectional view in Fig. 22.

(width × depth × height), resulting in a power density of $4.1\,\mathrm{kW/dm^3} = 67.4\,\mathrm{W/in^3}$.

The top PCB contains the control board with the sensors (e.g., phase current measurement), the primary-side power semiconductors, and their gate drivers. Furthermore, the filter capacitors, C_{f1}, and the DM filter inductors and capacitors of the first filter stage, $L_{\mathrm{dm},1}$ and $C_{\mathrm{dm},1}$, are soldered to the top PCB as well. The picture in **Fig. 13(b)** shows the hardware demonstrator without top PCB, revealing (from the front to the back) the arrangement of the EMI filter components (without C_{f1}, $L_{\mathrm{dm},1}$, and $C_{\mathrm{dm},1}$), the boost inductors/transformers, the external stray inductors, and the copper heat sink for the power semiconductors.

The power semiconductors are mounted with a thin layer of thermally conductive and electrically isolating foil onto a two-sided copper heat sink, with the semiconductors of the primary side mounted on top and those of the secondary side mounted on the bottom. The conductive heat sink is connected directly to the CM filter capacitors $C_{\mathrm{cmdc},1}$ and $C_{\mathrm{cmdc},2}$ and is grounded through PE.

The external stray inductor is connected in series to the secondary-side winding of the transformer (as described in [18]). Its magnetic core is realized with two E42/21/15 N95 ferrite core halves and features a distributed air gap of $3 \times 1.5\,\mathrm{mm}$. The coil is made with HF litz-wire (1200 strands with single-strand diameter of 71 µm) and consists of 12 turns.

TABLE V. EMI filter components with their nominal values (A_{L} value at 100 kHz for the nanocrystalline magnetic cores).

Component	Mfr.	Part number	Nom. val.	#
C_{f1}	TDK	B32754C2106K000	10 µF	1
C_{f2}	TDK	C5750X6S2W225K250KA	2.2 µF	21
$L_{\mathrm{dm},1}$	Wurth	74435581200	12 µH	1
$C_{\mathrm{dm},1}$	Wurth	890334025039CS	470 nF	1
	Murata	GA355XR7GB563KW06L	56 nF	1
$L_{\mathrm{dm},2}$	Wurth	74435582200	22 µH	1
$C_{\mathrm{dm},2}$	Wurth	890334025022CS	150 nF	2
	Murata	GA355XR7GB563KW06L	56 nF	1
$C_{\mathrm{cmdc},1}$	Kemet	F881BC153(3)300(2)	15 nF	5
	Murata	GA355DR7GF472KW01L	4.7 nF	2
$C_{\mathrm{cmdc},2}$	Kemet	F881BC153(3)300(2)	15 nF	1
	Murata	GA355DR7GF472KW01L	4.7 nF	1
$L_{\mathrm{cm},1}$	Vac	W380	11.6 µH	1
$C_{\mathrm{cm},1}$	Kemet	R413I247000M1K	47 nF	6
	Murata	GA355DR7GF472KW01L	4.7 nF	2
$L_{\mathrm{cm,ac}}$	Vac	W515	5.16 µH	1

The boost inductor/transformer employs a magnetic core that is realized with eight TDK E42/21/20 N95 ferrite core halves (giving four stacked E-cores). Each E-core, i.e., a set of two core halves, realizes a distributed air gap of $3 \times 0.5\,\mathrm{mm}$, which defines the main inductance of the boost inductor/transformer. Both the primary-side and the secondary-side coils are made with HF litz-wire (1200 strands with single-strand diameter of 71 µm) and have 5 turns on the primary side and 13 turns on the secondary side.

The components used for C_{f1}, C_{f2} (described in [18]), and the EMI filter described in this paper are summarized in **Table V**. The CM EMI filter inductors $L_{\mathrm{cm},1}$ and $L_{\mathrm{cm,ac}}$ each have 3 coils with 5 and 3 turns, respectively, using a solid copper wire with a diameter of $1.8\,\mathrm{mm}$. The DM and CM filter capacitors are realized by parallel connections of film capacitors and ceramic capacitors. The total volume of the designed EMI filter is $0.17\,\mathrm{dm^3}$ ($0.09\,\mathrm{dm^3}$ for the DM part and $0.08\,\mathrm{dm^3}$ for the CM part of the EMI filter).

B. Measured TFs of EMI propagation paths

The measurement results presented in this Section were obtained from small-signal measurements, i.e., the complete hardware setup was subject to voltages in the range of several volts. Accordingly, the port ac_1 was not connected to the three-phase ac lines in these measurements.

The aim of these measurements is to verify the EMI models derived in Section III together with the EMI filter using experimental results. According to the derived EMI noise models, four different noise sources need to be considered: $v_{\mathrm{dm},1}$, $v_{\mathrm{cm},1}$, $v_{\mathrm{dm},2}$, and $v_{\mathrm{cm},2}$. Each of these noise sources contributes to the voltage at the ac-LISN. Thus, all four TFs, from each noise source to the ac-LISN, must be known to calculate the voltage at the ac-LISN. The measurement of these four TFs is conducted directly on the hardware prototype, using a Vector Network Analyzer (VNA).

Fig. 14 depicts the measurement setup for measuring the TF from $v_{\mathrm{dm},1}$ to the ac-LISN as an example. A signal transducer injects the reference voltage of the VNA, i.e., a sinusoidal voltage with frequency f, at the switching nodes of

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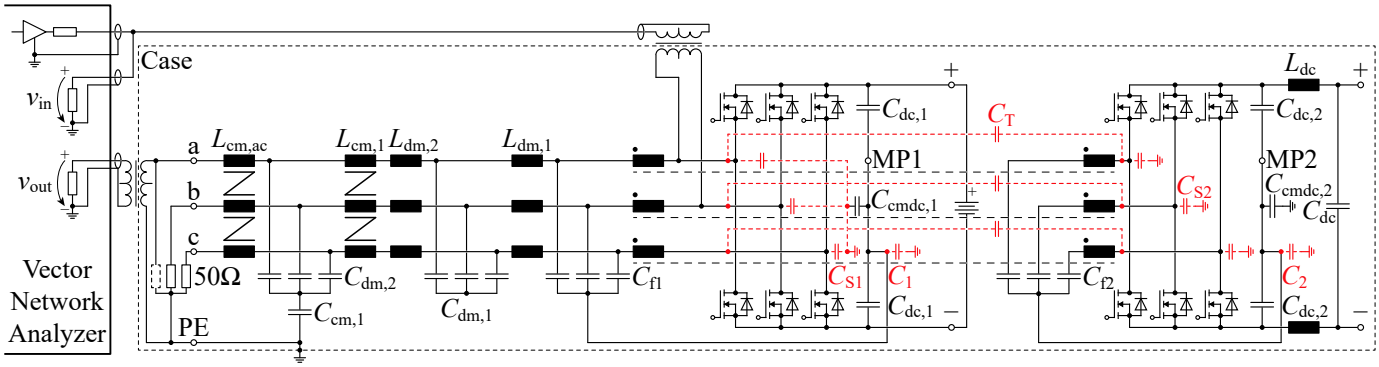

Fig. 14. Setup used to measure the TF of the EMI filter from the primary-side DM voltage source, $v_{\mathrm{dm},1}$, to the port ac_1 using a Vector Network Analyzer (VNA) that is connected to the hardware via two 1:1 transformers (T1-6T-X65+ by Mini-Circuits). The hardware is placed in an aluminum enclosure with the dimensions $400\,\mathrm{mm} \times 310\,\mathrm{mm} \times 110\,\mathrm{mm}$, which emulates a converter housing. A $9\,\mathrm{V}$ battery connected to the primary-side dc link prevents a clipping of the input signal by the antiparallel diodes of the MOSFETs. The semiconductors on the secondary side are all turned on. Similar configurations are used to measure the remaining three TFs of the EMI filter, i.e., with respect to the CM components and as seen from the secondary side.

two primary-side half-bridges of the power stage to emulate DM EMI noise. The VNA measures the reference voltage, v_{in}, and the voltage at port ac_1, v_{out}, where the three-phase lines would be connected through the ac-LISN. The HF impedance of the ac-LISN is emulated by three $50\,\Omega$ resistors, which are connected to port ac_1 (the resistor with dashed outline in Fig. 14 refers to the input resistance of the VNA). Due to the symmetry of the converter topology and the EMI filter network, it can be assumed that v_{in} is distributed equally between phase a and phase b and thus,

$$v_{\mathrm{dm,1,a}} = \frac{v_{\mathrm{in}}}{2},\ v_{\mathrm{dm,1,b}} = -\frac{v_{\mathrm{in}}}{2},\ v_{\mathrm{dm,1,c}} = 0 \qquad (30)$$

applies. In order to prevent the MOSFETs' antiparallel diodes from turning on and potentially clipping the reference voltage, the dc link of the half-bridges is precharged with a $9\,\mathrm{V}$ battery. Large resistors between the phases and in parallel with the dc link capacitors (intended for voltage measurement during operation of the converter) ensure that the potentials at the switching nodes will be approximately between the two potentials of the positive and the negative rails of the dc link. It should be noted that the non-linear output capacitances of the MOSFETs, C_{OSS}, are relatively large at $9\,\mathrm{V}$ dc link voltage. These capacitances are connected in parallel to the reference voltage source of the VNA. The additional loading of the VNA's output amplifier by C_{OSS} causes a voltage drop across the amplifier's inner impedance. However, due to the explicit measurement of the reference voltage at the system input, v_{in}, the impact of C_{OSS} on the measured TFs is minimized.

The remaining noise sources, in this case $v_{\mathrm{cm},1}$, $v_{\mathrm{dm},2}$, and $v_{\mathrm{cm},2}$, need to be set to zero. According to (30), the primary-side CM EMI noise voltage, $v_{\mathrm{cm},1}$, as defined in (13) is already zero for this measurement setup. Turning on all semiconductors on the secondary side sets the noise sources $v_{\mathrm{dm},2}$ and $v_{\mathrm{cm},2}$ to zero. It is to be noted that the measured TF needs to be multiplied by 2 to account for the $1/2$ in the excitation (30). Furthermore, a signal transducer must be inserted between port ac_1 of the converter and the VNA to enable this measurement, since the VNA and the converter share a common ground potential. The signal transducers used are off-the-shelf devices (T1-6T-X65+ by Mini-Circuits), which feature a bandwidth of $f \in [15\,\mathrm{kHz},\ 300\,\mathrm{MHz}]$. To achieve reproducible measurements with respect to parasitic capacitances, the hardware is placed in an aluminum EMI enclosure with the dimensions $400\,\mathrm{mm} \times 310\,\mathrm{mm} \times 110\,\mathrm{mm} = 15.7\,\mathrm{in} \times 12.2\,\mathrm{in} \times 4.3\,\mathrm{in}$ (width $\times$ depth $\times$ height) to emulate a converter housing.

To measure the TF from $v_{\mathrm{cm},1}$ to the ac-LISN, the circuit shown in Fig. 14 is modified as described in the following. The switching nodes of the converter phases a, b, and c are connected together and the VNA applies the reference voltage between this common switching node and the primary-side midpoint of the dc link, MP1, using a signal transducer (T1-6T-X65+). With this, the primary-side DM EMI noise sources are shorted, i.e., $v_{\mathrm{dm,1,a,b,c}} = 0$ applies. Note that by connecting the reference voltage to MP1, the primary-side dc link capacitances, $C_{\mathrm{dc},1}$, are in parallel to the input voltage and are therefore not included in the measurement. Due to the low impedances of the dc link capacitors, negligible implications on the measurement results can be assumed. The dc link of the half-bridges is kept precharged with the previously mentioned battery.

For the measurements of the TFs from the secondary-side EMI noise sources, $v_{\mathrm{dm},2}$ and $v_{\mathrm{cm},2}$, to the ac-LISN, the reference voltage is applied in the same way as for the measurements on the primary side, but on the secondary side. The $9\,\mathrm{V}$ battery is placed in parallel to the secondary-side dc link and the primary-side MOSFETs are turned on instead of the secondary-side MOSFETs.

Fig. 15 depicts measured and calculated magnitude responses of the four TFs. The blue curves refer to measurement results that were obtained for a resolution bandwidth of $3\,\mathrm{Hz}$, at 800 logarithmically distributed points in the frequency range $f \in [10\,\mathrm{kHz}, 30\,\mathrm{MHz}]$, and for a power level of the reference signal of $13\,\mathrm{dBm}$.[13] The dash-dotted green and dotted curves represent calculated results that have been obtained using the equivalent circuit diagrams shown in Fig. 7 and Fig. 8 and the filter networks shown in Fig. 11 and Fig. 12. In this context, the dotted curves depict the results under the assumption of ideal impedances of all components according to Table II,

[13]The set power level of the reference signal refers to the power that is dissipated in a $50\,\Omega$ matching resistor if only this $50\,\Omega$ resistor is connected to the output of the VNA; $0\,\mathrm{dBm}$ is equal to $1\,\mathrm{mW}$.

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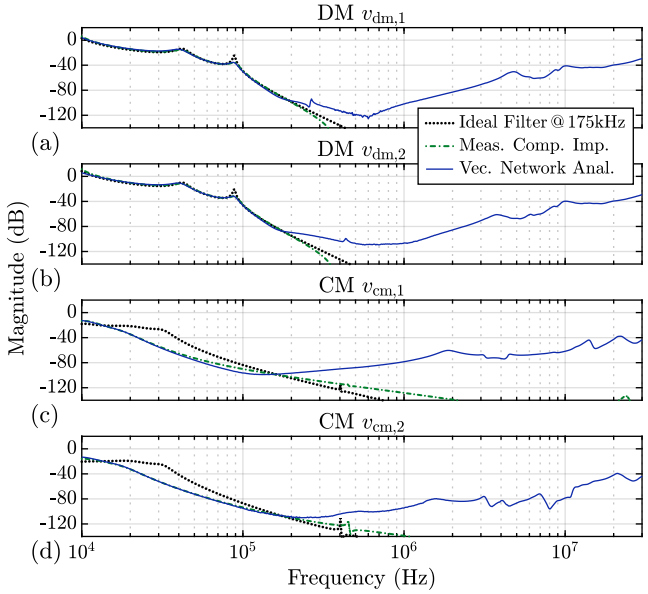

Fig. 15. Frequency responses of the EMI propagation paths of the whole converter measured from: (a) the primary-side DM voltage source, $v_{\mathrm{dm},1}$, (b) the secondary-side DM voltage source, $v_{\mathrm{dm},2}$, (c) the primary-side CM voltage source, $v_{\mathrm{cm},1}$, and (d) the secondary-side CM voltage source, $v_{\mathrm{cm},2}$. The dotted curves depict calculated results for constant component values, the dash-dotted green curves represent calculated results using measured impedance characteristics for all filter components, and the blue curves show the measured frequency responses of the filter. The dash-dotted green and the blue curves are in good agreement up to a frequency of $f = 200\,\mathrm{kHz}$. Parasitic effects, e.g., capacitive coupling between filter stages, prevent a further increase of the attenuation above this frequency.

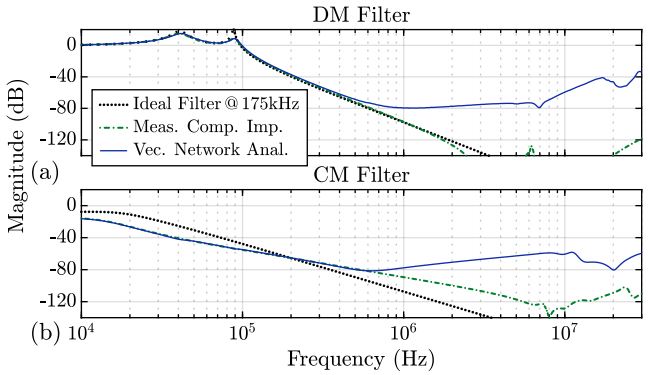

Fig. 16. Frequency responses of the (a) DM and (b) CM EMI filter. The dotted curves depict calculated results for constant component values, the dash-dotted green curves represent calculated results using measured impedance characteristics for all filter components, and the blue curves show the measured frequency responses of the filter. The dash-dotted green and the blue curves are in good agreement up to a frequency of $f = 500\,\mathrm{kHz}$. Parasitic effects, e.g., capacitive coupling between filter stages, prevent a further increase of the attenuation above this frequency.

Table III, and Table IV. Since the magnetic material of the CM filter inductors is highly dependent on the frequency, their A_{L} values were chosen to match the value of the material measured at $f = 175\,\mathrm{kHz}$. The dash-dotted green curves have been determined from measured frequency characteristics of all filter components. These frequency characteristics were measured separately for each component with an impedance measurement device (Agilent 4294A, $40\,\mathrm{Hz}$ to $110\,\mathrm{MHz}$) before the hardware was assembled. With this approach, non-ideal effects such as frequency dependency, series resistances, and component self-resonances are taken into account.

According to Fig. 15, the measured magnitude responses are in good agreement with the predictions at low frequencies $f < 200\,\mathrm{kHz}$, except for the CM attenuations calculated with the linearized CM filter inductors (dotted curves) that match the measurements only at the design frequency of $175\,\mathrm{kHz}$. For frequencies $f > 200\,\mathrm{kHz}$ a continuing increase of the attenuation is predicted but the measured attenuation no longer increases. This discrepancy is explained by the simultaneous presence of parasitic capacitive couplings between filter components, further investigated in Section V-D, and high filter attenuation in the range of $80\,\mathrm{dB}$ to $100\,\mathrm{dB}$ for $150\,\mathrm{kHz} < f < 1\,\mathrm{MHz}$. Due to these circumstances, a further increase of the attenuation is not feasible even at comparably low frequencies. In the context of an example, it is assumed that a parasitic coupling capacitance of $100\,\mathrm{fF}$ is effective in parallel with each phase of the EMI filter, i.e., between the line-side terminal of each phase and the switching node of the half-bridge of the same phase. A circuit simulation conducted in this regard reveals that the couplings caused by these parasitic capacitances are sufficient to prevent a further increase of the attenuation for $f > 200\,\mathrm{kHz}$. Above $f > 200\,\mathrm{kHz}$ the parasitic couplings between the components dominate the filter's attenuation characteristics.

For completeness, the calculated and measured TFs of the DM and CM parts of the EMI filter have been assessed as well. Similar to Section V-B, the calculations are conducted using ideal impedances and measured impedance characteristics of the individual components. The measurements are carried out with the VNA connected to the hardware realization of the EMI filter. **Fig. 16(a)** shows the measured and calculated attenuation characteristics of the DM filter, which agree well for low frequencies, $f < 500\,\mathrm{kHz}$. Above $f > 500\,\mathrm{kHz}$, the model predicts a further increase in attenuation, however, the measured attenuation no longer increases. This discrepancy is again explained by the simultaneous presence of parasitic capacitive couplings between filter components and high filter attenuation in the range of $80\,\mathrm{dB}$, due to which a further increase of the attenuation is not feasible as explained above. The comparison of the CM filter attenuation in **Fig. 16(b)** shows similar behavior, except that the CM attenuation calculated with the linearized CM filter inductances (dotted curve) agrees with the measurement only at the design frequency of $175\,\mathrm{kHz}$.

C. Rectifier operation

The conducted EMI noise of the D3ABC is measured for rectifier operation with load resistors connected to the ports dc_1 and dc_2 and for the operating voltages specified in Table I. The three phases of the mains are connected to port ac_1 through an ac-LISN and the load resistors are connected to ports dc_1 and dc_2 via the dc-LISNs, respectively. To investigate the implication of the secondary-side power level on the level of conducted EMI noise at port ac_1, two different scenarios with different loads, P_1 and P_2, are considered at the ports dc_1 and dc_2, respectively.

- Scenario 1 (S1): $P_1 = 4\,\mathrm{kW}$, $P_2 = 2.5\,\mathrm{kW}$

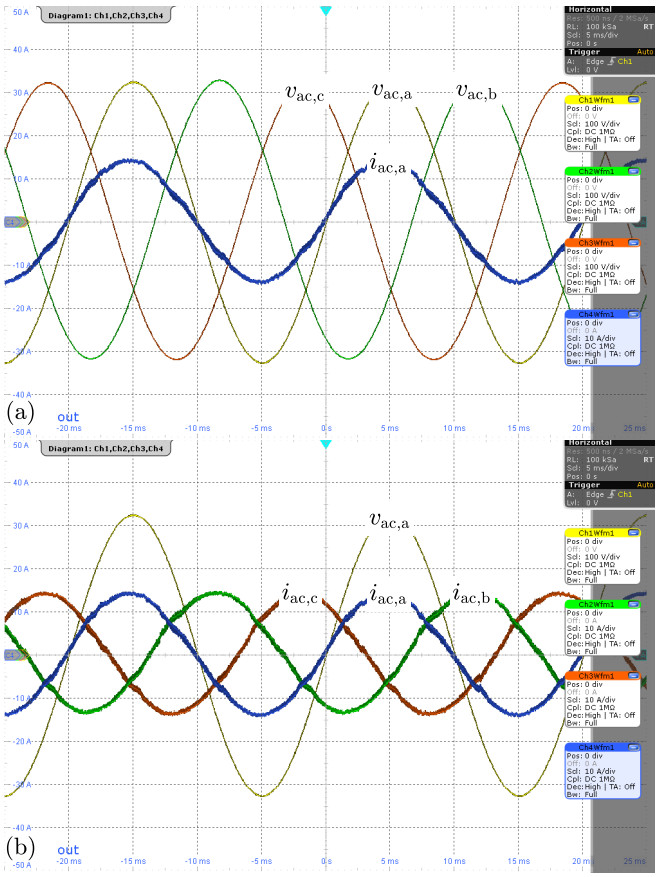

Fig. 17. Screenshots from an oscilloscope showing: (a) all three phase voltages (phase to neutral) and the phase current of phase a at port ac_1; (b) the phase voltage of phase a and all three phase currents at port ac_1. The converter operates as a PFC rectifier with a three-phase voltage source connected to the port ac_1 ($f_\mathrm{m} = 50\,\mathrm{Hz}$, $V_\mathrm{ac,rms} = 230\,\mathrm{V}$) and load resistors connected to the dc ports ($P_1 = 4\,\mathrm{kW}$ on dc_1 and $P_2 = 2.5\,\mathrm{kW}$ on dc_2).

- Scenario 2 (S2): $P_1 = 0$, $P_2 = 6.5\,\mathrm{kW}$

The total load, $P_1 + P_2 = 6.5\,\mathrm{kW}$, is limited by the maximum allowed rms current of the employed ac-LISN, $I_\mathrm{LISN,rms} < 10\,\mathrm{A}$. To comply with this limit, the power P_1 is reduced from $5\,\mathrm{kW}$, i.e., the power used to design the EMI filter in Section IV, to $4\,\mathrm{kW}$.

Fig. 17 shows the measured phase voltages, $v_\mathrm{ac,a}$, $v_\mathrm{ac,b}$, and $v_\mathrm{ac,c}$, together with the measured phase currents, $i_\mathrm{ac,a}$, $i_\mathrm{ac,b}$, $i_\mathrm{ac,c}$ for S1 (only four signals are measured at a time due to the limited number of measurement channels; for the purpose of reference, the voltage and current of phase a are shown in Fig. 17(a) and Fig. 17(b)). The waveforms of the phase voltages of phases a, b, and c depicted in Fig. 17(a) are sinusoidal and phase-shifted by $120\,^\circ$ with respect to each other, as described by (1). The currents in Fig. 17(b) are sinusoidal and in phase with the corresponding phase voltages, resulting in a Power Factor (PF) close to one, $\lambda = 0.994$. The Total Harmonic Distortion (THD) of the currents is $\mathrm{THD} \leq 5.6\,\%$. Similar waveforms result for the voltages and currents for S2, hence they are not shown here.

D. EMI measurements

To achieve reproducible EMI measurements, the hardware is placed in the same aluminum EMI enclosure used in Section V-B, with which the parasitic ground capacitances are defined. Furthermore, a CM EMI filter inductor is connected to dc_1, to evaluate the worst-case workload scenario with regard to CM EMI noise as described in Section III. This CM filter inductor is realized with a nanocrystalline core (W518 by Vacuumschmelze), which contains two windings with 5 turns each and features a CM inductance of $627\,\mu\mathrm{H}$ at $f = 100\,\mathrm{kHz}$.

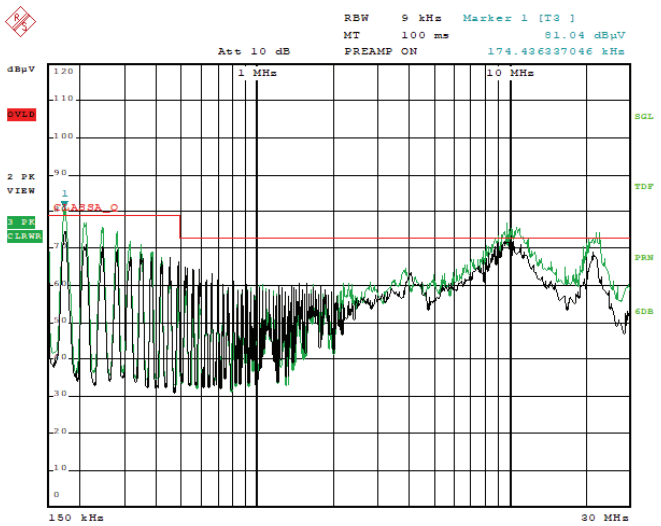

Fig. 18. Screenshot taken from the EMI test receiver (the shown result was measured for phase c). The converter operates as a PFC rectifier with a three-phase voltage source connected to port ac_1 ($f_\mathrm{m} = 50\,\mathrm{Hz}$, $V_\mathrm{ac,rms} = 230\,\mathrm{V}$), providing a total output power of $6.5\,\mathrm{kW}$ at the dc ports. The black curve, which was measured for an output power of $P_1 = 4\,\mathrm{kW}$ at dc_1 and $P_2 = 2.5\,\mathrm{kW}$ at dc_2, is below the CISPR class A limit for QP values (shown in red). The green curve, which was measured for $P_1 = 0$ and $P_2 = 6.5\,\mathrm{kW}$, slightly exceeds the limit at $f \approx \{175\,\mathrm{kHz}, 10\,\mathrm{MHz}, 21\,\mathrm{MHz}\}$.

The three measurement outputs of the ac-LISN, i.e., one for each phase, are connected one after another to a test receiver, which measures the EMI noise with a maximum peak detector (the maximum peak detector overestimates the EMI noise but allows for a substantially faster measurement compared to the QP detector). The EMI noise levels measured for phase a, b, and c are very similar (with deviations of less than $3.5\,\mathrm{dB}$ at $f = 175\,\mathrm{kHz}$) with phase c showing the highest level of EMI noise. **Fig. 18** depicts a screenshot of the test receiver's monitor illustrating the spectra of the EMI noise levels in phase c (black curve: S1, green curve: S2). In case of S1, the EMI noise is consistently below the class A QP limit. With regard to S2, the EMI noise slightly exceeds the limit at $f = 175\,\mathrm{kHz}$ by $2\,\mathrm{dB}$ and additionally at higher frequencies with a maximum exceedance of $4\,\mathrm{dB}$ at $f = 9.75\,\mathrm{MHz}$.

In order to experimentally verify the derived model, the measured spectra of EMI noise are compared to corresponding EMI noise spectra. In this context, the spectra are calculated using two different methods, which provides a deeper insight into the capabilities and limitations of the models derived in Section III. For the first method illustrated in **Fig. 19** on the left, the rms value spectra of the DM and CM EMI noise for the converter, $v_\mathrm{dm,t}$ and $v_\mathrm{cm,t}$, are calculated for S1 and S2 as described in Section III-C taking into account the filter capacitances $C_\mathrm{cmdc,1}$ and $C_\mathrm{cmdc,2}$. In a subsequent step, these spectra are multiplied by the associated, i.e., DM or CM, calculated filter TFs shown in Fig. 16 (with respect to

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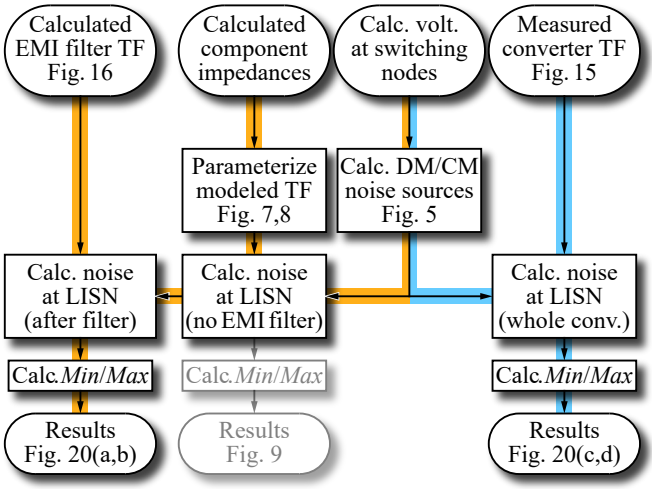

Fig. 19. Flow chart illustrating the procedures used to estimate EMI noise. The path on the left with orange background represents the fast calculation method which is solely based on analytical models and calculated (constant) component values. The path on the right with light blue background represents the accurate calculation method using measured TF to evaluate the EMI propagation paths.

magnitude and phase). Finally, the DM and CM components are summed up for each workload scenario by means of superposition, which gives the spectrum of the total EMI noise, $V_{\mathrm{emi,rms}}(f)$. This enables the calculation of the *Min* estimate, $V_{\mathrm{emi,min}}$, and the *Max* estimate, $V_{\mathrm{emi,max}}$, based on (17) and (18) (there, $V_{\mathrm{dm,rms}}$ must be replaced by $V_{\mathrm{emi,rms}}$). Since this calculation method uses the model with calculated component values, it allows a fast EMI noise estimation at an early stage of the converter design. Therefore, it is in the following referred to as fast method.

For the second method, the rms value spectra of the DM and CM EMI noise voltage components, $v_{\mathrm{dm},1}$, $v_{\mathrm{cm},1}$, $v_{\mathrm{dm},2}$, and $v_{\mathrm{cm},2}$, are determined for S1 and S2 from the (rectangular) voltages at the switching nodes of the primary-side and secondary-side half-bridges as described in Section III-C. In a subsequent step, these spectra are multiplied by the associated measured filter TF shown in Fig. 15. The resulting four noise spectra at the output of the filter, i.e., at the ac-LISN, are summed up for each workload scenario by means of superposition, which gives the spectrum of the total EMI noise, $V_{\mathrm{emi,rms}}(f)$. With $V_{\mathrm{emi,rms}}(f)$, again the *Min* and the *Max* estimates are calculated similarly to (17) and (18). Since this calculation method uses measured TFs of the actual hardware, it allows a more accurate estimation of the EMI noise and is therefore in the following referred to as accurate method.

Fig. 20(a) and **Fig. 20(b)** depict the obtained results for S1 and S2, respectively, using the fast method described above. The black curves reveal the measured EMI noise of phase c, the lightblue curves refer to the *Min* estimate and the orange curves to the *Max* estimate. The measured EMI noise level at the first spectral component entering the EMI regulated band, i.e., at $f = 175\,\mathrm{kHz}$, is as expected between $V_{\mathrm{emi,min}}$ and $V_{\mathrm{emi,max}}$. It is also evident that both, the measured and the estimated noise levels depend on the secondary-side load and show an increase in the measured noise level from $75\,\mathrm{dB\mu V}$ to $82\,\mathrm{dB\mu V}$ at $f = 175\,\mathrm{kHz}$ between scenario S1 in Fig. 20(a)

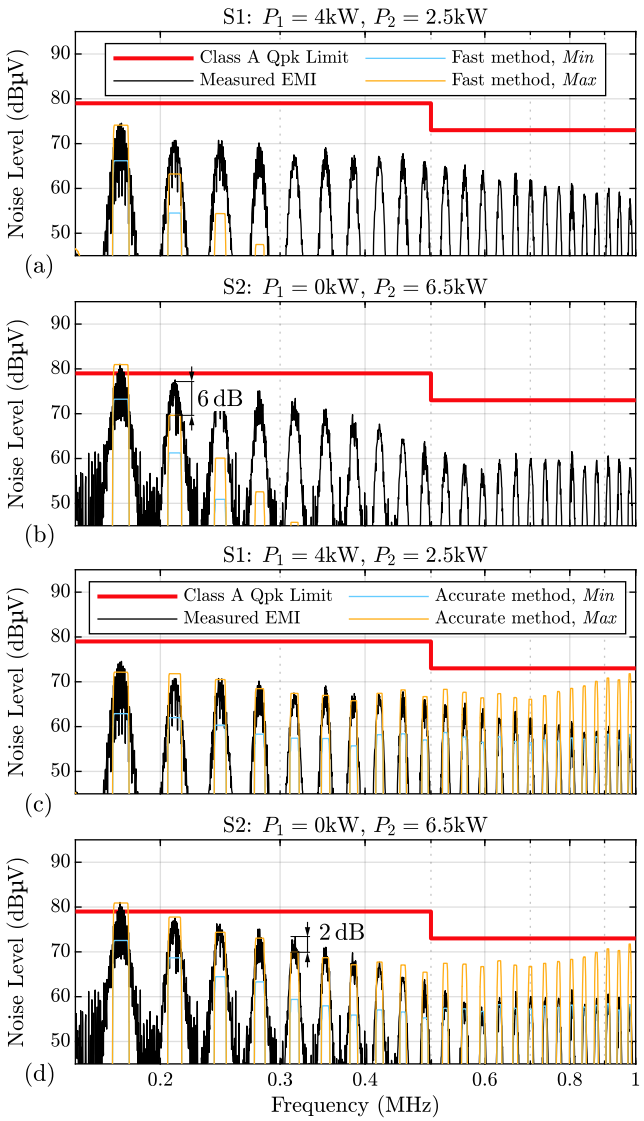

Fig. 20. Measured maximum peak EMI noise at phase c of the ac-LISN connected to the D3ABC. The converter operates as PFC rectifier with a three-phase voltage source connected to port ac_1 ($f_{\mathrm{m}} = 50\,\mathrm{Hz}$, $V_{\mathrm{ac,rms}} = 230\,\mathrm{V}$). The levels of EMI noise are measured for a total power of $6.5\,\mathrm{kW}$ and different distributions of the dc loads. The measured noise is compared to the *Min*/*Max* estimates obtained with the fast calculation method in (a) for $P_1 = 4\,\mathrm{kW}$ and $P_2 = 2.5\,\mathrm{kW}$ and in (b) for $P_1 = 0$ and $P_2 = 6.5\,\mathrm{kW}$ and with the accurate calculation method in (c) for $P_1 = 4\,\mathrm{kW}$ and $P_2 = 2.5\,\mathrm{kW}$ and in (d) for $P_1 = 0$ and $P_2 = 6.5\,\mathrm{kW}$.

and S2 in Fig. 20(b). This reveals a good agreement between measured and estimated noise levels at this frequency.

For harmonics above $f > 175\,\mathrm{kHz}$, the calculated attenuation is larger than the measured attenuation and the measurement is no longer located between the *Min*/*Max* estimates. To explain this discrepancy, the measured noise is compared to the results calculated with the accurate method as well. **Fig. 20(c)** and **Fig. 20(d)** depict the results for S1 and S2, respectively. For this method, the measured EMI noise levels are mostly located between $V_{\mathrm{emi,min}}$ and $V_{\mathrm{emi,max}}$, revealing a good agreement between measured and estimated noise levels over the entire frequency range under consideration. The remaining mismatch of up to $2\,\mathrm{dB}$ at certain frequencies, e.g., at $f = 315\,\mathrm{kHz}$ indicated in Fig. 20(d), can be explained by

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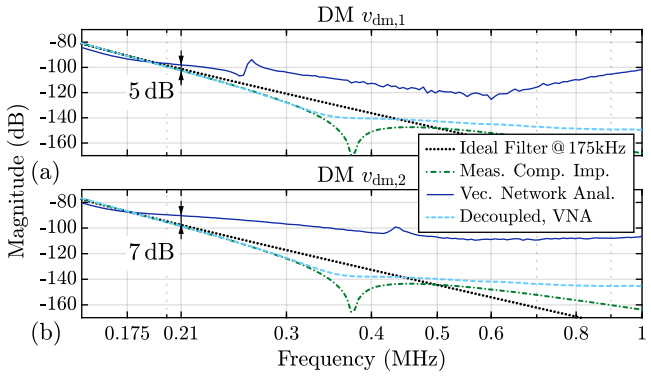

Fig. 21. Detailed view of the frequency responses depicted in Fig. 15(a) and Fig. 15(b). Each light blue dashed line shows the magnitude of the product of the measured TFs of the EMI filter and the converter without EMI filter, thus neglecting the parasitic couplings between converter and EMI filter. This has up to a frequency of $f = 450\,\mathrm{kHz}$ a lower attenuation than predicted by the calculation (dotted line). The resonance at approximately $350\,\mathrm{kHz}$ is the self-resonance of the large filter capacitance C_{f1}.

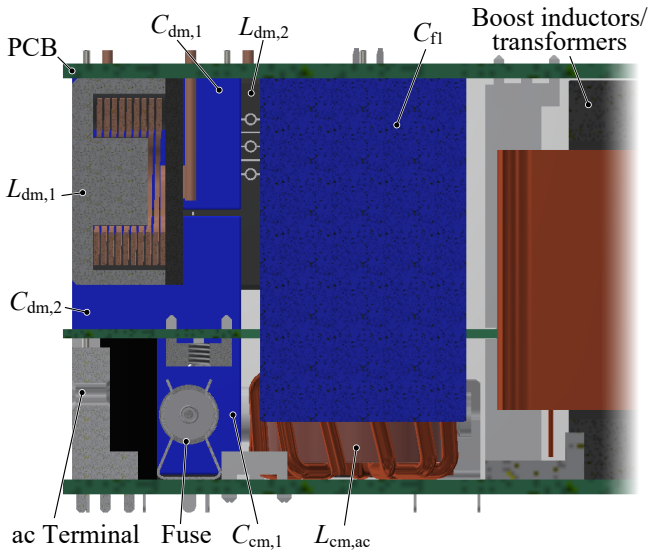

Fig. 22. Cross-sectional view created with a Computer Aided Design (CAD) software along the plane shown in Fig. 13(a) showing a part of the EMI filter. To achieve high power density, as required for industry-like demonstrator systems, the components are densely packed. This can lead to parasitic couplings between the converter and the EMI filter and between the different EMI filter stages.

component tolerances (supported by the measured difference of EMI noise of $3.5\,\mathrm{dB}$ between phases) or neglected noise sources, such as the gate driver supply, which is operated at a switching frequency of $f \approx 350\,\mathrm{kHz}$.

Thus, although all the curves of the *Min/Max* estimates shown in Fig. 20 have been determined on the basis of calculated voltage waveforms, substantially different results are obtained depending on whether the fast or the exact calculation method is used. Therefore, it can be assumed that the total attenuation of the conducted EMI, i.e., from the noise source to the ac-LISN, does not reach the calculated values. Since the DM EMI noise components in the frequency range up to $400\,\mathrm{kHz}$ predominate the CM components in the noise calculations, it is appropriate to examine the achieved total DM attenuation of filter and converter in more details.

As shown in **Fig. 21(a,b)**, the measured TFs of the DM EMI propagation paths (solid blue curves) achieve a lower attenuation than the calculated TFs already at the second harmonic, at $210\,\mathrm{kHz}$ ($5\,\mathrm{dB}$ for $v_{\mathrm{dm},1}$ and $7\,\mathrm{dB}$ for $v_{\mathrm{dm},2}$). These discrepancies are also visible in Fig. 20(a,b) as a difference of $6\,\mathrm{dB}$ (only marked in Fig. 20(b)). However, if the TFs of the converter without filter and the filter itself are measured separately with a VNA and the resulting TFs are multiplied together, the dashed light blue curves in Fig. 21(a,b) result, which would reveal a substantially higher attenuation of up to $140\,\mathrm{dB}$ up to $1\,\mathrm{MHz}$. At the interface between converter and EMI filter, the converter has the three filter capacitances C_{f1} and the EMI filter has the three filter inductances $L_{\mathrm{dm},1}$. The measured impedance $Z_{C\mathrm{f1}}$ is more than a factor of 100 smaller than the measured impedance $Z_{L\mathrm{dm},1}$ in the frequency range considered. Consequently, issues related to the input and output impedances at the interface between the converter and the EMI filter can be practically excluded. However, the reduced attenuation can be explained by means of parasitic couplings between the components of the EMI filter and the converter, since all components are densely packed to achieve a high power density of the converter. For example, the cross-sectional drawing of the converter shown in **Fig. 22** (i.e., along the plane shown in Fig. 13(a)) indicates that there is only a small gap between the large converter filter capacitance C_{f1} and the EMI filter capacitance $C_{\mathrm{dm},2}$. This leads to an increase in a parasitic capacitance that can be considered to be in parallel with several filter components ($L_{\mathrm{dm},1}$, $C_{\mathrm{dm},1}$, $L_{\mathrm{dm},2}$, $L_{\mathrm{cm},1}$). Consequently, this is a possible reason for the reduced attenuation of the realized EMI filter.

VI. Conclusion

This paper considers the D3ABC topology as three-phase rectifier without and with galvanic isolation, where the three-phase ac lines are connected to the primary-side ac port and different loads are connected to the primary- and secondary-side dc ports. After a description of the general principle of operation of the investigated converter, models for calculating the conducted DM and CM EMI noise at the primary-side ac port, ac_1, are derived. These models prove valuable in several aspects:

1) They provide a detailed insight regarding the sources and the propagation paths of conducted EMI in the D3ABC. In this regard, the main finding is that the level of conducted EMI noise at port ac_1 increases for increasing power at port dc_2, P_2, and that the EMI noise is almost independent of the power at port dc_1, P_1.
2) They enable the systematic design and optimization of the EMI filter for given specifications at an early stage of the converter design. This has been explained in the context of an example, for given dc link voltages ($V_{\mathrm{dc},1} = 800\,\mathrm{V}$, $V_{\mathrm{dc},2} = 400\,\mathrm{V}$), $P_2 = 2.5\,\mathrm{kW}$, and the QP limit of conducted EMI defined by CISPR 11 class A. The designed EMI filter has a total volume of $0.17\,\mathrm{dm}^3 = 10.4\,\mathrm{in}^3$ ($0.09\,\mathrm{dm}^3 = 5.5\,\mathrm{in}^3$ for the DM filter and $0.08\,\mathrm{dm}^3 = 4.9\,\mathrm{in}^3$ for the CM filter part) achieving together with the main part of the converter

a volume of $1.94\,\mathrm{dm}^3$ resulting in a power density of $4.1\,\mathrm{kW/dm}^3 = 67.4\,\mathrm{kW/in}^3$.

3) They correctly predict the conducted EMI noise at the ac port in the frequency range close to $150\,\mathrm{kHz}$, where the largest magnitudes occur in the spectrum of the (unfiltered) EMI noise. Deviations at higher frequencies are due to parasitic effects (parasitic capacitances, inductances, and couplings between components) that are not accounted for in the simplified models.

A hardware prototype of the D3ABC topology, which includes the designed EMI filter, serves for the experimental verification of the derived models for conducted EMI noise. The measured frequency responses of the TFs from the EMI noise sources of the converter to the port ac_1 are in good agreement with the frequency responses predicted by the models up to a frequency of $200\,\mathrm{kHz}$. In this regard, the model correctly predicts the increase in conducted EMI noise as a result of an increase of the power at port dc_2 from $P_2 = 2.5\,\mathrm{kW}$ to $P_2 = 6.5\,\mathrm{kW}$ (with a simultaneous decrease of the power at port dc_1 from $P_1 = 4\,\mathrm{kW}$ to $P_1 = 0$). Finally, the measurements of conducted EMI noise show that the hardware prototype meets the QP limit defined by CISPR 11 class A for $P_1 = 4\,\mathrm{kW}$ and $P_2 = 2.5\,\mathrm{kW}$.

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