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D. Neumayr,
D. Bortis,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

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D. Neumayr, D. Bortis, and J. W. Kolar Power Electronic Systems Laboratory, ETH Zurich, Switzerland. Email: neumayr@lem.ee.ethz.ch

***Index Terms*—Single-Phase PV Inverter, Power Pulsation Buffer, Active Power Decoupling, Ripple Port Module, High Power Density, CeraLink Capacitor, Ceramic Capacitor, Google Little Box Challenge**

***Abstract*—In single-phase power conversion systems, typically bulky electrolytic capacitors are installed in order to cope with the intrinsic double-line frequency power pulsation. However, since the voltage ripple at the dc bus is typ. limited to just a few percent of the nominal voltage, only a small fraction of the actually stored energy in the capacitors is used for the power decoupling. In this paper an auxiliary buffer converter is employed, shifting the double-line frequency power pulsation away from dc bus to a buffer capacitor. Being relieved from strict voltage ripple requirements, a larger voltage ripple is allowed across the buffer capacitor, significantly reducing the capacitance requirement. In this paper an ultra compact Power Pulsation Buffer (PPB) is designed for a $2\,\mathrm{kW}$ PV-inverter application by means of a comprehensive Pareto optimization. Besides compensating the power pulsation, the PPB must be able to quickly stabilize the dc bus in case of abrupt load variations and maintain an average buffer capacitor voltage. In this paper, a novel cascaded control structure is presented, meeting all aforementioned control objectives. A constructed prototype of the optimized PPB is presented in the paper and experimental measurements verify the outstanding performance of the proposed control system.**

I. Introduction

In single-phase ac/dc and dc/ac power conversion systems, typically bulky electrolytic capacitor are installed in order to cope with the intrinsic double-line frequency power pulsation. Since the voltage ripple at the dc bus is typ. limited to just a few percents of the nominal voltage in practical applications, the conventionally installed capacitors are poorly utilized since just a small fraction $\Delta E = C \cdot V_{\mathrm{dc}} \cdot \Delta v$ of the average stored energy $\frac{1}{2} C V_{\mathrm{dc}}^2$ is actually used for the buffering process. In order to drastically increase the power density of a single-phase inverter ($2\,\mathrm{kW}$ inverter designed for the Google Little Box Challenge [1]–[3]), an auxiliary circuit can be installed in parallel to the dc input of the inverter. One possible realization of such an auxiliary circuit, relying solely on passive components, is to connect a resonance circuit in parallel to the dc bus as displayed in Fig. 1 (a), where L_r and C_r are forming a notch filter tuned to twice the line frequency. Besides the unreasonable large inductor values, the main disadvantage of this approach are the high voltage stress across the filter components and the comparably high losses occurring in the inductor. A more effective way to shift the ripple power away from the dc bus is to use an active auxiliary circuit with additional buffer capacitors. In order to compensate the ac ripple power, the employed buffer capacitor must alternately store and release $\Delta E = \frac{S_b}{\omega}$ within a quarter of the mains period, where S_b is the apparent power of the single-phase load. These Active Power Decoupling (APD) methods have been extensively studied in literature in recent years and a comprehensive overview is given in [4]–[6]. Several selected dc-side connected Power Pulsation Buffer (PPB) circuits are shown in Fig. 1 (b)-(e). A buck topology as shown in Fig. 1 (b) is analyzed in [7], where the minimum required buffer capacitance is derived to be

$$C_{b,\min} = \frac{2 S_b}{\omega V_{\mathrm{dc}}^2}. \tag{1}$$

Likewise a boost topology as shown in Fig. 1 (c) can be used as shown in [8]. In order to keep the overall engineering effort and system complexity reasonable, the PPB should advantageously employ the same power semiconductors as used in the inverter stage (in the case at hand $600\,\mathrm{V}$ IFX normally-off GaN GIT power devices [2]). Thus, due to the imposed design restrictions, the boost topology is excluded from further analysis in this paper. A symmetrical half-bridge circuit as shown in Fig. 1 (d) is analyzed in [6], where two identical film capacitors are connected in series and the midpoint is connected to another phase leg through a small filter inductor. This topology has the advantage, that the employed buffer capacitors are also directly buffering the high voltage dc bus while handling the power pulsation. The smallest possible value required for an individual capacitor is

$$C_{b,\min} = \frac{4 S_b}{\omega V_{\mathrm{dc}}^2} \tag{2}$$

as calculated in [6]. Thus, the symmetrical half-bridge approach requires in total four times more capacitance compared to the buck-type topology. A stacked capacitor approach as illustrated in Fig. 1 (e), where an auxiliary capacitor is connected in series with a buffer converter, is proposed in [9], [10]. The auxiliary capacitor C_k can show a larger ripple voltage, given that the buffer converter exactly compensates the fluctuation, yielding a ripple free dc bus. One advantage of this approach is that, since the auxiliary capacitor is blocking most of the dc bus voltage, the buffer converter only needs to process a fraction of the average buffer power $\Delta E \cdot 4\omega/2\pi = \frac{2}{\pi} S_{\mathrm{b}}$ which is flowing into and then out of the buffer in every cycle. However, the reduced power processing comes at the price of an increased energy storage requirement.

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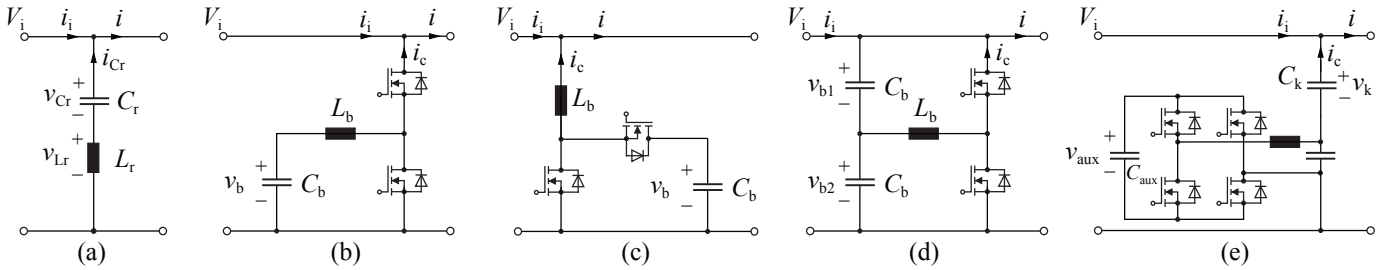

Fig. 1. Overview of common PPB topologies connected in parallel to the dc bus of a single-phase inverter or rectifier. (a) notch filter (b) buck (c) boost (d) flying capacitor (e) stacked capacitor approach.

The total maximal stored energy in both the buffer converter capacitor C_{aux} and the coupling capacitor C_k is 2.5 times larger than the theoretical minimum $\frac{S_b}{\omega}$ of the buck-type PPB topology [11]. Since the focus in this paper is primarily to achieve a high power-density of the PPB and/or to comply with the specifications of the Google Little Box Challenge [1] allowing an efficiency of $95\,\%$, the buck-type topology has been identified as most favorable because of the lowest buffer capacitance requirement. As mentioned before, applicable PPB topologies have been thoroughly studied in literature and an increase in power density compared to a passive capacitive dc bus buffering has been reported. However, a comprehensive design optimization aiming at highest possible power density of a PPB, has not been performed so far and therefore will be presented in Section II with special focus on the design and material selection of the buffer capacitor. Moreover, a comparison between a conventional dc bus capacitor approach and an optimally designed PPB is carried out, indicating at which voltage ripple requirement it becomes beneficial to implement a PPB.

Besides an optimal design of the PPB to achieve a high power density, a sophisticated control system is required in order to successfully compensate the fluctuating power. An APD control strategy applied to a single-phase PWM rectifier has been proposed in [5] using an ac side power decoupling circuit and in [7] using a buck-type decoupling circuit. In these rectifier applications, a dedicated feedback loop ensures a tightly regulated dc bus voltage and achieves good disturbance rejection. In conventional dc/ac converter systems, the dc bus voltage is typically well buffered and is therefore considered as a constant system input. However, as mentioned previously, systems employing a PPB allow a significant reduction in dc bus capacitance. As a consequence, in case of imperfect compensation of the fluctuating power and under abrupt load variations, the dc bus voltage might undergo large transients leading to significant output voltage distortion or even dielectric breakdown of the dc bus capacitor. Thus, employing a PPB in single-phase inverter applications, there is need to explicitly control the dc bus voltage. A control scheme which achieves good power decoupling and actively controls the dc bus voltage while maintaining a specified offset voltage across the buffer capacitor, is proposed in Section III of this paper. Subsequently, in Section IV, the constructed prototype will be presented and the performance of the proposed control concept will be assessed by means of experimental results.

II. $\eta\rho$-Pareto Optimal Design of a Buck-Type PPB

A. Mathematical Model of the Buck-Type PPB

Complying with the test setup specified in [1], the input of the inverter considered in the following is connected to a $V_S = 450\,\mathrm{V}$ power supply via a $R_S = 10\,\Omega$ resistor as shown in Fig. 2 (a). The selected buck-type PPB is connected in parallel to a small dc bus capacitor $C_{\mathrm{dc}} = 15\,\mu\mathrm{F}$ at the input of the dc/ac stage. In principle, the design of the PPB is independent of the implemented inverter topology, however the reactive power consumption of the installed EMI filter on the ac-side also has to be considered. The PPB is controlled to fully compensate the fluctuating power $p_{\mathrm{out,ac}}(t)$, resulting from the single-phase load and the EMI filter of the inverter stage. As a consequence, only a constant power P_0 must be provided by the power supply V_s and v_{dc} is relieved from the double-line frequency voltage ripple. Accordingly, the PPB must be dimensioned to cope with the apparent power

$$S_{\mathrm{b}} = \sqrt{P_{\mathrm{out}}^2 + (Q_{\mathrm{out}} + Q_{\mathrm{filt}})^2}, \tag{3}$$

wherein Q_{filt} is the reactive power of the EMI filter installed at the ac output of the inverter stage. The instantaneous power provided by the PPB (cf. Fig. 2 (a)) can be calculated according to

$$p_b = v_b \cdot i_b + v_{\mathrm{L,b}} \cdot i_b = v_b \cdot i_b + L_b \cdot \frac{\mathrm{d}}{\mathrm{d}t} i_b \cdot i_b \approx v_b \cdot i_b. \tag{4}$$

Neglecting the power contribution of the PPB inductor is reasonable, because when a mean buffer capacitor voltage of $V_b = 300\,\mathrm{V}$ and a reasonable inductor value of $20\,\mu\mathrm{H}$ is considered, then the peak power in the inductor only amounts to

$$\hat{p}_{\mathrm{L,b}} = \omega L_b \hat{i}_b^2 = \omega L_b \left(\frac{2\,\mathrm{kW}}{300\,\mathrm{V}}\right)^2 = 335\,\mathrm{mW}.$$

The fluctuating power is fully compensated if

$$v_b(t) \cdot i_b(t) = p_{\mathrm{out,ac}}(t) = S_{\mathrm{b}} \cos(2\omega t - \tilde{\phi}), \tag{5}$$

where $\tilde{\phi} = \arctan\left({}^{(Q_{\mathrm{out}}+Q_{\mathrm{filt}})}/_{P_{\mathrm{out}}}\right)$. Inserting the voltage/current relationship of the buffer capacitor yields the differential equation

$$v_b \cdot C_b \frac{\mathrm{d}v_b}{\mathrm{d}t} = S_{\mathrm{b}} \cos(2\omega t - \tilde{\phi}), \tag{6}$$

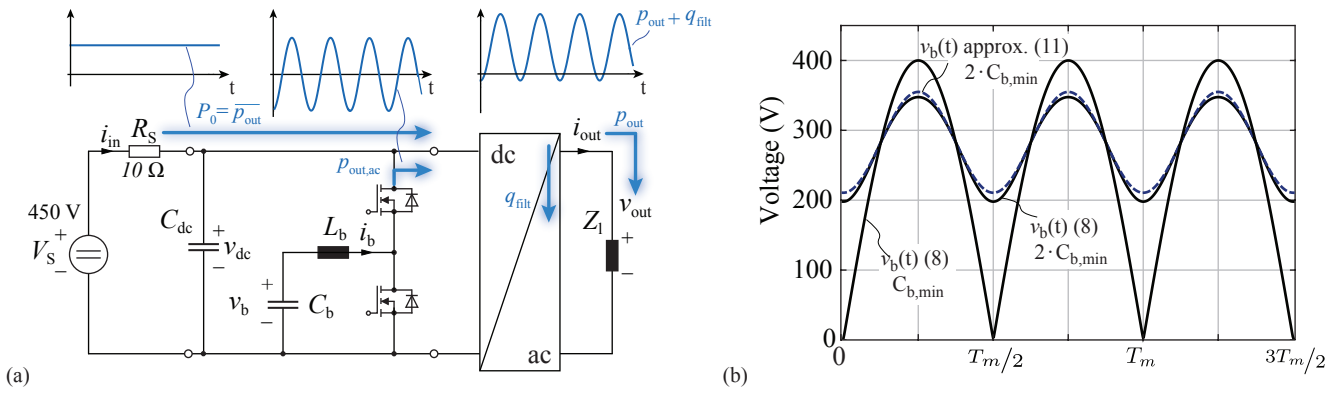

Fig. 2. (a) Buck-type PPB with input connection according to [1] and arbitrary single-phase inverter with load. Indicated is the constant power P_0 provided by the dc voltage source, the reactive power injected by the PPB and the fluctuating power of load and inverter stage EMI filter (b) Waveform of the buffer capacitor voltage for different buffer capacitance values.

with the analytical solution

$$v_b(t) = \sqrt{V_{\mathrm{b},0}^2 - \frac{S_\mathrm{b} \sin(2\omega t - \tilde{\phi})}{\omega C_b}}, \tag{7}$$

wherein $V_{\mathrm{b},0}$ is the buffer capacitor voltage at the start of the buffer cycle. Above expression is defined if

$$\omega C_b V_{\mathrm{b},0}^2 \geq S_\mathrm{b} \rightarrow C_b \geq \frac{S_\mathrm{b}}{\omega V_{\mathrm{b},0}^2}. \tag{8}$$

Setting $V_{\mathrm{b},0} = {}^{V_\mathrm{dc}}/\sqrt{2} = 282.84\,\mathrm{V}$, i.e. the voltage corresponding to half of the maximal stored energy ${}^1/_2 C_b V_\mathrm{dc}^2$, then the required minimal capacitance value given by equation (1),

$$C_{\mathrm{b,min}} = \frac{2S_b}{\omega V_\mathrm{dc}^2} = \frac{2 \cdot 2\,\mathrm{kW}}{2\pi 60\,\mathrm{Hz}(400\,\mathrm{V})^2} = 66.3\,\mu\mathrm{F}, \tag{9}$$

is obtained. Keep note that the voltage across the dc bus reduces from $V_S = 450\,\mathrm{V}$ to $400\,\mathrm{V}$ at rated power due to the specified $10\,\Omega$ dc input resistor.

In terms of transient response in case of abrupt load variations, at least $\approx 2 \cdot C_{\mathrm{b,min}}$ must be installed in a practical PPB implementation, as extensive circuit simulations revealed. Choosing $C_b >> C_{\mathrm{b,min}}$ allows to adjust the initial voltage $V_{\mathrm{b},0}$, which becomes a degree of freedom in the design of the buffer capacitor. A linear approximation of the square root function of (7) at $V_{\mathrm{b},0}$ yields

$$v_b(t) \approx V_{\mathrm{b},0} - \frac{1}{2} \frac{S_b \sin(2\omega t - \tilde{\phi})}{\omega C_b V_{\mathrm{b},0}}, \tag{10}$$

which is a good approximation of (7) if $C_b > 130\,\mu\mathrm{F}$ and $V_{\mathrm{b},0} > 225\,\mathrm{V}$ as shown in Fig. 2 (b). The resulting voltage ripple across the buffer capacitor is essentially a double-line frequency sinusoid with amplitude $\frac{1}{2}\frac{S_b}{\omega C_b V_{\mathrm{b},0}}$ superimposed to a dc bias $V_{\mathrm{b},0}$. The dimensioning and loss calculation of the buffer capacitor presented in this paper relies on this simplification as it will be explained in the next section.

B. Design Space of the Optimization

In [2] several key technologies and components have been identified to design an ultra compact dc/ac converter for the Google Little Box Challenge, which are adopted in this work to design and implement the PPB, comprised of a half-bridge, a high frequency (HF) inductor and the buffer capacitor. As mentioned in the introduction, in order to keep the overall engineering effort and system complexity at reasonable levels, both PPB and inverter employ the same WBG power semiconductor technology. In particular, new normally-off gallium nitride gate injection transistors (GaN-GiT) in combination with a novel high-performance gate drive circuit [12] are used. The bridge leg is operated with a triangular current mode (TCM) modulation scheme [13] in order to achieve zero voltage switching (ZVS) in all operating points. Due to reduced switching losses and accordingly reduced heat sink volume, a higher efficiency and power density is expected when TCM is applied. Moreover, a rather high switching frequency in the range of 200kHz-1MHz results in a significantly reduced volume of the inductor. However, outlined in [2], the required large HF current ripple leads to increased conduction losses which reduces the profit of soft-switching gained with the TCM. Therefore also conventional PWM modulation is considered for the bridge-leg, since the large turn-on switching losses associated with PWM can be reduced when a relatively high current ripple is allowed. In [14], advanced models for winding and core loss calculation and thermal models for HF inductor design are presented. Adopting these models to a large variety of available core geometries, N87 ferrite material and available HF-litz wires, an optimal inductor in terms of volume can be identified for a given inductance value and current waveform. Despite the reduced capacitance requirement, the buffer capacitor still comprises a large portion of the PPBs overall volume. Thus, the selected capacitor technology defines to a large extend the resulting power density and plays a critical role in the design of the PPB. Since much smaller capacitance values are needed compared to a conventional passive capacitive dc buffering, thin-film and ceramic capacitors become a viable option. The performance of class II ceramic capacitors with various temperature characteristics (X6S, X7R, ...), metalized polyester (PEN), metalized polypropylene (PP) and electrolytic capacitors subject to large voltage swing operation was comprehensively studied in [15],

revealing that $2.2\,\mu F$, $450\,V$ X6S class II ceramic capacitors from TDKs C575 series feature by far the highest energy density. Class II ceramics are characterized by a high relative permittivity and are therefore well suited for energy storage application. Adversely, the relative permittivity is not constant but strongly depends, among several other factors, on the applied dc bias voltage. With increasing dc bias voltage, the effective capacitance of class II ceramics drastically drops, decreasing capacitance density at operating voltage levels. Quite on the contrary, the capacitance of recently launched CeraLink capacitors (EPCOS/TDK) comprised of an antiferroelectric Pb-Lanthanum-Zirconimum-Titanate (PLZT) ceramic, is increasing with dc bias voltage offering the highest capacitance at dc bus voltage levels [16]. Identified as the two most promising ceramic capacitors for large voltage swing buffer applications, a comprehensive performance analysis of TDK's $2.2\,\mu F$, $450\,V$ class II X6S capacitor and EPCOS/TDK's $2\,\mu F$, $650\,V$ 2^{nd} generation CeraLink is provided in [17]. In particular, the experimentally determined capacitance and loss density with respect to applied dc bias and $120\,Hz$ sinusoidal voltage ripple is determined for several operating temperatures. Reconsidering the approximation of $v_b(t)$ in (10) and a particular value of C_b and $V_{b,0}$ from the design space listed in Tab. I, the operating point of the buffer capacitor can be calculated. Given the operating point and a ceramic material from the design space, the prevailing large-signal capacitance density is extracted from the data set provided in [17]. This allows to accurately calculate the number of single capacitor chips mounted in parallel to meet the requested value C_b in the given large-signal operating point, despite the non-linear behavior of the considered ceramic materials. Likewise, the power losses occurring in the capacitor assembly caused by continuously storing and releasing $\Delta E = \frac{S_b}{\omega} = 5.31\,J$ is extracted from the data in [17]. Additional losses due to the high frequency current ripple in i_b is negligible, since the ESR of the buffer capacitor assembly is vanishingly low at the considered switching frequencies. Moreover, voltage $V_{b,0}$ at the beginning of a buffer cycle, or the mean buffer voltage according to (10), can be adjusted by the employed control system as proposed in Section III and is considered a further degree of freedom in the design. Depending on the large-signal ripple and bias properties of the respective capacitor technology, different bias voltages might lead to the optimal design. However, in order to have enough energy margin to cope with load transients, the bias voltage must be kept within certain bounds. Specifically, given C_b then $V_{b,0}$ must be chosen such that

$$1/2 C_b \cdot V_{b,0}^2 \in [E_{0,\min}, E_{0,\max}]\,, \tag{11}$$

where the interval boundaries of the mean energy E_0 are given by

$$E_{0,\min} = E_m + \frac{\Delta E}{2}, \quad E_{0,\max} = E_{\max} - E_m - \frac{\Delta E}{2},$$

with the maximal energy $E_{\max} = 1/2 C_b V_{dc}^2$ and an empirically chosen energy margin $E_m = 25\,\%$ of $\Delta E = 1.4\,J$. The design space of the optimization is summarized in Tab. I.

TABLE I
SYSTEM PARAMETERS & SEARCH LOCUS OF THE PPB PARETO OPTIMIZATION

Feature	**Range/Option**
S_{out}	$2\,kW$
Q_{filt}	$250\,VAr$
V_S	$450\,V$
Capacitor Technology	$450\,V$ class II X6S (TDK-C5750X6S2W225M250KA)
	$650\,V$ 2^{nd} generation CeraLink
C_b	$[120\,\mu F,\ 350\,\mu F]$
$V_{b,0}$	$1/2 C_b \cdot V_{b,0}^2 \in [E_{0,\min}, E_{0,\max}]$
Inductor Technology	N87 ferrite, HF litz wire
L_b	$[10\,\mu H, 60\,\mu H]$
Modulation	TCM, f_s from $200\,kHz$ to $1\,MHz$
	PWM, $f_s = 140\,kHz$
Heat sink	$CSPI = 25.7\,\frac{kW}{K\,dm^3}$

C. Pareto Optimal PPB Designs

Given the aforementioned design space and elaborate loss and volume models of the utilized components, the performance of several buck-type PPB configurations was calculated. Fig. 3 (a) displays the performance of the calculated designs in the $\eta\rho$-performance space. In particular, PPB designs with class II and CeraLink capacitors, both either with TCM or conventional PWM modulation, are distinguished by color. Moreover, the performance of PPB designs with TCM, CeraLink buffer capacitor and fixed voltage $V_{b,0} = 300\,V$ is also discernible in the figure. As reference, the $\eta\rho$-performance of a conventional dc bus assembly, which will be introduced in subsection II-D, is also shown. Clearly noticeable, designs with class II X6S ceramic outperform those with CeraLink capacitors. The highest power density of $41.3\,\frac{kW}{dm^3}$ ($677.1\,W/in^3$) and an efficiency of $99.4\,\%$ (P2) is achieved with TCM modulation, $C_b = 110\,\mu F$ with X6S capacitors, and $L_b = 30\,\mu H$. As presented in the large-signal capacitor analysis in [17], the CeraLink capacitors exhibits much higher $120\,Hz$ losses than TDK's C575 series X6S. In particular, considering a specific buffer capacitor operating point for comparison, $V_{b,0} = 300\,V$ and $130\,V_{pp}$ voltage ripple, then the X6S exhibits a loss density of $38\,\frac{mW}{cm^3}$ as opposed to $1.42\,\frac{W}{cm^3}$ of the CeraLink, while the capacity density of both ceramic material is quite similar (X6S $7.8\,\frac{\mu F}{cm^3}$, CeraLink $8.4\,\frac{\mu F}{cm^3}$) [17]. This explains the drop in efficiency of the PPB designs with CeraLink capacitors as shown in Fig. 3 (a), and the reduction in power density due to the higher cooling effort. As a consequence, power density optimal designs with X6S (P2),(P3) feature a low total buffer capacitance around $110\,\mu F$, accordingly a large $120\,Hz$ voltage ripple around $180\,V_{pp}$ amplitude, and a mean voltage $V_{b,0}$ around $300\,V$. On the other hand, optimal designs employing the CeraLink capacitor, feature comparably high total capacitance values around $200\,\mu F$ and a consequently low voltage ripple with around $80\,V_{pp}$ amplitude in order to to keep the losses small. Moreover, since the capacity density of the CeraLink capacitors increases with applied bias, optimal results (P4), (P5) exhibit increased bias voltages $V_{b,0} \approx 330\,V - 340\,V$. Also

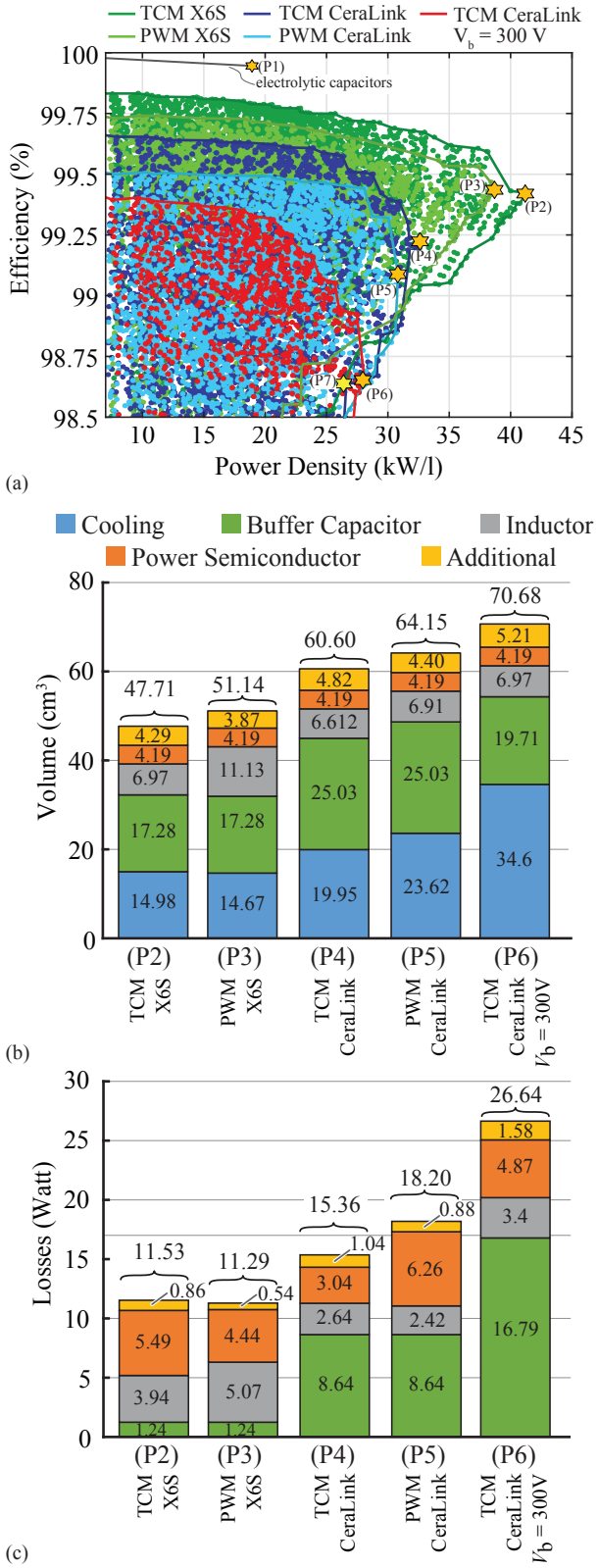

Fig. 3. Results of the buck-type PPB design optimization. (a) $\eta\rho$-plot of the calculated designs with indicated pareto fronts. (b) Volume distribution of the optimal designs (P2)-(P6) (c) Loss distribution of the optimal designs (P2)-(P6).

noticeable in the $\eta\rho$-space, designs using TCM modulation feature higher efficiency compared to PWM modulation with $f_s = 140\,\mathrm{kHz}$. Designs (P2)-(P5) feature remarkable high power density, and by looking at the $\eta\rho$-plot it is very tempting to realize design (P2). Although, these designs work very well in a steady-state operation point they might not handle transients so well since due to the high voltage ripple or the high bias voltage, only a small voltage margin to the maximal voltage V_{dc} is present. This voltage margin, in case of design (P2) roughly $50\,\mathrm{V}$, is needed to cope with abrupt inverter load drops which are most critical when they occur at rated power due to low dc bus voltage $V_{\mathrm{dc}} = 400\,\mathrm{V}$. Accordingly, in order to ensure good transient performance of the PPB right from the design, a more pragmatic optimization with $V_{\mathrm{b},0} = 300\,\mathrm{V}$ was carried out also shown in Fig. 3 (a). The volume of the PPB is dominated by the buffer capacitor as shown in Fig. 3 (b). Also the volume required for cooling is significant, especially in the case of design (P6). As stated earlier, optimal designs using CeraLink feature a higher total buffer capacitance, consequently occupying more volume. The loss distribution of the optimal designs is given in Fig. 3 (c), revealing the almost negligible losses occurring in the X6S designs (P2),(P3), and the allmost 7 times higher losses in the CeraLink designs (P4),(P5). Astounding are the dominating losses in the CeraLink capacitor of the pragmatic design (P6), which drastically reduces efficiency and substantially increases the heat sink volume. Clearly, the buffer capacitor operating point occurring at steady-state in design (P6) is not optimal given the performance of the CeraLink. The category *additional* shown in Fig. 3 (b) & (c) includes the volume and loss data of the current zero-crossing detector (required for TCM operation), analog measurement circuits, metal enclosure of the PPB, and the power consumption of the heat sink fans, respectively. Given the gained insights from the $\eta\rho$-space of the calculated designs, it is clearly advisable to realize a PPB using class II X6S capacitors. However, practical manufacturing considerations have to be included in the decision making. In order to realize $110\,\mu\mathrm{F}$ roughly 150 single X6S chips must be mounted in parallel (Note the reduction of capacitance of a individual chip due to the applied dc bias). With the known issue of ceramic cracking due to mechanical and thermal stress, this certainly requires advanced packaging techniques in order to achieve a reliable assembly. On the other hand, the CeraLink capacitor is available in a package with 20 chips mounted in parallel by means of a silver sintered connection onto a common lead-frame which is able to absorb mechanical stress. Due to the easier and more reliable assembly of the buffer capacitor, it was decided to realize the $28\,\frac{\mathrm{kW}}{\mathrm{dm}^3}$ ($458.8\,\mathrm{W/in}^3$) design (P6) in hardware, with $C_b = 150\,\mu\mathrm{F}$ comprised of individual $2\,\mu\mathrm{F}$ CeraLink capacitors despite the higher losses, and the pragmatic bias voltage $V_{\mathrm{b},0} = 300\,\mathrm{V}$. The actually achieved $26.12\,\frac{\mathrm{kW}}{\mathrm{dm}^3}$ ($428\,\mathrm{W/in}^3$) power density and $98.65\,\%$ efficiency of the implemented prototype, discussed in Section IV, is indicated with (P7) in Fig. 3 (a).

D. Electrolytic capacitors versus optimal PPB

From the results of the PPB optimization, a very good estimate of the achievable volume and efficiency of the PPB

is available. This allows to compare the PPB with a conventional, passive dc bus comprised of electrolytic capacitors and to determine the voltage ripple requirement $\frac{\Delta V}{V}$ when it actually becomes beneficial in terms of volume to employ a PPB concept and accept the increased hardware effort of the converter system. Considering a conventional dc bus, then for a particular voltage ripple threshold $\Delta V = \epsilon V_{\mathrm{dc}}$ the minimal required capacitance value is given by

$$C_{\mathrm{dc}} = \frac{2 \cdot \Delta E}{V_{\mathrm{dc,max}}^2 - V_{\mathrm{dc,min}}^2} = \frac{S_b}{\omega \epsilon V_{\mathrm{dc}}^2}, \tag{12}$$

where the average dc bus voltage

$$V_{\mathrm{dc}} = \frac{V_s}{2} + \frac{\sqrt{V_s^2 - 4R_s P_0}}{2} \tag{13}$$

depends on the real power $P_0 = S_b \cdot \cos(\tilde{\phi})$ (cf. Fig. 2). A volume model was extracted by means of a least-square fit to the calculated boxed volumes of all possible dc bus assemblies generated with the ultra compact $450\,\mathrm{V}$ electrolytic capacitors listed in [18], allowing at the most five capacitors to be connected in parallel. The resulting volume of the dc bus with respect to the voltage ripple threshold is depicted in Fig. 4. Decreasing ΔV results in a larger volume since more

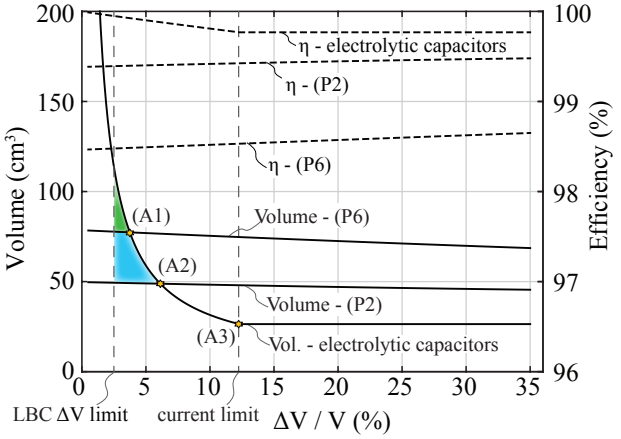

Fig. 4. Volume and efficiency comparison between conventional dc bus with electrolytic capacitors and optimally designed PPB with respect to ΔV threshold.

electrolytic capacitors have to be installed to meet the more stringent requirement. Likewise, relaxing the voltage ripple requirement results in a volume reduction until the specified ripple current limitation of the electrolytic capacitor prevents a further reduction in volume (A3). Given the calculated ESR for each capacitor assembly obtained from the data provided in [18], the power losses caused by the double-line frequency charging current,

$$I_{\mathrm{Cdc,rms}} = \frac{\omega C_{\mathrm{dc}} \Delta V}{\sqrt{2}} = \frac{S_b}{\sqrt{2} \cdot V_{\mathrm{dc}}}, \tag{14}$$

is calculated and the resulting efficiency is depicted in Fig. 4. The Pareto optimal design (P2) with TCM and class II X6S capacitors and the implemented design (P6) with TCM and CeraLink capacitors were chosen for the volume benchmarks. Typically, the control system as proposed in Section III achieves complete ripple cancellation, but it can be modified to tolerate a certain ΔV across C_{dc}, which changes the rated power of the PPB design according to $\tilde{S}_b = S_b - \Delta E_{\mathrm{dc}} \omega$. The performance of the designs (P2) and (P6) were recalculated for several voltage ripple thresholds. As indicated by intersection (A2) between the total volume of design (P2) and the electrolytic capacitor, it becomes beneficial (only considering volume) to employ a PPB if a $^{\Delta V}/_{V} = 6.04\,\%$ or less is demanded. For the actually implemented design (P6) with CeraLink the intersection (A1) occurs at $^{\Delta V}/_{V} = 3.7\,\%$. Also indicated in the plot is the voltage ripple threshold of $3\,\%$ specified in [1], which reveals that roughly $35\,\mathrm{cm}^3$ of volume were saved by means of the PPB. Concerning efficiency, Fig. 4 shows that passive capacitive dc buffering with electrolytic capacitors always achieves a higher efficiency compared to an optimal designed PPB (P2) regardless of voltage ripple requirement.

III. Cascaded Control of the PPB

The main objective of the proposed PPB control system shown in Fig. 5 [19] is to exactly compensate the pulsating power caused by the single-phase ac load and the EMI filter of the inverter stage, such that only a constant power P_0 is drawn from the dc source. Control subsystem (a) - *Active Power Decoupling* - computes the PPB current reference to compensate the fluctuating power. First, $p_{out,ac}$ is calculated by means of subtracting the average power $\overline{p_{\mathrm{out}}} = P_0$ from the instantaneous load power $p_{\mathrm{out}} = v_{\mathrm{out}} \cdot i_{\mathrm{out}}$, with measured output voltage v_{out} and current i_{out} of the inverter. The reactive power of the EMI filter is considered by means of filter capacitor C_f, where the instantaneous power of the filter is given by

$$p_{\mathrm{out,Q}} = v_{\mathrm{C,f}} \cdot i_{\mathrm{C,f}} = v_{\mathrm{out}} \cdot C_f \cdot \frac{\mathrm{d}}{\mathrm{d}t} v_{\mathrm{out}}. \tag{15}$$

In order to achieve a compensation of the fluctuating power at the dc bus, the instantaneous power $v_b \cdot i_b$ (cf. (4)) provided by the PPB must equal the sum $P_{\mathrm{C,ff}} = p_{out,ac} + p_{\mathrm{out,Q}}$. Dividing power $P_{\mathrm{C,ff}}$ by the prevailing buffer capacitor voltage v_b yields the compensation current reference $i^*_{C,\mathrm{ff}}$ which is used as a feed-forward term as shown in Fig. 5 (a). Besides neglecting the power contribution of L_b, inaccuracies and delays in the signal acquisition and computation of the controller, fluctuating power $P_{\mathrm{C,ff}}$ cannot be completely compensated by means of the feed-forward control. In order to eliminate any possible remaining voltage ripple at the dc bus, additional resonant compensators [20]

$$C_{\mathrm{R},m}(s) = \frac{2K_{i,m}s}{s^2 + (m \cdot \omega)^2} \tag{16}$$

are employed, wherein parameter $m \in 2, 4, 6$ sets the resonant frequency of the compensator to the first three even multiples of the mains frequency. As long as there is a spectral component with frequency $m \cdot \omega$ in the error signal $e_m = 0 - v_{\mathrm{dc}}$ seen by the respective resonant compensator, the amplitude of the sinusoidal controller output will increase, requesting more current of that particular frequency to be injected at the dc bus. If the feed-forward current $i^*_{C,\mathrm{ff}}$ cannot be computed due to

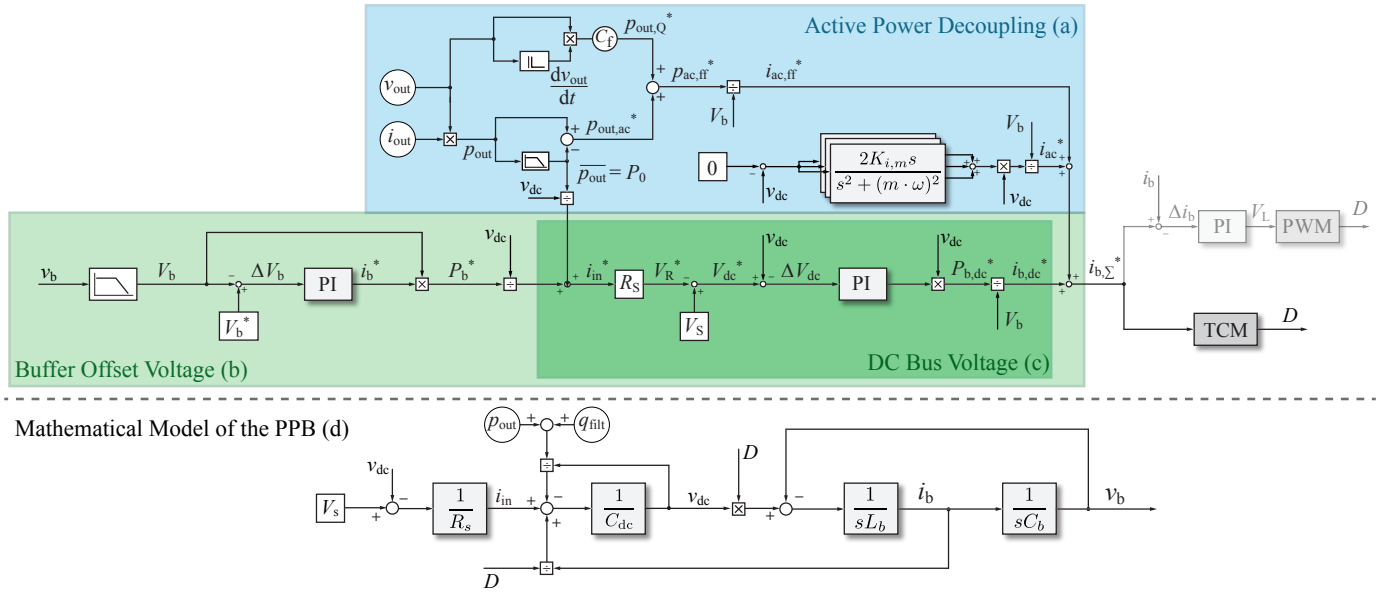

Fig. 5. Proposed cascaded control structure of the buck-type PPB employed in an inverter application. (a) Compensation of the pulsating power by means of feed-forward control and resonant compensators. (b) Control of the average buffer capacitor voltage. (c) Control of the dc bus voltage. (d) Mathematical model of the buck-type PPB.

lack of measurements in an existing application, the resonant compensators still achieve a good cancellation of double-line frequency voltage ripple at steady-state, but without feed-forward control the transient behavior will be deteriorated. Control subsystem (b) - *Buffer Offset Voltage* - is employed to keep the mean value of the buffer capacitor voltage $\overline{v_b} = V_b$ at a chosen reference. If only control aspects are considered, then the reference voltage of the buffer capacitor V_b^* is set to voltage level

$$V_{b,\mathrm{mid}} = {}^{V_{dc}}/_{\sqrt{2}} = 282.8\,\mathrm{V} \tag{17}$$

corresponding to half of the maximal stored energy. Maintaining the bias of the buffer capacitor at $V_{b,\mathrm{mid}}$ results in symmetrical energy margins, and load step-up and step-down can be handled equally well. However, as outlined in Section II, the dc bias of the buffer capacitor strongly affects the $\eta\rho$-performance results since (i) the prevailing capacitance density of the considered ceramic capacitors is strongly dependent on the dc bias and (ii) the amplitude of current i_b is inversely proportional to v_b. Therefore, a compromise between transient handling capability and $\eta\rho$-performance must be made. In case of the realized PPB presented in Section IV, the reference voltage V_b^* is set to 300 V. As a result of the current needed for the ac power decoupling, the buffer capacitor voltage features a distinctive double-line frequency voltage ripple. In order to extract the mean buffer voltage V_b, a low-pass filter, specifically a moving-average filter with window size of one 120 Hz period, is employed. A Proportional Integral (PI) compensator is used to compute current i_n^* needed to charge or discharge the buffer capacitor to meet the reference value as it is shown in Fig. 5 (b).

The inner loop of the cascaded control structure depicted in Fig. 5 (c) is required to tightly regulate the average dc bus voltage under all load conditions. The input current reference of the converter is given by

$$i_\mathrm{in}^* = i_b^* \frac{V_b}{v_\mathrm{dc}} + \frac{P_0}{v_\mathrm{dc}}, \tag{18}$$

which includes the current needed to adjust the buffer capacitor bias, and the current needed to provided real power P_0 to the load. Current i_b^* computed by the outer PI-controller, is referred to dc bus voltage levels by means of the scaling factor $\frac{V_b}{v_\mathrm{dc}}$. Since it is assumed that there is no 120 Hz ripple present in the dc bus voltage, low-pass filtering of v_dc is not necessary which increases the phase-margin of the cascaded control loop. Given the converter input current, the dc bus voltage reference is calculated with the equation

$$V_\mathrm{dc}^* = V_S - R_S \cdot i_\mathrm{in} \tag{19}$$

$$= V_S - R_S \cdot \left(i_b^* \cdot \frac{V_b}{v_\mathrm{dc}} + \frac{P_0}{v_\mathrm{dc}} \right). \tag{20}$$

It should be noted, that instead of computing V_dc^* under the assumption of a constant input resistance R_S, an additional PI-compensator can be used to regulate the converter input current as depicted in Fig. 6. The output of the PI-compensator is the required voltage across impedance Z_i and is subtracted from source voltage V_S to obtain V_dc^*. Despite the fact that an

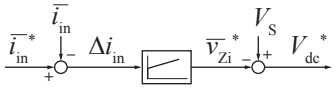

Fig. 6. Calculating V_dc^* by means of additional input current controller.

additional current measurement is required, using a dedicated control loop for the input current is particularly useful when the impedance between source and converter is not known. The inner-loop PI-compensator then controls v_dc to meet the

reference V_{dc}^{*}. Referring the output of the PI-compensator to the buffer capacitor voltage level by means of scaling with v_{dc}/V_b yields the mean buffer current reference $i_{\mathrm{b,dc}}^{*}$, required to keep both V_b and v_{dc} at the desired average values. Due to the cascaded structure, controlling the dc bus voltage has always priority over the mean buffer capacitor voltage. This has significant advantages in case of abrupt load changes, since the average buffer capacitor voltage V_{b} can be temporarily deflected from the reference V_b^{*}, keeping v_{DC} tightly controlled. Assuming a strict unidirectional power flow from the dc supply (no current sinking capability), then, in case of an stepwise load drop from for instance $1\,\mathrm{kW}$ to $0\,\mathrm{kW}$, the energy stored in the converter system at the very moment of load change, namely the energy stored in the passive components of the inverter stage and the PPB inductor, is absorbed in the larger buffer capacitor and not in the at least factor of 10 smaller dc bus capacitance. This prevents overshoots or sags in v_{DC}, even under harsh load transients.

Eventually, the individual current references $i_{\mathrm{C,ff}}^{*}$, i_C and $i_{\mathrm{b,dc}}$ are then summed to obtain $i_{\mathrm{B},\Sigma}^{*}$, is then forwarded to a Triangular Current Mode (TCM) modulator, which calculates the turn-on and turn-off times of the power transistors such that, on average over one switching cycle, the current in the buck inductor meets $i_{\mathrm{B},\Sigma}^{*}$. Alternatively, an additional feedback loop in combination with Pulse Width Modulation (PWM) can be applied to control the inductor current as shown on the right in Fig. 5. A satisfying initial set of control parameters for the PI and Resonant compensators has been empirically determined by means of extensive simulations. During testing of the converter prototype (see Section IV), the control parameters listed in Tab. II were fine tuned.

TABLE II
EMPIRICALLY DETERMINED CONTROL PARAMETERS

Controller	Parameter	Value
Resonator 120 Hz	$K_{\mathrm{i},2}$	7.5
Resonator 240 Hz	$K_{\mathrm{i},4}$	2.5
Resonator 360 Hz	$K_{\mathrm{i},6}$	1.25
Inner PI compensator - v_{dc}	K_p	0.1
	K_i	3.0
Outer PI compensator - v_b	K_p	0.0185
	K_i	0.055

IV. HARDWARE REALIZATION AND EXPERIMENTAL VERIFICATION

Benefiting from the gained insights of the design optimization in Section II, a prototype of the buck-type PPB as shown in Fig. 7 (a) was designed and constructed. The design parameters and selected features of the realized system are summarized in Tab. III. The PPB is equipped with a large-signal equivalent capacitance of $150\,\mu\mathrm{F}$, composed of 108 individual $2\,\mu\mathrm{F}$ /650 V CeraLink capacitors. By the courtesy of EPCOS/TDK, a custom package with 18 capacitor chips mounted together on silver coated copper lead frames was available. The efficiency of the constructed PPB at $2\,\mathrm{kW}$ rated power is $98.65\,\%$ as depicted in Fig. 7 (a) which amounts to $27\,\mathrm{W}$ of losses. In order to extract the power losses, an optimized forced-air cooling heat sink with a CSPI of $25.7\,\frac{\mathrm{kW}}{\mathrm{dm^3\,K}}$ was utilized. The total volume of the realized PPB including the cooler amounts to $76.55\,\mathrm{cm}^3$ which corresponds to a power density of $26.12\,\frac{\mathrm{kW}}{\mathrm{dm}^3}$ ($428\,\mathrm{W/in}^3$). Combined with a $2\,\mathrm{kW}$ high power density inverter stage designed for the Google Little Box Challenge [2], the constructed PPB was experimentally tested in the laboratory. The novel control system presented in Section III was implemented on a *TMS320F28335* from Texas Instruments Delfino series, located on a designated control PCB of the inverter stage. Besides the Digital Signal Controller (DSC), the control board contains a Lattice XP2 FPGA, dedicated to implement the TCM modulator with zero-crossing detection, and analog circuitry to measure the dc bus voltage and the output voltage and current of the inverter stage, required to implement the proposed PPB control system. Since the occupied volume and power consumption of the control related electronics is entirely contributed to the inverter stage, it is omitted from the PPB loss and volume balance (cf. Fig. 3 (c) & (d)), except for the buffer capacitor voltage measurement which was taken into account.

The steady-state performance at $2\,\mathrm{kW}$ rated power of the implemented PPB controller is illustrated by the scope measurements shown in Fig. 8. It can be seen from the recorded dc bus voltage and the converter input current (cf. i_{in} in Fig. 2), that the power pulsation was successfully shifted from the dc bus to the buffer capacitor which features a distinctive $100\,\mathrm{V_{pp}}$, $120\,\mathrm{Hz}$ voltage ripple. The inductor current waveform is a result of the employed TCM modulation, clearly showing the envelope of the double-line frequency charging currents. In order to verify the dynamic performance of the implemented control system, the inverter was subject to load variations. The transient performance of the PPB subject to a load step from $0\,\mathrm{W}$ to $700\,\mathrm{W}$ is depicted in Fig. 9. Triggered by the load step, the average buffer capacitor voltage drops $50\,\mathrm{V}$ below the $300\,\mathrm{V}$ at steady-state. Simultaneously, the PPB controller starts to compensate the power pulsation by means of injecting an appropriate current in the dc bus. As a consequence, a distinct $120\,\mathrm{Hz}$ voltage ripple develops at the buffer capacitor immediately after the load step. After a transient time of $60\,\mathrm{ms}$, the average buffer capacitor voltage has recovered and the intrinsic single-phase power pulsation is completely compensated by the PPB. During the transient, a small ripple is visible in the dc bus voltage. Take note that because of the $10\,\Omega$ input resistor (cf. Fig. 2), the average dc bus voltage decreases with increasing power and therefore settles at a lower value after the transient. The reactive power drawn by the EMI filter of the inverter stage is compensated by the PPB, thus a small ripple is present in the buffer capacitor voltage prior to the load step although no load is connected to the inverter. Analogously, a step down from $700\,\mathrm{W}$ to $0\,\mathrm{W}$ is depicted in Fig. 10. Prior to the load step at $t = 11\,\mathrm{ms}$, the converter system was operating in steady-state exhibiting a $50\,\mathrm{V}$ peak-to-peak voltage ripple in the buffer capacitor. Triggered by the load drop, the average buffer capacitor voltage temporarily increases up to $350\,\mathrm{V}$ and settles after approximately $60\,\mathrm{ms}$ to the reference value. The dc bus voltage remains tightly controlled during the entire transient,

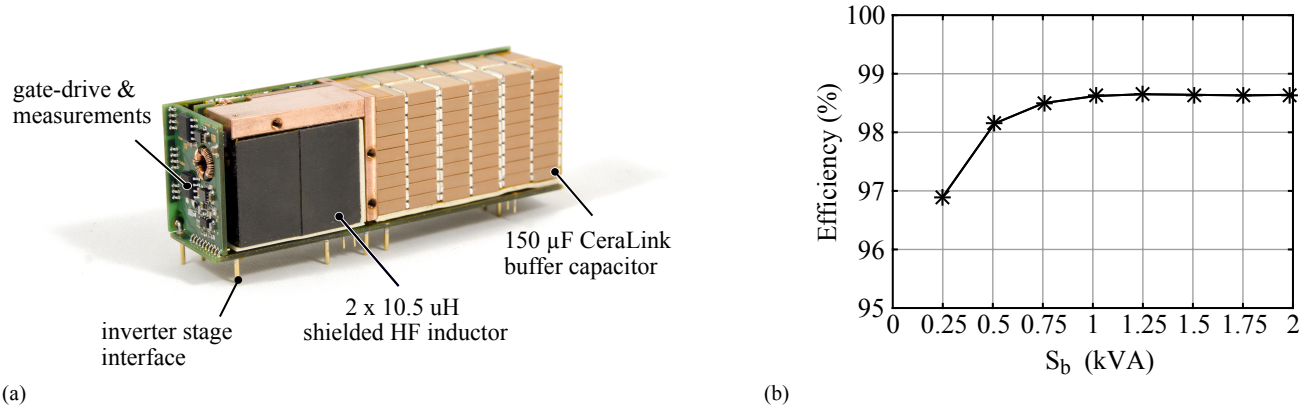

Fig. 7. (a) Hardware implementation of the 2 kW PPB designed for the Google Little Box Challenge (cf. design P6 in Fig. 3 (a)). The dimension of the shown PPB prototype is 86 mm × 27.5 mm × 20 mm (3.4 in × 10.8 in × 0.8 in). The heat sink is not shown in the picture. (b) Efficiency of the constructed prototype with respect to apparent power S_b.

TABLE III
REALIZED 2 kW BUCK-TYPE PPB SPECIFICATIONS

Feature	Value	Description
Volume (no cooling)	47.3 cm^3 (2.9 in^3)	Boxed volume of the constructed PPB without cooler
Volume (with cooling)	76.6 cm^3 (4.7 in^3)	Total boxed volume of PPB with a CSPI = 25.7 $\frac{\mathrm{kW}}{\mathrm{K\,dm}^3}$ heat sink
Capacitor volume	24.6 cm^3 (1.5 in^3)	Tot. volume of installed buffer capacitor
η	98.65 %	Efficiency at 2 kW
L_b	21 µH	2 times 10.5 µH in series
C_b	150 µF	Equivalent large signal capacitance of installed CeraLink capacitor

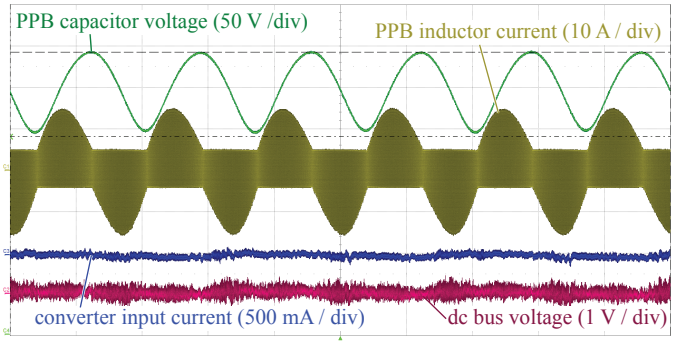

Fig. 8. Steady-state performance of the realized PPB at 2 kW rated power. The timebase of the measurement is 5 ms/div. Probes for measuring the converter input current and the dc bus voltage are ac coupled in order to highlight the excellent ripple cancellation.

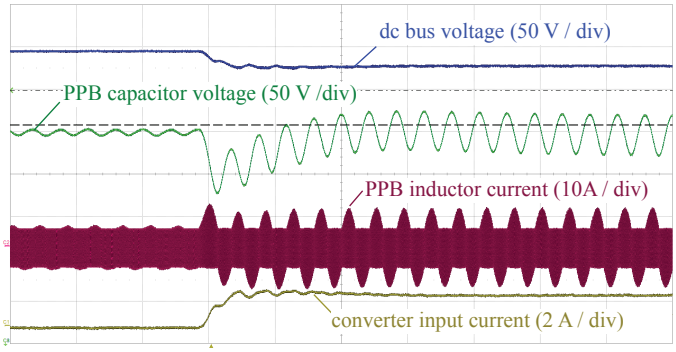

Fig. 9. PPB transient response to an abrupt load step from 0 W to 700 W. The timebase of the measurement is 20 ms/div.

showing virtually no overshoot but a small voltage ripple of $\Delta V \approx 5\,\mathrm{V}$ during the transient.

This surpasses the required performance of the application in [1], where load steps of maximal 500 VA had to be handled within 1 s. Due to the 10 Ω resistor of the application, the dc bus voltage settles at a higher value after the transient.

V. CONCLUSION

In order to increase the power density and shrink the overall volume of an existing single-phase inverter design, bulky electrolytic capacitor were replaced by means of an active PPB. Having the lowest requirement on the buffer capacitor size, the buck-type buffer topology was chosen as the most promising. A Pareto optimization of the PPB was carried in order to find the design with the highest possible power density, focusing on the dimensioning and loss calculation of the buffer capacitor. The optimal PPB design was then compared to a conventional electrolytic capacitor dc bus assembly, to identify at which voltage ripple requirement it starts to become beneficial to use a PPB. In Section III a novel cascaded control structure for a PPB was presented, achieving tight control of the dc bus voltage while maintaining an average buffer capacitor voltage, and power decoupling between dc and ac side. A realized prototype of the buck-type PPB achieving an overall volume of 76.6 cm^3 (4.7 in^3) and a peak efficiency of 98.7 % at rated

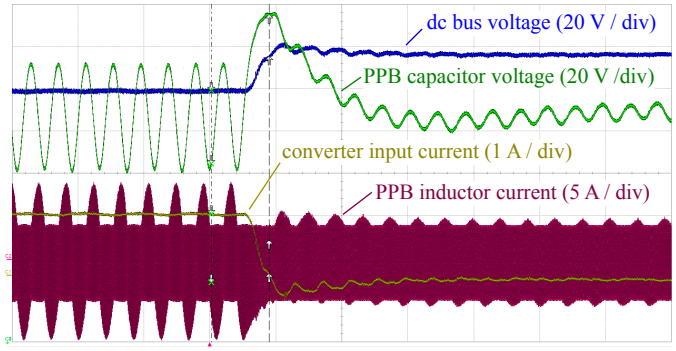

Fig. 10. PPB transient response to an abrupt load drop from 700 W to 0 W. The timebase of the measurement is 20 ms/div.

power, was presented in Section IV. The realized PPB was tested in combination with a 2 kW inverter stage designed for the Google Little Box Challenge. The performance of the PPB including the proposed control system, subject to stepwise load changes, was demonstrated by means of experimental waveforms.

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References

[1] Goolge, "Detailed inverter specifications, testing procedure, and technical approach and testing application requirements for the Little Box Challenge," Google, Tech. Rep., 2015. [Online]. Available: https://www.littleboxchallenge.com

[2] D. Bortis, D. Neumayr, and J. W. Kolar, "$\eta\rho$ -Pareto optimization and comparative evaluation of inverter concepts considered for the Google Little Box Challenge," in *Proc. of 17th IEEE workshop on Control Model. Power Electron. (COMPEL) [Submitted for Publication]*, 2016.

[3] J. W. Kolar, D. Bortis, D. Neumayr, and M. Kasper, "Little Box Challenge," in *Keynote Presentation at the 9th IEEE International Conference on Integrated Power Electronics Systems (CIPS)*, 2016.

[4] Z. Qin, Y. Tang, P. C. Loh, and F. Blaabjerg, "Benchmark of AC and DC active power decoupling circuits for second-order harmonic mitigation in kW-scale single-phase inverters," in *Proc. of IEEE Energy Convers. Congr. Expo. (ECCE)*, 2015, pp. 2514–2521.

[5] L. Hongbo, Z. Kai, Z. Hui, F. Shengfang, and X. Jian, "Active power decoupling for high-power single-phase PWM rectifiers," *IEEE Trans. on Power Electronics*, vol. 28, no. 3, pp. 1308–1319, 2013.

[6] T. Yi, F. Blaabjerg, L. Poh Chiang, J. Chi, and W. Peng, "Decoupling of fluctuating power in single-phase systems through a symmetrical half-bridge circuit," *IEEE Trans. on Power Electronics*, vol. 30, no. 4, pp. 1855–1865, 2015.

[7] W. Ruxi, F. Wang, D. Boroyevich, R. Burgos, L. Rixin, N. Puqi, and K. Rajashekara, "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. on Power Electronics*, vol. 26, no. 5, pp. 1430–1443, 2011.

[8] A. C. Kyritsis, N. P. Papanikolaou, and E. C. Tatakis, "A novel parallel active filter for current pulsation smoothing on single stage grid-connected AC-PV modules," in *Proc. of Eur. Conf. on Power Electron. Appl.*, 2007, pp. 1–10.

[9] Q. Shibin, L. Yutian, C. Barth, L. Wen-Chuen, and R. C. N. Pilawa-Podgurski, "Architecture and control of a high energy density buffer for power pulsation decoupling in grid-interfaced applications," in *Proc. of 16th IEEE workshop on Control Model. Power Electron. (COMPEL)*, 2015, pp. 1–8.

[10] S. Qin, Y. Lei, C. Barth, W.-C. Liu, and R. C. N. Pilawa-Podgurski, "A high-efficiency high energy density buffer architecture for power pulsation decoupling in grid-interfaced converters," in *Proc. of IEEE Energy Convers. Congr. Expo. (ECCE)*, 2015, pp. 149–157.

[11] J. W. Kolar, "Approaches to overcome the Google/IEEE Little-Box Challenges," in *Keynote Presentation at the 37th IEEE International Telecommunications Energy Conference (INTELEC)*, 2015.

[12] D. Bortis, D. Neumayr, O. Knecht, and J. W. Kolar, "Comprehensive Evaluation of GaN GIT in Low- and High-Frequency Bridge Leg Applications," in *Proc. of IEEE Energy Convers. Congr. Expo. (ECCE Asia) [Accepted for Publication]*, 2016.

[13] C. Marxgut, J. Biela, and J. W. Kolar, "Interleaved Triangular Current Mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," 2010, pp. 1725–1732.

[14] R. M. Burkart, H. Uemura, and J. W. Kolar, "Optimal inductor design for 3-phase voltage-source PWM converters considering different magnetic materials and a wide switching frequency range," in *Proc. of Int. Power Electron. Conf. (ECCE ASIA, IPEC)*, 2014, pp. 891–898.

[15] C. B. Barth, I. Moon, Y. Lei, S. Qin, and R. C. N. Pilawa-Podgurski, "Experimental evaluation of capacitors for power buffering in single-phase power converters," in *Proc. of IEEE Energy Convers. Congr. Expo. (ECCE)*, 2015, pp. 6269–6276.

[16] G. F. Engel, "Design and materials of antiferroelectric capacitors for high density power electronic applications," in *Proc. of 9th Intern. Conf. on Integr. Power Electron. Syst. (CIPS)*, 2016, pp. 3–9.

[17] D. Neumayr, D. Bortis, J. W. Kolar, and J. Konrad, "Comprehensive large-signal performance analysis of ceramic capacitors for power pulsation buffers," in *Proc. of 17th IEEE workshop on Control Model. Power Electron. (COMPEL) [Submitted for Publication]*, 2016.

[18] TDK, "Aluminum electrolytic capacitors B43640," Tech. Rep. November, 2015.

[19] J. W. Kolar, D. Bortis, O. Knecht, F. Krismer, and D. Neumayr, "Inverter zum Austausch elektrischer Energie zwischen einem DC-System und einem AC-System," Patent Pending, September 24, 2015.

[20] D. Zmood and D. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Trans. on Power Electronics*, vol. 18, no. 3, pp. 814–822, 2003.