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***Abstract*—This paper investigates the operation of the Dual Three-Phase Active Bridge (D3AB) converter topology as a multi-port converter, by taking the three-phase ac port and dc port on the primary side ($\mathbf{ac_1}$ and $\mathbf{dc_1}$) and the galvanically isolated three-phase ac port and dc port on the secondary side ($\mathbf{ac_2}$ and $\mathbf{dc_2}$) simultaneously into account. The basic working principle of the D3AB topology under multi-port operation and a strategy to achieve independent power transfer between the four ports are described. It is found that the realization of a power transfer between $\mathbf{ac_1}$ and $\mathbf{ac_2}$, which can be operated with different line voltages and line frequencies, is particularly challenging, as compared to $\mathbf{dc_1}$–$\mathbf{dc_2}$ operation. Therefore, this mode of operation is further analyzed and suitable modulation schemes are developed to achieve sinusoidal ac currents, constant dc-link voltages, and reduced low-frequency power pulsations between the ac ports. The derived analytical results are verified by means of circuit simulations and experiments, for a primary-side ac rms phase voltage of $\mathbf{115\,V}$ and line frequency of $\mathbf{50\,Hz}$, a secondary-side ac rms phase voltage of $\mathbf{57.5\,V}$ and line frequency of $\mathbf{77\,Hz}$, and an output power of $\mathbf{675\,W}$.**

I. Introduction

Future power grids tend to be more distributed to allow a realistic integration of renewable energy systems and enable end users to generate, store, and manage parts of the energy they consume [1]. Multi-port power electronics converters are facilitating the exchange of electric energy between the existing ac grid and various dc and/or ac sources/loads. This includes storage systems for ensuring energy balance and galvanic isolation between different ports in order to allow local grounding and compliance with safety regulations. Typical realizations of suitable multi-port power converters employ multiple conversion stages, e.g., the converter systems with common dc-link considered in [2]–[5]. Still, recent literature reveals that single-stage multi-port topologies, which provide galvanic isolation, dc ports, and a direct interface to three-phase ac systems, are feasible [6], [7].

This paper further pursues the D3AB topology presented in [7]. The fundamental idea behind the D3AB topology is to utilize the High-Frequency (HF) voltage components (switching frequency and above) occuring across the boost inductors of a three-phase two-level Voltage Source Converter (VSC). In a first step, the three boost inductors are equipped with secondary-side windings, which results in three HF transformers. In a second step, the secondary-side windings of the transformers are connected to the switching nodes of an additional, secondary-side three-phase VSC as shown in **Fig. 1**. Finally, the depicted six filter capacitors, termed C_{f1} on the primary side and C_{f2} on the secondary side, are installed to provide low-impedance return paths for the HF currents in the HF transformers. Together with the stray inductances of the HF transformers, this structure realizes a three-phase Dual Active Bridge (DAB) converter topology between dcport 1 ($\mathrm{dc_1}$) and dc port 2 ($\mathrm{dc_2}$) in Fig. 1, which are well documented in literature [8]–[10]. At the same time, the D3AB converter maintains the capabilities of ac–dc power conversions on the primary and the secondary side and allows the transfer of power between ac port 1 ($\mathrm{ac_1}$) and ac port 2 ($\mathrm{ac_2}$). **Table I**

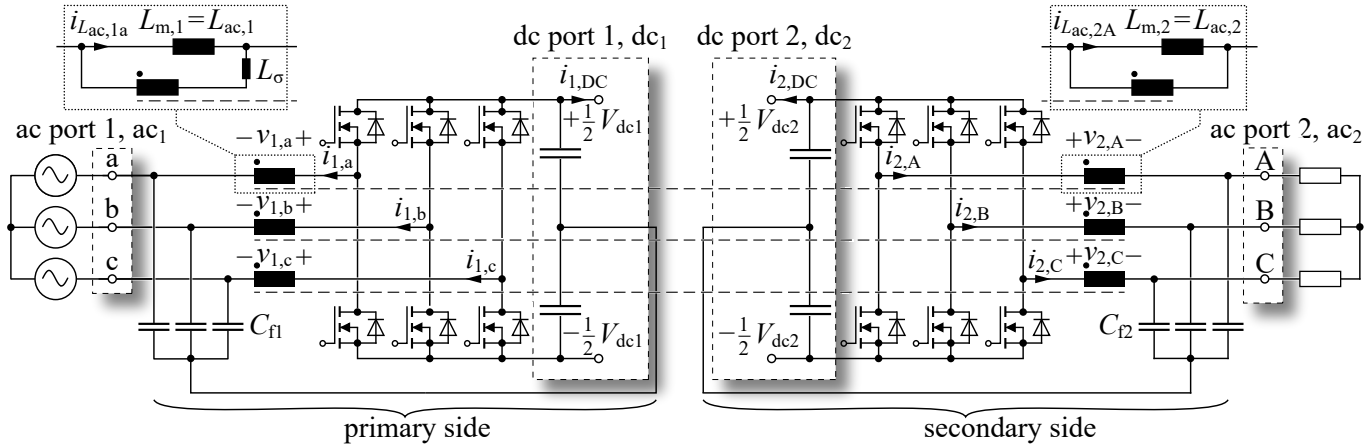

Fig. 1. Dual Three-Phase Active Bridge (D3AB) topology with a ac and dc port on primary side ($\mathrm{ac_1}$, $\mathrm{dc_1}$) and a galvanically isolated ac and dc port ($\mathrm{ac_2}$, $\mathrm{dc_2}$) on the secondary side.

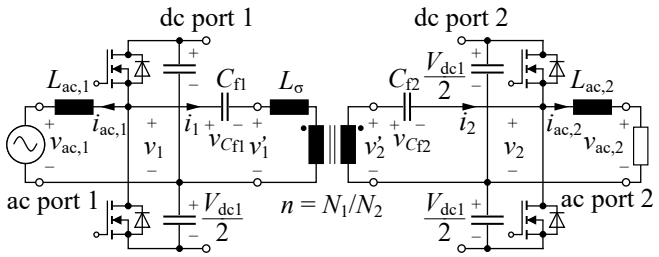

Fig. 2. Single-phase equivalent system with the two boost inductances $L_{\mathrm{ac},1}$ and $L_{\mathrm{ac},2}$, the stray inductance L_σ, and the isolating HF transformer with turns ratio n.

lists the main specifications and component values of the considered system.

Both, the primary side and the secondary side of the D3AB converter are based on the topology presented in [11], however, the Common Mode (CM) inductors between the HF transformers are avoided and the filter capacitors are directly connected back to the mid-point in order to utilize both, the Differential Mode (DM) and the CM components for the operation of the three-phase DAB converter. Accordingly, the three phases of the D3AB converter are not mutually coupled and each phase of the D3AB converter can be considered separately with the single-phase equivalent circuit shown in **Fig. 2**, which is similar to the circuit first presented in [12].[1] The single-phase equivalent circuit is of considerably lower complexity than the full D3AB converter and is particularly useful to explain the mechanism of the isolated power transfer between the primary and the secondary side of the D3AB converter.

This paper explains the basic working principle of the D3AB topology for bidirectional multi-port operation (ac_1–dc_1, dc_1–dc_2, ac_2–dc_2, ac_1–ac_2) in **Section II**, followed by the derivation of the possible operation modes for the three-phase DAB part of the converter in **Section III**. In **Section IV** the challenge of Low-Frequency (LF) power pulsation is investigated and a modulation scheme without LF pulsation of the total power flow of all three phases is derived. By way of example, **Section V** presents the converter's capability to achieve solely ac_1–ac_2 operation with arbitrary frequencies and amplitudes at primary and secondary sides.

[1] In this paper, each phase of the D3AB converter is operated with a power that is subject to a Low Frequency (LF) fluctuation with twice the grid frequency, e.g., to achieve sinusoidal currents at the ac ports. Furthermore, in a three-phase system, the sum of the power in all three phases is constant at the dc-link. For this reason, the overall calculation of the power needs to take the sum of the power waveforms of the three single-phase circuits of Fig. 2 into consideration.

TABLE I. Main specifications and component values of the D3AB topology.

ac_1 voltage (rms)	$V_{\mathrm{ac},1} = 0\,\mathrm{V}..240\,\mathrm{V}$
ac_1 frequency	$f_{\mathrm{m},1} = 0\,\mathrm{Hz}..400\,\mathrm{Hz}$
dc_1 voltage	$V_{\mathrm{dc}1} = 800\,\mathrm{V}$
ac_2 voltage (rms)	$V_{\mathrm{ac},2} = 0\,\mathrm{V}..120\,\mathrm{V}$
ac_2 frequency	$f_{\mathrm{m},2} = 0\,\mathrm{Hz}..400\,\mathrm{Hz}$
dc_2 voltage	$V_{\mathrm{dc}2} = 400\,\mathrm{V}$
Maximal output power	$P_{\mathrm{out}} = 8\,\mathrm{kW}$
Switching frequency	$f_{\mathrm{s}} = 35\,\mathrm{kHz}$
Primary-side dc-link capacitor	$C_{\mathrm{dc}1} = 2 \times 12\,\mu\mathrm{F}$
Secondary-side dc-link capacitor	$C_{\mathrm{dc}2} = 2 \times 37\,\mu\mathrm{F}$
Primary-side filter capacitor	$C_{\mathrm{f}1} = 3 \times 10\,\mu\mathrm{F}$
Secondary-side filter capacitor	$C_{\mathrm{f}2} = 3 \times 21.5\,\mu\mathrm{F}$
Primary-side ac inductance	$L_{\mathrm{ac},1} = 3 \times 231\,\mu\mathrm{H}$
Secondary-side ac inductance	$L_{\mathrm{ac},2} = 3 \times 34\,\mu\mathrm{H}$
Stray inductance	$L_\sigma = 3 \times 89\,\mu\mathrm{H}$
Transformer turns ratio	$n = 2.6$

II. Multi-Port Operation of the D3AB Converter

The single-phase equivalent circuit of Fig. 2 indicates that the examined system can be separated into three subsystems, i.e., primary-side ac_1–dc_1 converter, an isolated dc_1–dc_2 converter, and a secondary-side dc_2–ac_2 converter. In order to gain a deeper understanding if a separate analytical consideration of these power conversion mechanisms is feasible, the frequency spectrum of the active power is examined at the primary-side switching node of phase a (same analogue spectra result for phases b and c),

$$P_{1,\mathrm{a}}(f) = \Re\left[\underline{V}_{1\mathrm{a,MP}}(f)\underline{I}^*_{1,\mathrm{a}}(f)\right]. \tag{1}$$

In (1), $\underline{V}_{1\mathrm{a,MP}}(f)$ denotes the phasor of the voltage between the primary-side switching node of phase a and the primary-side dc mid-point for a given frequency, f, and $\underline{I}^*_{1,\mathrm{a}}(f)$ refers to the complex conjugate of the phasor of the primary-side current in phase a for frequency f; $\underline{I}_{1,\mathrm{a}}$ is computed from $i_{1,\mathrm{a}}(t)$ in **Fig. 1**. **Fig. 3** illustrates $P_{1,\mathrm{a}}(f)$ for a power conversion according to [7], i.e., from ac_1 to dc_2 with an output power of 8 kW, a line frequency at ac_1 of $f_1 = 50\,\mathrm{Hz}$, and a switching frequency of $f_{\mathrm{s}} = 35\,\mathrm{kHz}$. According to this result, the power transfer can be separated into a LF part with negative power (primary-side VSC consumes energy) and a HF part with positive power (primary-side VSC provides energy). The LF part of the spectrum refers to ac_1–dc_1 power conversion on the primary side. The HF part of the spectrum denotes the dc_1–dc_2 power conversion. Accordingly, the ac_1–dc_1 power transfer without galvanic isolation and dc_1–dc_2 operation with galvanic isolation can be analyzed separately, as illustrated in **Fig. 4**, provided that f_{s} is several orders of magnitude higher than the line frequencies f_1 and f_2 at ac_1 and ac_2, respectively.

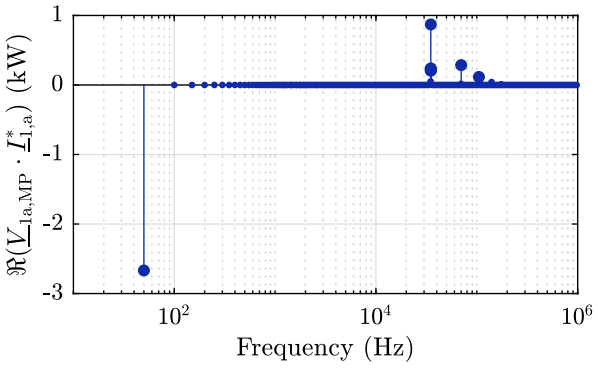

Fig. 3. Power transferred in a single phase, e.g., phase a, in frequency domain for the ac_1–dc_2 operation described in [7] with line frequencies $f_{\mathrm{m}} = 50\,\mathrm{Hz}$ and a switching frequency of $f_{\mathrm{s}} = 35\,\mathrm{kHz}$.

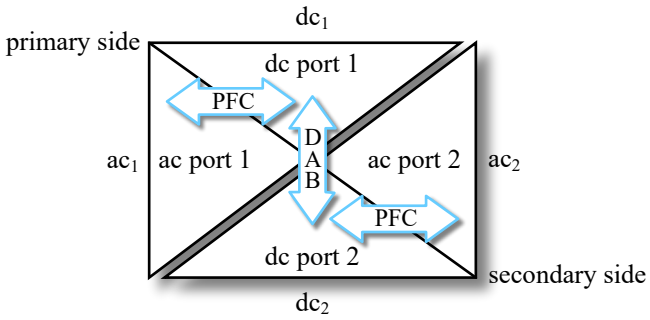

Fig. 4. The power transfer between the four ports of the D3AB converter can be separated into ac_1–dc_1 and ac_2–dc_2 operation w/o galvanic isolation and dc_1–dc_2 operation w/ galvanic isolation. For ac_1–dc_1 and ac_2–dc_2 the corresponding VSCs is operated according to (7) and (8) to achieve Power Factor Correction (PFC) functionality. The power transfer dc_1–dc_2 is utilizing the DAB functionality.

A. Ac–dc conversion without isolation

Three sinusoidal voltages are present at ac_1 and ac_2 of the D3AB converter of Fig. 1,

$$v_{\mathrm{ac},1,\mathrm{a,b,c}}(t) = V_{\mathrm{ac1,peak}} \sin\left(2\pi f_1 t + \theta_{\mathrm{a,b,c}}\right), \tag{2}$$

$$v_{\mathrm{ac},2,\mathrm{A,B,C}}(t) = V_{\mathrm{ac2,peak}} \sin\left(2\pi f_2 t + \theta_{\mathrm{A,B,C}} + \Theta\right), \tag{3}$$

featuring amplitudes $V_{\mathrm{ac1,peak}}$ and $V_{\mathrm{ac2,peak}}$, line frequencies f_1 and f_2 (which are part of the LF spectrum), phase shifts $\theta_{\mathrm{a,b,c}} \in \{0\,^\circ, 120\,^\circ, 240\,^\circ\}$ and $\theta_{\mathrm{A,B,C}} \in \{0\,^\circ, 120\,^\circ, 240\,^\circ\}$ between the primary-side phases and secondary-side phases, respectively, and an initial phase shift, Θ, between the primary and the secondary side at $t = 0$.

At the line frequencies f_1 and f_2, the impedances of the boost inductances $L_{\mathrm{ac},1}$ and $L_{\mathrm{ac},2}$ are small. This leads to negligible LF voltage drops across them, i.e., the local average values of the voltages across $L_{\mathrm{ac},1}$ and $L_{\mathrm{ac},2}$, evaluated over one switching period, are approximately zero,

$$\langle v_{L1,\mathrm{a,b,c}} \rangle_{T_\mathrm{s}} \approx 0, \qquad \langle v_{L2,\mathrm{A,B,C}} \rangle_{T_\mathrm{s}} \approx 0. \tag{4}$$

Accordingly, the HF transformers feature negligible LF couplings between their primary and secondary sides, which further confirms that the two three-phase VSCs can be analyzed independently for the primary and the secondary side, cf. Fig. 4.

In the presented analysis, the three-phase VSCs are operated without LF CM components, i.e., with purely sinusoidal modulation without third harmonic injection. As a consequence, at low frequencies, the primary-side potential at the star-point of the mains is equal to the primary-side potential at the star-point of the filter capacitors C_{f1}, $\varphi_{01} \approx \varphi_{\mathrm{MP1}}$ in Fig. 1. The same applies on the secondary side: $\varphi_{02} \approx \varphi_{\mathrm{MP2}}$. As a consequence, the line voltages appear across the filter capacitors. In order to comply with (4), the local average values of the voltages at the switching nodes,

$$\langle v_{1,\mathrm{a,b,c}} \rangle_{T_\mathrm{s}} = \left(D_{1,\mathrm{a,b,c}} - \frac{1}{2}\right) V_{\mathrm{dc},1}, \tag{5}$$

$$\langle v_{2,\mathrm{A,B,C}} \rangle_{T_\mathrm{s}} = \left(D_{2,\mathrm{A,B,C}} - \frac{1}{2}\right) V_{\mathrm{dc},2}. \tag{6}$$

need to be equal to the respective line voltages, which defines the duty cycles for all six half-bridges,

$$D_{1,\mathrm{a,b,c}}(t) \approx \frac{1}{2}\left[1 + m_1 \sin\left(2\pi f_1 t + \theta_{\mathrm{a,b,c}}\right)\right], \tag{7}$$

$$D_{2,\mathrm{A,B,C}}(t) \approx \frac{1}{2}\left[1 + m_2 \sin\left(2\pi f_2 t + \theta_{\mathrm{A,B,C}} + \Theta\right)\right], \tag{8}$$

using the two modulation indexes $m_1 = 2V_{\mathrm{ac1,peak}}/V_{\mathrm{dc},1}$ and $m_2 = 2V_{\mathrm{ac2,peak}}/V_{\mathrm{dc},2}$. The controller slightly adjusts the duty cycles of (7) and (8) in order to achieve PFC rectifier or inverter operation with defined power levels on the primary and the secondary side, as illustrated in Fig. 4.

Using this control, the local average values of the instantaneous power flow in each half-bridge, $\langle p_{1,\mathrm{a,b,c}} \rangle_{T_\mathrm{s}}$ and $\langle p_{2,\mathrm{A,B,C}} \rangle_{T_\mathrm{s}}$, pulsate with twice the line frequency. However, in symmetric three-phase systems, the total power over all three phases is constant, which allows to design the dc-link capacitor considering only HF current components (switching frequency and above) and no LF components. As a consequence, the dc-link capacitors for three-phase converters can be much smaller than, e.g., those used in single-phase converters.

B. Dc–dc conversion with galvanic isolation

The isolated power transfer between dc_1 and dc_2 is explained for a single phase, using the equivalent circuit depicted in Fig. 2. The described mechanism applies to all three phases of the D3AB converter in an independent manner, i.e., the dc–dc power flow of each of the three phases is controlled separately.

The half-bridges on the primary and the secondary side employ the same switching frequency, $f_\mathrm{s} = 1/T_\mathrm{s}$, to control the phase currents by applying rectangular voltages to the isolating transformers, v_1' and v_2', featuring voltage components at the switching frequency and above. The filter capacitors C_{f1} and C_{f2} block the LF voltage components and, with this, prevent a saturation of the magnetic core of the transformer.[2]

The difference between v_1' and $n\,v_2'$ is applied to the transformer's stray inductance, L_σ, and causes a change of the inductor current. The HF phase shift between the two rectangular voltages, φ_p, as defined in **Fig. 5(a)**, is used to change the shape of the current i_1. This allows to control the power transferred between dc_1 and dc_2, as illustrated in Fig. 4, using the phase shift φ_p in a way known for DAB dc–dc converters.

Since the three isolated dc–dc converters of the D3AB converter can be operated at different power levels, the total power of all three phases is not necessarily constant. Accordingly, suitable functions for the phase shifts denoted $\varphi_{\mathrm{p,aA}}(t)$, $\varphi_{\mathrm{p,bB}}(t)$, and $\varphi_{\mathrm{p,cC}}(t)$ need to be identified in order to maintain a cancellation of LF power pulsations in the dc-links of the primary and the secondary side, which is particularly challenging because the duty cycles $D_{1,\mathrm{a,b,c}}$ and $D_{2,\mathrm{A,B,C}}$ are continuously changing according to (7) and (8). The respective derivations are presented in the subsequent Sections III and IV.

[2]In addition, v_1' and v_2' are also applied to $L_{\mathrm{ac},1}$ and $L_{\mathrm{ac},2}$, respectively, resulting in triangular inductor currents. In a practical implementation, these triangular currents are blocked by a line-side Electromagnetic Interference (EMI) filter (not shown in Fig. 1).

III. DAB Operating Modes

In order to identify possible functions for the phase shifts, $\varphi_{\mathrm{p,aA,bB,cC}}(t)$, that lead to constant total power, the relation between the phase shift and the power level of the dc_1–dc_2 converter part of a single phase of the D3AB converter, i.e., a single-phase DAB converter, needs to be known in a first step.

The local average value (over one switching period) of the power flow of a single-phase DAB converter is defined with

$$\langle p\rangle_{T_\mathrm{s}}(t) = \langle p\rangle(t) = \frac{1}{T_\mathrm{s}}\int_0^{T_\mathrm{s}} p(t+\tau)\,\mathrm{d}\tau = \frac{1}{T_\mathrm{s}}\int_0^{T_\mathrm{s}} v_1'(t+\tau)\,i_1(t+\tau)\,\mathrm{d}\tau. \quad (9)$$

For the evaluation of (9), the waveforms of $v_1'(t)$ and $i_1(t)$ need to be known. In this regard, $v_1'(t)$ is known if the duty cycle D_1 and the phase shift φ_p are defined. However, $i_1(t)$ has to be calculated, e.g., by integrating the time derivative of $i_1(t)$,

$$i_1(t) = I_0 + \int_0^t \left(\frac{\mathrm{d}i_1(\tau)}{\mathrm{d}\tau}\right)\mathrm{d}\tau \quad (10)$$

(I_0 denotes the initial current at $t = 0$), since the time derivative of i_1 can be directly determined with the waveforms of the voltages $v_1'(t)$ and $nv_2'(t)$ that are applied to the HF transformer and the stray inductance, cf. Fig. 2,

$$\frac{\mathrm{d}i_1(t)}{\mathrm{d}t} = \frac{v_1'(t) - n\,v_2'(t)}{L_\sigma}. \quad (11)$$

For the assumption of constant dc-link voltages V_{dc1} and V_{dc2} and constant voltages across the filter capacitors, the voltage across L_σ changes only at four instants during one switching period, i.e., whenever a rising or a falling edge of $v_1'(t)$ or $v_2'(t)$ occurs. The instants of these events are termed $t_{1\uparrow}$, $t_{1\downarrow}$, $t_{2\uparrow}$, and $t_{2\downarrow}$, where the subscripts refer to rising ($\uparrow$) and falling ($\downarrow$) edges of $v_1'(t)$ and $v_2'(t)$, respectively. If $t_{1\uparrow}$ is used as a reference, the subsequent instants $t_{1\downarrow}$, $t_{2\uparrow}$, and $t_{2\downarrow}$ can occur in any order, as defined by the duty cycles, D_1 and D_2, and the phase shift, φ_p. In total, six permutations of $\{t_{1\downarrow}, t_{2\uparrow}, t_{2\downarrow}\}$ can be distinguished, representing the six operating modes of this DAB converter, which are consecutively numbered with I to VI. Fig. 5(b) shows example waveforms for $v_1'(t)$, $nv_2'(t)$, and $i_1(t)$ for the six operating modes.

By way of example, (9) and (10) are evaluated for operating mode I, cf. Fig. 5(a), which features four time intervals with constant voltage across L_σ that are delimited with the times t_1, t_2, t_3, and T_s. With this, the voltages $v_1'(t)$ and $v_2'(t)$ are defined as

$$v_1'(t) = \begin{cases} +\frac{V_{\mathrm{dc1}}}{2} - \langle v_{\mathrm{Cf1}}\rangle & \forall \quad 0 \le t < t_2, \\ -\frac{V_{\mathrm{dc1}}}{2} - \langle v_{\mathrm{Cf1}}\rangle & \forall \quad t_2 \le t < T_\mathrm{s}, \end{cases} \quad (12)$$

$$v_2'(t) = \begin{cases} -\frac{V_{\mathrm{dc2}}}{2} + \langle v_{\mathrm{Cf2}}\rangle & \forall \quad 0 \le t < t_1, \\ +\frac{V_{\mathrm{dc2}}}{2} + \langle v_{\mathrm{Cf2}}\rangle & \forall \quad t_1 \le t < t_3, \\ -\frac{V_{\mathrm{dc2}}}{2} + \langle v_{\mathrm{Cf2}}\rangle & \forall \quad t_3 \le t < T_\mathrm{s}, \end{cases} \quad (13)$$

for operating mode I, whereas the voltages across the filter capacitors C_{f1} and C_{f2} are obtained by solving the condition for steady-state operation,

$$i_1(t) = i_1(t + T_\mathrm{s}), \quad (14)$$

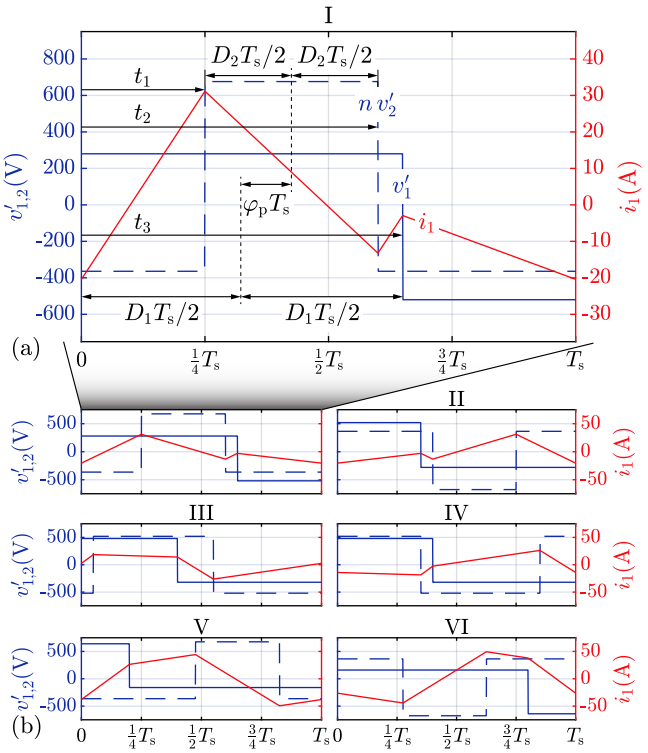

Fig. 5. (a) Definitions of D_1, D_2, and load angle φ with calculated waveforms over one switching period, T_s, with $f_\mathrm{s}\,L_\sigma \approx 3.4\,\Omega$, $n = 2.6$, $V_{\mathrm{dc1}} = 800\,\mathrm{V}$, $V_{\mathrm{dc2}} = 400\,\mathrm{V}$, $D_1 = 0.4$, $D_2 = 0.5$ and $\varphi \approx 29\,^\circ$ and (b) all possible operation modes for this DAB converter.

which results in

$$\langle v_{\mathrm{Cf1}}\rangle = \left(D_1 - \frac{1}{2}\right)V_{\mathrm{dc1}}, \quad \langle v_{\mathrm{Cf2}}\rangle = \left(D_2 - \frac{1}{2}\right)V_{\mathrm{dc2}}. \quad (15)$$

Since the voltages $\langle v_{\mathrm{Cf1}}\rangle$ and $\langle v_{\mathrm{Cf2}}\rangle$ are assumed to be constant, the average of the current i_1 has to be zero, allowing to solve for the current I_0. With this, (9) can be evaluated, which gives

$$\langle p\rangle = P_0\left[\varphi_\mathrm{p}\,2D_2\,(1 - D_1)\right] \quad (16)$$

for operating mode I. For the remaining operating modes, the expressions for $\langle p\rangle$ are determined in the same manner.

In a next step, the different functions derived for $\langle p\rangle$, i.e., one function for each operating mode, are solved with respect to φ_p for a given power, P ($P > 0$ refers to power transferred from dc_1 to dc_2). It is found that operating modes V and VI are redundant, i.e., the same power is achieved with operating modes I to IV. However, operating modes V and VI lead to higher rms currents in the HF transformer than modes I to IV. For this reason, only the operating modes I to IV are further considered.

Since the permutations of $\{t_{1\downarrow}, t_{2\uparrow}, t_{2\downarrow}\}$ depend on D_1, D_2, and φ_p, the condition that must be fulfilled such that a particular operating mode applies depends on D_1, D_2, and φ_p, too. **Table II** lists these conditions for modes I to IV and presents the expressions derived for φ_p, which depend on the

TABLE II. Conditions for operating modes I to IV and solutions for the phase shift, φ_p, for each operating mode that sets the power level of a single DAB converter phase equal to the reference power, P.

Mode	Conditions	φ_p
I	$\lvert\varphi_\mathrm{p}\rvert < \frac{D_1-D_2}{2} \wedge D_1 > D_2$	$\varphi_{\mathrm{p,I}} = \frac{e_1}{2D_2(1-D_1)}$
II	$\lvert\varphi_\mathrm{p}\rvert < \frac{D_2-D_1}{2} \wedge D_1 < D_2$	$\varphi_{\mathrm{p,II}} = \frac{e_1}{2D_1(1-D_2)}$
III	$\varphi_\mathrm{p} > \frac{\lvert D_1-D_2\rvert}{2} \wedge \varphi_\mathrm{p} < \frac{D_1+D_2}{2}$	$\varphi_{\mathrm{p,III}} = e_3 - \sqrt{e_2 - e_1}$
IV	$\varphi_\mathrm{p} < -\frac{\lvert D_1-D_2\rvert}{2} \wedge \varphi_\mathrm{p} > -\frac{D_1+D_2}{2}$	$\varphi_{\mathrm{p,IV}} = -e_3 + \sqrt{e_2 + e_1}$
	$e_1 = P/P_0$	
	$e_2 = D_1\,(1-D_1)\,D_2\,(1-D_2)$	
	$e_3 = \frac{1}{2}\,[D_1\,(1-D_2) + D_2\,(1-D_1)]$	

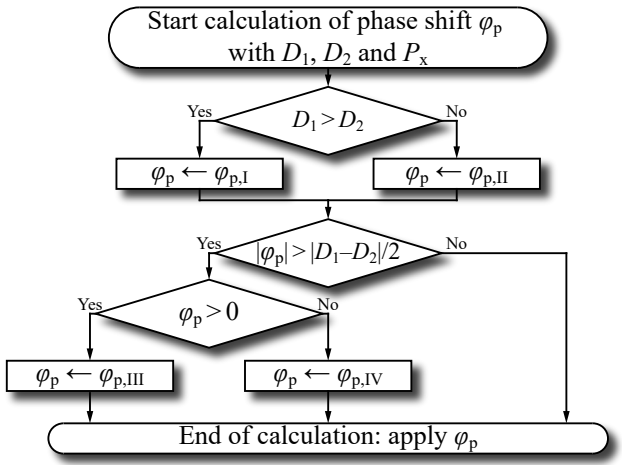

Fig. 6. Algorithm used to identify the current mode each DAB converter phase is operated in and to calculate the corresponding phase shift φ_p.

duty cycles, the power in a single phase, P, and a common factor P_0,

$$P_0 = \frac{n\,T_\mathrm{s}\,V_\mathrm{dc1}\,V_\mathrm{dc2}}{2L_\sigma}. \tag{17}$$

Fig. 6 illustrates the flow chart of the algorithm that is used to determine the operating mode and the phase shift, φ_p.

Finally, the expressions for the minimum and maximum power levels in each operating mode are needed in the following Section, to identify the maximum possible power that can be transferred between the two dc ports. **Table III** lists the expressions for the phase shifts that lead to minimum and maximum power levels as well as the functions for minimum and maximum power levels that can be achieved in a single phase and for a given operating mode.

TABLE III. Expressions for the minimum and maximum power levels, P_min and P_max, that are feasible in each operating mode.

	φ_p	Power
I	$\frac{D_1-D_2}{2}$	$P_{\mathrm{I,max}} = P_0\,[D_2\,(1-D_1)\,(D_1-D_2)]$
	$\frac{D_2-D_1}{2}$	$P_{\mathrm{I,min}} = P_0\,[-D_2\,(1-D_1)\,(D_1-D_2)]$
II	$\frac{D_2-D_1}{2}$	$P_{\mathrm{II,max}} = P_0\,[D_1\,(1-D_2)\,(D_2-D_1)]$
	$\frac{D_1-D_2}{2}$	$P_{\mathrm{II,min}} = P_0\,[-D_1\,(1-D_2)\,(D_2-D_1)]$
III	$\frac{D_1(1-D_2)+D_2(1-D_1)}{2}$	$P_{\mathrm{III,max}} = P_0\,[D_1\,(1-D_1)\,D_2\,(1-D_2)]$
	–	$P_{\mathrm{III,min}} = \begin{cases} P_{\mathrm{I,max}}, D_1 > D_2 \\ P_{\mathrm{II,max}}, D_1 < D_2 \end{cases}$
IV	–	$P_{\mathrm{IV,max}} = \begin{cases} P_{\mathrm{I,min}}, D_1 > D_2 \\ P_{\mathrm{II,min}}, D_1 < D_2 \end{cases}$
	$-\frac{D_1(1-D_2)+D_2(1-D_1)}{2}$	$P_{\mathrm{IV,min}} = P_0\,[-D_1\,(1-D_1)\,D_2\,(1-D_2)]$

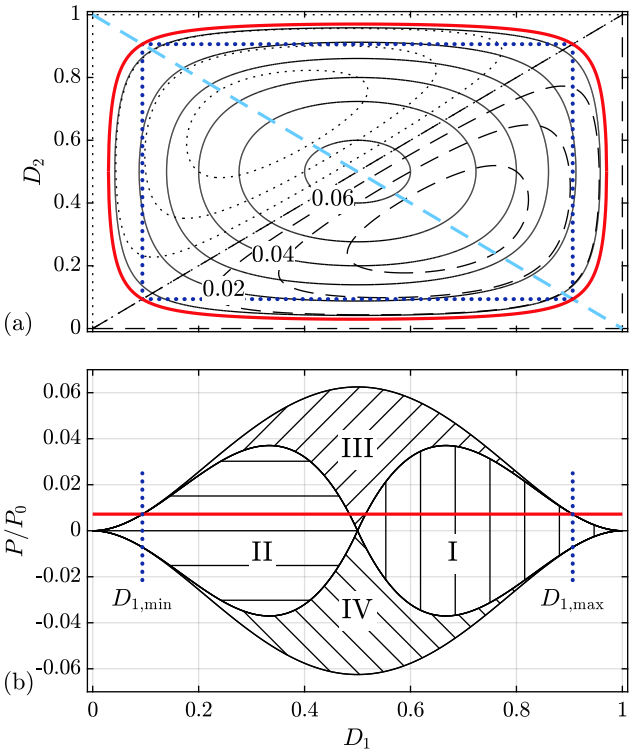

Fig. 7. (a) Contour plot of the maximum power for modes I to III and (b) cut along the dashed light-blue line through the maximum power contour plot. Red line represents a solution with constant power in each phase.

IV. Cancellation of LF Power Pulsation

LF power pulsation cancellation is achieved if the sum over the average power levels of all three DAB converter phases is constant,

$$\langle p_\Sigma \rangle\,(t) = \langle p_\mathrm{aA} \rangle\,(t) + \langle p_\mathrm{bB} \rangle\,(t) + \langle p_\mathrm{cC} \rangle\,(t) \stackrel{!}{=} \text{const.} \tag{18}$$

A second condition is added to ensure same loading of each phase of the converter, i.e., $\langle p_\mathrm{aA} \rangle\,(t)$, $\langle p_\mathrm{bB} \rangle\,(t)$, and $\langle p_\mathrm{cC} \rangle\,(t)$ are required to have same waveforms and are only shifted in time by a time shift T,

$$\langle p_\mathrm{aA} \rangle\,(t) \stackrel{!}{=} \langle p_\mathrm{bB} \rangle\,(t-T) \stackrel{!}{=} \langle p_\mathrm{cC} \rangle\,(t+T). \tag{19}$$

The conditions (18) and (19) are fulfilled if $\langle p_\mathrm{aA} \rangle\,(t)$, $\langle p_\mathrm{bB} \rangle\,(t)$, and $\langle p_\mathrm{cC} \rangle\,(t)$ are equal and constant,

$$\langle p_\mathrm{aA} \rangle = \langle p_\mathrm{bB} \rangle = \langle p_\mathrm{cC} \rangle = \langle p \rangle\,(D_1, D_2) = \frac{P_\mathrm{x}}{3}, \tag{20}$$

where P_x denotes the overall reference power level for the dc–dc (three-phase DAB) converter part of the D3AB converter system. In this regard, power is transferred from dc_1 to dc_2 if $P_\mathrm{x} > 0$ applies and the opposite is true if P_x is negative. Accordingly, P_x can be used as a control parameter to control, e.g., the dc-link voltage at dc_2, V_dc2.

To keep the power of each phase constant, we have to guarantee that for any combination of D_1 and D_2 each phase can provide the required power, which is assessed based on the expressions for the maximum power levels listed in Table III. The contour plot in **Fig. 7**(a) reveals the maximum power levels for operating modes I to III, normalized to P_0, i.e.,

$P_{\mathrm{I,max}}/P_0$, $P_{\mathrm{II,max}}/P_0$, and $P_{\mathrm{III,max}}/P_0$, for D_1, $D_2 \in [0, 1]$. The solid black contour lines labeled with 0.02, 0.04, and 0.06 are associated with mode III and represent the highest possible power for any combination of D_1 and D_2. The dashed and dotted black lines represent the maximum power levels of modes I and II, respectively, which are strictly less than the maximum power levels of mode III (and strictly greater than the minimum power of mode IV). It is to be noted that the minimum power achieved with mode IV, $P_{\mathrm{IV,min}}$, features the same characteristic as the maximum power of mode III, $P_{\mathrm{III,max}}$, but with a negative sign. Therefore, maximum possible power in reverse direction is achieved with mode IV. For the sake of clarity, the presented explanations are confined to a power transfer from the primary to the secondary side, i.e., operating modes I to III. However, an extension to bidirectional operation is directly feasible.

The dotted blue rectangle represents the area of possible combinations of the duty cycles, which are given as

$$\frac{1}{2}(1-m_1) \le D_1 \le \frac{1}{2}(1+m_1) \tag{21}$$

$$\frac{1}{2}(1-m_2) \le D_2 \le \frac{1}{2}(1+m_2) \tag{22}$$

for the modulation indexes m_1 and m_2. Within the entire ranges defined by (21) and (22), the chosen power, $P_{\mathrm{x}}/3$, has to be less than $P_{\mathrm{III,max}}$ (and greater than $P_{\mathrm{IV,min}}$).

A constant power $P_{\mathrm{x}}/3$ corresponds to a plane in the D_1-D_2-domain and the intersection of this plane with the curved surface defined with $P_{\mathrm{III,max}}(D_1, D_2)$ delimits feasible combinations of D_1 and D_2 that allow for DAB converter operation at this defined power level. The red contour line shown in Fig. 7(a) illustrates this intersection for $P_{\mathrm{x}}/3 = 0.97\,\mathrm{kW}$.

In order to gain more insight into the mode limits defined by the equations listed in Table III, Fig. 7(b) shows a cut along the dashed light-blue diagonal line in the contour plot of Fig. 7(a), whereas the cut is projected to the D_1 axis. The hatched areas represent the regions of corresponding operating modes I to IV [which correspond to volumes in the contour plot of Fig. 7(a)]. The white areas without labels, i.e., above mode III and below mode IV, denote unreachable power levels. The solid red line in Fig. 7(b) refers to the reference power level, $P_{\mathrm{x}}/3 = 0.97\,\mathrm{kW}$. According to the example depicted in the Fig. 7(b), mainly modes I and II are used; mode III applies only for a small region where D_1 and D_2 are close to 0.5.

The reference power level depicted in Fig. 7 crosses $P_{\mathrm{III,max}}(D_1, D_2)$ at the corners of the duty cycle area delimited by (21) and (22) (using $m_1 = m_2 = 0.8125$, cf. Section II-A and **Table I**). Considering this limit, the maximum value of P_{x} is calculated using

$$P_{\mathrm{x,max}} = \min\Big[\,3\,P_{\mathrm{III,max}}\big|_{D_1 \to \frac{1}{2}(1\pm m_1),\, D_2 \to \frac{1}{2}(1\pm m_2)}\Big] \tag{23}$$

(due to symmetry, all four combinations of D_1 and D_2 give the same result). For $m_1 = m_2 = m$,

$$P_{\mathrm{x,max}} = \frac{3}{16} P_0 \big(m^2 - 1\big)^2, \qquad 0 < m < 1 \tag{24}$$

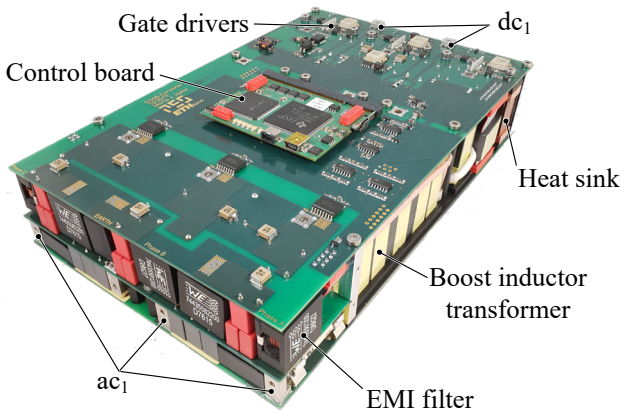

Fig. 8. Hardware demonstrator of a D3AB power converter with 8 kW power for ac_1–dc_2 operation. The outer dimensions are 150 mm × 240 mm × 54 mm = 5.91 in × 9.45 in × 2.13 in (width × depth × height). The top-side PCB contains the power semiconductors of the primary side, the bottom-side PCB the power semiconductors of the secondary side, and the boost inductors are in between. The ports ac_2 and dc_2 are not visible in this picture.

results, which, for $m = 0.8125$ and the values listed in Table I, gives a maximum power for all three phases of $P_{\mathrm{x}} = 2.9\,\mathrm{kW}$.[3]

V. Simulation and Experimental Verification

The described procedure for ac–ac operation of the D3AB converter is verified by means of simulation and experiment. The simulation and the experiment employ a D3AB converter system that is parameterized according to Table I. The experimental verification is conducted with the hardware depicted in **Fig. 8**, which employs SiC MOSFETs for the power switches (C3M0016120K on the primary side and C3M0010090K on the secondary side, both manufactured by Cree) and ferrite cores for the coupled boost inductors / HF transformers (each boost inductor employs four stacked pairs of E42/21/20 / N95 cores manufactured by TDK/Epcos). It is to be noted that the hardware used for experimental verification has been designed for a different aim, i.e., for power transfer from ac_1 to dc_2 [7]. In order to avoid an overloading of the power components in case of ac_1–ac_2 operation, simulation and experiment are conducted at reduced dc-link voltages of $V_{\mathrm{dc1}} = 400\,\mathrm{V}$ and $V_{\mathrm{dc2}} = 200\,\mathrm{V}$. A three-phase voltage source with $V_{\mathrm{ac1,rms}} = 115\,\mathrm{V}$ and $f_1 = 50\,\mathrm{Hz}$ is connected to ac_1 and a three-phase resistive load to ac_2; ac_2 is operated with $V_{\mathrm{ac2,rms}} = 57.5\,\mathrm{V}$ and $f_2 = 77\,\mathrm{Hz}$. With this, the modulation indexes are identical to the modulation indexes used in Section IV, i.e., $m_1 = m_2 = 0.8125$ applies. The power provided by the DAB part of the converter covers the output power and parts of the losses; in addition, a certain margin between the provided power and the maximum power is considered to enable control. For this reason, the output power at ac_2 has been reduced from the maximum value of 725 W (which results for the reduced dc-link voltages) to 675 W.

[3] A comparison to Table I reveals that this value is considerably below the rated power of the system of $P_{\mathrm{out}} = 8\,\mathrm{kW}$. However, the maximum power for ac–ac operation could be increased if $\langle p_{\mathrm{aA,bB,cC}} \rangle$ are not kept constant, which is subject to current research on the D3AB converter system.

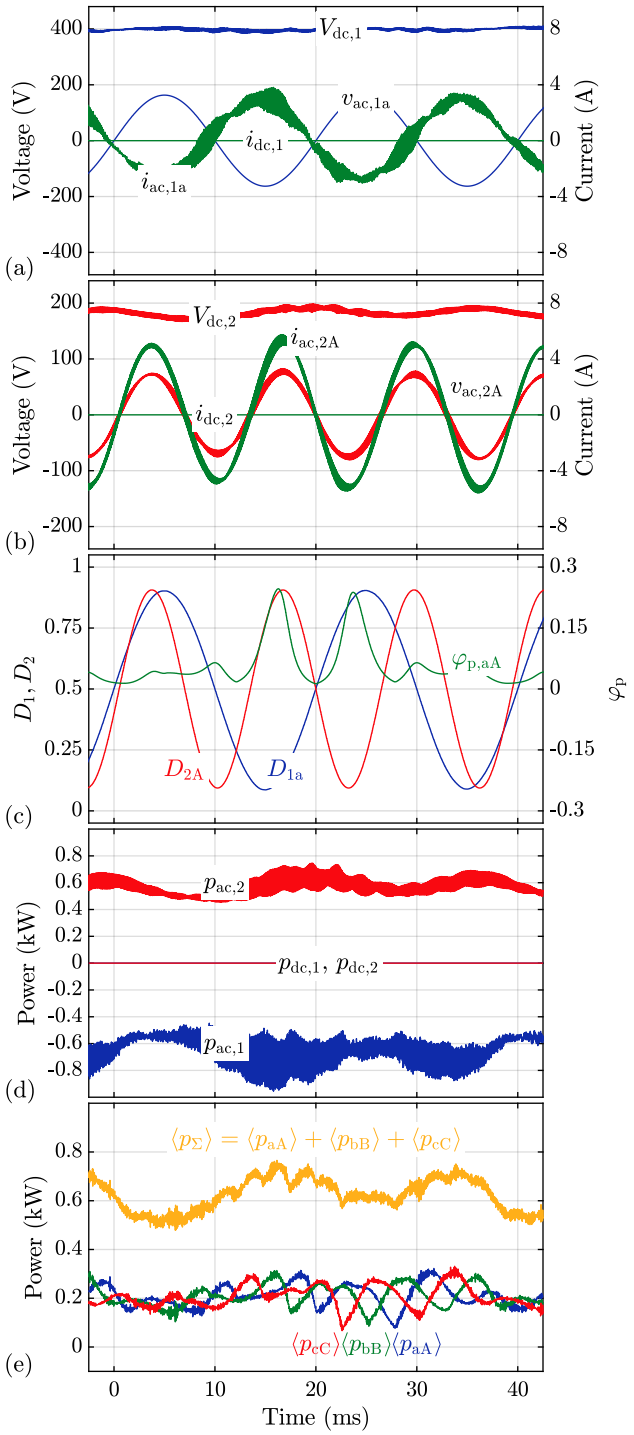

Fig. 9. Circuit simulation results for ac_1–ac_2 operation with $V_{dc,1} = 400\,\mathrm{V}$, $V_{dc,2} = 200\,\mathrm{V}$, $V_{ac1,rms} = 115\,\mathrm{V}$, $V_{ac2,rms} = 57.5\,\mathrm{V}$, $f_1 = 50\,\mathrm{Hz}$, $f_2 = 77\,\mathrm{Hz}$, and a resistive load with $R_{load} = 14.7\,\Omega$ on each phase of ac_2 resulting into $p_{ac,2} = 675\,\mathrm{W}$.

The primary-side VSC controls the primary-side line currents, $i_{ac1,a,b,c}$, to be sinusoidal and in phase to the corresponding line voltages and to achieve a constant dc-link voltage at dc_1. The phase shifts $\varphi_{p,aA,bB,cC}$ are controlled to achieve a constant dc-link voltage at dc_2, $V_{dc,2}$. Finally, the ac phase voltages at ac_2 are generated in open loop, by changing the duty cycles according to (8).

The results of the circuit simulations are shown in **Fig. 9**.

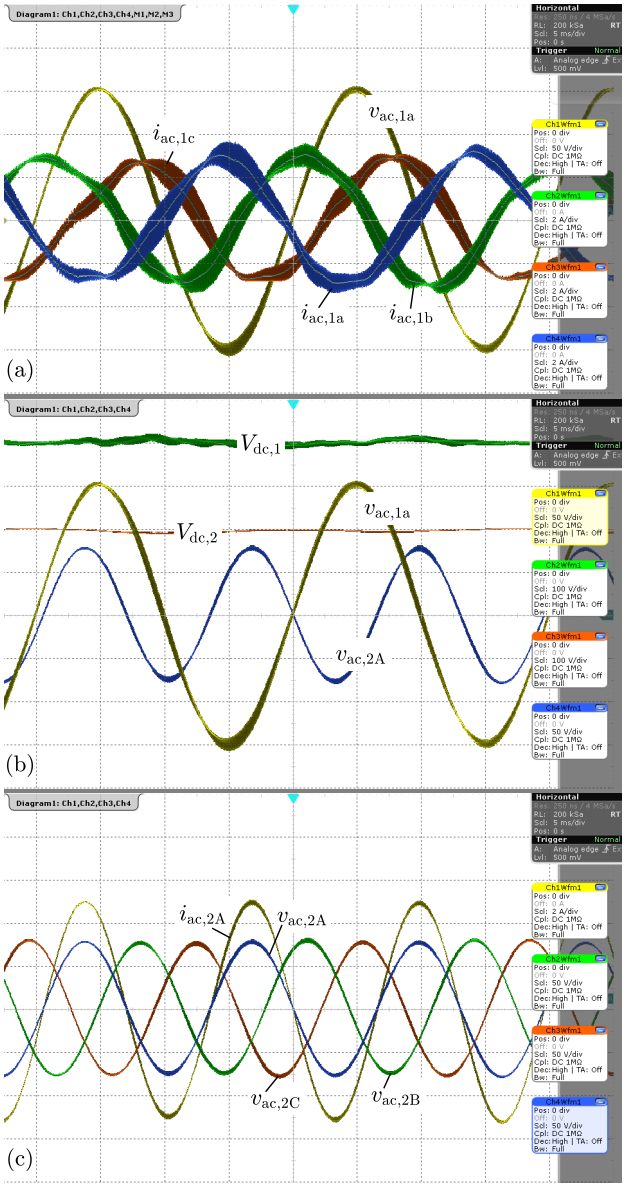

Fig. 10. Measurement results with same conditions as for the circuit simulation Fig. 9. (a) Sinusoidal currents at ac_1 [2 A/div] and the phase voltage of phase a [50 V/div] as a reference; (b) both dc-link voltages [100 V/div] and phase a voltages [50 V/div] of primary and secondary side; (c) sinusoidal voltages at ac_2 [50 V/div] and the current of phase a [2 A/div] as a reference. All measurements are synchronized and have a time resolution of [5 ms/div] .

Fig. 9(a) reveals a phase shift of 180 ° between the primary-side line voltages and the line currents of the same phase, corresponding to a PFC rectifier operation at the primary side, cf. Section II-A. The phase current, $i_{ac,1a}$, is subject to LF and HF distortions. The LF distortions in $i_{ac,1a}$ are due to fluctuations of the instantaneous power levels of each DAB converter phase, $\langle p_{aA} \rangle$, $\langle p_{bB} \rangle$, and $\langle p_{cC} \rangle$, as shown in Fig. 9(e), which is addressed to current-dependent time delays of the power switches, e.g., due to the employed dead times of 80 ns that are used to avoid short circuits in the bridge legs. As a consequence, the resulting total power, $\langle p_\Sigma \rangle$ shows a peak-to-peak LF ripple of 200 W. For this reason, also the instantaneous power levels at ac_1 and ac_2 are subject to LF variations, cf. Fig. 9(d), which cause LF distortions in $i_{ac,1a}$

and $V_{\mathrm{dc},2}$. The observed HF distortions in $i_{\mathrm{ac},1\mathrm{a}}$ are related to the optimized EMI filter that achieves a high attenuation only for $150\,\mathrm{kHz} < f < 30\,\mathrm{MHz}$, to fulfill the EMI requirements.[4] The secondary-side line voltage and the line current of phase A are in phase, i.e., inverter operation applies, as shown in Fig. 9(b).

Fig. 10 presents the measurement result for ac_1–ac_2 operation with an output power of $675\,\mathrm{W}$. Fig. 10(a) depicts the primary-side line voltage of phase a and all primary-side phase currents. The highlighted current waveforms in Fig. 10(a) are obtained by applying a low-pass filter with a cut-off frequency of $10\,\mathrm{kHz}$ to the measured phase currents, in order to illustrate LF distortions. Fig. 10(b) shows the voltages at all four ports and Fig. 10(c) all three secondary-side phase voltages as well as the secondary-side ac current in phase A. The measured waveforms match well to the simulated waveforms depicted in Fig. 9, which confirms the findings discussed above, also with regard to the distortions of the primary-side phase currents. Yet, the shown result represents a first verification. Different improvements can be implemented to reduce such distortions, e.g., feed-forward of current-dependent time delays of the power semiconductors to achieve a more constant power provided by the DAB converter phases. The analysis and implementation of possible improvements is currently investigated.

VI. Conclusion

In this paper the working principle for a quad-port ac_1–dc_1–dc_2–ac_2 operation of an isolated Dual Three-Phase Active Bridge (D3AB) Converter is derived with focus on preventing LF power pulsation between the ports. The analysis is split into the operation of the converter at line frequency and at HF, i.e., switching frequency and above, allowing to separate the power transfer mechanism of ac to dc power conversion without galvanic isolation, e.g., between ac_1 and dc_1, from the mechanism that features a power transfer between the two dc ports. Ac to dc power conversion without galvanic isolation is achieved with the well-known method used in three-phase PFC rectifiers/inverters, where the corresponding duty cycles $D_{1,\mathrm{a,b,c}}$ and $D_{2,\mathrm{A,B,C}}$ of each bridge-leg are controlled to achieve sinusoidal line currents, defined active (and reactive) powers at the ac ports, constant dc-link voltages at the dc-link capacitors, and, in case of an ideally symmetric three-phase system, no LF pulsations of the total powers converted by the three-phase PFC rectifiers/inverters. The power transfer between the two dc ports is similar to that of three single-phase DAB dc–dc converters, where the phase shifts, $\varphi_{\mathrm{p,aA,bB,cC}}$, are used to adjust the transferred power. However, different to a common DAB converter, the duty cycles $D_{1,\mathrm{a,b,c}}$ and $D_{2,\mathrm{A,B,C}}$ do not remain as a degree of freedom. In this context, a method is proposed, which adjusts $\varphi_{\mathrm{p,aA,bB,cC}}$ such that the sum of the average power levels over a switching period of all DAB phases remains constant for all combinations of duty cycles, i.e., LF power pulsation is also avoided in the DAB part of the D3AB converter. The functionality of the procedure is verified by means of simulations and experiments for ac_1–ac_2 operation with a power of $675\,\mathrm{W}$ at ac_2, a primary-side line frequency of $f_1 = 50\,\mathrm{Hz}$, and a secondary-side line frequency of $f_2 = 77\,\mathrm{Hz}$. Both, simulations and experiments confirm the feasibility of the proposed method and demonstrate the great flexibility of the D3AB converter system, e.g., if needed, the power flow could be immediately reversed or redirected from one port to another. Yet, residual LF power pulsations are observed, which are assigned to non-idealities of the demonstrator hardware, e.g., current-dependent time delays in the half-bridges, and to the considered system itself, since the employed converter is optimized for a different aim, i.e., power transfer from ac_1 to dc_2 and high power density. In this regard, future research will be conducted towards further optimized modulation schemes, with focus on maximum power, component stresses, and improved quality of the input current.

[4]It is to be noted that the boost inductors used in the considered system feature comparably low inductances, since the D3AB converter has been designed for operation from ac_1 to dc_2 and optimized with respect to a high power density. This, however, further increases the difficulty to achieve very high quality sinusoidal line currents on the primary side in case of ac–ac operation.

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