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Analysis of a Solid-State Transformer Employing Capacitively Isolated Series-Stacked Converter Cells and a Single Medium-Frequency Transformer

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***Abstract*—Solid-state transformers (SST) provide voltage scaling and galvanic isolation between medium-voltage (MV) and low-voltage (LV) dc busses. Most SST topologies arrange several isolated dc-dc converter cells in an input-series, output-parallel (ISOP) configuration, whereby each cell's medium-frequency transformer (MFT) must withstand the very high lightning impulse (LI) surge test voltage resulting in a significant volume overhead from bushings and clearance distances. This paper focuses on an alternative structure that employs capacitive isolation of the individual cells (CC-SST) and thus requires only a single output-side MFT with LI withstand capability, whose dry-type isolation, advantageously, is not stressed with high dc voltages during normal conditions, which ensures a long lifetime of the insulation material. The operating principle of the CC-SST is thoroughly explained using an exemplary system (12 kV dc input, 800 V dc output, 400 kW), and design challenges, in particular circulating currents among the converter cells, are highlighted. Finally, a comparative evaluation against a similar concept using ISOP-connected MFTs indicates that the capacitive coupling approach could achieve an efficiency improvement of up to 0.5 percentage points without an increase in size.**

***Index Terms*—Solid-state transformer, capacitive isolation, input-series output-parallel (ISOP), dc transformer, medium voltage.**

I. Introduction

In high-power applications supplied from the medium-voltage (MV) grid, solid-state transformers (SSTs) replace conventional low-frequency transformers (LFTs) with medium-frequency transformers (MFTs) and power electronic conversion stages on both, the MV input and the (typically) low-voltage (LV) output side. Originally developed for space- and weight-constrained applications, in particular onboard traction vehicles [1], [2], SSTs are widely considered as important building blocks of a future smart grid due to the increase in functionality compared to LFTs [3]. However, in typical ac-ac grid applications, the combination of efficiency, robustness, and costs of an LFT are very hard to beat [4]. In contrast, there is a high interest in SSTs for MVac-LVdc applications like datacenter power supplies [5], electrolysis [6], and especially for high-power EV charging [7]–[15] (where several industrial demonstrators with several hundred kilowatts rated power have been built [11], [13], [14] and full-load efficiencies of 98% have been measured [11]). Finally, MVdc grids are envisioned for reinforcing or replacing the existing ac grid in utility [16], [17] and traction

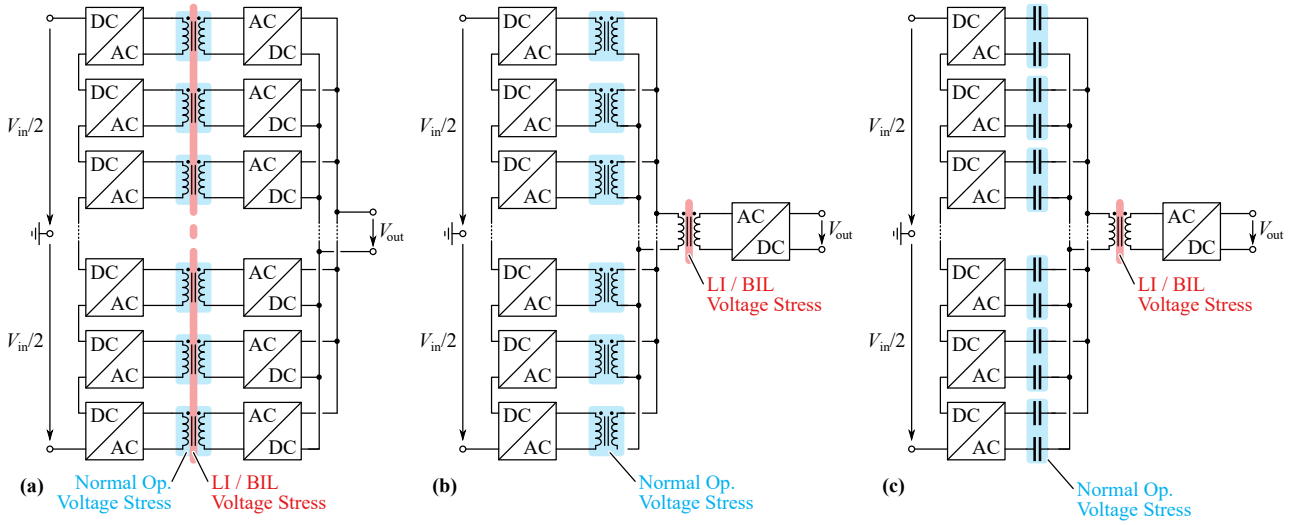

Fig. 1. MVdc-LVdc SST topologies. **(a)** Conventional multicell system with one MFT per converter cell that is rated for LI tests and subject to continuous MV stress in normal operation. **(b)** Inductively-coupled multicell SST (IC-SST) proposed in [30], where the coupling MFTs operate with MV stress under normal conditions whereas, advantageously, the main MFT does not; only the main MFT is rated for LI stress. **(c)** Capacitively-coupled multicell SST (CC-SST) proposed in [39], where the coupling MFTs are replaced by coupling capacitors, i.e., off-the-shelve components with negligible losses.

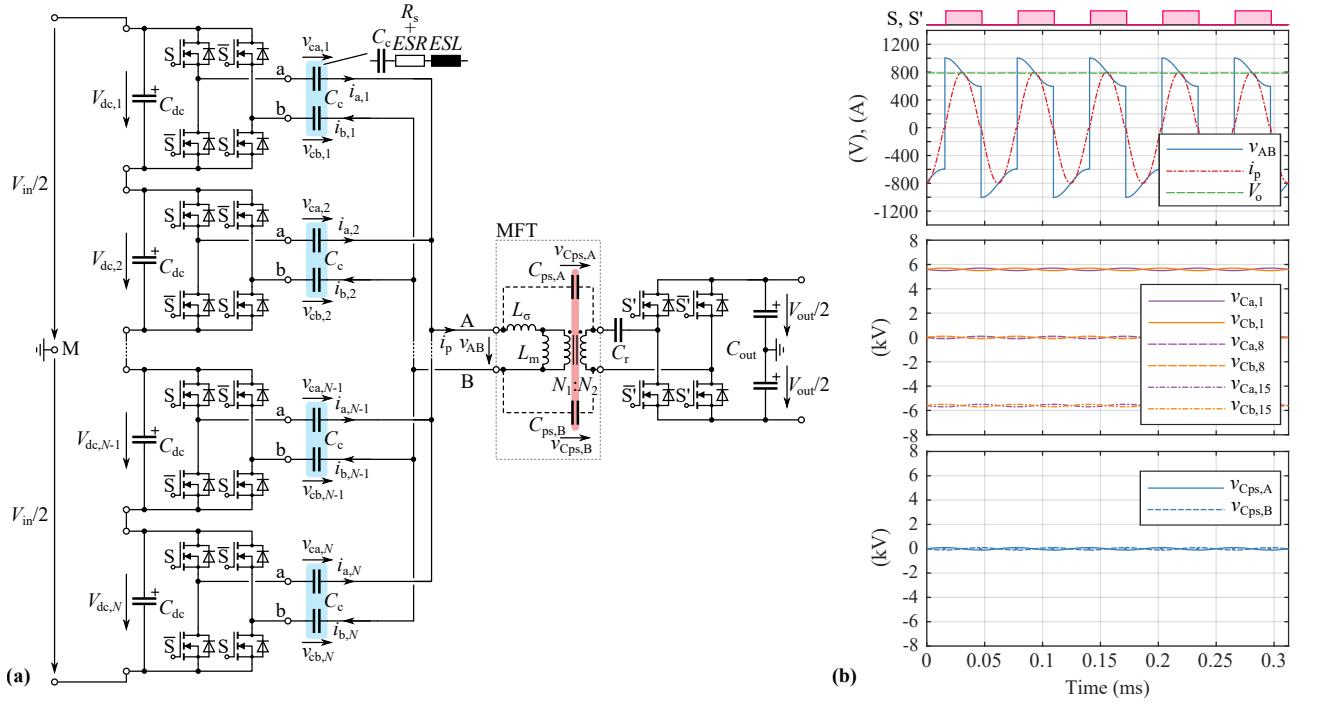

Fig. 2. (a) Detailed power circuit of the CC-SST from **Fig. 1c** (for the sake of clarity the representation is limited to 4 cells whereas 15 cells are employed in the actual system, see **Tab. I**), and **(b)** simulated key waveforms for operation as a DCX (considering 15 stacked cells, see **Section II-A**). Note the limited voltage stress of the MFT insulation ($v_{\mathrm{Cps,A}}$ and $v_{\mathrm{Cps,B}}$) in normal operation.

[18] applications, as well as aboard future hybrid or all-electric ships [19].

In all these cases, essentially an isolated MVdc-LVdc converter is at the SST's core. Whereas cutting-edge 10+ kV SiC transistors enable standard converter topologies to interface at least lower MV levels [20]–[22], modular approaches have the advantage of scalability and support, in principle, higher voltage and power ratings without direct series connection or direct paralleling of transistors, respectively. Therefore, most SST topologies, e.g., [2], [11], [13], [14], [23], [24], are built from many identical dc-dc converter modules that each contain an MFT and which are configured in an input-series, output-parallel (ISOP) arrangement as shown in **Fig. 1a**. A drawback of this fully modular topology, however, is that the primary-to-secondary insulation of each individual MFT is stressed with high dc offset voltages in normal operation *and* must also be able to withstand the (significantly higher) lightning impulse (LI) test voltages[1] prescribed in standards [25]–[27]. As in addition the power rating of a single MFT is only a fraction of the SST's rated power, the overhead in terms of volume created by these high isolation requirements (e.g., large bushings [28]) limits the SST's power density ("modularization penalty" [29]).

Fig. 1b shows a first option to address this drawback, which has been published recently [30]: The secondary-side converter stages of all cells are merged and an additional MFT processing the rated power is introduced. The converter cells are inductively coupled (IC-SST) via MFTs to a common ac link on the primary-side of the main MFT.[2] Advantageously, only the main MFT must provide LI withstand capability but is not stressed with high dc voltages under normal operation because the dc offset voltages appear across the coupling MFTs' insulation (we will discuss the underlying mechanism later in **Section II**). Therefore, the insulation systems of the coupling MFTs and of the main MFT can be optimized for their sole respective task. The coupling MFTs can be air-insulated and do not require large bushings, as they only need to pass partial-discharge (PD) testing but not LI tests, which would require significantly larger clearance distances. Aiming for a compact implementation, the main MFT thus should employ dry-type (solid) insulation.[3] As discussed above, advantageously the circuit structure of the IC-SST prevents a continuous MV stress of the main MFT's solid insulation, which greatly reduces the risk for PD and hence simplifies achieving a highly durable insulation system [30].[4] Furthermore, only the main LFT requires bushings with sufficient clearance to withstand LI tests, but given the higher power rating compared to the coupling MFTs, the overhead is less pronounced.

However, the second MFT in the power conversion path reduces the achievable efficiency by typically 0.25 to 0.5 percentage points. In general, transformers have been replaced by capacitors to achieve galvanic separation with lower losses in

[1]Note that the terms "lightning impulse" (LI) and "basic impulse level" (BIL) are employed interchangeably.

[2]As an aside, note the similarity to MF ac power distribution concepts such as described, e.g., in [31]–[33].

[3]Oil isolation should be avoided due to the fire hazard and environmental considerations.

[4]Note that this is conceptually similar to the hybrid air/solid insulation concept for an MFT described in [34].

low-voltage systems [35]–[37], but have also been considered for fully modular MVdc-LVdc converters [38]. Therefore, **Fig. 1c** shows a capacitively-coupled SST (CC-SST) topology, which has been proposed in [39]. Advantageously, the small MFTs are replaced by off-the-shelve capacitors with typically very low losses. Again, these capacitors take the dc offset voltages such that the main MFT finds similar conditions as in the IC-SST approach.[5] Even though very promising, the CC-SST topology has not yet received much attention in the literature. Therefore, this paper first describes the operating principle and the design of an exemplary CC-SST in **Section II** and then addresses the design challenges arising from the high-frequency (HF) ac-side coupling of several converter cells in **Section III**. Finally, **Section IV** provides a comparative evaluation of the CC-SST against the IC-SST, and **Section V** concludes the paper.

II. CC-SST Operating Principle and Design

Fig. 2a shows a detailed power circuit diagram of a CC-SST. Considering the exemplary specifications from **Tab. I** and operation as a dc transformer (DCX; details below), **Fig. 2b** shows simulated key waveforms that illustrate the following discussion of the CC-SST's operating principle. The dc input voltage of $V_{\mathrm{dc}} = 12\,\mathrm{kV}$ is compatible with an ac-dc power-factor-correcting (PFC) rectifier frontend interfacing the 6.6 kV MV grid (considering 10% grid overvoltage and about 15% modulation reserve).

To describe the CC-SSTs operating principle, it is useful to consider the equivalent circuit shown in **Fig. 3a**, which then can be split into a differential-mode (DM) and a common-mode (CM) equivalent circuit. The following discussion assumes that the total input dc voltage distributes equally among the input-side dc-link capacitors as

$$V_{\mathrm{dc},i} = \frac{V_{\mathrm{in}}}{N}, \tag{1}$$

where N is the number of cascaded converter cells. For the considered specifications, $V_{\mathrm{dc,cell},i} = 800\,\mathrm{V}$ and thus 1200 V power transistors offer sufficient blocking voltage margin. Furthermore, the desired output voltage of $V_{\mathrm{out}} = 800\,\mathrm{V}$ results in an advantageous unity turns ratio of the MFT.

A. DCX Operation

Operating the CC-SST as a resonant converter in the half-cycle discontinuous-conduction-mode, i.e., with a resonance frequency, $f_0 = 16.5\,\mathrm{kHz}$, slightly higher than the switching frequency $f_{\mathrm{s}} = 16\,\mathrm{kHz}$, results in an almost load-independent output voltage without the need for active control [43], [44], i.e., it acts as a "dc transformer" (DCX) with fixed voltage transfer ratio. Furthermore, the coupling capacitors and the MFT's leakage inductance can be utilized to form the resonant tank, while the MFT's magnetizing current facilitates soft-switching for all transistors [45].

[5]There are also other SST topologies with only a single MFT, which are based on the modular-multilevel converter (MMC) [40]–[42]. However, there, typically the DM voltage applied to the transformer is in the order of the dc input voltage to limit the currents processed by the converter cells [40].

Table I
Exemplary specifications and parameters of the CC-SST shown in **Fig. 2**.

Symbol	Description	Value
V_{in}	Input dc voltage	12 kV
V_{out}	Output dc voltage	800 V
P_{nom}	Rated power	400 kW
N	Number of cells	15
$V_{\mathrm{dc},i}$	Cell dc voltage	800 V
f_s	Switching frequency	16 kHz
f_0	Resonance frequency	16.5 kHz
C_{c}	Coupling capacitor capacitance	5 µF
ESL	Equivalent series inductance	80 nH
ESR	Equivalent series resistance	0.4 mΩ
R_{s}	Series resistance	1.7 mΩ
$N_1 : N_2$	Transformer turns ratio	1 : 1
L_σ	Leakage inductance	2.5 µH
L_{m}	Magnetizing inductance	1 mH
C_{ps}	Isolation capacitance	250 pF
LI / BIL	Lightning impulse voltage (RI)	59 kV
C_{r}	Secondary-side resonant capacitor	not used

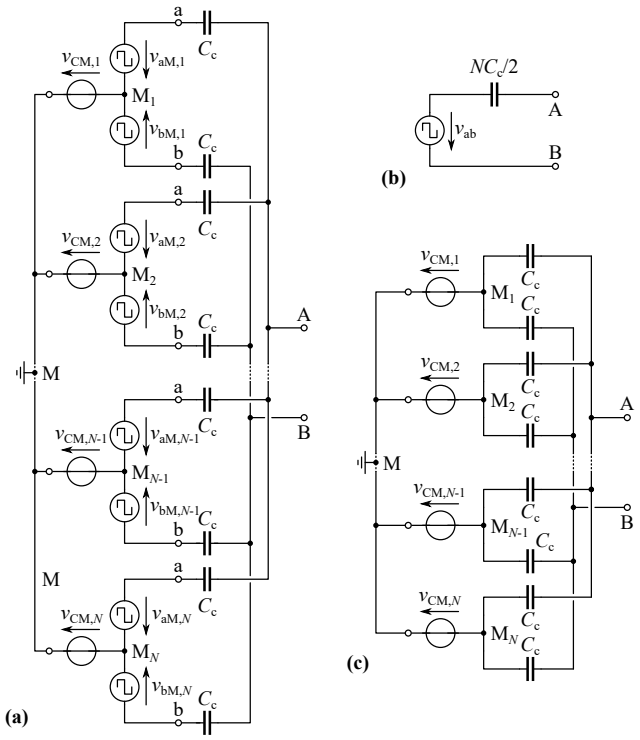

Fig. 3. (a) Schematic representation of the the primary-side part of the CC-SST (limited to 4 of 15 cells, see **Tab. I**) from **Fig. 2a** and decomposition into **(b)** DM and **(c)** CM equivalent circuits.

In the CC-SST, all primary-side full-bridges operate with equal dc voltage and switch synchronously. Hence, from a power-transfer perspective, all N converter cells are connected in parallel and thus can be represented by single voltage source in the DM equivalent circuit from **Fig. 3b**. Similarly, the effective series capacitor follows as

$$C_{\mathrm{c,DM,eff}} = N\frac{C_{\mathrm{c}}}{2}, \tag{2}$$

where C_{c} is the coupling capacitance and $C_{\mathrm{c,DM,eff}} = 37.5\,\mu\mathrm{F}$ follows. This rather high value requires a quite small leakage

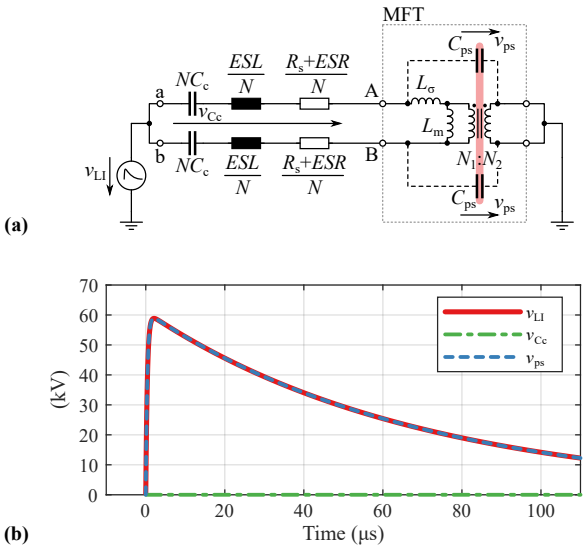

Fig. 4. **(a)** Equivalent circuit representation of the CC-SST for LI testing, where the the LI test voltage is applied to the a- and b-terminals of all cells connected together. **(b)** Transient simulation with v_{LI} as a standard 1.2/50 µs LI test voltage waveform with a peak value of 58.7 kV. Note that the voltage across the coupling capacitors (including the ESL) remains essentially zero.

inductance of the MFT transformer, i.e.,

$$L_\sigma = \frac{1}{4\pi^2 f_0^2 C_{c,DM,eff}}, \tag{3}$$

which evaluates to $L_\sigma = 2.5\,\mu H$. This is a low value but compatible with MFT realizations described in the literature [46], [47]. To cope with higher stray inductances (to which also parasitic inductances of the wiring between the converter cells and the MFT must be added), a secondary-side series capacitor, C_r, could be introduced to reduce the effective series capacitance as needed for maintaining the desired resonance frequency, f_0; here, we do not further consider this in the interest of a focused analysis.

B. DC Offset Voltages

As mentioned, the coupling capacitors take the respective cell's dc CM offset voltage, which we now illustrate using the CM equivalent circuit from **Fig. 3c**. Considering the positive half cycle, i.e., the cells' terminal voltages are $V_{ab,i} = V_{dc,i}$ (again assuming equal dc voltage sharing), the cell's offset voltages correspond to the CM voltage of the two output terminals a and b with respect to a (virtual) input voltage midpoint M. With

$$v_{a,i} = \frac{V_{in}}{2} - (i-1)\frac{V_{in}}{N} \quad \text{and} \tag{4}$$

$$v_{b,i} = \frac{V_{in}}{2} - i\frac{V_{in}}{N}, \tag{5}$$

the CM offset voltages become

$$v_{CM,i} = \frac{1}{2}\left(v_{a,i} + v_{b,i}\right) = \frac{V_{in}}{2}\left(1 - \frac{2i-1}{N}\right). \tag{6}$$

For the opposite (negative) switching state with $V_{ab,i} = -V_{dc}$, the same value results, i.e., ideally $v_{CM,i} = const.$. The zero state ($v_{ab} = 0$) should not be used to prevent the generation of HF CM voltages. As the coupling capacitors present low impedance at high frequencies, any generated HF CM voltage components would appear at the MFT terminals and contribute to isolation stress; however, in contrast to fully capacitvely isolated systems [35]–[38], the MFT suppresses HF CM currents. To handle short CM voltage spikes, e.g., resulting from not perfectly aligned switching transitions, small CM chokes (e.g., clamp-on cores) can be placed at the output terminals of each cell [39].

Not considering such non-idealities but full symmetry of the circuit, we have

$$v_{CM,i} = -v_{CM,N+1-i} \quad \forall\ i \in [1, N] \tag{7}$$

and hence the CM voltage of the terminals A and B of the MFT's primary-side winding with respect to the input voltage midpoint is ideally zero by a simple voltage divider consideration (see **Fig. 3c**). Thus, if the input voltage midpoint, M, is grounded or is guaranteed to be close to earth potential (as is typically the case), the MFT's insulation is not subject to any MVdc stress in normal operation.

C. Coupling Capacitor Selection

From the above considerations, the maximum CM voltage offset that defines the voltage rating of the series capacitors occurs for $i = 1$ or $i = N$ and amounts to

$$\max\left|v_{CM,i}\right| = \frac{V_{in}}{2}\left(1 - \frac{1}{N}\right) \le \frac{V_{in}}{2}. \tag{8}$$

Hence, the dc voltage rating of the coupling capacitors is about 6 kV for the case at hand.

In DCX operation, the capacitor rms current becomes

$$\tilde{i}_{Cc} = \frac{\pi P}{2\sqrt{2} N V_{dc}}\sqrt{\frac{f_0}{f_s}}, \tag{9}$$

which evaluates to about $\tilde{i}_{Cc} = 38\,A$. In contrast to pure resonant capacitors, the CC-SST's coupling capacitors are subject to a very high dc offset voltage; the HF ac voltage component resulting from the resonant current should remain comparably small to limit the maximum DM voltages applied to the MFT's primary-side winding. Hence, the usage of the coupling capacitors is similar to that of dc-link capacitors. Thus, we consider a typical series of standard metallized polyproylene film capacitors (AIC E51 DC). The most compact capacitor that meets the combined requirements of dc voltage rating and rms current capability (limited by the permissible temperature rise) is the E51.P22-502R20/H with $C_c = 5\,\mu F$ and an 8 kV dc voltage rating[6]. The capacitor features a boxed volume of 1.8 dm^3 (90 mm diameter, 220 mm length). The total volume of all 30 coupling capacitors thus becomes 53.5 dm^3 and corresponds, at $P = 400$ kW, to a power density of 7.5 kW/dm^3, i.e., comparable to typical MFTs.

[6]Despite including some margin, the selected capacitor rated for 8 kV dc is more compact than those rated with 6 kV dc. As this is due to the specific components available in the considered series, there is, in principle, potential for more compact implementations.

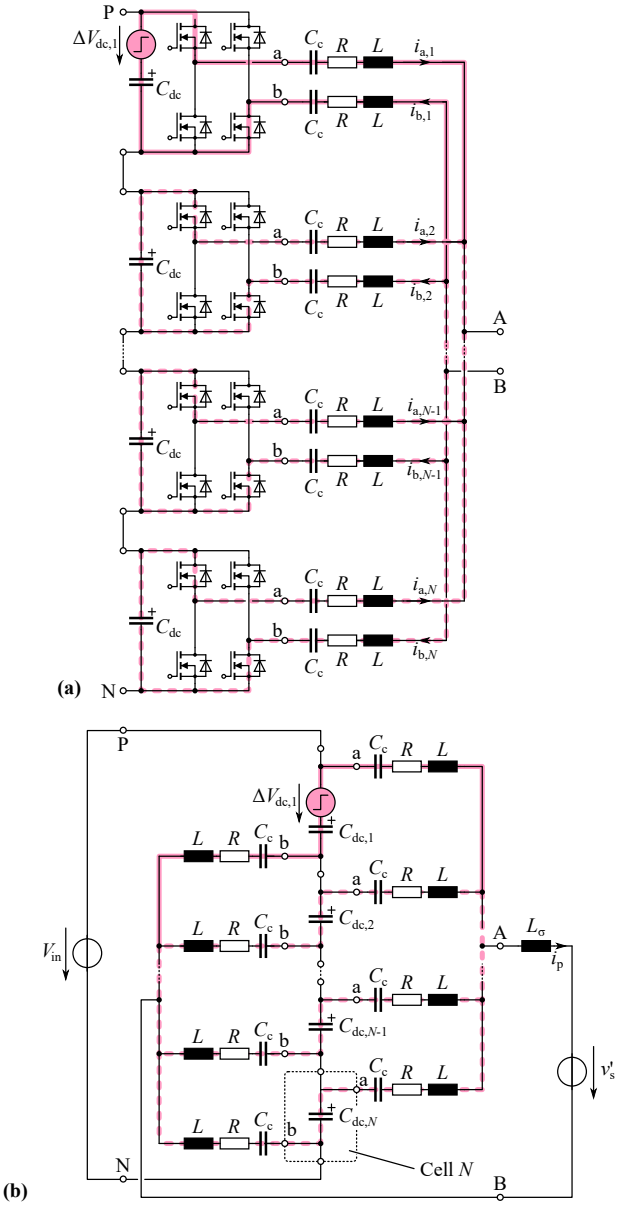

Fig. 5. **(a)** Visualization of circulating current paths in the CC-SST during a positive voltage pulse and **(b)** equivalent circuit representation, where R includes the capacitor's ESR and R_s as well as the on-state resistance, R_{on}, of one transistor; L includes the ESL and, possibly, an explicit series inductance, L_c. The excitation ΔV_{dc} is either caused by dc voltage imbalances among the cells due to component tolerances or by switching time mismatches.

The capacitor losses result from the ohmic series resistance, R_s, and from dielectric losses (resulting from the ac component of the capacitor voltage) that are characterized by the dielectric's $\tan\delta = 2 \cdot 10^{-4}$ as

$$P_c = \tilde{i}_c^2 R_s + \tilde{i}_c^2 \overbrace{\frac{\tan\delta}{2\pi f_s C_c}}^{ESR} \tag{10}$$

per capacitor (see also **Tab. I**). For the selected capacitor, $P_c = 3\,\mathrm{W}$ and hence the total coupling capacitor losses are 90 W or 0.023% of the rated power. This is far less than what coupling MFTs of the IC-SST would dissipate.

D. Transient LI Voltage Sharing

Whereas the coupling capacitors relieve the MFT's insulation from any high dc voltage stress, it must withstand the LI tests described in standards such as IEC 62477-2, which we consider here as an example. For the mentioned grid voltage of 6.6 kV (from which the 12 kV dc input voltage has been deduced above), the standard requires an LI test voltage (1.2/50 µs pulse shape) with 58.7 kV peak value (OVC-III, reinforced isolation).

Whereas SST protection concepts in general must consider also the propagation of a lightning surge inside of the primary-side converter stages [24], [25], [27], from the MFT insulations' perspective, a meaningful test is to apply the LI test voltage as a CM voltage between the a- and b-terminals of all cells connected together and ground. The equivalent circuit shown in **Fig. 4a** represents this situation. As the LI pulse is a HF waveform, the impedances formed by the (equivalent, i.e., paralleled) coupling capacitors and the MFT's primary-to-secondary isolation capacitances, C_{ps}, define the voltage sharing. Given that C_c is in the µF range whereas C_{ps} is, maximally, in the nF range,

$$v_{Cc} = \frac{C_{ps}}{C_{Cc} + C_{ps}} v_{LI} \leq \frac{10^{-9}}{10^{-6} + 10^{-9}} v_{LI} \approx \frac{1}{1000} v_{LI}, \tag{11}$$

i.e., the coupling capacitors see less than one volt per one kilovolt of the applied LI pulse. The simulation results shown in **Fig. 4b** confirm this and also indicate that the presence of the capacitor's ESL does not result in significant voltage drops.[7]

III. CC-SST Design Challenges

Under ideal conditions, the CC-SST thus appears as a very interesting approach. However, considering real-world non-idealities such as component tolerances or switching time mismatches, challenges arise in the design of a CC-SST, which are briefly outlined in the following.

A. Component Tolerances and Current Sharing

The total primary-side MFT current i_p distributes to the cells according to the impedances of the respective series elements (i.e., the coupling capacitors, but also lumped series inductances, L, and resistances, R, which include parasitics[8] and—as discussed later—possibly dedicated series inductors); i.e., equally in case of perfectly matched component values. However, off-the-shelve, the selected capacitors are only available with a ±5% tolerance rating, i.e., impedance mismatches must be expected.

As an example, suppose that only the coupling capacitor connected to the a-terminal of cell 1 has a different (higher)

[7] The highest frequency required for largely defining the standard pulse shape is about 300 kHz; whereas the impedance of an exemplary (large) isolation capacitance of 1 nF is 530 Ω at this frequency, the impedance of an exemplary (large) series inductance of 1 µH is only 1.9 Ω, i.e., still more than two orders of magnitude smaller; the selected capacitors feature a much lower ESL = 80 nH.

[8] At the selected switching frequency, the coupling capacitors dominate the impedances even in the presence of stray inductances from cabling, etc. of up to several µH.

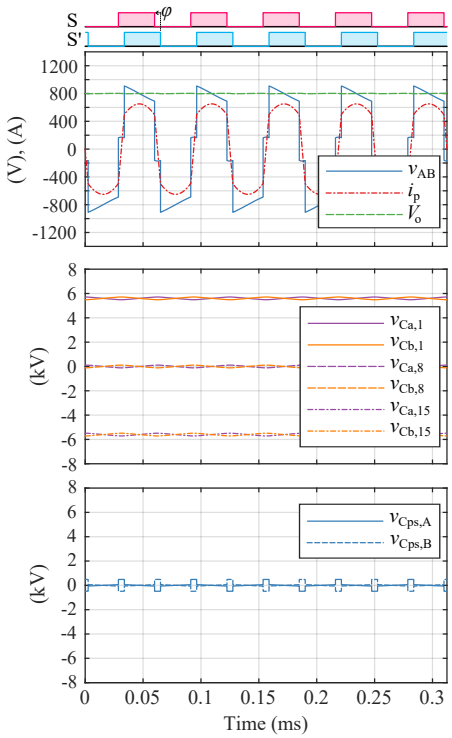

Fig. 6. Simulated key waveforms of the CC-SST operating as a DAB (with L_{DAB} = 9.4 µH, implemented with L_c = 33 µH and L_σ = 5 µH). Note the phase shift, φ, between the primary-side and secondary-side switching commands (S and S', respectively).

value than all other coupling capacitors. Intuitively, one would think that thus the currents in *both* output terminals (a and b) of cell 1 would be higher than in all other cells (due to the lower impedance of the coupling capacitor connected to terminal a). However, as can be seen from the equivalent circuit in **Fig. 5b**, this is not necessarily true, as, given the much lower impedances of the cells' dc-link capacitors, essentially the b-terminals of *all* cells are connected in parallel; i.e., the excess current flowing into the a-terminal of cell 1 distributes to the b-terminals of all other cells, thereby affecting the charge balance of *all* dc link capacitors. This is an example only; in general, during one switching state, all cells (including their coupling and dc-link capacitors) form an impedance network from which the ac current (and hence power) distribution and ultimately the steady-state dc voltage sharing among the cells can be found. In this way, component tolerances of the coupling capacitors can lead to unequal dc voltages of the cells.

B. Circulating Currents

In case the cell's dc voltages are not equal, though, the voltage difference appears as a step voltage excitation upon changing of the switching state (indicated in **Fig. 5** by the step voltage sources) and drives circulating currents between the cells. Note that also mismatches of the switching timings have the same effect, as then temporarily one cell might apply the opposite voltage at its terminals a and b compared to the other cells.

Similar issues have been described for SSTs based on a multi-winding transformer, where stacked primary-side converter cells and a single secondary-side rectifier stage are coupled via a single magnetic core [1]. As a countermeasure, the decoupling impedance between the primary-side converter cells should be maximized, which in [1] is achieved by minimizing the series resonant capacitor and thus maximizing the resonant circuit's characteristic impedance. However, the feasibility of this approach is limited in the CC-SST, as the DM voltage ripple of the coupling capacitors should remain comparably low; first, because off-the-shelve capacitors with high dc voltage rating do not support very high voltage ripples (ripple currents), and, second, because otherwise the DM voltage applied to the MFT's primary-side winding increases to values above V_{dc}, which diminishes the advantages of the CC-SST concept regarding insulation stress of the MFT.

Alternatively, small inductors, L_c, could be placed in series to the coupling capacitors [39], as indicated in **Fig. 5**. For example, consider a switching time mismatch of Δt_{sw} = 100 ns, i.e., cell 1 switches from positive to negative output voltage 100 ns before all other cells. During that interval, essentially twice the dc-link voltage is applied to the series connection of cell 1's two L_c (all other cells act in parallel, in this example, and hence the contribution of their inductors is at least an order of magnitude lower and thus neglected). Then, to limit the peak current built up during Δt_{sw} to 25% of the peak resonant current, the required series inductance becomes

$$L_c = \frac{V_{dc} N \Delta t}{0.25 \cdot \hat{i}_p}, \tag{12}$$

which evaluates to L_c = 6 µH. Placing such series inductors, of course, reduces the leakage inductance budget for the main MFT further, or, alternatively, requires a reduction of the coupling capacitances with the limits discussed above. In addition, damping would be required at the resonance frequency of the circulating current loops, which is dominated by the series connection of a cell's two coupling capacitors and two series inductors. However, for the exemplary L_c and C_c, a resonance frequency of 29 kHz results, which is close to the operating frequency (f_s = 16 kHz) of the circuit. This renders the damping of oscillatory circulating currents without introducing high losses challenging.

C. DAB Instead of DCX Operation

Finally, the CC-SST could also operate as a dual active bridge (DAB) converter, which has been mentioned in [35] and then thoroughly analyzed for a capacitively isolated cascaded-cells LV system without any transformer in [37]. A DAB converter inherently requires an inductive series impedance in the ac link, i.e., the resonance frequency of the coupling capacitors and the series inductors, including the MFT's leakage inductance, must be far below the switching frequency and hence *both* elements can have large values. Advantageously, additional series inductance can be distributed to the cells as discussed above (L_c), but without impact on the sizing of the coupling capacitors.

The upper limit for the total effective series inductance

follows from the desired power transfer capability as [37]

$$L_{\mathrm{DAB}} = \frac{V_{\mathrm{out}}^2}{2\pi P_{\mathrm{nom}} f_{\mathrm{s}}} \varphi_{\mathrm{nom}} \left(1 - \frac{\varphi_{\mathrm{nom}}}{\pi}\right). \tag{13}$$

With a typical nominal phase shift of $\varphi_{\mathrm{nom}} = \pi/4$, $L_{\mathrm{DAB}} = 9.4\,\mu\mathrm{H}$ results. The series inductors of the cells are

$$L_{\mathrm{c}} = (L_{\mathrm{DAB}} - L_{\sigma}) \cdot \frac{N}{2}, \tag{14}$$

and thus, assuming $L_{\sigma} = 5\,\mu\mathrm{H}$ (about twice the low value required by the DCX operation), $L_{\mathrm{c}} = 33\,\mu\mathrm{H}$ results, i.e., a relatively high decoupling impedance between the converter cells. As shown in [37], the soft-switching mechanism of the DAB converter contributes to equal dc voltage sharing among the cells in spite of component tolerances or switching time mismatches (within certain limits) and therefore mitigates the source of the circulating current issue. Note further that during an LI test, the explicit series inductors would saturate and hence not adversely impact the voltage sharing between coupling elements and the main MFT discussed above in **Section II-D**.

Thus, **Fig. 6** shows simulated key waveforms of the CC-SST operating as a DAB converter with the aforementioned selection of L_{c}. The resonance frequency of $f_0 = 8.5\,\mathrm{kHz}$ is still relatively close to the switching frequency of $f_{\mathrm{s}} = 16\,\mathrm{kHz}$, which reflects in the primary current waveform's rounded top; a slightly larger coupling capacitance would result in the typical trapezoidal DAB current. The rms current stress of the coupling capacitor remains similar, but the series inductors contribute additional losses, which, to some extent, reduces the advantage of the CC-SST over the IC-SST.

IV. Comparative Evaluation

The IC-SST and the CC-SST topologies are largely equal except for the coupling elements, which facilitates a straightforward first comparison of volume and loss estimates. Based on typical data found for prototypes described in the literature [29], the following assumptions are made: The power electronic converter stages on the MV and on the LV side each have relative losses of 0.25% and a power density of $3\,\mathrm{kW/dm^3}$. The MFTs have relative losses of 0.5% and a power density of $7.5\,\mathrm{kW/dm^3}$; the (negligible) losses and the volume of the coupling capacitors have been calculated in **Section II-C**. Finally, the series inductors required for DAB operation are assumed to have half the losses and twice the power density of the coupling MFTs.

Using these admittedly very general estimates, **Fig. 7** compares the volumes and relative losses of the IC-SST and the CC-SST (for DCX and DAB operation); a more detailed quantitative comparison of the approaches is subject of future research. Clearly, all solutions feature similar volumes; the sensitivity on the assumptions regarding the power densities is low, as the power converter stages that contribute the major share of the volume are identical for all three variants. On the other hand, the CC-SST shows a clear efficiency gain of 0.25 percentage points compared to the IC-SST, which is a direct consequence of replacing coupling MFTs with coupling capacitors. This

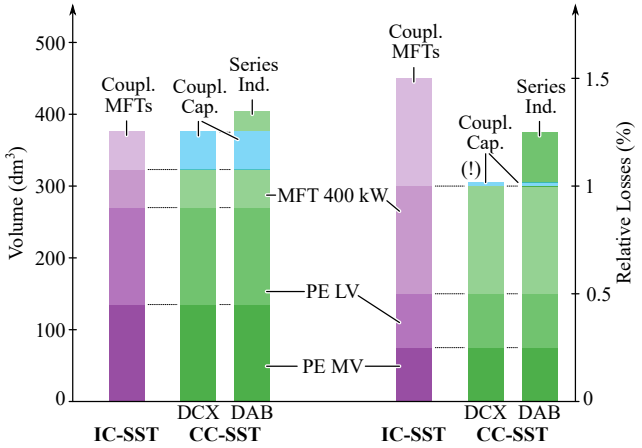

Fig. 7. Comparison of volume and loss estimates for the IC-SST (see **Fig. 1b**) and the CC-SST (see **Fig. 1c**) operated as DCX or DAB converter. Note that the loss contribution of the coupling capacitors is negligible in all cases.

advantage is reduced if DAB operation is considered instead of DCX operation. To prevent this, DCX operation should be used, which would require very precise timing of switching instants and, e.g., low-jitter gate drivers [48], i.e., increased complexity of the signal processing subsystems, as well as tight tolerances of the coupling capacitors. Alternatively, further countermeasures against the circulating current issue discussed in **Section III-B** should be explored.

V. Conclusion

The capacitively-coupled SST (CC-SST) topology features significant advantages over conventional SST topologies: first, there is only a single medium-frequency transformer (MFT) which must withstand lightning impulse (LI) surges but whose isolation is not subject to high MVdc stress during normal operation, which prevents potentially accelerated aging of dry-type insulation systems. Moreover, being rated at the full power, the overhead incurred by the isolation (e.g., bushings, etc.) remains limited. The capacitive isolation of the individual converter cells can be implemented using off-the-shelve film capacitors (lower implementation effort compared to isolation transformers, see **Fig. 1b**) with negligible losses. On the other hand, the direct coupling of several converter cells via a common ac link creates challenges, specifically the suppression of circulating currents that arise as a consequence of component tolerances or switching time mismatches. Future research should clarify and identify mitigation methods, compare operating modes, and also aim at a more detailed quantitative comparison against alternatives, such as the inductively-coupled SST (IC-SST), the conventional multicell topology, and, in particular, also single-MFT topologies based on modular-multilevel converter (MMC) structures.

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