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Abstract: **There is an increasing demand for three-phase mains interfaced high power EV chargers that provide a wide output voltage range while featuring low losses and a high power density. In this context, a synergetic control structure for a two-stage three-phase boost PFC rectifier with subsequent DC/DC buck stage was proposed, which allows to only switch one out of the three rectifier bridge legs, leading to switching loss savings of over 66 %. This is achieved by varying the voltage of the intermediate DC-link, which features a small capacitance, with six times mains frequency, always following the maximum three-phase mains line-to-line voltage. Although this concept has been proven to work correctly for ideal three-phase mains conditions, it is unclear whether it can safely operate under irregular three-phase grid conditions such as heavy harmonic distortions, unbalances, phase failures, and grid overvoltages caused by, e.g., lightning. Hence, after a short review of the employed synergetic control structure, this paper focuses on the operation of the proposed boost-buck converter for an application subject to a wide variety of three-phase grid disturbances. Comprehensive analysis with respect to irregular grid conditions is performed, resulting in a slight modification of the converter's front-end and its control structure in order to be able to handle faulty mains conditions. The proposed hardware and control modifications enabling the proper converter functionality under regular and irregular grid conditions are verified by circuit simulations. Finally, design guidelines are given for the hardware implementation of a resilient three-phase grid interfaced EV charger that can fulfill all required grid standards.**

I. Introduction

The proliferation of Electric Vehicles (EVs) results in a growing demand for EV chargers that can handle a wide output voltage range due to widely varying battery voltages used by different EV manufacturers. A typical high-power EV charging architecture comprises a medium voltage (MV) transformer, where non-isolated AC/DC converters are directly connected to individual sets of three-phase secondary-side windings [1].

In case of a transformer secondary line-to-line RMS voltage of 400 V and a widely varying battery voltage of 200-750 V [2], the non-isolated AC/DC converter has to feature boost and buck capability, in order to allow an adaption of the transformer output voltage to the EV battery voltage level.

In **Fig. 1**, the conventional two-stage solution of such a non-isolated AC/DC converter system is shown. It consists of a boost-type three-phase PFC rectifier front-end, generating a constant intermediate DC-link voltage u_{pn} in between $U_{\mathrm{ll,max}}$ and $U_{\mathrm{o,max}}$, according to the required momentary output voltage U_{o}, where $U_{\mathrm{ll,max}}$ and $U_{\mathrm{o,max}}$ denote the maximum grid line-to-line voltage and the maximum required output voltage, respectively. This stage is followed by a subsequent DC/DC buck converter that regulates the output voltage in case of $U_{\mathrm{o}} < U_{\mathrm{ll,max}}$. Consequently, a wide output voltage range can be covered. However, especially during *buck mode* operation, i.e., when the output voltage U_{o} is below the instantaneous maximum line-to-line voltage $u_{\mathrm{ll,max}}$, the maximum achievable efficiency is clearly limited by the two-stage energy conversion of such EV charger systems. Hence, in order to reduce the converter losses during this operating mode, a so-called *synergetic* control strategy was presented in [3]–[5], that allows to only switch one of the three rectifier stage bridge-legs.

The synergetic control of the three-phase boost PFC rectifier and the subsequent buck stage can directly be applied to the two-stage topology shown in **Fig. 1**, hereafter referred as the Boost-buck Voltage Source Rectifier, Bb-VSR. However, a smaller DC-link capacitor C_{pn} has to be used, such that instead of generating a constant intermediate DC-link voltage, during buck operation ($U_{\mathrm{o}} < u_{\mathrm{ll,max}}$), the capacitor voltage u_{pn} can be controlled by the subsequent DC/DC converter to always follow the instantaneous maximum line-to-line voltage $u_{\mathrm{ll,max}}$. Consequently, the high-side switch of the PFC rectifier stage half-bridge with the most positive phase voltage and the low-side switch of the half-bridge with the most negative phase voltage can be continuously turned-on within a 60°-wide interval (cf. $1/3$ in **Fig. 2**). The input currents of the phases with the most positive and negative voltages are then controlled by u_{pn}, which in turn is controlled by the subsequent DC/DC buck converter. Hence, only the input half-bridge corresponding to the medium input phase voltage has to be pulse-width modulated in order to control the corresponding input current, which means that only one out of the three PFC rectifier bridge-legs, and/or the bridge leg carrying the lowest current is switching at any point in time ($1/3$ operation).

However, when the output battery voltage is higher than the instantaneous maximum line-to-line voltage ($U_{\mathrm{o}} > u_{\mathrm{ll,max}}$), i.e. for *boost mode*, the three-phase PFC rectifier steps up the input voltage by switching either two or three of its bridge-legs ($2/3$ or $3/3$ operation, and/or Discontinuous or Continous PWM [6]), such that the constant DC-link voltage equals the battery voltage ($u_{\mathrm{pn}} = U_{\mathrm{o}}$), and the buck stage is clamped by turning its high-side switch on.

A cascaded control scheme for the Bb-VSR, similar to the one in **Fig. 1**, was initially presented in [5] focusing mainly on buck mode operation, i.e., $U_{\mathrm{o}} < u_{\mathrm{ll,max}}$, and proved to work correctly for ideal mains conditions. A demonstration of the operation of the Bb-VSR under ideal mains conditions is shown in **Fig. 2**, where in extension of [5] also a smooth transition of the output voltage U_{o} between buck and boost mode operation is obtained. All presented simulations are considering a system of 10 kW rated power.

Given that the Bb-VSR operates at the modulation index limit, there is no DC-link voltage margin that would allow to control the input current in case of a grid overvoltage. Moreover, a small DC-link capacitance is required by the synergetic control (unlike conventional boost converters, where typically a relatively large capacitance is present in the DC-link [7]), whose voltage reacts

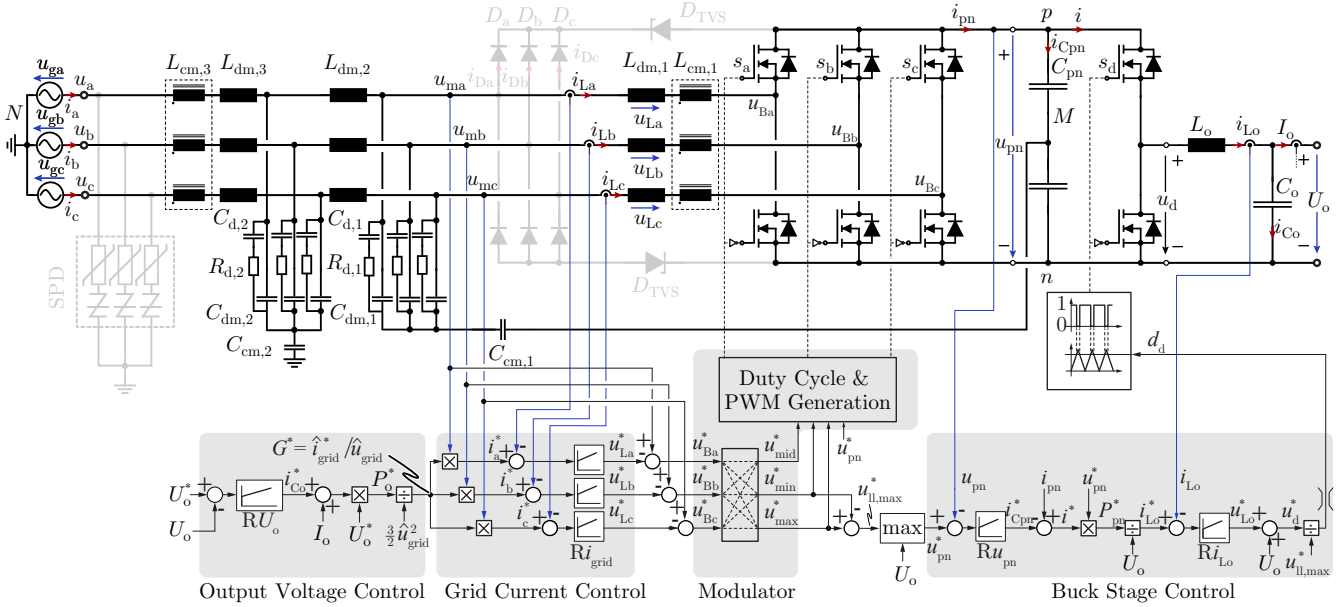

Fig. 1. Cascaded output voltage control structure for the Bb-VSR, where the required measurements are indicated in blue. The voltages across the capacitors C_{dm1} are measured ($u_{ma,mb,mc}$) and used as phase voltages in the control.

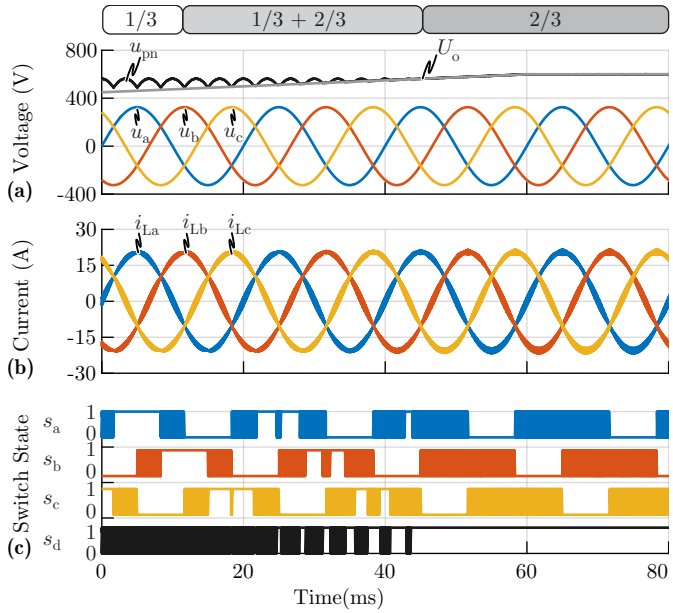

Fig. 2. Simulation of the characteristic waveforms of the Bb-VSR: **(a)** the input grid voltages $u_{a,b,c}$ (measured at the converter input, between line to ground), intermediate DC-link voltage u_{pn}, output battery voltage U_o and **(b)** boost inductor currents $i_{La,Lb,Lc}$, **(c)** gate signals of the three-phase PFC rectifier stage and the buck stage. The main simulation parameters are: switching frequency 140 kHz (for both converter stages), C_{pn}=10 µF, L_o=100 µH and C_o= 5 mF (to emulate the behaviour of batteries), for other components refer to **Table II**. When $U_o < u_{ll,max}$, only one of the PFC rectifier bridge-legs is operating at any point in time (1/3 operation) together with the buck stage bridge-leg. When $U_o > u_{ll,max}$, the high-side switch of the buck stage is clamped, and two out of three rectifier stage bridge-legs are switching (2/3 operation, also known as Discontinous PWM [6])

sharply to inrush currents. Hence, the question arises if this is a feasible solution when operated in a grid with unbalanced three-phase voltages, harmonic distortions, and voltage surges caused by, e.g., lightning, which could cause permanent damage to the hardware.

Hence, in this paper, a comprehensive approach is taken for both the topology and the control structure, to analyze its robustness under irregular three-phase mains conditions, as this is essential to the applicability of the proposed system as an EV charger. The most important critical grid conditions for three-phase rectifiers are summarised in **Section II** and are discussed based on related standards. Subsequently, the Bb-VSR and its control structure are tested by means of simulations for a selection of the most critical grid irregularities: harmonics in **Section III**, voltage dips and phase voltage interruptions in **Section IV**, and overvoltages in **Section V**, verifying that the proposed approach with the corresponding modifications is indeed suitable for ensuring reliable operation. Furthermore, **Section V** provides design guidelines for the resilient design of an overvoltage clamping circuit, which are also useful for conventional boost-type grid-connected three-phase PFC rectifiers. Finally, conclusions are drawn in **Section VI**.

II. Overview of the Immunity Requirements in Standards for Power Supplies Under Irregular Grid Conditions

The standards of immunity requirements [8]–[11] specify different irregular grid conditions that power supplies need to withstand, among which the IEC standards are mainly used in European countries, while similar IEEE standards are widely applied in North America. In this paper, the IEC standards will be used to evaluate different critical conditions. As the Bb-VSR is mainly designed for charging applications, the standards dedicated for this purpose will be considered here [8,9].

The grid faults mentioned in [8,9] can be classified into two main categories: voltage dips and interruptions, and overvoltages. In addition, there are also standards specifying immunity requirements for harmonic distortions of the three-phase grid voltages [12,13], which, however, are not mandatory for EV chargers. Nevertheless, they are widely applied for equipment in medical and semiconductor industry applications, and are required to be considered for equipment containing phase-controls or other zero-crossing detection techniques [10], which is the case for 1/3 operation of the rectifier stage. Therefore, they are considered in this paper as well. **Table I** summarizes the classification of all considered irregular grid conditions. In order to evaluate the immunity capability of the equipment under test (EUT), three performance criteria are defined: A (normal performance), B (degradation of performance during

TABLE I
CLASSIFICATION OF IRREGULAR GRID CONDITIONS AND IMMUNITY REQUIREMENTS FOR EV CHARGERS

Phenomenon		Standards (IEC 61000-)	On-Board Charger	Off-Board Charger	Performance Criteria
Harmonics		2-4, 4-13	×	×	/
Voltage Dips & Interruptions	Voltage Dips	4-11 (phase current < 16 A) 4-34 (phase current > 16 A)	×	✓	B
	Interruptions		×	✓	C
	Voltage Variations		×	×	/
Overvoltages	Voltage Surge	4-5	✓	✓	B
	Fast Transients or Bursts	4-4	✓	✓	B
	Oscillatory Overvoltages	4-12, 4-18	×	×	/

TABLE II
COMPONENT VALUES FOR THE CONSIDERED EMI FILTER

Component	Parameter	Component	Parameter
$L_{dm,1}$	163.5 µH	$C_{dm,1}$	850 nF
$L_{cm,1}$	2.9 mH	$C_{cm,1}$	87 nF
$C_{d,1}$	212 nF	$R_{d,1}$	66.1 Ω
$L_{dm,2}$	29 µH	$C_{dm,2}$	2.1 µF
$C_{d,2}$	517 nF	$R_{d,2}$	17.8 Ω
$C_{cd,2}$	5 nF	$R_{cd,2}$	199 Ω
$L_{dm,3}$	11.7 µH	$L_{cm,3}$	2 mH

the test is allowed, automatic recovery required), and C (loss of function is allowed, restored by simple operations). These criteria are specified in **Table I** for each aforementioned grid irregularity. Depending on the location of the charger (on-board or off-board), the requirement is different, which is indicated with "✓"(obligatory) or "×"(not obligatory) for each test. The detailed test procedures are specified in the IEC61000-4 series, which will be discussed and simulated in the following sections for all three main categories of grid irregularities (harmonics, voltage dips and interruptions, and overvoltages).

However, in order to get conclusive results from the simulations of the irregular grid conditions, not only should the aforementioned two converter stages be taken into account, but also the upstream EMI filter needs to be considered. This is especially important for abrupt changes in the grid voltages, as the EMI filter defines the transient behavior of the total converter system to a large extent. Thus, an EMI filter is placed in front of the converter, using the same structure and component values as in [14], which are repeated in **Table II**. The noise level is verified to comply with CISPR Class A EMI requirements. To take into account the effects of inrush currents, the inductors in the EMI filter, except for $L_{dm,1}$ and $L_{cm,1}$ which are protected by the bypass diodes ($D_{a,b,c}$), are simulated with the reluctance models using saturable cores [15]–[18], with saturation characteristics extracted from measurements. As a reference, $L_{dm,2}$ and $L_{dm,3}$ drop to 50% of the nominal value at 45 A and 30 A respectively, while $L_{cm,3}$ drop to 50% of the nominal value at 110 A differential mode current or 150 mA common mode current.

III. MAINS VOLTAGE HARMONICS

There are two relevant standards concerning grid voltage harmonics: one specifies the compatibility levels [12], and the other one specifies the immunity levels [13]. The given test voltage levels of both standards are summarized in **Table III** for the first five odd non-multiple-of-three harmonics. The test levels for compatibility are lower than the respective test levels for immunity, but in contrast to the immunity test levels, where the standard specifies two particular ways to combine the harmonics, the compatibility test levels can be combined arbitrarily (regarding mutual phase shifts) in order to test the worst-case scenario. As for $1/3$ operation, it is crucial to ensure the automatic clamping of the required phases with the respective highest and lowest voltage values in all operating conditions. Thus, a worst-case grid voltage waveform is created, where the phase voltages $u_{a,b,c}$ intersect three times every 60° (cf. **Fig. 3**). Hence, the clamped phase changes three times instead of only once every 60°, as in nominal operation. This waveform was created by superimposing the 5th, 7th, 11th, 13th and 17th voltage harmonics to the 50 Hz fundamental voltage component, with the maximum amplitudes specified in [12] and phases specifically chosen to create a repeating cross-over between the phase voltages. Accordingly, in order to still achieve a resistive input behavior of the EV charger, the intermediate DC-link voltage u_{pn} has to be able to follow the maximum instantaneous (distorted) line-to-line voltage. **Fig. 3** shows the simulated waveforms of u_{pn} and the resulting input phase currents $i_{a,b,c}$. It can be seen that the DC-link voltage controller dynamics is high enough and ensures an ohmic behavior of the EV charger.

TABLE III
TEST LEVELS FOR HARMONICS

Order	Compatibility Test levels% U_n	Immunity Test levels% U_n
5	8	12
7	7	10
11	5	7
13	4.5	7
17	4	6
...	...	...

IV. MAINS VOLTAGE DIPS AND INTERRUPTIONS

Voltage dips and short interruptions originate primarily from short circuits or sudden large load steps in the network [19,20]. This kind of fault is classified into three sub-categories [19,20]: voltage dips, interruptions, and voltage variations. Voltage dips refer to one-phase voltage dips, including line-to-line dips and line-to-neutral dips, whereby the latter is obviously not required for power supplies without a neutral connection. Interruptions stand for the dropout of all three phases at the same time, lasting for 250 (50 Hz) or 300 (60 Hz) cycles. During this time interval, the converter does not have to continue working. As it is similar to the start-up process, this test will not be further discussed here. The third phenomenon, voltage variations, represents the voltage sag of all three phases happening simultaneously by the

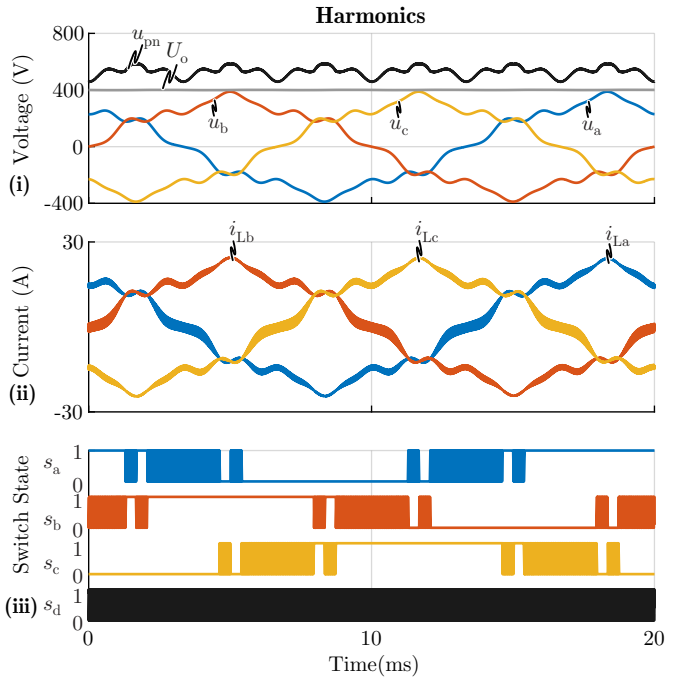

Fig. 3. Simulation waveforms for voltage harmonics occurring in the three phases: **(i)** grid phase voltages $u_{a,b,c}$ (measured at the input of converter, from line to ground), intermediate DC link voltage u_{pn}, and output voltage U_o (controlled to 400 V), **(ii)** currents $i_{La,Lb,Lc}$ in the boost inductors of the PFC rectifier stage and **(iii)** gate signals of the three-phase PFC rectifier and the buck stage.

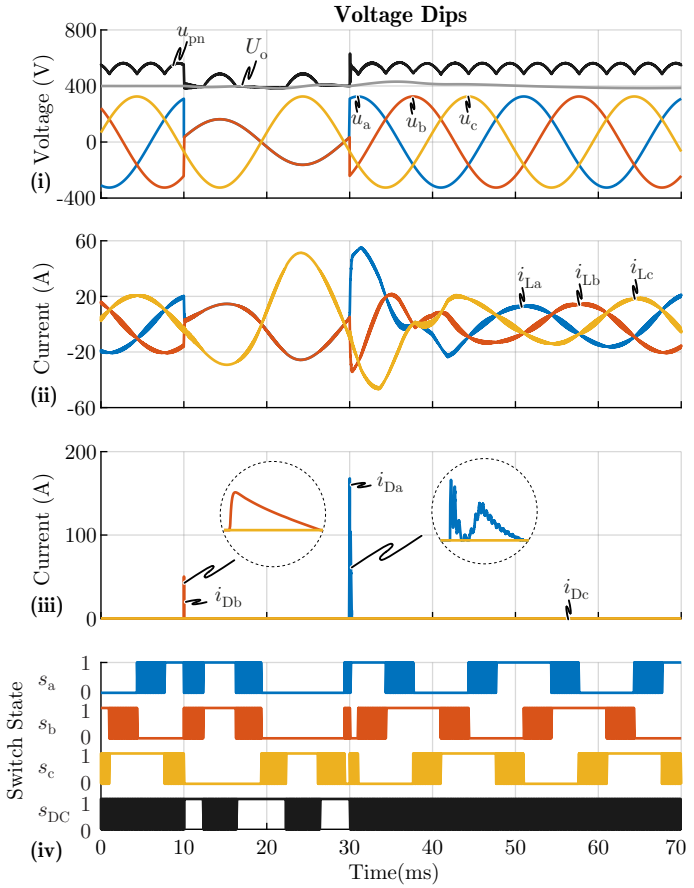

Fig. 4. Simulation waveforms for phase-to-phase voltage dip occurring from phase *a* and *b*: **(i)** grid phase phase voltages $u_{a,b,c}$ (measured at the input of converter, from line to ground), intermediate DC link voltage u_{pn}, and output voltage U_o (controlled to 400 V), **(ii)** currents $i_{La,Lb,Lc}$ in the boost inductors of the PFC rectifier stage, **(iii)** currents in the upper bypass diodes of $D_{a,b,c}$, **(iv)** and gate signals of the three-phase PFC rectifier and the buck stage.

same amplitude, usually caused by continuously varying loads connected to the network [19,20]. The preferred test level is 70% of the nominal voltage, with a voltage fall time of 1 µs to 5 µs, staying at the reduced voltage for one cycle and then gradually going back to normal during 25 cycles. It needs to be noted that this test is not obligatory. Moreover, it does not entail extra challenges for the proposed synergetic Bb-VSR, i.e., the converter which survives the voltage dip tests can also pass the voltage variation tests. Therefore, this grid irregularity will not be further discussed here.

For the following simulations of the voltage dips, the test generator is directly connected to the EUT, and maintains low output impedance over the fault. Therefore, to consider the worst-case scenario, the grid impedance is not included (which would further limit the inrush currents in a real installation), and the inrush currents are only limited by the EMI filter. Furthermore, it is assumed that the fault occurs at the peak of the line-to-line voltage.

The voltage dip tests should be performed for each phase-to-neutral voltage (when a neutral conductor is present) and phase-to-phase voltage. The preferred test levels and duration of class 3 (highest level, harshest environment, for 50 Hz mains frequency) are: 0% during $^1/_2$ cycle, 0% during 1 cycle, 40% during 10 cycles, 70% during 25 cycles and 80% during 250 cycles. The rise and fall times are between 1 µs to 5 µs. As for $^1/_3$ operation, it is especially important to see how the controller reacts for a phase-to-phase voltage dip to 0%, when two phases have the same voltage and there is no phase with a voltage in between (which would be high-frequency modulated in normal operation). Thus, the 0% line-to-line voltage dip between phase *a* and *b* is simulated and shown in **Fig. 4**. There are two acceptable methods presented in [19,20] to perform the voltage dip tests as shown in **Fig. 5**, and the more realistic one [19,20] (method 2) is chosen for the simulation in **Fig. 4**. It can be noted that, using this method for the 0% line-to-line voltage dip test, both the amplitude and the phase of the affected two voltages (u_a and u_b) change when the fault happens, ending up in the same resulting vector, which is 180° phase-shifted with respect to the remaining phase voltage (u_c), as can be seen in **Fig. 4(i)**.

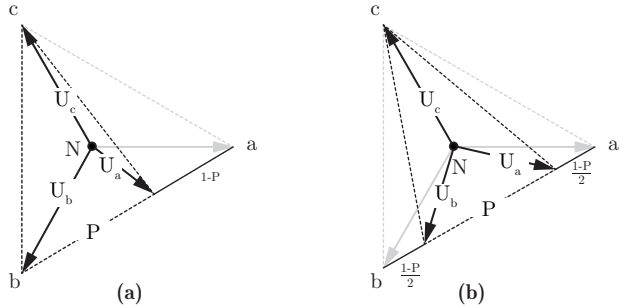

Fig. 5. Phasor diagrams for phase-to-phase voltage dip between phase *a* and *b*, where P is the relative amount of the remaining u_{ab}: **(a)** method 1 (easier to realize in test labs [20]), **(b)** and method 2 (more realistic [20], simulated in **Fig. 4** for P = 0).

According to the control structure of **Fig. 1**, the reference voltage u^*_{pn} is defined as the maximum of the output voltage U_o and the maximum line-to-line input voltage reference $u^*_{ll,max} = u^*_{max} - u^*_{min}$, which in turn is generated from the rectifier voltage references (u^*_{Ba}, u^*_{Bb} and u^*_{Bc}). Thus, due to the loss of u_{ab}, the maximum line-to-line voltage ($u_{ac} = u_{bc} = -^3/_2 u_c$) no longer features a six-pulse shape, but instead varies with twice the mains frequency. Since it reaches zero every half mains

cycle, it inherently intersects with U_o, whereby the converter always alternates between buck and boost mode operation. Since the controller is designed to ensure the emulation of an ohmic load, the currents in three phases are changing in the same way as the voltages. However, the converter still manages to draw sinusoidal currents from the mains, as shown in **Fig. 4(ii)**. It needs to be noted that, as there is no voltage in between u_{max} and u_{min}, when u^*_{pn} is set to follow $u^*_{ll,max}$, all three half-bridges in the rectifier stage are clamped. This proves the proper operation of the clamping function even under fault conditions.

Furthermore, due to the pulsating input power with twice the mains frequency, the output voltage starts to fluctuate. With the high bandwidth of the output voltage control, the controller would try to correct this low-frequency ripple in the output voltage, leading to distortions in the input phase currents. Accordingly, there is a trade-off between keeping currents sinusoidal and the fast control of the output voltage [21] and/or the amount of installed output capacitance C_o.

During the fault, u^*_{pn} is set by the controller to U_o when $u^*_{ll,max} < U_o$. Hence, when the voltage steps back to its nominal value, there will be a large voltage difference between the instantaneous maximum line-to-line voltage $u_{ll,max}$ and u_{pn}, especially when U_o is low and $u_{ll,max}$ is high. Since u_{pn} inherently follows $u_{ll,max}$, the controllability of the input currents is temporarily lost, generating a large inrush current, which is only limited by the EMI filter. To prevent these large inrush currents from flowing through the semiconductors and therefore, potentially damaging them, bypass diodes $D_{a,b,c}$, which can handle such surge currents have to be placed between the grid interface and the input of the converter, as shown in **Fig. 1**. Similar measures are used for the protection of single-phase PFC rectifiers at the end of a hold-up period [7]. It can be seen in **Fig. 4(iii)**, that when the voltage comes back, the inrush current up to 170 A (i_{Da}) flows through the bypass diodes instead of the less robust MOSFETs. With an appropriate selection of the bypass diodes, as e.g. *P*600*M* [22] with a surge current capability of 600 A for 8.3 ms, the Bb-VSR can survive the voltage dip test.

In buck mode, u_{pn} closely follows the line-to-line voltage. For the considered power rating and a realization using SiC MOSFETs, the voltage drop across the first stage of the EMI filter (L_{dm1} and L_{cm1}) and the MOSFETs can easily reach 2 V∼3 V (during clamping), which is higher than the forward voltage drop of most diodes. Therefore, it is likely for the bypass diodes $D_{a,b,c}$ to conduct at normal operation, making it difficult to control the grid currents. Therefore, in order to ensure that these diodes are blocking in nominal operation, transient-voltage-suppression (TVS) diodes (D_{TVS}) with a higher breakdown voltage of 5 V are placed in the bypass path, which can easily withstand surge currents of hundreds of amperes (e.g., *SMCJ*5.0*A-TR* from STMicroelectronics [23]).

V. Overvoltages

There are mainly two kinds of overvoltages that can occur in a grid [24]: oscillatory and impulsive overvoltages. The oscillatory overvoltages result from, e.g., capacitor bank energization, whereby the impulsive overvoltages are usually caused by lightning strikes. As shown in **Table I**, it is obligatory for power supplies to withstand two different kinds of impulsive overvoltages, as defined in [25] and [26,27]. The first one, referred to as *surge*, features voltage pulses in the microsecond range, while the second one, referred to as *fast transients or bursts*, is in the nanosecond range. Due to the short duration and low energy of the latter one, a converter that survives the voltage surge, should also survive fast transients or bursts at the same voltage level.

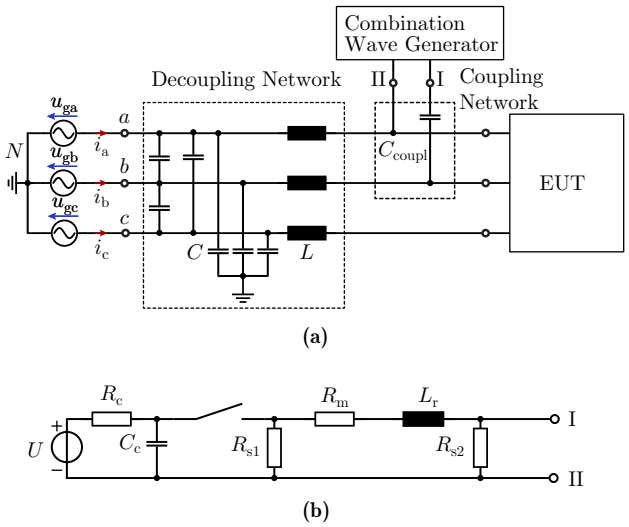

Fig. 6. Test setup for surge immunity tests with **(a)** connections of the three-phase voltage source, decoupling network ($C = 30\,\mu F$, $L = 1.5\,mH$), combination wave generator (CWG), coupling network (a $18\,\mu F$ capacitor C_{coupl} for line-to-line tests, or a $9\,\mu F$ capacitor C_{coupl} in series with a $10\,\Omega$ resistor for line-to-ground tests), and the EUT, **(b)** the schematic of the CWG ($R_c = 1000\,\Omega$, $C_c = 9.98\,\mu F$, $R_{s1} = 9.39\,\Omega$, $R_m = 0.83\,\Omega$, $L_r = 10.7\,\mu H$, $R_{s2} = 25.5\,\Omega$).

Therefore, in the following sections, only the surge voltage pulse tests will be analyzed. The test levels are shown in **Table IV** for both line-to-line tests (L-L) and line-to-ground tests (L-G), depending on the environment and the charger type.

Table IV
Overvoltage Test Levels

Charger type	Location	Test Level L-L	Test Level L-G
On-board	/	1 kV	2 kV
Off-board	Residential		
	Other than residential	2 kV	4 kV

A. Test Setup

The required test setup is shown in **Fig. 6(a)** [25]. The combination wave generator (CWG) [28], which is used for generating the voltage pulses, is connected to the EUT through the coupling network. The line-to-line surge tests require a coupling capacitor C_{coupl} of $18\,\mu F$, while the line-to-ground surge test requires a $9\,\mu F$ coupling capacitor in series with a $10\,\Omega$ resistor. The decoupling network [29], comprising inductors and capacitors, is placed in front of the CWG to prevent its high current and voltage from damaging the three-phase voltage source. The schematic of the CWG is shown in **Fig. 6(b)**. The voltage surge is generated by releasing the energy in the precharged capacitor C_c. Hence, after the electronic switch is turned on, the output voltage of the CWG rises to the required peak value (test level) in $1.2\,\mu s$, before decaying to half of its peak value within the following $50\,\mu s$. Due to different configurations of the coupling network, the current sourcing capability of the CWG is different in line-to-line and line-to-ground tests. Even though the line-to-ground tests specify higher voltage, their short-circuit currents are much lower than for the line-to-line tests.

B. Simulation Results for On-Board Chargers and Residential Off-Board Chargers Without Surge Protection Devices (SPDs)

The simulations are first carried out for voltage impulses at lower test levels, i.e., a line-to-line voltage surge of 1 kV between phases *a* and *b*, and a line-to-ground voltage surge of 2 kV between phase *b* and ground. In this first simulation, no

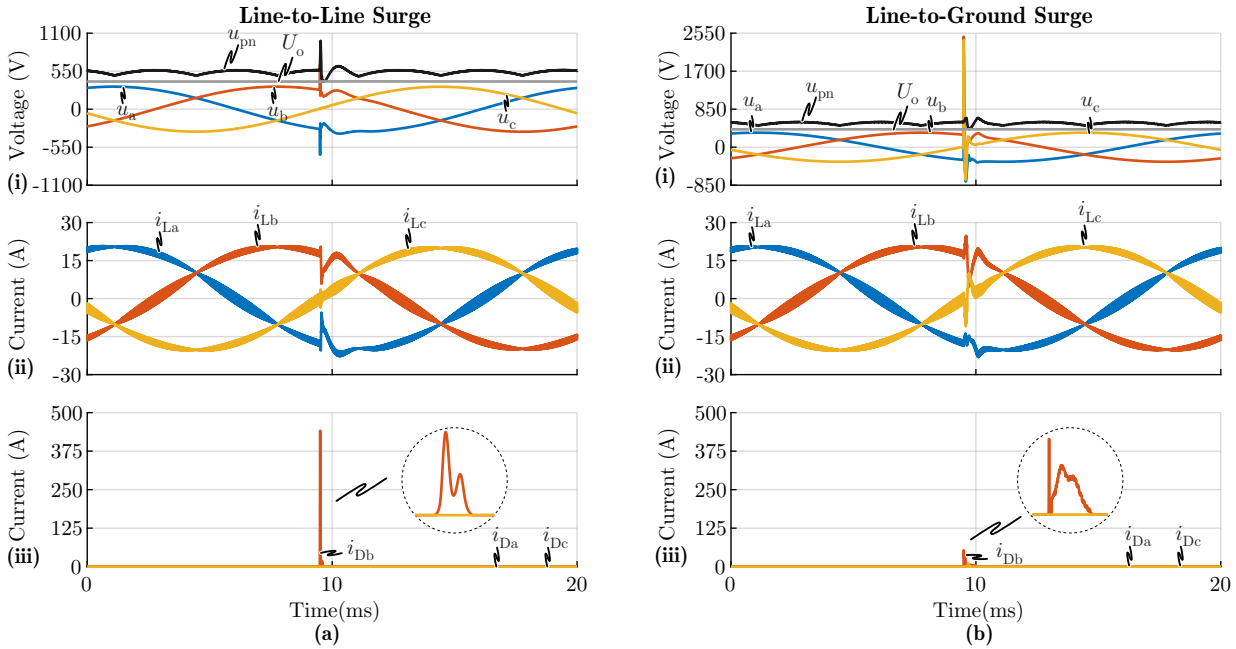

Fig. 7. Simulation waveforms for **(a)** line-to-line surge test at 1 kV, applied between phase *a* and *b* and **(b)** line-to-ground surge test at 2 kV, applied to phase *b*: **(i)** grid phase voltages $u_{a,b,c}$ (measured at the input of the converter, from line to ground), intermediate DC link voltage u_{pn}, and output voltage U_o (controlled to 400 V), **(ii)** currents $i_{La,Lb,Lc}$ in the boost inductors of the PFC rectifier stage, **(iii)** currents in the upper bypass diodes of $D_{a,b,c}$. No SPDs are considered.

surge protection devices (SPDs) are employed and the EUT is simulated as it is. The simulation results of both tests are shown in **Fig. 7**, where the phase voltages $u_{a,b,c}$ are measured at the input of the converter (EUT) between each phase and ground. As shown in **Fig. 7(a.i)**, the maximum u_{pn} in the line-to-line surge test reaches 1000 V. As the rectifier of the Bb-VSR is based on 1200 V SiC MOSFETs, this stage can survive the overvoltage due to the voltage surge without being damaged.

For a line-to-ground fault, u_{pn} reaches only 600 V, as the surge current provided by the CWG is much smaller compared to the line-to-line test setup. Though, the three phase voltages $u_{a,b,c}$ with respect to the ground are quite high, owing to the small capacitance between line and ground (e.g. C_{cm2} and parasitic capacitance). In **Fig. 7(a)(b)**, it can be seen during both tests, that most of the surge currents flow through the bypass diodes and not through the switches, whereby the diodes effectively protect the switches from being destroyed. Even though the maximum surge current reaches 450 A, it is still within the ratings of the chosen diodes, which is why it can be concluded that even though the intermediate DC link capacitor C_{pn} is comparably small, the Bb-VSR can still survive overvoltages as specified in the standards for low surge levels. However, it can also be inferred that, if the higher test level would be applied, as required for non-residential off-board chargers, u_{pn} would easily go beyond 1200 V. Consequently, under this circumstance, surge protection devices are inevitable, which will be discussed in the following sections.

C. Recommended Applications of the SPDs

Star Connection of SPDs in three-phase power supplies is highly recommended in [30], as shown in **Fig. 1.** Whether it is necessary to connect an extra SPD between the neutral and ground point depends on the configuration of the connected low voltage (LV) network. It is recommended to install this SPD, if the distance between the converter and the PE-N bonding point on the grid side is above 10 m [30]. As the extra SPD connecting the neutral and the ground mainly affects the line-to-ground voltage instead of the line-to-line voltage, it has no effect on u_{pn} in case of a fault, and therefore has no impact whether the converter will be damaged or not. Therefore, for simplicity reasons, the TN-C network, where a combined PEN conductor is applied [31,32], is used here as an example.

Voltage Ratings of SPDs are selected based on the breakdown voltage of the equipment and the maximum continuous operating voltage (U_c) of the grid. It is recommended to have a protection level 20% lower than the breakdown voltage of the employed power semiconductors. Hence, for the considered Bb-VSR with 1200 V devices, the clamping voltage should be lower than 960 V. Another important parameter is the maximum continuous operating voltage of the SPDs, denoted as $U_{c,SPD}$. To prevent the SPDs from being triggered under normal operating conditions, $U_{c,SPD}$ has to be higher than the maximum continuous operating voltage U_c of the grid. It is specified that the temporary overvoltages U_{TOV} in the grid, which last longer than 5 s, should be considered as the continuous operating voltage [30], which is around 30% to 50% higher than the nominal voltage for the considered LV grid. Therefore, it is recommended to select $U_{c,SPD}$ to be 50% higher than the nominal system voltage (RMS). For the considered LV network with a RMS line-to-neutral voltage of 230 V, $U_{c,SPD}$ should be selected to be around 345 V.

D. Selection of the Surge Protection Devices

Varistors are widely used for overvoltage protection due to their low price and simplicity in terms of application. However, their use comes with the disadvantage of a relatively high clamping voltage, as e.g. for a varistor with a U_c of 350 V, the final clamping voltage is usually around 900 V. Considering the star connection of the three phase voltages, the maximum line-to-line voltage, which would be applied on u_{pn}, could go beyond 1200 V and, therefore, destroy the switches. Thus, it is not safe to use varistors with high U_c. One option would be to choose varistors with lower U_c, if the connected LV network is not subject to high U_{TOV}. However, alternative solutions need to be considered in a harsher environment.

Transient-Voltage-Suppression (TVS) Diodes would be such an alternative choice, as they react much faster on overvoltages than varistors and are behaving like Zener diodes,

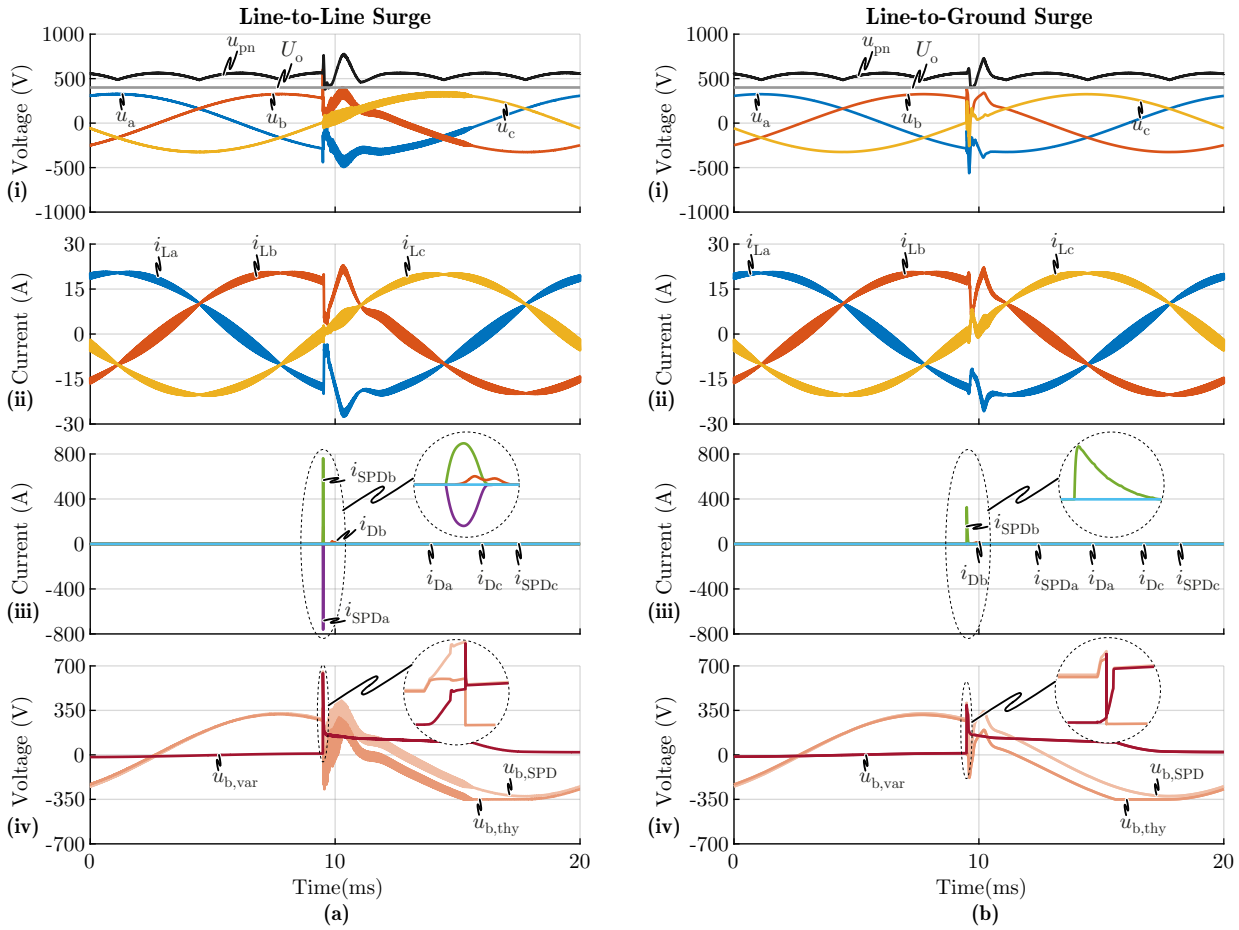

Fig. 8. Simulation waveforms for **(a)** line-to-line surge test at 2 kV, applied between phase *a* and *b* and **(b)** line-to-ground surge test at 4 kV, applied to phase *b*: **(i)** grid phase voltages $u_{a,b,c}$ (measured at the input of converter, from line to ground), intermediate DC link voltage u_{pn}, and output voltage U_o (controlled to 400 V), **(ii)** currents $i_{La,Lb,Lc}$ in the boost inductors of the PFC rectifier stage, **(iii)** currents in the upper bypass diodes of $D_{a,b,c}$, and **(iv)** varistor voltage $u_{b,var}$, thyristor voltage $u_{b,thy}$ and the total SPD voltage $u_{b,SPD}$ of phase *b* (cf. **Fig. 1**).

clamping to their breakdown voltage in case of overvoltages. However, high-voltage and high-current TVS diodes are usually very expensive.

Two-Stage Protection is a second possibility which is also considered in literature [30]. The first stage is usually a varistor with a high U_c, followed by a second stage consisting of a TVS diode with a lower current handling capability and a lower clamping voltage as well. As an inductor is used to connect the first and the second stage of this SPD design, it is clear that this solution is usually quite bulky compared to the previous approaches.

Varistors Combined with Surge Protection Thyristors are considered in [33], which achieve a low clamping voltage and a high U_c, with reasonable cost and are therefore considered as the most promising solution for the application at hand. The surge protection thyristor is a switching type SPD, i.e., its impedance is very high when no surge is present, but can drop to a low value relatively fast in case of a voltage surge. The internal structure can be found in [34]. As a switching type SPD, it can be modeled using a normal thyristor with a Zener diode controlling its gate [35]. Thus, when there is a voltage surge, the Zener diode breaks down and a gate current results, providing a firing pulse for the thyristor. When the voltage surge is gone and the current in the thyristor decreases below the threshold, it will turn off automatically. Based on the voltage ratings discussed in the last section, an appropriate varistor ($V20E130P$, U_c at 130 V [36]) and surge protection thyristor ($P3500SDLRP$, U_c at 320 V [37]) can be selected, both from *Littelfuse*. LT spice models of the chosen devices can be found in [38] and were used to extract the parameters of the SPDs, such that they can be modeled properly in a system-level simulation. According to the datasheet values, the parasitic capacitance of the varistor (1900 pF) is much higher than the one of the thyristor (65 pF), whereby during regular operation and the rising edge of the voltage surge, most of the voltage is directly applied to the surge protection thyristor, which is crucial for the combined varistor/thyristor circuit to function as intended. Moreover, the leakage current at the nominal voltage (10 µA for the varistor and 5 µA for the thyristor) implies a slightly larger off-state resistance of the surge protection thyristor, whereby in steady-state, most of the voltage is applied across the thyristor, preventing the low-voltage varistor from being triggered in normal operation. In case of a voltage surge, the thyristor is therefore triggered first, whereby all the surge voltage is then applied across the varistor, which finally clamps at a rather low voltage level. However, as the parasitic values of the devices may vary in reality, extra resistors and capacitors should be used in parallel to the SPDs, in order to ensure the aforementioned coordination between the varistor and the surge protection thyristor.

E. Simulation Results with SPDs

The simulation results for a line-to-line surge voltage of 2 kV and a line-to-ground surge voltage of 4 kV are shown in **Fig. 8.** With the SPDs diverting the surge energy, the peak value of u_{pn} is much smaller compared to **Fig. 7**, reaching 800 V in the line-to-line surge test and 730 V in the line-to-ground test, even though the test level is higher. The clamping process is shown

in detail in **Fig. 8(a.iv)(b.iv)** based on the voltages across the varistor $u_{\mathrm{b,var}}$, the thyristor $u_{\mathrm{b,thy}}$ and the total SPD $u_{\mathrm{b,SPD}}$ for phase b, where the positive terminal of the CWG is connected to. It can be noted that, most of the surge voltage is applied to the thyristor first, and when it breaks down at around 350 V, the total voltage drops as well since there is not enough current charging the parasitic capacitance of the varistor. Then as the current increases, the voltage $u_{\mathrm{b,var}}$ across the varistor increases as well and finally is clamped at 370 V. When the surge voltage is gone, $u_{\mathrm{b,var}}$ will not drop to zero immediately due to the lack of negative current discharging its parasitic capacitance. Owing to $u_{\mathrm{b,var}}$, the thyristor will reach its breakdown voltage in another direction afterwards. At this point, the negative current will increase slightly and the varistor parasitic capacitance will be discharged to nearly zero. It needs to be noted that the thyristor will not break down as the discharging current is not large enough for the firing pulse, which is in the range of a few hundred milliamperes [37].

The maximum current through the SPDs is lower than 800 A and lasts less than 20 µs, which is within the ratings of the selected SPDs. The maximum current through the bypass diodes is 160 A, which is also within its surge current rating. For the line-to-line surge voltage, the current flows into one phase, then coming back through another phase, so there are two branches of SPDs in the surge current path, leading to higher total clamping voltage than in the line-to-ground test, where only one SPD branch is activated.

Therefore, it can be concluded that the SPD network works for both types of voltage surges. With the previous discussions, the Bb-VSR is proved to be capable of withstanding the required grid irregularities, including harmonics, voltage dips and interruptions, and overvoltages, and hence can be utilized in real-world applications.

VI. Conclusions

In this paper, a synergetic control structure for a Bb-VSR is analyzed, that allows for significant loss savings in the PFC rectifier stage and features wide DC output voltage range and at the same time, guarantees the continuation of converter operation for a wide variety of grid disturbances and irregularities, which need to be considered in EV charger applications. A review and summary of the low-voltage (LV) grid standards are provided, and the test methods for irregular grid conditions are described. The critical grid conditions are identified, and it is shown that a safe operation is ensured for all critical grid conditions, by means of either appropriate control of the converter, or additional protection circuitry. Moreover, current spikes following grid voltage steps or grid voltage surges are analyzed in detail, including the behavior of the EMI filter components under such conditions. Based on this analysis, a comprehensive guideline for the selection of overvoltage protection circuits and elements is derived.

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