Power Electronic Systems
Laboratory

Proceedings of the Conference on Power Electronics and Intelligent Motion (PCIM Europe 2022),
Nuremberg, Germany, May 10-12, 2022

Next Generation GaN-based Architectures: From 240W USB-C Adapters to 11kW EV On-Board Chargers with Ultra-high Power Density and Wide Output Voltage Range

M. Kasper,
J. Azurza,
G. Deboy,
Y. Li,
M. Haider,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

pcim
EUROPE

Next Generation GaN-based Architectures: From 240W USB-C Adapters to 11kW EV On-Board Chargers with Ultra-high Power Density and Wide Output Voltage Range

Matthias J. Kasper[1], Jon Azurza Anderson[1], Gerald Deboy[1], Yunni Li[2], Michael Haider[2], Johann W. Kolar[2]

[1] Infineon Technologies Austria AG, Siemensstr. 2, 9500 Villach, Austria
[2] Power Electronic Systems Laboratory, ETH Zürich, Physikstr. 3, 8092 Zürich, Switzerland

Corresponding author: Matthias J. Kasper, matthias.kasper@infineon.com

The Power Point Presentation will be available after the conference.

Abstract

The inherent advantages of GaN devices compared to their Silicon counterparts, i.e. absence of reverse recovery charge, lower output and gate charges, etc., enable the operation of power electronic systems based on GaN devices at considerably higher switching frequencies. This facilitates the design of systems with power densities far beyond the limits of state-of-the-art Si systems, which is demonstrated in this paper with two very different examples: a 240 W mobile charger with two USB-C output ports covering very wide output voltages of 5-48 V, and a three-phase 11 kW on-board charger with an output voltage range of 250-1000 V.

1 Introduction

In the recent years a trend towards greater environmental awareness and a more sustainable way-of-life has started, which has also lead to the commitment towards a reduction of electronic waste. In this context, the European Union has just recently announced the need for an universal charger solution for all portable devices, based on the USB-C standard [1]. Such a universal charger will have to cover a wide range of output voltages as well as to be operable from all mains voltages globally, with a power rating high enough to charge multiple devices at the same time, and yet still has to have a compact form factor.
Very similarly, fast charging station for electric vehicles (EV) also need to operate with a wide output voltage range in order to interface the different battery voltage ranges of EVs. The requirement for power electronic converters to operate with wide input and/or output voltages might not necessarily be mandated by end-users, but could also result from the effort to reduce development costs and to benefit from economies-of-scale. Instead of developing on-board chargers (OBCs) in EVs for different battery voltage ranges, significant cost and time savings in the development can be obtained by using an OBC approach that covers a wide range of battery voltages.

For the aforementioned application examples, the operating voltage ranges that have to be covered by the converter system are widening, but only those solutions which do not compromise in power density will be successful in the market. For this challenging design requirement, the specific characteristics of Gallium Nitride Gate Injection High Electron Mobility Transistors (GaN GIT HEMTs) in comparison to their Silicon Superjunction (Si SJ) or Silicon Carbide (SiC) counterparts and the advantages in hard- and soft-switching operation are essential. The key benefits of GaN GIT HEMTs are the absence of any reverse recovery charge, the on-state resistance-related ten-fold reduction of the output charge w.r.t Si SJ devices, the very linear characteristic of the output capacitance, the lower gate charge, and additionally, the lower temperature dependency of the on-state resistance [2]. This enables converter systems based on GaN GIT HEMTs to not only operate at higher switching fre-

quencies but also to combine different modulation and/or control schemes in order to optimize the efficiency for each operation point.

2 Wide-Output Voltage Range 240W USB-C Chargers/Adapters

In recent years, the number of mobile consumer devices such as mobile phones, tablets, laptops, etc. has increased dramatically and driven the need for a universal adapter for all of those devices. Such an adapter will not only improve the user experience, but ultimately also reduce electronic waste if the sale of the chargers is unbundled from the sale of the electronic devices. Furthermore, the latest revision of the USB-PD (Power Delivery) standard includes voltages up to 48 V, which, in combination with the 5 A rating of USB-C cables, provides the possibility to charge devices with up to 240 W [3]. Thus, the current generation of single port USB chargers with only 65 W of output power will no longer be sufficient for the consumer market, for which a new generation of higher power adapters with dual USB-PD ports is explored below.

2.1 System requirements

The challenges to realize such an adapter are the combination of wide ranges of input voltage (90-265 V_{RMS}) and output voltage (5-48 V), PFC requirement, and the supply of two independent output ports while still maintaining a high power density. The full set of specifications is summarized in **Tab. 1**.
Particular attention has to be paid to the thermal aspects of the converter design. Since the only means of heat dissipation in the charger are natural convection and radiation, shrinking the system volume for highest densities reduces also the available surface area of the converter for heat dissipation. Based on the formulas of [4], the required efficiency of a charger with 240 W can be calculated for a maximum allowable surface temperature (cf. **Fig. 1**) in dependency of the power density, assuming that the losses are evenly distributed within the converter. This clearly highlights, that any power density target in this application is inherently coupled to an efficiency target, as a maximum surface temperature (i.e. $70°$C) must not be exceeded.

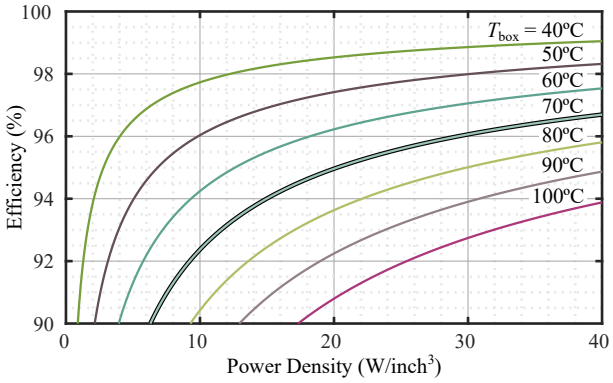


Fig. 1: Minimum required efficiency for systems with a power rating of 240 W in dependency of the power density for different maximum surface temperatures T_{box}.

2.2 Conceptualization

In order to identify the best suited topologies and the system partitioning for the future generation of high-density adapters, several different topologies and concepts of partitioning the control and isolation function can be considered, as shown in **Fig. 2**.

Regarding options for the PFC (rectifier) stage, the main groups of classification are boost-type, buck-type, or buck-boost-type PFCs (cf., **Fig. 2(a-d)**). While boost-type PFCs always provide a DC-link voltage higher than the peak value of the grid voltage (see **Fig. 2(a)**), buck-type PFCs are able to provide a lower DC-link voltage and thus could simplify the design of the subsequent DC/DC stage. In single phase systems, however, buck-type PFCs as depicted in **Fig. 2(b)** suffer from a discontinuous input current, since only in time intervals when the mains voltage is higher than the DC-link voltage can any current be drawn from the mains, thus not fulfilling the Class D equipment current harmonic

Tab. 1: Main specifications of the next-generation of USB-C chargers.

Parameter	Value
Input Voltage Range	1ϕ, $90-265\,V_{rms}$
Rated Output Power	240 W
USB-C PD 3.1 Output Voltage	$5-48$ V
USB-C PD 3.1 Output Current	5 A
EMI Compliance	Class B
Maximum Ambient Temperature	$40°$
Maximum Surface Temperature	$70°$

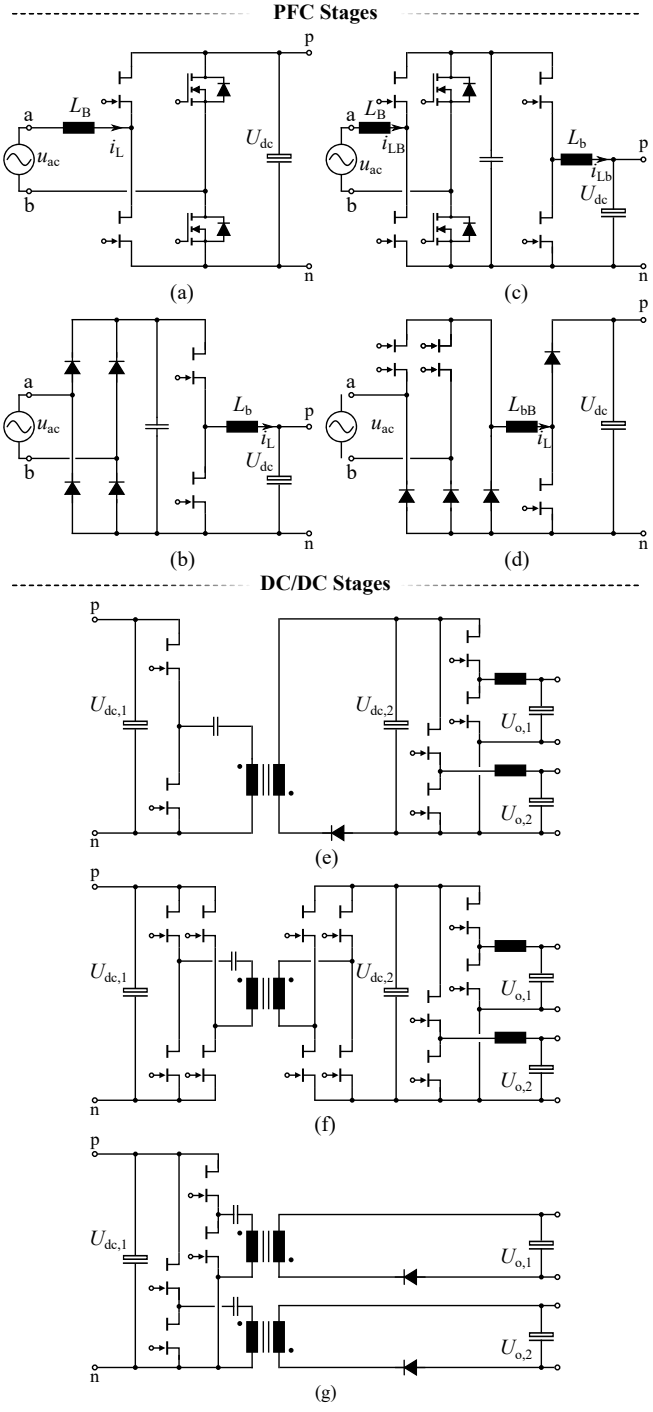


Fig. 2: Overview of different topology options for the 240 W charger: (a-d) PFC rectifier options and (e-g) DC/DC converter options.

limitations imposed by [5]. This is especially a problem at the lowest mains voltage of 90 V_{rms} and thus renders buck-type PFCs as unsuitable for this application. This leaves boost-type PFCs such as the Totem-Pole or buck-boost-type PFCs as preferred solutions. The latter one can be realized as a cascade connection of a boost-type PFC and a buck stage, cf., **Fig. 2(c)**, which would require

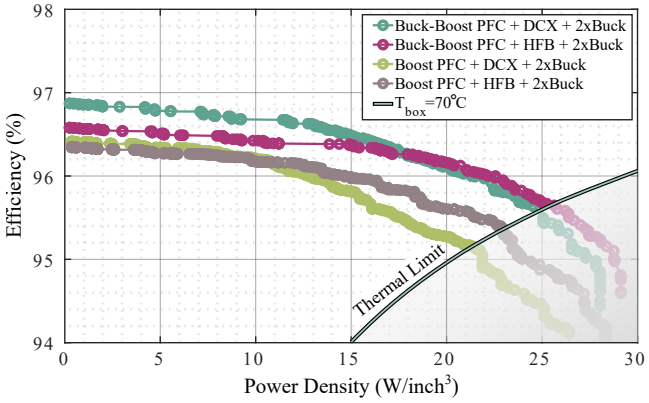


Fig. 3: Pareto optimization results for the different topology options to realize the 240 W charger. The efficiency is calculated at 90 V_{rms} input and full load. The power density is calculated based on the boxed volumes of the components including an outer case around the system. The thermal limit line is calculated for a maximum surface temperature of 70 °C at an ambient of 25 °C.

two magnetic components to realize both the boost and the buck inductor, or alternatively with a lower component count by employing reverse blocking (bidirectional) devices [6][7], cf., **Fig. 2(d)**. Since these are not yet commercially available, this interesting solution will not be considered further.

Following the PFC stage, the DC/DC conversion stage has to provide galvanic isolation for safety reasons and the independent control of two USB-C ports. This can be realized in different ways, as shown in **Fig. 2(e-g)**. The first option shown in **Fig. 2(e)** is to use a DC/DC converter stage that can provide isolation and regulation at the same time, like the Hybrid Flyback (HFB) converter [8], followed by two buck converters. This potentially allows to permanently turn on the buck stage with the highest output voltage, as this would be the voltage regulation set-point for the HFB. Alternatively, the first DC/DC conversion stage could be a stage that only provides isolation and no regulation, such as the "DC-transformer" (DCX) converter with a fixed conversion ratio, as in **Fig. 2(f)**. This simplifies the control since only a fixed duty cycle of 50% has to be provided and the converter at the same time operates with a very high efficiency at the resonance frequency. The drawback is, however, that the buck stages will interface a varying input voltage and non of them can be permanently turned on at any time. As a last option, two regulating and isolating converters can be employed, one for each output port, like for instance, the HFB

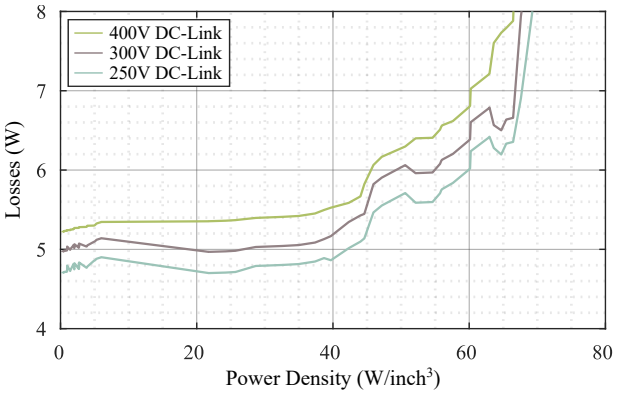


Fig. 4: Effect of DC-link voltage reduction on different Totem-Pole PFC stage designs depending on the power density (including case) for different DC-link voltage levels at full load operation and 90 V_{rms} input.

as shown in **Fig. 2(g)**. This, however, requires two transformers which each have to be rated for the full power of the converter and thus renders this solution as unsuitable for highest power densities.

2.3 Multi-objective optimization

Based on this first assessment, four different solutions have emerged as promising candidates for the next generation of charger, given by the combination of either a boost-type or a buck-boost-type PFC combined with either a HFB or a DCX, always together with two buck converters. In the next step, these system solutions are comparatively evaluated by means of multi-objective optimization [9]. This methodology considers all available degrees of freedom in the design of each concept by sweeping all design parameters on system as a well as on component level, and by calculating the performance of each design with accurate system and component models. As a result, an efficiency vs. power density (η-ρ) Pareto front is calculated for each topology as shown in **Fig. 3**, indicating the achievable trade-off between the performance dimensions. The selected operation point is at full load and lowest input voltage, since this leads to the highest rms-values of input currents and therefore the highest losses and is thermally typically the most critical operation point. For the calculation of the power density a casing with a thickness of 2.5 mm on each side (including stand-off) is assumed.

As can be seen, power densities in the range of 24-25 W/inch^3 are achievable with PFC topologies that allow to lower the DC-link voltage. This is due

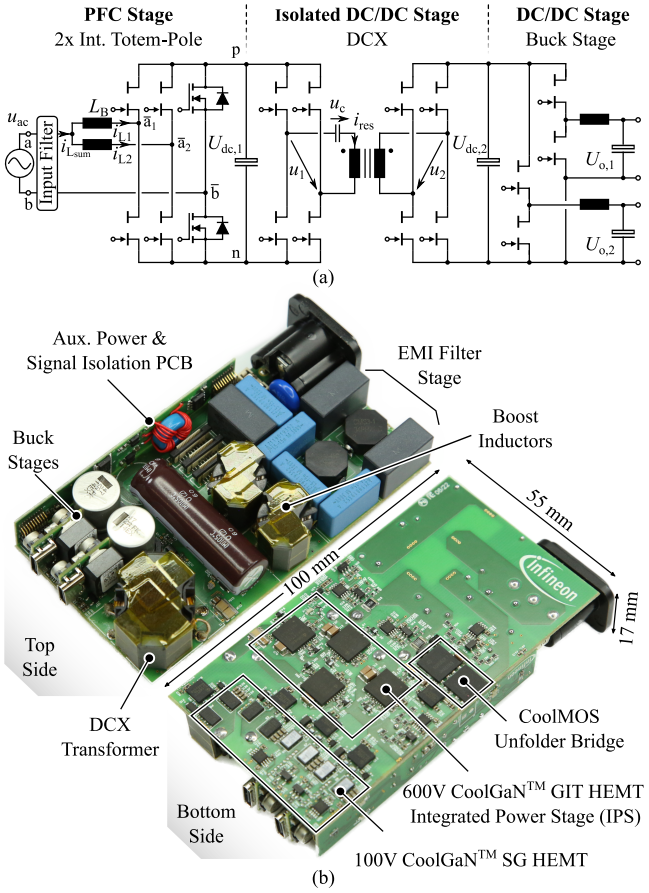


Fig. 5: (a) Selected circuit schematic of the charger/adapter, and (b) top and bottom side views of the realized hardware demonstrator of the 240W dual-port USB-C charger (100 mm x 55 mm x 17 mm) with an uncased power density of 42 W/inch^3 and a weight of 113 g. The full system efficiency is 95.3 % at rated power with 90 V_{rms} input and 48 V output.

to the fact that with lower DC-link voltages one the one hand the current ripple of the PFC input current reduces, and on the other hand less output charge Q_{oss} is stored in the parasitic capacitances of the switches. This leads to reduced switching losses in hard-switching and/or less required circulating current to achieve ZVS. Since the shown buck-boost topology requires a higher number of active devices compared to a Totem-Pole PFC, a similar benefit can achieved by operating a Totem-Pole PFC as a boost-follower circuit. In that mode, the DC-link voltage is dynamically varied depending on the input rms-voltage, which leads to a reduction in losses as shown in **Fig. 4** for designs with different power densities.

Based on the this analysis, a Totem-Pole PFC with boost-follower modulation is selected in combina-

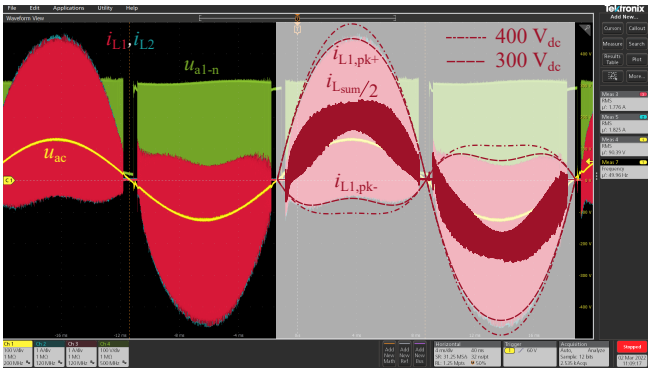
tion with a DCX and two buck stages for the realization as a hardware demonstrator with an uncased power density of 42 W/inch^3 which translates to a cased power density of around 25 W/inch^3 (cf. **Fig. 5**). The main component parameters of the demonstrator can be found in **Tab. 2**.
In the following paragraphs, the design details of the different stages are explained in more details.

2.3.1 PFC stage

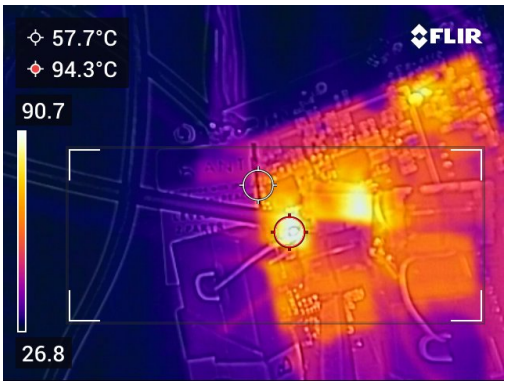
The PFC stage is designed to achieve ZVS over the whole line cycle for all load conditions and/or input rms-voltages by operating with continuous conduction mode (CCM) with a fixed switching frequency of 400 kHz per bridge-leg at lowest line voltage. Since this mode leads to a large ripple current seen by the boost inductor and the switches, two interleaved high-frequency bridge-legs are selected. This is beneficial from several aspects: firstly, the average current in each bridge-leg is only half of the entire PFC current, which also cuts the required current ripple on each inductor for achieving ZVS in half; secondly, by phase-shifting the bridge-legs by 180 ° the effective switching frequency seen by the EMI filter is doubled which reduces the required filter attenuation and consequently the EMI filter size; thirdly, the losses are spread among a larger number of components which prevents the creation of hot-spots. The benefits of the combination of high current ripple CCM modulation for ZVS and parallel interleaving are also confirmed in [10].
The operation at full-load and lowest input voltage of 90 V with a DC-link voltage of 300 V is shown

Tab. 2: Main components of the 240 W charger demonstrator.

Parameter	Value
Totem-Pole PFC Stage	
Boost inductors L_B	38.3 µH, RM7 core, N49 ferrite, 0.8 mm air-gap, 26 turns, 120x40 µm litz
HF switches	600 V Integrated CoolGaN™ GIT HEMTs 140 mΩ_{typ} half-bridge IGI60F1414A1L
LF switches	600 V Si SuperJunction CoolMOS™ 48 mΩ_{typ} IPL60R060CFD7
DC-link capacitor	450 V, 68 µF
Sw. Freq. f_{sw}	400 kHz (per bridge leg)
EMI filter	2-stage filter
DCX Stage	
Primary switches	Integrated CoolGaN™GIT half-bridge IGI60F1414A1L
Secondary switches	100 V CoolGaN™ SG HEMTs 2.5 mΩ_{typ} IQC0800NLS
Transformer	RM10LP core, N49 ferrite, 0.13 mm air-gap, 28 turns prim., 80x40 µm litz, 5 turns sec., 250x40 µm litz, $L_m = 339\,\mu H$, $L_{res} = 12.3\,\mu H$
Sw. Freq. f_{sw}	425 kHz
ZVS Buck Stage	
Switches	100 V CoolGaN™ SG HEMTs 2.5 mΩ_{typ} IQC033G10LS1SC
Buck Inductor L_{buck}	2.8 µH, RM5 core, N49
Sw. Freq. f_{sw}	475 kHz



(a)



(b)

Fig. 6: Measurement results of PFC stage: (a) Waveforms of the PFC stage operating at 90 V_{rms}, outputting 300 V_{dc} and 240 W. The effect of different DC-link setpoints on the current ripple envelope and the sum of both inductor currents (halved, for representation purpose) is also highlighted. (b) Thermal image at the same operating point, showing that the switches are defining the hot-spot during thermal steady state operation.

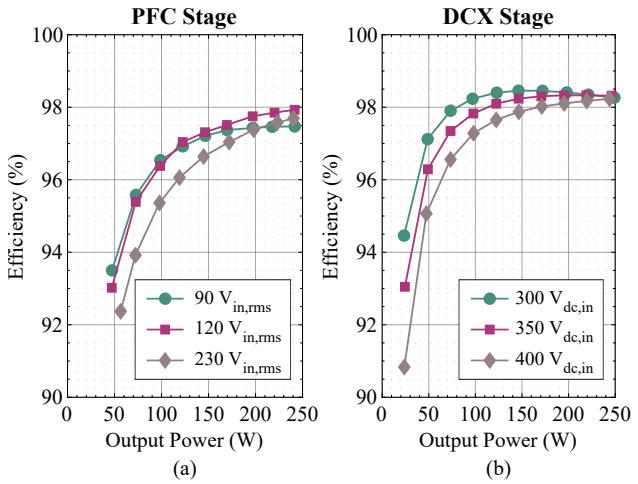


Fig. 7: Efficiency measurements of (a) the PFC stage at 300 V_{dc} output for 90 V_{rms} and 120 V_{rms} input, and at 400 V_{dc} output for 230 V_{rms}, and (b), the DCX stage, whose output voltage is then given directly by the transformer turns ratio.

in **Fig. 6(a)** together with the thermal image in **Fig. 6(b)**. In addition, the variations of the upper and lower current boundaries for higher DC-link voltages up to 400 V are also depicted. As can be seen, the current ripple increases with rising DC-link voltage and leads to larger conduction losses in the inductor and the switches, as well as larger core losses in the inductors, highlighting the benefits of the boost-follower mode which adaptively lowers the DC-link voltage. Additionally, the optimal frequency modulation (OFM) scheme can also be applied for further loss savings [11], and the dead-time of the transitions can be trimmed as a function of the operating point to reduce the third-quadrant conduction losses in the GaN GIT HEMTs.
The efficiency of the PFC stage over the entire load range is shown in **Fig. 7(a)** for selected input rms-voltages.

2.3.2 DCX stage

The DCX converter is designed to operate at a resonance frequency of $425\,\mathrm{kHz}$ and to achieve ZVS independent of the load by utilizing only the magnetizing current for the ZVS transition. The turns ratio of the transformer $(5.6:1)$ is selected such that the DC-link voltage range of $300-400\,\mathrm{V}$ is mapped to an input voltage range for the buck stage of $52-71\,\mathrm{V}$, enabling the use of $100\,\mathrm{V}$ rated Schottky Gate (SG) GaN HEMT devices as synchronous rectifiers of the DCX stage. For a highly compact realization the leakage inductance of the transformer

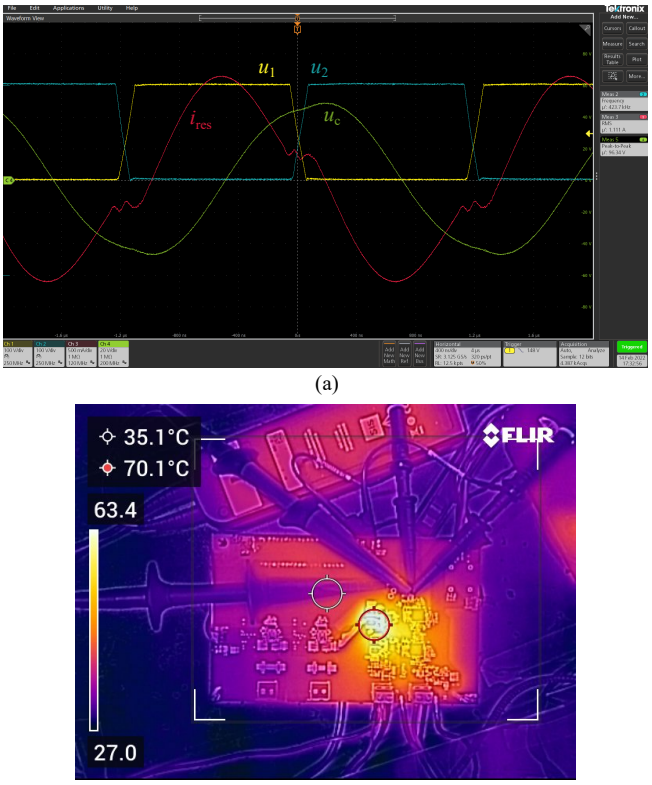


Fig. 8: Measurement results of DCX stage: (a) Waveforms of the DCX operating at 300 V_{dc} input, 52 V_{dc} output, and 240 W. (b) Thermal image at the same operating point focusing on the semiconductors.

is utilized as resonant inductor.
The current and voltage waveforms for the operation at full-load are shown in **Fig. 8(a)** for an input voltage of $300\,\mathrm{V}$. In addition, the thermal image for this load point is depicted in **Fig. 8(b)**, whereas the efficiency over the entire load range is reported in **Fig. 7(b)**.

2.4 Summary

With the selected system design parameters of the 240 W USB-C charger as shown above an overall system efficiency of 95.3 % can be achieved at full load operation with an input voltage of 90 V_{rms} and an output voltage of 48 V. The power density of the system reaches 42 W/inch^3 (uncased) outperforming state-of-the-art Si chargers on the market by around a factor of 2.

3 Ultra-High Density Three-Phase 11kW On-Board Chargers

As EV sales are soaring, the requirements for on-board chargers (OBCs) are getting ever more demanding, and the original equipment manufacturers (OEMs) are requiring a volume and weight decrease of the OBCs, in order to be able to free space for other components and to reduce the weight of the vehicles. The state-of-the-art power density for OBCs with Si devices is around 2 kW/L. Utilizing WBG devices, the goal is to reach 6 kW/L, i.e. a factor of 3 improvement. It is in this context, that the influence of GaN devices in such chargers will be analyzed.

3.1 System requirements

To reach the 6 kW/L power density goal, the main challenge is to deal with the wide input and output voltage range specifications. The input voltage is defined by the grid codes of the different geographic regions and poses a challenge for the PFC rectifier stages, similar to those previously described for the USB-C charger. The output voltage range is defined by the EV battery voltage range and poses a challenge for the DC/DC stages, which must be able to provide full power for a wide output voltage range. This leads to a difficult trade-off between entering hard-switching loss regimes or increased RMS currents [12]. Secondly, with increasing renewable energy generation fed into the grid, EVs are seen as a key player to stabilize the grid supplying peak power shaving when plugged in, and hence, bidirectional power processing of the OBCs is required. Thirdly, OBCs have to be able to operate both from single-phase (1-Φ) and three-phase (3-Φ) grids. Assuming that the current (and therefore also the power) available per phase is limited by a fuse, a 230 V_{rms} (line-to-neutral) system with a 16 A-rated fuse can e.g. provide 3.6 kW in 1-Φ configuration and 11 kW in 3-Φ configuration. This would be suitable for a traditional 3-Φ system, such as a Vienna Rectifier. However, if the same OBC were to operate in the USA, a 240 V_{rms} split 1-Φ grid interface limited by a 40 A fuse would require 9.6 kW single-phase operation. For this challenging requirement, several solutions have been proposed in literature, ranging from an unfolder bridge-leg for the return path [13] to a neutral phase connected to the midpoint of the DC-link [14].

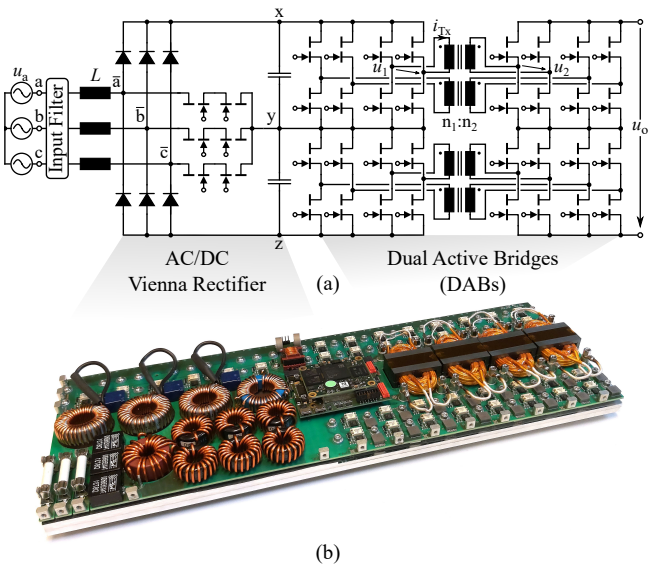


Fig. 9: 10 kW EV charger demonstrator: (a) Circuit schematic, consisting of a Vienna rectifier followed by 4 DAB DC/DC converters. (b) The realized hardware demonstrator, featuring an uncased power density of 10kW/L and measuring 17.8 mm x 400 mm x 140 mm.

3.2 Topology investigation and key power density enablers

As a starting point to outline the path towards future generations of ultra high-density OBCs, a 3-phase 10 kW EV battery charger system with very wide output voltage and a power density of 10 kW/L shown in **Fig. 9**, for which the specifications of **Tab. 3** are taken as a starting point for these investigations. This system employs a Vienna rectifier PFC providing a regulated split DC-link, to which four cascaded Dual Active Bridges DC/DC converters (DABs) with 600 V rated GaN GIT HEMTs are connected for output voltage regulation. DABs are inherently bidirectional topologies and are able to operate with ZVS in both buck and boost mode, making them a preferred choice for high frequency operation in EV chargers and OBCs. Note that replacing the rectifier diodes of the Vienna Rec-

Tab. 3: Main specifications of the realized EV charger.

Parameter	Value
Rated Output Power	10 kW
Input Voltage	3ϕ, 320-530 $V_{ll,rms}$
Output Voltage	250-1000 V_{dc}
Max. Output Current	25 A
EMI Compliance	Class B

tifier with active switches provides means for synchronous rectification and enables fully bidirectional power conversion. All of the key system parameters can be found in **Tab. 4**.

There are three key enablers that allow to increase the power density. The first one is a novel 1/3-PWM synergetic modulation scheme [15], which consists in utilizing the DC/DC stage to control the DC-link voltage such that in the AC/DC stage always only one of the three phases is switching at a given point in time. This has two advantages, the first is a dramatic reduction of losses (mainly given by a more than two third reduction of the switching losses in the AC/DC stage), and the second, that it allows to reduce the DC-link voltage to the absolute minimum for a boost-type system, i.e., to the value of the maximum line-to-line voltage and/or the six-pulse envelope of the line-to-line voltages. The latter is advantageous for the DC/DC stage, as it reduces the voltage transfer ratio that has to be provided by the subsequent DC/DC converters. For instance, for the minimum system output voltage of 250 V, there is no need to boost the DC-link voltage to, e.g., 800 V, but it can be kept to the maximum line-to-line voltage, i.e., having a six-pulse shape between 490-565 V, thus reducing the buck range of the DC/DC stage.

Tab. 4: Main components of 10 kW EV charger demonstrator.

Parameter	Value
Vienna Rectifier Stage	
Boost Ind. L	36 µH, Magnetics Molypermalloy Powder (MPP), 55550 Core, 36 turns, 1.4 mm wire
Switches	600 V CoolGaN™ GIT HEMT 55 mΩ_{typ} IGOT60R070D1
Diodes	1200 V SiC Schottky CoolSiC™ IDM10G120C5
Gate Drivers	Single-Channel Functionally Isolated EiceDRIVER™ 1EDF5673K
Sw. Freq. f_{sw}	560 kHz
Dual Active Bridge Stage	
Prim. & Sec. Switches	600 V CoolGaN™ GIT HEMT 55 mΩ_{typ} IGOT60R070D1
Gate Drivers	Single-Channel Functionally Isolated EiceDRIVER™ 1EDF5673K
Transformer	ELP38/8/25 core, N97 ferrite, no air-gap, 16 turns prim., 990x40 µm litz, 10 turns sec., 1320x40 µm litz, $L_{res} = 12.3\,\mu H$
Sw. Freq. f_{sw}	140-400 kHz

The second enabler are the DABs. By comprising of two active full-bridges, this topology allows to have a wide voltage range controllability. However, the challenge lies in finding an optimal trade-off between conduction losses (in the transformer and semiconductor devices), and the switching losses. The most favourable operating point for the DABs is where the voltage transfer ratio between the primary and the secondary matches the turns ratio, like in the case of **Fig. 10(b)**, where low RMS currents are obtained as well as ZVS transitions in all bridge-legs. However, when it comes to modulating the DAB outside it's natural voltage transfer ratio, there are advanced modulation schemes that can be used to minimize the losses for a given set of operating parameters [12]. For the DABs in this prototype, the modulation scheme has been numerically optimized such that the DAB operation is divided into three parts:

- Buck Mode: Here, $u_{\text{out}} < n \cdot u_{\text{in}}$, where u_{out} and u_{in} are the output and input voltages of the DAB, respectively, and $n = \frac{n_2}{n_1} = 0.625$ the transformer turns ratio. For this case, the duty cycle of the primary side is calculated as, $d_1 = n\frac{u_{\text{out}}}{u_{\text{in}}}$, the duty cycle of the secondary side (d_2) is kept constant at d_2 = 0.5, and the switching frequency is kept constant at 140 kHz (see **Fig. 10(a)**). In this operating rage, full-ZVS is achieved in three bridge-legs of the DAB (both of the bridges on the secondary and one on the primary), while the remaining bridge-leg achieves ZVS for part of the operating range, which however, doesn't cause large switching losses as both the switching frequency and switched voltage are low.
- $u_{\text{out}} = n \cdot u_{\text{in}}$ Mode: For this case, the duty cycle of both the primary and secondary side are kept constant at $d_1 = d_2$ = 0.5, and the switching frequency linearly increases from 140 kHz to 195 kHz until the maximum input voltage of the DAB, which is half of the maximum allowed DC-link voltage and corresponds to around 425 V. In this range, full-ZVS is achieved in all of the four bridge-legs of the DAB, and exemplary measured waveforms can be seen in (see **Fig. 10(b)**).

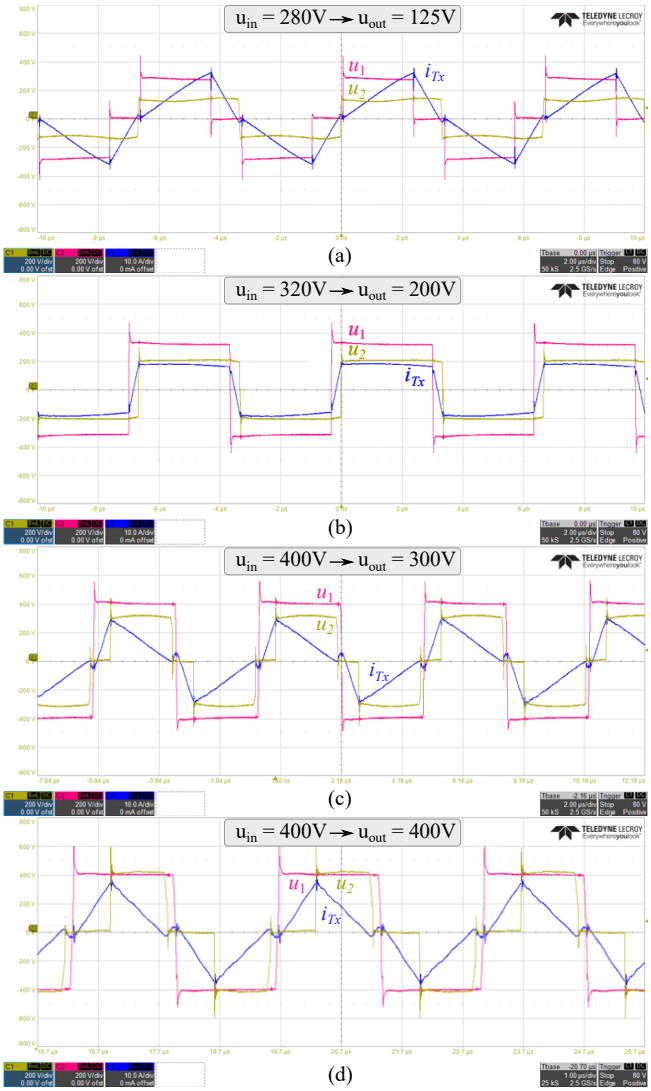


Fig. 10: (a)-(d) Key waveforms of the designed DAB (taken on one module) for different input and output voltage ratios. In (a), waveforms are taken for the maximum module output current (12.5 A); (b-d): waveforms for maximum power operation of the module (2.5 kW).

– Boost Mode: Here, $u_{\text{out}} > n \cdot u_{\text{in}}$, the primary side duty cycle is selected to be $d_1 = 0.5$, while the secondary side duty cycle and the switching frequency are calculated such that the maximum range of ZVS can be achieved. As a result, the switching frequency increases in a non-linear fashion from 195 kHz until 400 kHz, depending on the voltage transfer ratio, cf., **Figs. 10(c-d)**. For a certain range in the boost mode, even if full ZVS cannot be achieved in all the bridge-legs, in the worst case only one of the half-bridge is hard-switched at zero load current, to reduce the switching losses as far as possible, whereas all other half-bridges achieve full-ZVS.

In all of the above cases, the control degree of freedom is the phase shift between the primary and the secondary side, which then allows to actively control the power flow from primary to secondary or vice versa.

The third and last enabler of the achieved power density and flat profile of the EV charger are the GaN GIT HEMT devices, cf., **Tab. 4**. As previously described, advantage is taken out of their small output capacitance vs. Si and SiC devices, that facilitates full-ZVS at lower switched currents [16]. Further key advantages are very low specific R_{dson} values, and the capability to operate in partial-hard and hard-switched modes.

Hence, it is a combination of advanced control and modulation methods, together with the multifaceted superior performance of GaN devices under different switching conditions, that allows to unlock the next-level of power density in EV chargers.

4 Conclusions and Outlook

This work shows that the challenge found in a broad range of applications combining wide input and/or output voltage ranges with high power density requirements can be well addressed with GaN HEMTs. On the one hand, these devices have superior figure-of-merits which makes them suitable for operation at high frequency, and on the other hand they also enable the use of advanced modulation and control schemes due to the fact they are suitable to operate in both hard- and soft-switching regimes.
This ultimately requires from the power electronics designer to master a more complex system design space which contains, besides the degrees of freedom of the design of the electrical components, also the degree of freedom of the control strategies, offered by digital controllers. This can only be comprehensively optimized by means of multi-objective optimization that yields the optimum system design within the given electrical and thermal constraints.

References

[1] EU. “Commission Proposes a Common Charger for Electronic Devices - Factsheet.” (Sep. 23, 2021), [Online]. Available: https://ec.europa.eu/docsroom/documents/46754.

[2] G. Deboy, O. Haeberlen, and M. Treu, “Perspective of Loss Mechanisms for Silicon and Wide Band-Gap Power Devices,” *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 2, pp. 89–100, 2017.

[3] USB 3.0 Promoter Group, “Universal Serial Bus Power Delivery Specification, Revision 3.1,” Tech. Rep., Jan. 12, 2022.

[4] W. Rohsenow, *Handbook of Heat Transfer*. New York: McGraw-Hill, 1998.

[5] International Electrotechnical Commission (IEC), *61000-3-2 Standard*.

[6] W. Wei, L. Hongpeng, J. Shigong, and X. Dianguo, “A Novel Bridgeless Buck-Boost PFC Converter,” in *Proc. of the IEEE Power Electronics Specialists Conf.*, 2008, pp. 1304–1308.

[7] F. Vollmaier, N. Nain, J. Huber, J. W. Kolar, K. K. Leong, and B. Pandya, “Performance evaluation of future t-type pfc rectifier and inverter systems with monolithic bidirectional 600 v gan switches,” in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 5297–5304.

[8] A. Medina-Garcia, M. Schlenk, J. Cruz-Cozar, D. P. Morales, and N. Rodriguez, “Study of WBG Switches Benefits on Asymmetrical Half-bridge Flyback Converter,” in *Proc. of the Int. Conf. for Power Electronics and Intelligent Motion (PCIM Europe)*, 2021, pp. 1–6.

[9] J. W. Kolar, J. Biela, and J. Miniböck, “Exploring the Pareto Front of Multi-Objective Single-Phase PFC Rectifier Design Optimization - 99.2% Efficiency vs. 7kW/dm^3 Power Density,” in *Proc. of the Int. IEEE Power Electronics and Motion Control Conference (IPEMC)*, 2009, pp. 1–21.

[10] J. Le Lesle, R. Caillaud, F. Morel, N. Degrenne, C. Buttay, R. Mrad, C. Vollaire, and S. Mollov, “Optimisation of an Integrated Bidirectional Interleaved Single-Phase Power Factor Corrector,” in *Proc. of the Int. Conf. for Power Electronics and Intelligent Motion (PCIM Europe)*, 2018, pp. 1–8.

[11] D. Neumayr, D. Bortis, E. Hatipoglu, J. W. Kolar, and G. Deboy, “Novel Efficiency-Optimal Frequency Modulation for High Power Density DC/AC Converter Systems,” in *Proc. of the IEEE Int. Future Energy Electronics Conf. (IFEEC - ECCE Asia)*, 2017, pp. 834–839.

[12] F. Krismer, “Modeling and Optimization of Bidirectional Dual Active Bridge DC-DC Converter Topologies,” Ph.D. dissertation, Power Electronic Systems Laboratory, ETH Zurich, 2010.

[13] P. Papamanolis, D. Bortis, F. Krismer, D. Menzi, and J. W. Kolar, “New EV Battery Charger PFC Rectifier Front-end Allowing Full Power Delivery in 3-Phase and 1-Phase Operation,” *Electronics*, vol. 10, no. 17, p. 2069, 2021.

[14] M. Hagemeyer, P. Wallmeier, F. Schafmeister, and J. Böcker, “Comparison of Unidirectional Three-and Four-Wire-Based Boost PFC-Rectifier Topologies for Non-Isolated Three-Phase EV On-Board Chargers Under Common-Mode Aspects,” in *Proc. of the IEEE Applied Power Electron. Conf. and Expo. (APEC)*, 2021, pp. 569–576.

[15] J. Azurza Anderson, M. Haider, D. Bortis, J. W. Kolar, M. Kasper, and G. Deboy, “New Synergetic Control of a 20kW Isolated Vienna Rectifier Front-End EV Battery Charger,” in *Proc. of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019, pp. 1–8.

[16] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, “ZVS of Power MOSFETs Revisited,” *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016. DOI: 10.1109/TPEL.2016.2574998.