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ZVS Modulation Scheme for Reduced Complexity Clamp-Switch TCM DC-DC Boost Converter

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***Abstract*— DC-DC boost converter Zero-Voltage-Switching (ZVS) modulation schemes such as Triangular Current Mode (TCM) offer a highly efficient operation but suffer from large switching frequency variations, which are complicating the EMI filter design and the digital control. As a solution, a tri-state boost converter operated in ZVS mode, referred to as Clamp-Switch TCM (CL-TCM) operation can be introduced, which allows to limit the switching frequency variation significantly. This paper presents two variations of the CL-TCM boost converter with reduced number of active switches in the circuit, which are suitable for high input-to-output voltage conversion ratios. In addition, the ZVS modulation schemes, its limitations, the converter design and the controller implementation are presented and analyzed in detail for both converter topologies. The timing calculations for the switching signals are provided for two operating modes, either offering a minimized switching frequency variation and minimized RMS inductor current or a constant switching frequency operation, which in turn comes at the expense of an increased RMS inductor current. The ZVS operation and the operating modes are experimentally verified using a hardware prototype.**

***Index Terms*—DC-DC boost converter, zero voltage switching (ZVS), tri-state boost, clamp switch, triangular current mode (TCM)**

I. Introduction

Zero-Voltage-Switching (ZVS) DC-DC buck or boost converters are commonly realized using a Triangular Current Mode (TCM) operation with variable switching frequency [1]–[4] or a Synchronous Conduction Mode (SCM) operation with a fixed switching frequency [5]–[7]. The main disadvantage of the SCM operation is the significantly reduced partial load efficiency due to the large peak-to-peak inductor current ripple which is remained constant even at light load conditions. The TCM operation mode instead offers a much higher partial load efficiency, which in turn comes at the expense of a large switching frequency variation and hence, complicates the filter design and the implementation of the digital control.

In order to overcome these drawbacks, an additional clamp-switch can be introduced in parallel to the boost inductor, which allows to limit the switching frequency variation significantly, while achieving a high partial load efficiency similar to the TCM operation. Such a topology is implemented in [8] and in the Picor Cool-Power ZVS Buck Regulator series provided by Vicor Corp. and is described in [9]. ZVS of the switches in the half-bridge configuration is enabled as for the SCM and TCM operation by reversing the flow direction of the inductor current in each switching period, and as a result, allowing for ZVS for each switch in the half-bridge.

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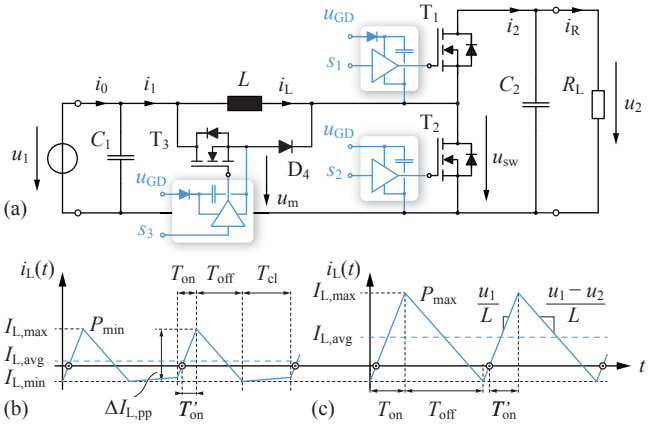


Figure 1: (a) Proposed 3-switch Clamp-Switch TCM (CL-TCM) boost converter topology. (b)-(c) typical CL-TCM converter inductor current waveforms at minimum and maximum output power.

The clamp-switch boost converter topology considered in this paper is depicted in **Fig. 1(a)** and was proposed in a similar form as a hard-switched converter in [10], which is referred to as tri-state boost converter and which allows to improve the dynamic performance of the converter by eliminating the right-half-plane zero in the small signal control-to-output transfer function. In another more recent application presented in [11], a hard-switched tri-state boost converter was used on the receiver side of a wireless power transfer system, which allows to implement an adaptive resonant frequency tuning and load matching.

In [12] and [13], a relatively complicated ZVS modulation scheme referred to as Clamp-Switch TCM (CL-TCM) operation was introduced, where the clamp-switch is realized with an anti-series connection of two active switches. The modulation scheme allows for ZVS for all switches, independent of the output power level and without restrictions on the input-to-output voltage conversion ratio, given the natural boundaries for boost operation. A similar ZVS operation was achieved with a bidirectional buck-boost converter for the use in hybrid electric vehicles, as described in [14].

In this paper, a simplified ZVS modulation scheme [12] is proposed for the CL-TCM converter which allows to reduce the hardware complexity and which increases the reliability of the converter by replacing the clamp-switch used in [8], [13] with an anti-series connection of an active switch and a

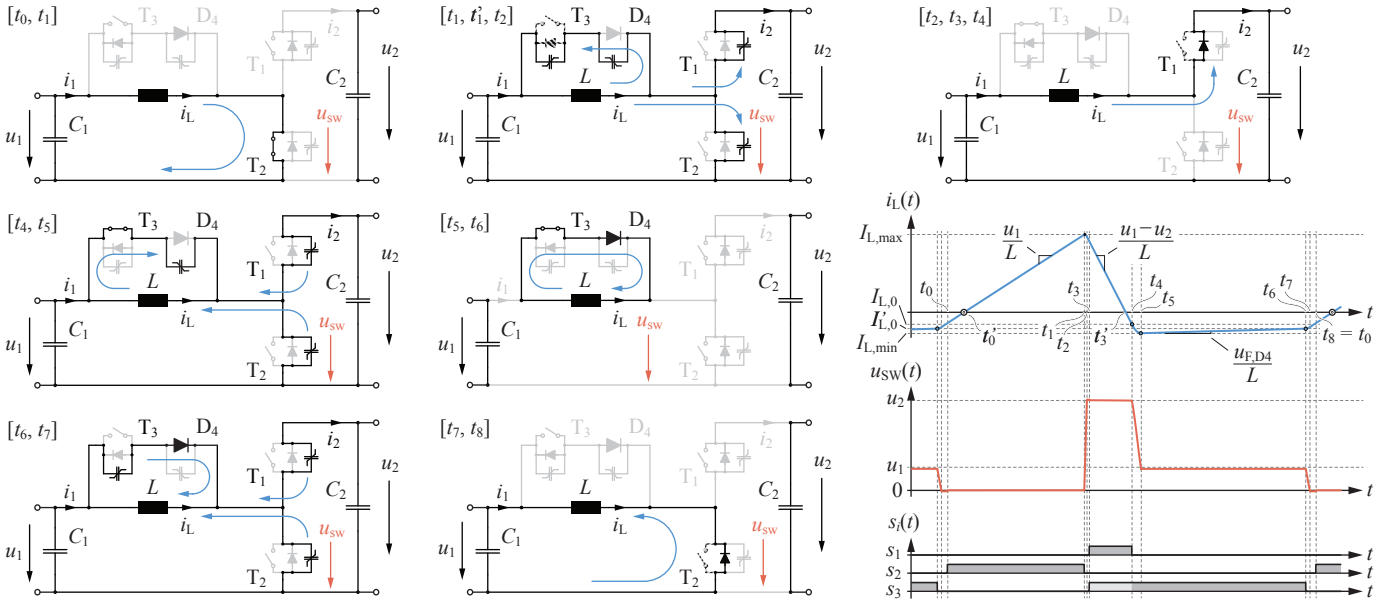


Figure 2: Operating states of the proposed 3-switch CL-TCM modulation scheme for a full switching cycle $[t_0, t_8]$. Typical waveform of the inductor current i_L and the switch-node voltage u_sw, belonging to the switch control signals s_i.

single diode, as shown in **Fig. 1(a)**. In this paper, this type of converter is referred to as 3-switch CL-TCM boost converter and allows for zero-voltage switching and unidirectional power flow. Furthermore, in this paper, a unidirectional 2-switch CL-TCM converter operation is proposed and explained in detail, which allows for ZVS of all switches as well, but reduces the complexity of the converter hardware and the modulation scheme to a minimum. The proposed converter structures and ZVS modulation schemes come at the expense of restrictions on the input-to-output voltage conversion ratio and output power range, as it will be explained in detail in **Section II**. The design of the boost inductance and the calculation of the timing intervals T_on, T_off and T_cl (cf. **Fig. 1(b)** and **(c)**) are presented in **Section III**. In addition, two converter operating modes, either offering a variable or constant switching frequency operation are analyzed and compared. In **Section IV**, the controller implementation is explained for both converter types and in **Section V**, the experimental verification of the ZVS operation and the proposed operating modes is presented. In addition, a DC-DC efficiency comparison for the different CL-TCM converter types is given in the same section. Concluding remarks are given in **Section VI**.

II. Modulation Scheme

Typical inductor current waveforms for the considered CL-TCM converter operation at minimum and maximum output power are shown in **Fig. 1(b)** and **(c)** respectively. At maximum output power, the CL-TCM operation corresponds to the TCM operation, i.e. the clamp switch T_3 is unused. The inductor current has a triangular shape with a negative inductor current $I_\mathrm{L,min}$ at the end of time interval T_off that allows for ZVS of the low-side switch T_2 at the beginning of the subsequent time interval T_on. At light load conditions, the clamp-switch allows to introduce a free-wheeling state for the inductor current after the turn-off of switch T_1 and hence, allows to stretch the switching period as it is shown in **Fig. 1(b)**. As a result, the switching frequency variation can be controlled depending on the output power and on the voltage conversion ratio. The maximum switching frequency f_max occurs always at the maximum voltage conversion ratio, whereby the maximum feasible operating frequency is mainly limited by the time delays in the measurement and control circuit, as the switching time intervals need to be calculated and synchronized to the zero-crossings of the inductor current, as explained in detail in **Section IV**.

The ZVS modulation scheme proposed in this paper allows to reduce the number of active switches in the circuit topology and is explained in the following. However, as already mentioned, the reduced hardware complexity comes at the expense of a restriction on the input-to-output voltage conversion ratio in order to achieve ZVS for all switches, and, neglecting the forward voltage drop of the diodes, can be expressed by

$$u_2 \geq \frac{C_\mathrm{T3} + C_\mathrm{D4}}{C_\mathrm{D4}} u_1 \,, \tag{1}$$

which reduces to $u_2 \geq 2u_1$ if $C_\mathrm{T3} = C_\mathrm{D4}$ applies. Where C_T3 and C_D4 denote the parasitic output capacitance of switch T_3 and the junction capacitance of diode D_4 respectively. Nonetheless, a unidirectional operation and voltage step-up ratios according to (1) are common in numerous applications, such as in module integrated converters for photovoltaic systems [15]–[17], fuel-cell based backup energy systems and uninterruptible power supplies [18], [19] as well as in automotive applications [20], [21].

The main focus of this paper is on the operation of the 3-switch CL-TCM converter topology shown in **Fig. 1(a)**. However, the ZVS modulation scheme can be extended to a 2-switch CL-TCM operation as well, where the high-side switch T_1 is replaced by a diode. This type of operation and the ZVS conditions are explained later in this section.

Note that both converter topologies allow to use a bootstrap gate drive power supply for the clamp-switch T_3 (cf. **Fig. 1(a)**), which simplifies the hardware complexity significantly.

A. 3-Switch CL-TCM Operation

First, the detailed principle of operation and ZVS modulation scheme is explained for the 3-switch CL-TCM converter, based on the operating states and the corresponding inductor current i_L and switch-node voltage u_{sw} waveform shown in **Fig. 2**.

A useful representation for the analysis of the ZVS operation of the converter is provided by the state-plane diagram [22], [23], which in this case displays the switch-node voltage u_{sw} with respect to the inductor current i_L scaled by the characteristic impedance of the resonant circuit formed by the inductor and the parasitic output capacitances of the switches and diodes, as shown in **Fig. 3(a)**. Assuming constant parasitic capacitances, the resonant voltage and current transitions are described with

$$\begin{aligned} Z_0 i_L(t) &= Z_0 I_{L,i} \cos(\omega_0 t) + (u_1 - U_{sw,i}) \sin(\omega_0 t) \\ u_{sw}(t) &= u_1 - (u_1 - U_{sw,i}) \cos(\omega_0 t) + Z_0 I_{L,i} \sin(\omega_0 t) \end{aligned} \quad (2)$$

which represents a circle with the center located at $Z_0 i_L = 0$ and $u_{sw} = u_1$. At the beginning of the resonant transition, the inductor current has the value $I_{L,i}$ and the switch-node voltage is $U_{sw,i}$. The radius of the circle can be expressed with

$$R = \sqrt{(u_1 - U_{sw,i})^2 + (Z_0 I_{L,i})^2}\,, \text{ with } Z_0 = \sqrt{\frac{L}{C_{tot}}}\,, \quad (3)$$

where C_{tot} is the total capacitance of the resonant circuit.

Despite of the non-linearity of the parasitic capacitance of the switches and diodes, the analysis provided in this paper considers constant capacitances only, in order to simplify the formalism and to give a meaningful insight into the operation of the converter. The analysis however could be extended to non-linear capacitances as well, as it is shown in [2], [13], [24]. Further it is assumed that the steady state input and output voltage u_1 and u_2 are constant, which is ensured by proper input and output filter design. The diode forward voltage drops are denoted with $u_{F,Dx}$ and $x \in [1, 4]$ and the turn-off process of each switch is considered to be free of power losses.

Starting with the first time interval $[t_0, t_1]$, switch T_2 is turned on and the body diode of switch T_3 is blocking the input voltage and prevents a short circuit of the input capacitor C_1. Hence, the inductor current rises linearly. The inductor current zero crossing is detected at t_0' in switch T_2 and is used to synchronize the switching times and the gate drive control signals s_i to the actual inductor current waveform as described in **Section IV**. Hence, the remaining inductor current build-up time interval T_{on}' (cf. **Fig. 1(a)**) and the time interval T_{off} are calculated such that the required average inductor current and the current $I_{L,0}$ needed at t_4 to allow for ZVS of the switches in the following time intervals, are achieved.

When the inductor current reaches the value $I_{L,1}$ at time t_1, switch T_2 is turned off and the inductor current starts to charge the parasitic output capacitance of switch T_2, while

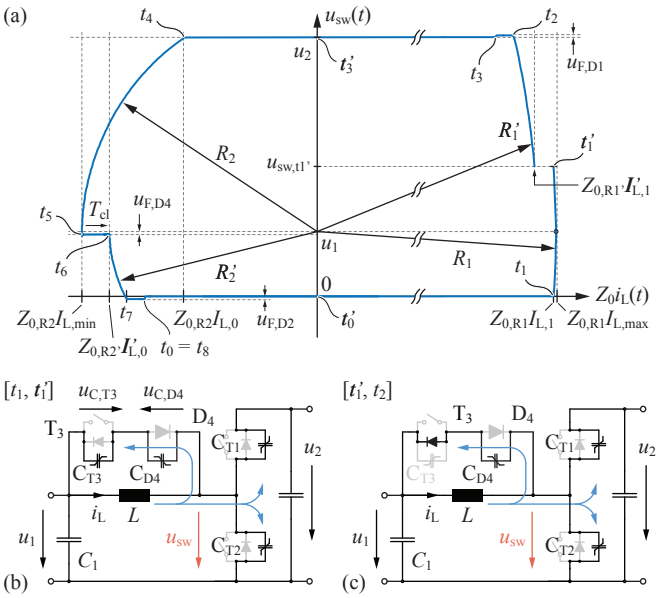


Figure 3: (a) state-plane diagram, showing the scaled inductor current $Z_0 i_L(t)$ with respect to the switch-node voltage $u_{sw}(t)$ for the 3-switch CL-TCM converter operation. (b)-(c) Operating states of the converter during the time interval $[t_1, t_1']$ and $[t_1', t_2]$ respectively.

discharging the output capacitance of T_1. Initially, the voltage across the parasitic capacitance $C_{T,3}$ is $(u_1 - u_{F,D4})$ and the voltage across diode D_4 is $-u_{F,D4}$. Hence, the parasitic output capacitance of switch T_3 is discharged and the junction capacitance of D_4 is charged, as shown in **Fig. 3(b)**. Due to the series connection of C_{T3} and C_{D4}, the total capacitance that needs to be charged by the inductor current is $C_{tot,R1} = C_{T1} + C_{T2} + C_{T3}C_{D4}/(C_{T3} + C_{D4})$. The resonant transition is described in the state-plane diagram with a circle around the center located at $u_{sw} = u_1$ and $i_L = 0$ and a radius given by

$$R_1 = \sqrt{u_1^2 + (Z_{0,R1} I_{L,1})^2}\,, \text{ and } Z_{0,R1} = \sqrt{\frac{L}{C_{tot,R1}}}\,. \quad (4)$$

The maximum inductor $I_{L,max} = R_1/Z_{0,R1}$ is reached as soon as the switch-node voltage u_{sw} is equal to the input voltage u_1. At time t_1', the switch-node voltage at which the voltage across T_3 approaches zero voltage and its body diode D_3 starts to conduct, can be calculated according to

$$\begin{aligned} u_{sw,t1'} &= \frac{C_{T3}+C_{D4}}{C_{D4}} (u_1 + u_{F,D3} - u_{F,D4}) \\ &\approx \frac{C_{T3}+C_{D4}}{C_{D4}} u_1 \end{aligned}\,, \quad (5)$$

if $u_{F,D3} \approx u_{F,D4}$ applies. Note that if $C_{D4} \gg C_{T3}$, the body diode of T_3 will start to conduct as soon as u_{sw} approaches u_1, where the inductor current reaches its maximum current $I_{L,max}$. In contrast, if $C_{T3} > C_{D4}$, the capacitance C_{T3} can be discharged to zero only if $(u_2 + u_{F,D1}) \geq u_{sw,t1'}$, which is equal to (1) if the forward voltage drop of the diodes are neglected. If the condition (1) is not met, soft-switching of switch T_3 cannot be achieved in the following operating states.

As soon as the body diode of T_3 starts to conduct, the total capacitance of the resonant circuit changes to $C_{tot,R1'} = C_{T1} + C_{T2} + C_{D4}$, as it is shown in **Fig. 3(c)**. Hence, the

characteristic impedance of the resonant circuit decreases, which appears as a discontinuity in the state-space trajectory as shown in **Fig. 3(a)**. The inductor current at time t_1' is given by

$$I'_{\mathrm{L},1} = \frac{1}{Z_{0,\mathrm{R1}}}\sqrt{R_1^2 - \left(u_{\mathrm{sw,t1'}} - u_1\right)^2}\,, \tag{6}$$

and hence, using $Z_{0,\mathrm{R1'}} = \sqrt{L/C_{\mathrm{tot,R1'}}}$, the radius R_1' can be calculated according to

$$R_1' = \sqrt{\left(u_{\mathrm{sw,t1'}} - u_1\right)^2 + \left(Z_{0,\mathrm{R1'}} I'_{\mathrm{L},1}\right)^2}\,. \tag{7}$$

If it is assumed that $u_{\mathrm{F,D3}} \approx u_{\mathrm{F,D4}}$ and $C_{\mathrm{T3}} = C_{\mathrm{D4}}$, the switch-node voltage at time t_1' is $u_{\mathrm{sw,t1'}} = 2u_1$ and the inductor current is $I_{\mathrm{L},1} = I'_{\mathrm{L},1}$, and hence, equation (7) is reduced to

$$R_1' \approx \sqrt{u_1^2 + \left(Z_{0,\mathrm{R1'}} I_{\mathrm{L},1}\right)^2}\,. \tag{8}$$

In this case, if the initial inductor current $I_{\mathrm{L},1}$ is large enough, C_{D4} is charged up to the voltage $(u_2 - u_1)$, assuming that the diode $\mathrm{D_4}$ and the body diode of switch $\mathrm{T_1}$ have the same forward voltage drop. At time t_2, the body diode of switch $\mathrm{T_1}$ starts to conduct and clamps the voltage across $\mathrm{T_1}$ to the diode forward voltage drop $u_{\mathrm{F,D1}}$. If the diode voltage drop $u_{\mathrm{F,D1}}$ is neglected, the condition for ZVS operation of switch $\mathrm{T_1}$ follows from $R_1' \geq (u_2 - u_1)$, and using (8), the condition can be expressed with

$$I_{\mathrm{L},1} \geq \frac{1}{Z_{0,\mathrm{R1'}}}\sqrt{u_2\left(u_2 - 2u_1\right)}\,, \quad \text{for} \quad (u_2 > 2u_1)\,. \tag{9}$$

If conditions (1) and (9) are met, switch $\mathrm{T_1}$ can be turned on at t_3 at nearly zero voltage and since the parasitic output capacitance of $\mathrm{T_3}$ was discharged completely during $[t_1, t_1']$, switch $\mathrm{T_3}$ can be turned on at any time between t_3 and t_4 without causing losses. The critical operating point, where ZVS of switch $\mathrm{T_1}$ could be lost is at minimum output power and maximum output voltage.

During time interval $[t_3, t_4]$ switch $\mathrm{T_1}$ is in on-state and the inductor current is supplied to the output and is decreasing linearly and reverses its flow direction at time t_3'.

At t_4, switch $\mathrm{T_1}$ is turned off and the negative inductor current $I_{\mathrm{L},0}$ starts to discharge the parasitic capacitances of switch $\mathrm{T_2}$ and diode $\mathrm{D_4}$, while charging the output capacitance of switch $\mathrm{T_1}$. Hence, during $[t_4, t_5]$, the total equivalent resonant capacitance is $C_{\mathrm{tot,R2}} = C_{\mathrm{tot,R1'}} = C_{\mathrm{T1}} + C_{\mathrm{T2}} + C_{\mathrm{D4}}$ and the resonant transition is described in **Fig. 3(a)** as a circle with a radius given by

$$R_2 = \sqrt{\left(u_2 - u_1\right)^2 + \left(Z_{0,\mathrm{R1'}} I_{\mathrm{L},0}\right)^2}\,. \tag{10}$$

As soon as the voltage u_{sw} reaches a value of $(u_1 - u_{\mathrm{F,D4}})$ at t_5, the diode $\mathrm{D_4}$ starts to conduct and the inductor clamping time interval $[t_5, t_6]$ is initiated. During this interval, the inductor current is free-wheeling in the clamp-switch and no energy is delivered from the input to the output of the converter. Hence, the clamping time interval can be used as a degree of freedom to control the switching period and the amount of power delivered to the load.

Due to the forward voltage drop of the diode $\mathrm{D_4}$, the inductor current is increasing with a slope of $\mathrm{d}i_L/\mathrm{d}t = u_{\mathrm{F,D4}}/L$, if the ohmic losses in the inductor current loop are neglected. This needs to be taken into account, specifically if the clamping time interval T_{cl} is large, since the inductor current amplitude at t_6, denoted with $I'_{\mathrm{L},0}$, could increase to a value where ZVS of switch $\mathrm{T_2}$ could not be achieved anymore at time t_8. The negative inductor current $I'_{\mathrm{L},0}$ at the turn-off of switch $\mathrm{T_3}$ at t_6 can be calculated with good approximation according to

$$I'_{\mathrm{L},0} \approx I_{\mathrm{L,min}} + \frac{u_{\mathrm{F,D4}}}{L} T_{\mathrm{cl}} \quad \text{and} \quad I_{\mathrm{L,min}} = -\frac{R_2}{Z_{0,\mathrm{R1'}}}\,. \tag{11}$$

During $[t_6, t_7]$, the inductor current continues discharging the parasitic output capacitance of switch $\mathrm{T_2}$ and charges the parasitic output capacitance of $\mathrm{T_1}$. The output capacitance of switch $\mathrm{T_3}$ is charged as well by part of the inductor current flowing through diode $\mathrm{D_4}$. Hence, the total equivalent resonant capacitance changes to $C_{\mathrm{tot,R2'}} = C_{\mathrm{T1}} + C_{\mathrm{T2}} + C_{\mathrm{T3}}$ and the radius R_2' in **Fig. 3(a)** is given by

$$R_2' = \sqrt{u_{\mathrm{F,D4}}^2 + \left(Z_{0,\mathrm{R2'}} I'_{\mathrm{L},0}\right)^2}\,, \text{ and } Z_{0,\mathrm{R2'}} = \sqrt{\frac{L}{C_{\mathrm{tot,R2'}}}}\,. \tag{12}$$

As soon as the switch-node voltage u_{sw} reaches a voltage of $-u_{\mathrm{F,D2}}$ at t_7, the parasitic output capacitance of switch $\mathrm{T_3}$ is charged up to the input voltage u_1 and the diode $\mathrm{D_4}$ stops conducting. At the same time, the body diode of switch $\mathrm{T_2}$ starts to conduct and the inductor current again starts to rise linearly as shown in **Fig. 2** in the time interval $[t_7, t_8]$. The switch $\mathrm{T_2}$ can then be turned on at nearly zero voltage as long as the inductor current is negative, since its body diode would prevent a current flow in the reverse direction and the parasitic output capacitance of $\mathrm{T_2}$ would be charged again as soon as the inductor current gets positive.

The condition for ZVS operation of switch $\mathrm{T_2}$ follows directly from condition $R_2' \geq u_1$ and is given by

$$I'_{\mathrm{L},0} \leq -\frac{1}{Z_{0,\mathrm{R2'}}}\sqrt{u_1^2 - u_{\mathrm{F,D4}}^2} \approx -\frac{u_1}{Z_{0,\mathrm{R2'}}}\,, \tag{13}$$

which is mainly dependent on the inductor current $I_{\mathrm{L},0}$ and the duration of the clamping time interval T_{cl}, if the input and output voltage are constant.

Note that if $u_2 \geq 2u_1$ applies and considering traditional TCM operation only, i.e. $T_{\mathrm{cl}} = 0$, a zero voltage transition of the switch-node voltage u_{sw} in the time interval $[t_3', t_7]$ can always be achieved, even when starting with an inductor current $I_{\mathrm{L},0} = 0$. This allows to reduce the converter hardware complexity further, by replacing the switch $\mathrm{T_1}$ by a single diode $\mathrm{D_1}$ as shown in **Fig. 4(a)**. This modification allows to increase the converter reliability as the number of active components in the circuit is reduced. However, the conduction losses are increased as well, but compared to the power losses occurring in the case of a hard-switched boost converter solution, the additional diode conduction losses are acceptable.

The operation principle, the limitations and the conditions for ZVS operation of the 2-switch CL-TCM converter are explained in the following, based on the state-plane diagram shown in **Fig. 4(b)**, which depicts the resonant transition during the time intervals with negative inductor current.

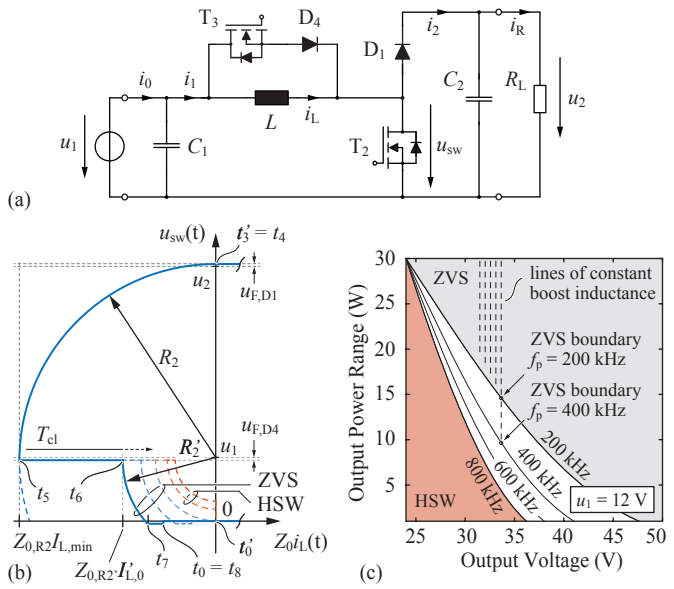


Figure 4: (a) 2-switch CL-TCM converter topology. (b) Associated state-plane diagram showing the resonant transition during the time intervals with negative inductor current. (c) Region of Zero-Voltage-Switching (ZVS) and Hard-Switching (HSW) operation for the 2-switch CL-TCM converter with respect to output power, for the converter designed for different output voltages and switching frequencies f_p in the range of 200 kHz to 800 kHz.

B. 2-Switch CL-TCM Operation

The states of operation during $[t_0, t_2]$ are the same as for the 3-switch CL-TCM converter. If condition (9) is met, diode D_1 starts to conduct at t_2 and the inductor current starts to decrease linearly. Switch T_3 can be turned on at any time between t_2 and t_3', without causing switching losses. At $t_3' = t_4$, when the inductor current reverses its flow direction, D_1 stops to conduct naturally and the resonant transition is initiated. The inductor current starts to charge the junction capacitance of D_1 and as soon as the switch-node voltage u_sw reaches a value of $(u_1 - u_{\mathrm{F,D4}})$, close to the minimum inductor current $I_\mathrm{L,min}$, the clamping time interval is started. The decrease of the switch-node voltage, as a result of D_1 blocking a current flow in the reverse direction, can be detected easily. Hence, also the start of the clamping time interval at t_5 can be detected without the need for an additional inductor current zero crossing detection and allows to simplify the controller implementation, as it is explained in detail in **Section IV**.

After the clamping time interval T_cl, switch T_3 is turned off and the inductor current further discharges the parasitic output capacitance of switch T_2. If the the negative inductor current $I'_{\mathrm{L},0}$ at t_6 is large enough, the voltage across T_2 is reduced to zero and at t_7 its body diode starts to conduct. Hence, switch T_2 can be turned on at nearly zero voltage at time t_8.

Since the inductor current $I_{\mathrm{L},0}$ at the beginning of the resonant voltage transition at t_4 is zero and cannot be controlled, the ZVS operation of switch T_2 at t_7 depends on the input-to-output voltage ratio, the characteristic impedance of the resonant circuit and on the duration of the clamping time interval T_cl, and hence also on the output power of the converter. The radius R_2 of the circle describing the resonant transition in the state-plane diagram in **Fig. 4(b)** is given by $R_2 = (u_2 + u_{\mathrm{F,D1}} - u_1)$ and hence, the minimum inductor current $I_\mathrm{L,min}$ can be expressed with

$$I_\mathrm{L,min} = -\frac{R_2}{Z_{0,\mathrm{R2}}}\,, \text{ and } Z_{0,\mathrm{R2}} = \sqrt{\frac{L}{C_\mathrm{D1} + C_\mathrm{T2} + C_\mathrm{D4}}}\,. \tag{14}$$

The radius R'_2 of the circle describing the resonant transition after the clamping time interval (cf. **Fig. 4(b)**) is given in (12), using $C_{\mathrm{tot,R2'}} = C_\mathrm{D1} + C_\mathrm{T2} + C_\mathrm{T3}$. In order to allow for ZVS for switch T_2 at time t_8, the condition $R'_2 \geq u_1$ must be fulfilled. By taking (11) for the inductor current $I'_{\mathrm{L},0}$ and assuming that $u^2_{\mathrm{F,D4}} \ll \left(Z_{\mathrm{Z0,R2'}} I'_{\mathrm{L},0}\right)^2$ applies in (12), the ZVS condition for T_2 can be expressed with

$$\frac{1}{Z_{0,\mathrm{R2}}}\left(u_2 + u_{\mathrm{F,D1}} - u_1\right) - \frac{u_{\mathrm{F,D4}}}{L} T_\mathrm{cl} \geq \frac{u_1}{Z_{0,\mathrm{R2'}}}\,. \tag{15}$$

If it is further assumed that $(u_2 + u_{\mathrm{F,D1}} - u_1) \approx (u_2 - u_1)$ and $Z_{0,\mathrm{R2}} = Z_{0,\mathrm{R2'}} = Z_0$, i.e. if $C_{\mathrm{T3}} = C_{\mathrm{D4}}$, condition (15) is simplified to

$$u_2 \geq 2u_1 + Z_0 \frac{u_{\mathrm{F,D4}}}{L} T_\mathrm{cl}\,. \tag{16}$$

Note that if the clamping-time interval $T_\mathrm{cl} = 0$, i.e. at maximum output power, expression (16) is reduced to the condition $u_2 \geq 2u_1$, which is equal to the ZVS condition of the traditional TCM operation with $i_{\mathrm{L},0} = 0$ [2].

As an example, **Fig. 4(c)** shows the ZVS boundary according to (16), where the 2-switch CL-TCM converter is designed according to (17)-(22), as described in **Section III-A**, for a fixed input-to-output voltage conversion ratio, a maximum output power of $P_\mathrm{max} = 30\,\mathrm{W}$, and a switching frequency f_p ranging from 200 kHz to 800 kHz. It is evident that at a voltage conversion ratio of $u_2 = 2u_1$, the 2-switch CL-TCM converter allows ZVS operation only at the specified maximum output power, which corresponds to the traditional TCM operation, and as soon as the output power is reduced, the introduction of the clamping time interval leads to hard-switching immediately. This is a main limitation of the 2-switch CL-TCM converter. However, at larger voltage conversion ratios, the output power range allowing for ZVS operation is extended significantly, and is highly dependent on the specified switching frequency and input voltage of the converter, as these parameters determine also the value of the boost inductance.

However, the 3-switch CL-TCM converter allows for ZVS operation even in the hard-switching region of the 2-switch CL-TCM converter, since it allows to adjust the negative inductor current $I_{\mathrm{L},0}$ accordingly in order to achieve zero-voltage-switching.

III. Operating Modes

In this section, two operating modes of either the 2-switch or 3-switch CL-TCM converter are outlined and equations for the calculation of the boost inductance value and the switching time intervals T_on, T'_on, T_off and T_cl are provided.

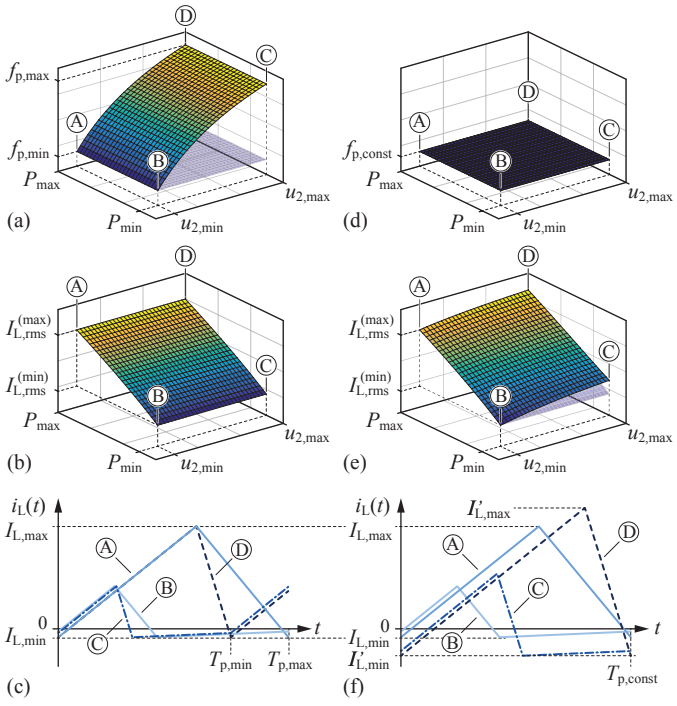


Figure 5: Switching frequency variation, inductor RMS current variation and inductor current waveforms for variable switching frequency operating (a)-(c) and for constant switching frequency operation (d)-(f).

A. *Variable Switching Frequency Operation*

The main objectives of the first mode of operation is the minimization of the switching frequency variation and the simultaneous minimization of the inductor RMS current for a variable output power $P \in [P_{2,\min}, P_{2,\max}]$ and a variable output voltage $u_2 \in [u_{2,\min}, u_{2,\max}]$. It is assumed that the input voltage u_1 has a constant value. As explained above, the clamping time interval $T_{\rm cl}$ is used as an additional degree of freedom to control the switching frequency variation of the converter. Considering the typical inductor current waveforms shown in **Fig. 1(b)** and **(c)**, it is beneficial to emulate TCM operation at maximum output power, i.e. by reducing the clamping time interval $T_{\rm cl}$ to zero [8], and hence reducing the inductor RMS current to a minimum, while maintaining ZVS operation. This however implies, that if the minimum inductor current $I_{\rm L,min}$ is fixed, the switching frequency will vary with changes of the input and/or the output voltage, due to the changing slopes of the inductor current. In contrast, if the terminal voltages are fixed and the output power is varied, the switching frequency can be maintained constant by introducing the clamping time interval. The inductor RMS current could be reduced only by increasing the switching frequency, while approaching the TCM operation again, which is not desirable in this case.

As reported in [8] for constant switching frequency operation, and assuming a lossless operation of the converter, i.e. $P_1 = P_2$, the inductor must be designed according to

$$L = \frac{u_1\,(u_{2,\min} - u_1)}{2u_{2,\min} f_{\rm p,min}\,(P_{1,\max}/u_1 - I_{\rm L,min})}\,, \tag{17}$$

in order achieve TCM operation at maximum output power and minimum output voltage $u_{2,\min}$. If, as described in the following, a variable switching frequency is allowed, the converter operates always at or above the minimum switching frequency $f_{\rm p,min}$.

For an accurate calculation of the switching time intervals $T_{\rm on}$, $T'_{\rm on}$, $T_{\rm off}$ and $T_{\rm cl}$, the increase of the minimum inductor current $I_{\rm L,min}$ to

$$I'_{\rm L,0} = I_{\rm L,min} + \frac{u_{\rm F,D4}}{L} T_{\rm cl}\,, \tag{18}$$

during the clamping time interval cannot be neglected. This is specifically the case for the operation at low output power and low output voltage when the clamping time interval $T_{\rm cl}$ is large. Assuming that the resonant voltage transition time intervals are much shorter than the switching period, the time interval $T_{\rm on}$ can be calculated for a desired average input current $I_{1,\rm avg} = P_1/u_1$ using

$$T_{\rm on} = \frac{L}{u_1}\sqrt{4I_{1,\rm avg}\left(\frac{P_{1,\max}}{u_1} - I_{\rm L,min}\right) + I_{\rm L,min}^2} - \frac{L}{u_1} I_{\rm L,min} - \frac{u_{\rm F,D4}}{u_1} T_{\rm cl}\,, \tag{19}$$

which is independent of the output voltage variation. The switching time intervals labeled with $T_{\rm off}$ and $T_{\rm cl}$ (cf. in **Fig. 1(b)** and **(c)**) are calculated according to

$$T_{\rm off} = \frac{T_{\rm on}\,(u_{\rm F,D4} - u_1) - T_{\rm p,P(max)} u_{\rm F,D4}}{u_1 - u_2 - u_{\rm F,D4}}\,, \tag{20}$$

$$T_{\rm cl} = T_{\rm p,P(max)} - T_{\rm on} - T_{\rm off}\,, \tag{21}$$

using the switching period $T_{\rm p}$, evaluated for the nominal input power $P_{1,\max}$, which follows from (17) and is given by

$$T_{\rm p,P(max)} = \frac{2u_2 L\,(P_{1,\max}/u_1 - I_{\rm L,min})}{u_1\,(u_2 - u_1)}\,. \tag{22}$$

After the clamping time interval, the inductor current starts rising from $I'_{\rm L,0}$ and at the current zero crossing at t'_0, the remaining on-time interval $T'_{\rm on}$ is set by the control circuit, which is calculated with

$$T'_{\rm on} = T_{\rm on} + \frac{L}{u_1} I_{\rm L,min} + \frac{u_{\rm F,D4}}{u_1} T_{\rm cl}\,. \tag{23}$$

Note that the switching time intervals are calculated iteratively, since the clamping time interval $T_{\rm cl}$ is not known initially. Hence, starting with $T_{\rm cl} = 0$ in (19), the switching time intervals (19)-(21) and (23) can be calculated within few iterations. In order to further improve the accuracy of the inductance and switching time interval calculations, the DC-DC efficiency $\eta_{\rm P(max)}$ at maximum output power can be estimated in advance and hence, the predicted maximum input power $P_{1,\max} = P_{2,\max}/\eta_{\rm P(max)}$ can be used in (17) and (19)-(22).

Using (17) and (22), the maximum switching frequency can be calculated according to

$$f_{\rm p,max} = f_{\rm p,min} \cdot \frac{u_{2,\min}}{u_{2,\max}} \cdot \frac{(u_{2,\max} - u_1)}{(u_{2,\min} - u_1)}\,, \tag{24}$$

which is obtained at maximum output voltage and is independent of the output power. Note that for large input to output voltage conversion ratios $u_2 \gg u_1$, the switching frequency variation is very small, i.e. $f_{\rm p,min} \approx f_{\rm p,max}$.

B. Constant Switching Frequency Operation

Generally, a varying switching frequency operation is not desired in EMI sensitive applications as it spreads the noise emissions over a wide spectral range and therefore complicates the filter design. Therefore, the second mode of operation allows to maintain a constant switching frequency by adjusting the clamping time interval and/or the minimum inductor current [8]. Note that this mode of operation cannot be achieved with the 2-switch CL-TCM converter, since the magnitude of the minimum inductor current $I_{\mathrm{L,min}}$ must be controllable.

The boost inductance can be calculated according to (17) with the desired constant switching frequency $f_{\mathrm{p,const}}$. In order to maintain the switching frequency while the output voltage is allowed to vary, the minimum inductor current $I_{\mathrm{L,min}}$ needs to be adjusted during the converter operation according to

$$I'_{\mathrm{L,min}} = \frac{u_1^2\,(u_1 - u_2) + 2L f_{\mathrm{p,const}} P_{1,\max} u_2}{2L f_{\mathrm{p,const}} u_1 u_2}\,. \qquad (25)$$

The switching time intervals T_{on}, T'_{on}, T_{off} and T_{cl} can then be calculated by inserting (25) into (18)-(23) and $T_{\mathrm{p,P(max)}} = 1/f_{\mathrm{p,const}}$ into (20)-(21).

In order to outline the differences of the variable and the constant switching frequency operation, the switching frequency variation, the RMS inductor current - which gives an indication for the converter power losses - and the typical inductor current waveforms are illustrated in **Fig. 5(a)-(f)** for both modes. The CL-TCM converter is operated with variable output voltage and variable output power, and is designed for the same minimum switching frequency. **Fig. 5(a)** shows the variation of the switching frequency for the first operating mode. The switching frequency is kept constant for a fixed voltage conversion ratio and increases with increasing output voltage. In contrast, the RMS inductor current remains constant for a fixed output power and variable output voltage and is increasing almost linearly with increasing output power and fixed output voltage, as it is shown in **Fig. 5(b)**. The inductor current waveforms for the converter operating points labeled with (A)-(D) are shown in **Fig. 5(c)**.

The constant switching frequency operating mode of the CL-TCM converter (cf. **Fig. 5(d)**) comes at the expense of an increased RMS inductor current at higher voltage conversion ratios, as it is shown in **Fig. 5(e)**. Hence, the converter power losses are increased at high output voltage, due to the larger peak-to-peak inductor current ripple shown in **Fig. 5(f)**, which is necessary to maintain the constant switching frequency. Therefore, this mode of operation should be used only for applications which inherently limit the variation of the input and output voltage to a narrow range or which have a large voltage conversion ratio.

In the following section, the controller implementation for the CL-TCM converter operated at variable switching frequency is explained in detail.

IV. Controller Implementation

A. 3-Switch CL-TCM Control

The inductor current zero crossing detection is the key feature that is required to implement the digital control of

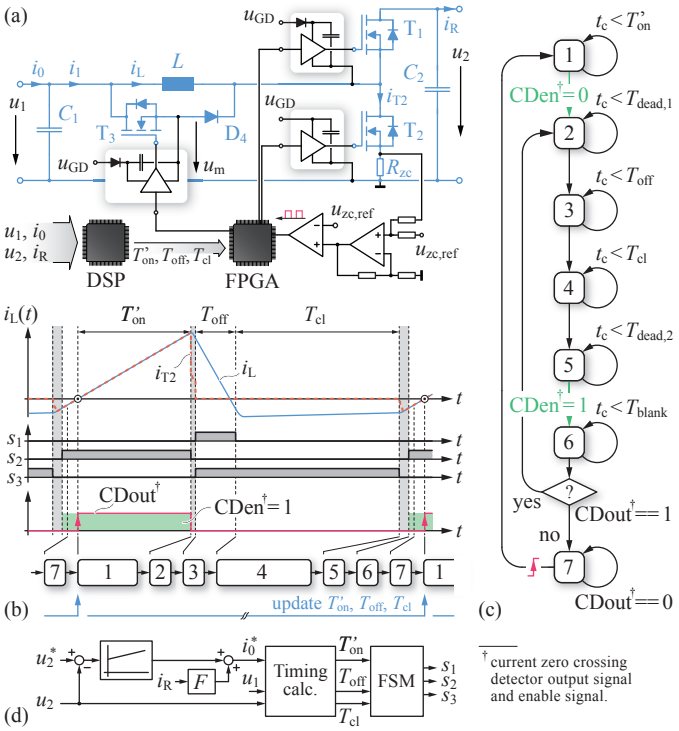


Figure 6: (a) Realization of the control circuit and current zero crossing detection for the 3-switch CL-TCM converter. (b) 3-switch CL-TCM current waveforms, modulator states and (c) modulator state machine. (d) 3-switch CL-TCM output voltage control with load current feed-forward.

the 3-switch CL-TCM converter. An effective implementation of the zero crossing detection is shown in **Fig. 6(a)**, where the low-side switch current i_{T2} is sensed in order to detect the current zero crossing at the rising edge of the inductor current, as it is illustrated in **Fig. 6(b)**. The timing values T'_{on}, T_{off} and T_{cl} are calculated by a Digital Signal Processor (DSP) and are transmitted to a Field Programmable Gate Array (FPGA), which implements the modulator Finite State Machine (FSM) shown in **Fig. 6(c)** and which generates the gate control signals s_i, $i \in [1,3]$. A counter t_{c} within the FPGA is used to set the duration of the switching time intervals. After the on-time T'_{on} in state 1 has expired, the current zero crossing detector is disabled and the modulator enters state 2, which sets the first dead-time interval $T_{\mathrm{dead,1}}$ for the switches. In state 3, switch $\mathrm{T_1}$ and $\mathrm{T_3}$ are enabled and with the expiration of T_{off}, the modulator enters the clamping time-interval in state 4, followed by the second dead-time interval in state 5. After the dead-time, switch $\mathrm{T_2}$ is turned on and the current zero crossing detector is enabled. However, its output is blanked in the first place in order to prevent the detection of an erroneous current zero crossing due to the charging of the boot-strap capacitors of the high-side gate drivers or due to a hard-switching event at the turn-on of switch $\mathrm{T_2}$. After the blanking time interval, which can be as short as 100 ns, the current zero crossing detector output signal is evaluated. If the detector output is indicating that the inductor current is already positive, the state machine continues with state 2 in order to reduce the inductor current until its value is below zero when exiting

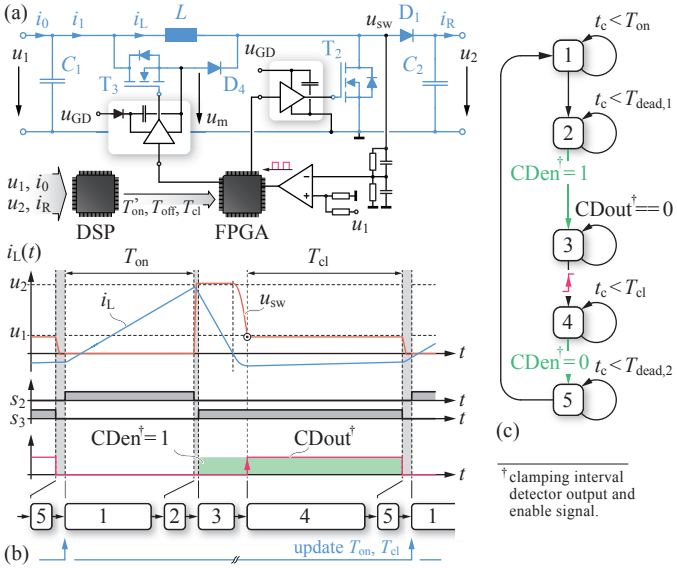
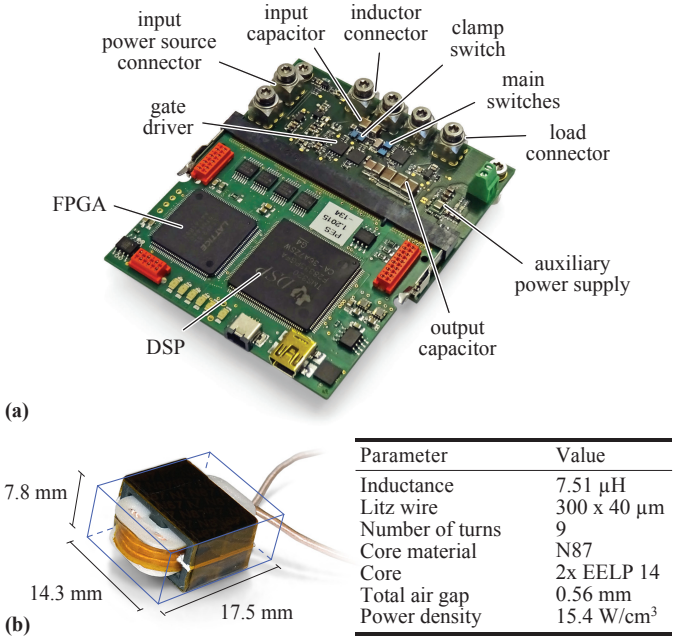


Figure 7: (a) Realization of the control circuit for the 2-switch CL-TCM converter. (b) 2-switch CL-TCM current/voltage waveforms, modulator states and (c) modulator state machine.



Parameter	Value
Inductance	7.51 µH
Litz wire	300 x 40 µm
Number of turns	9
Core material	N87
Core	2x EELP 14
Total air gap	0.56 mm
Power density	15.4 W/cm³

Figure 8: (a) Hardware prototype of the CL-TCM converter including the FPGA/DSP control board. (b) Realization and technical specifications of the inductor used for the measurements.

state 6. If the inductor current is negative at the end of state 6, the modulator enters state 7 and waits for the detection of the current zero crossing, which then triggers the start of the modulation sequence from the beginning.

A very simple and effective implementation of the output voltage control of the converter is shown in **Fig. 6(d)**. A single PI-controller and a load current feed-forward is used to set the input current target i_0^*. Since the inductor current can be controlled directly cycle by cycle, the converter allows for a highly dynamic operation. However, since the evaluation of the timing values is computationally expensive, the values T'_{on}, T_{off} and T_{cl} may be updated only every n-th cycle, i.e. the modulator state machine runs with the same set of timing values for few switching cycles until the values are updated at the beginning of the first state (cf. **Fig. 6(b)**). Further note that for the controller implementation it is not necessary to calculate the timing values iteratively for every update, since the iteration process is performed within the periodic control sequence, using the last clamping time interval T_{cl} as initial condition for the next timing calculation.

Another solution to determine the timing values is to generate a look-up table with pre-calculated timing values and to interpolate the actual values online, according to the look-up table and the measured input and output voltage and the input current set-point.

B. 2-Switch CL-TCM Control

The realization of the control circuit of the 2-switch CL-TCM converter is shown in **Fig. 7(a)**. In this case, the synchronization of the modulator state machine to the inductor current can be realized with very little hardware effort. As shown in **Fig. 7(b)**, if the current in D_1 reaches zero within the falling edge of the inductor current, D_1 stops to conduct and the switch-node voltage u_{sw} starts to decrease. As soon as the switch-node voltage falls below the input voltage u_1, D_4 starts to conduct and initiates the clamping time interval. As a main advantage of the 2-switch topology, the start of the clamp-switch time interval can be detected easily by comparing the switch-node voltage u_{sw} with the input voltage u_1, as shown in **Fig. 7(b)**, using a comparator circuit with a propagation delay as small as 5 ns and a very low hardware effort.

The modulator state machine is shown in **Fig. 7(c)**. After the pre-calculated on-time T_{on} and the first dead-time interval have expired, the clamping interval detector is enabled and switch T_3 is enabled. The decreasing inductor current is supplied to the output via diode D_1 and the modulator state machine waits in state 3 for the rising edge of the detector output signal, indicating that the clamping interval is initiated. After the clamping time interval T_{cl} has expired, T_3 is turned off and after a short dead-time interval, the control sequence starts from the beginning. The output voltage control of the 2-switch CL-TCM converter can be implemented as shown in **Fig. 6(d)**.

In the following section, the operating modes and the ZVS operation of the CL-TCM converter are verified experimentally using a hardware prototype.

V. Measurements

Fig. 8(a) shows the hardware prototype of the CL-TCM converter. The EPC2016C GaN FETs are used for the switches T_1-T_3, operated with the half-bridge gate driver LM5113. For the diode D_4 the Schottky diode MBR1H100SFT3G was used because of its low forward voltage drop and is also placed in anti-parallel configuration with each GaN FET. Note that the prototype includes a GaN FET in parallel to D_4 as well, in order to allow for the 4-switch CL-TCM operation presented in [13], which however is turned off permanently during the 2-switch and 3-switch CL-TCM converter measurements. The converter is controlled with a DSP/FPGA board comprising a

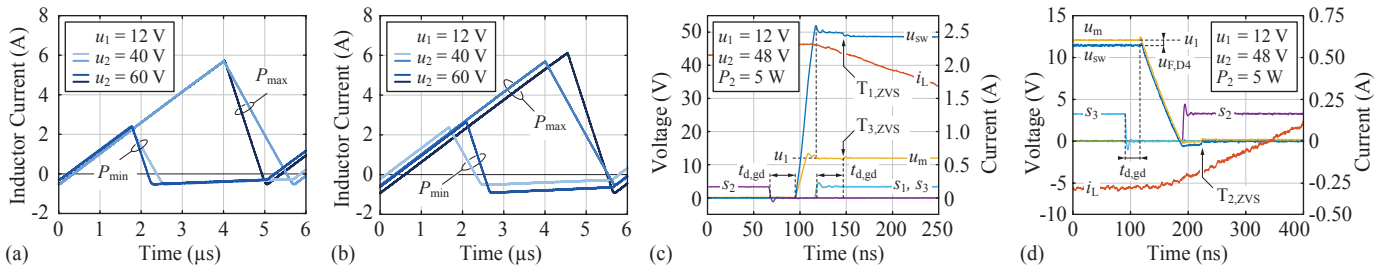


Figure 9: Measurement of the inductor current waveform for the variable switching frequency operation (a) and constant switching frequency operating mode (b) of the 3-switch CL-TCM converter. (c)-(d) Verification of the ZVS operation of the switches T_1, T_3 and T_2 respectively.

Texas Instruments TMS320F28335 DSP and a Lattice LFXP2-5E FPGA. The specifications and the realization of the inductor used for the measurements are shown in **Fig. 8(b)**.

During the measurements, the converter was operated in open-loop mode and the timing values for the modulator state-machine are calculated offline. The input voltage is set to a constant value of 12 V. The output voltage range is set to 40-60 V, with a nominal output voltage of 48 V, as typical e.g. for telecom applications, and the output power range is set to 5-30 W. **Fig. 9(a)** shows the inductor current waveform for the variable switching frequency operating mode of the 3-switch CL-TCM converter. It can be seen that the switching frequency varies only by a factor 1.14 between 175 kHz and 199 kHz, which is due to the large voltage conversion ratio. In **Fig. 9(b)**, the inductor current waveforms are shown for constant switching frequency operation and the increased peak-to-peak inductor current ripple at the higher output voltage is clearly evident. In this case however, the RMS inductor current is only a factor of 1.03-1.23 higher compared to the variable frequency operating mode.

The ZVS operation of the switches T_1-T_3 is shown in **Fig. 9(c)** and **(d)** for an output voltage of 48 V and at minimum output power. In **Fig. 9(c)** the resonant voltage transition of the switch-node voltage u_{sw} is shown at the maximum inductor current. The voltage transition is initiated with the turn-off the switch T_2 after a gate drive propagation delay $t_{d,gd}$ of approximately 27 ns. The inductor current is large enough to discharge the parasitic output capacitance of switch T_1 well within the dead-time interval of 50 ns. The output capacitance of switch T_3 is discharged even faster as indicated by the clamp-switch midpoint voltage u_m. Hence, the two switches T_1 and T_3 can be turned on simultaneously after the dead-time interval without causing switching losses. At the end of the clamping time interval shown in **Fig. 9(d)**, the resonant voltage transition is initiated with the turn-off of switch T_3. The negative inductor current discharges the parasitic output capacitance of switch T_2 until its diode starts to conduct. Accordingly, switch T_2 can be turned on at nearly zero voltage after the dead-time interval of 100 ns.

The results for the 2-switch CL-TCM converter operation are shown in **Fig. 10** for a fixed input and output voltage of 12 V and 48 V respectively. **Fig. 10(a)** shows the measured inductor current waveforms for variable output power and **Fig. 10(b)** shows the verification of the calculation of the switching time intervals according to (14) and (19)-(22).

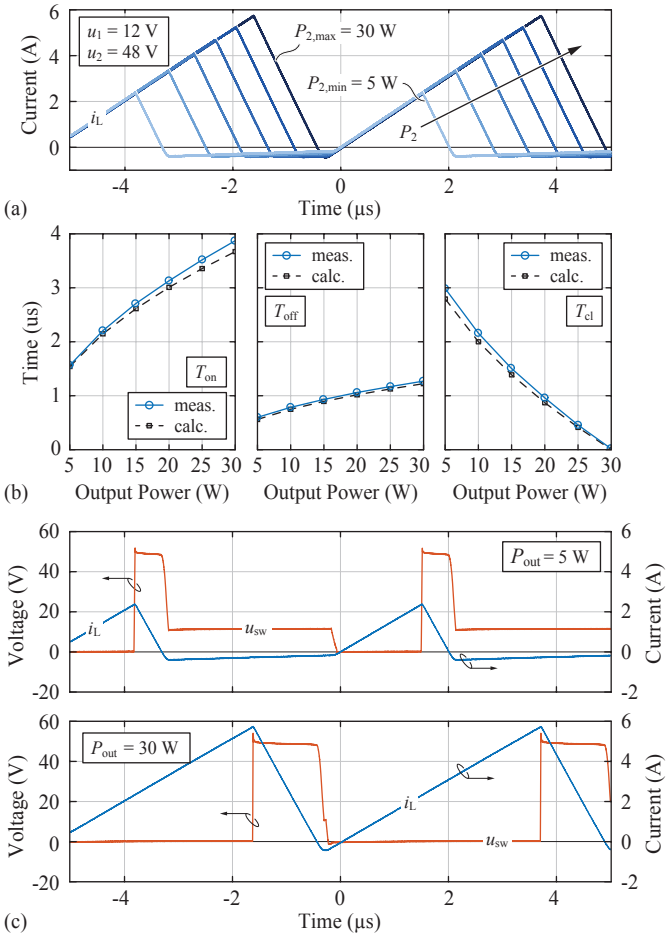
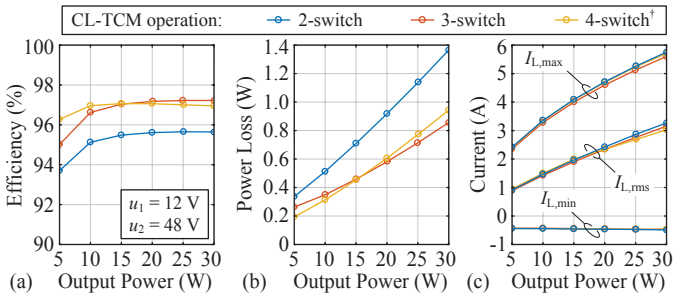


Figure 10: (a) Measurement of the inductor current waveforms for the 2-switch CL-TCM converter operation for fixed input/output voltages and variable output power. (b) Measured and calculated switching time intervals T_{on}, T_{off} and T_{cl}. (c) Measured waveforms of the switch-node voltage u_{sw} and the inductor current waveform for minimum and maximum output power.

In order to simplify the calculation, it is assumed that the converter causes no power losses and that the capacitances C_{D1}, C_{T2} and C_{D4}, used in (14), have a value of 352 pF, which is the total charge equivalent capacitance [24] of the EPC2016C GaN FET in parallel to the Schottky diode at an output voltage of 48 V. For the diode forward voltages a value of 0.6 V is used, which is the typical forward voltage drop of the Schottky diode MBR1H100SFT3G at 300 mA and 25 °C. The measured waveforms of the switch-node voltage u_{sw} and



†4-switch CL-TCM operation according to [12] and [13].

Figure 11: (a)-(b) Measured DC-DC efficiency and power loss at variable output power, for the proposed 2-switch and 3-switch CL-TCM operation as well as for the 4-switch CL-TCM operation explained in [12], [13]. Note that these measurements do not include the constant power loss of the DSP/FPGA control board. (c) Measured minimum, maximum and RMS inductor current.

the inductor current i_{L} are shown in **Fig. 10(c)** for minimum and maximum output power.

The measured DC-DC efficiency and the power loss of the proposed converter operations are shown in **Fig. 11(a)** and **(b)** respectively. The input and output power is calculated, based on the measurement of the terminal voltages and currents using Agilent 34410A multimeters. The power loss caused by the current and voltage measurement circuits, which amount to 37.2 mW and the gate-drive power losses are measured separately and are included in the total power loss and efficiency calculation. However, the measurements do not include the constant power loss of 994 mW caused by the DSP/FPGA control board, since it is not optimized for the hardware prototype at hand and it could be designed with significantly reduced footprint and power loss.

As shown in **Fig. 11(a)**, a maximum efficiency of 97.2 % was obtained for the 3-switch CL-TCM operation at maximum output power. The efficiency of the 2-switch operation is almost 1.5 % lower compared to the 3-switch operation, which is due to the conduction losses caused in diode D_1. It is important to note, that the diodes used in the hardware prototype are intended to lower the voltage drop across the GaN switches during the short dead-time interval and are not suited to carry the inductor current for a much longer time. Therefore, a more suitable diode such as the V10PL45-M3 Schottky rectifier diode could be used for D_1 to improve the efficiency of the 2-switch CL-TCM converter.

In order to provide a complete comparison, the DC-DC efficiency is measured as well for the 4-switch CL-TCM converter operation proposed in [13]. It can be seen in **Fig. 11(a)** that the 4-switch CL-TCM converter achieves a higher efficiency at low output power when compared to the 3-switch operation, which is due to the decreased power losses occurring during the clamping time interval. However, at maximum output power, the 4-switch CL-TCM converter shows a lower performance, because of the increased diode conduction power loss during the dead-time intervals.

The minimum and maximum inductor current, as well as the RMS inductor current is shown in **Fig. 11(c)** for each converter operation. The minimum inductor current cannot be controlled for the 2-switch CL-TCM converter operation and therefore, the same negative current was chosen for the 3-switch and 4-switch CL-TCM converter operation, in order to achieve the same operating frequency, which is in a range of 187-194 kHz. As expected, the maximum and the RMS inductor current do not significantly differ among the different CL-TCM converter operations. Hence the main differences in the power loss measurement mainly arise from the different diode conduction losses and also from the different gate-drive power losses, as the number of active switches varies for the different CL-TCM converters.

VI. Conclusions

The CL-TCM DC-DC boost converter allows for ZVS of all switches and offers a significantly reduced switching frequency variation when compared to the traditional TCM operation [13], which in turn simplifies the filter design in EMI sensitive applications and relaxes the requirements for the digital control.

In this paper, two CL-TCM boost converter topologies with reduced hardware complexity and its ZVS modulation schemes are proposed. Additionally, the limitations for ZVS operation, the timing calculations and the controller implementation are presented and analyzed in detail for both converter topologies. The reduced complexity of the CL-TCM converter hardware and modulation scheme, however, comes at the expense of a unidirectional power flow and a restriction on the minimum input-to-output voltage conversion ratio, which is required to ensure ZVS operation for all the switches.

In addition to the ZVS modulation schemes, two operating modes of the CL-TCM converter are compared in this paper. The first operating mode allows for minimum switching frequency variation and a minimized RMS inductor current, which is achievable with both the 2-switch and the 3-switch CL-TCM converter. The second mode of operation allows for constant switching frequency operation and is achieved with the 3-switch CL-TCM converter only, because it allows to control the negative inductor current. However, the constant switching frequency operation has limitations regarding the converter efficiency, since the RMS inductor current increases as the output voltage is increased. Hence, this mode of operation is intended mainly for applications requiring a small input or output voltage operating range or a high voltage conversion ratio.

It is important to note that the modulation scheme and the operating modes presented in this paper are not limited to CL-TCM boost converters only, but could be adapted easily for an unidirectional buck-type CL-TCM converter operation as well. Further note that the CL-TCM converter topologies presented in this paper and in [13] deliver their benefits specifically in applications with higher output voltage and higher output power, where the control power losses are negligible.

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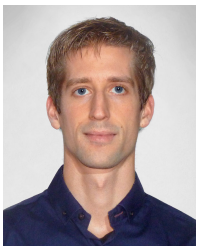

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