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Zero-Voltage-Switching Auxiliary Circuit for Minimized Inductance Requirement in Series-Resonant DC/DC Converter Systems

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Zero-Voltage-Switching Auxiliary Circuit for Minimized Inductance Requirement in Series-Resonant DC/DC Converter Systems

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***Abstract*—For power electronic converter systems, the cost and the size of the magnetic components are typically limiting factors when it comes to overall production costs and power density. This especially holds for soft-switching high-frequency applications, where a resonant discharge of the output capacitances of the semiconductors relies on sufficient amount of energy stored in the main magnetic components, i.e. inductors or transformers, yielding a substantial increase in their volumes. In this paper, an alternative solution is introduced, where a small auxiliary circuit is used to ensure soft-switching of the power transistors, whereby the aforementioned volume of the main magnetic components can be significantly reduced. The proposed auxiliary circuit provides zero-voltage-switching conditions independent of the applied voltages, the switching frequency and the output power level, without significantly increasing the circuit complexity or the control effort. The new concept is first analyzed based on simple analytical calculations and circuit simulations, and is then experimentally verified by means of hardware demonstrators related to a 3.6kW 250...500V/250...500V series-resonant DC/DC converter application. Finally, it is shown that the auxiliary circuit can also be used to pre-charge the output capacitor of a converter system, which allows to further reduce the size of the main magnetic components.**

***Index Terms*—soft-switching, auxiliary circuit, pre-charging circuit.**

I. Introduction

In recent years, the general trend towards greater electrification in transportation gave rise to a substantial increase in demand for electric vehicles (EVs). Consequently, due to the enormous commercial potential in the automotive sector, a competitive market evolved for all different kinds of power electronic converter systems, which are finally employed in EVs, such as e.g. battery chargers, DC/AC inverters and isolated DC/DC step-down converters. Hence, each of these converters needs to be optimized with respect to cost, power density and efficiency in order to develop competitive products. Some of the most expensive and most bulky parts in these converter systems are the magnetic components, i.e. the inductors and the transformers, which is why the converter systems should be designed in such a way, that the magnetic components can be built using low-cost technologies and are showing a low volume. Nowadays, PCB integration of the windings of the magnetic components is considered to be the most cost-effective solution, as the expensive wire-wrapping process is omitted and huge current densities can be allowed.

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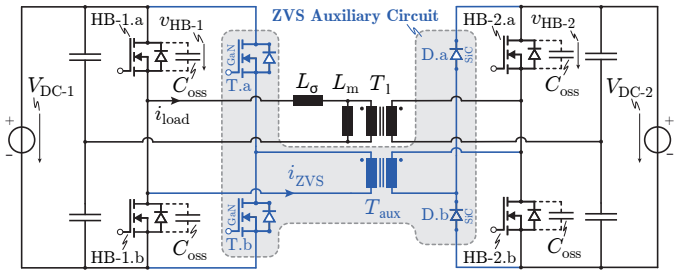


Fig. 1. Topology of a conventional series-resonant converter (SRC) with the main transformer T_1, the series-resonant inductance L_σ and two capacitive voltage dividers, which are used as resonant capacitors. Furthermore the grey-shaded components correspond to the proposed additional zero-voltage-switching (ZVS) auxiliary circuit, which comprises an active GaN half-bridge, a passive half-bridge with SiC diodes, as well as a small auxiliary transformer T_{aux}.

Unfortunately, it is extremely challenging to achieve large inductance values with a reasonable efficiency in PCB-integrated magnetics [1]–[3], which is why the inductance requirements in such converter systems should be minimized. However, the actual size of the magnetic components mainly depends on two factors: The maximum output power of a considered converter system and the amount of magnetic energy, which needs to be stored temporarily. Especially the later has a huge impact on the volume of the magnetic components and highly depends on the selected topology and the switching frequency, as a high switching frequency generally reduces the amount of magnetic energy which needs to be stored intermediately [4]. However, this unfortunately is not the only aspect, as in high-frequency (HF) applications zero-voltage-switching (ZVS) of the power switches is absolutely necessary for an efficient converter operation, which needs to be ensured by means of additional magnetic energy, stored in one of the main magnetic components [5]. This additional energy, in turn, increases the volume of the respective main magnetic component, which is why a high switching frequency does not necessarily result in smaller magnetic components [6], [7]. In order to clarify this statement, the ZVS operation of power switches is explained based on the simple series-resonant converter (SRC) topology shown in **Fig. 1**. For simplicity reasons, and without loss of generality, it is assumed that the converter is operated as a so-called DC-transformer, i.e. with unity voltage transfer ratio. Accordingly, a turns ratio of $n = 1 : 1$ and a switching frequency close to the

TABLE I. Specifications of a 3.6 kW DC-Transformer for Automotive Applications.

Input Voltage	$V_{\mathrm{DC}-1}$	250 V...500 V
Output Voltage	$V_{\mathrm{DC}-2}$	250 V...500 V
Output Power	P_{out}	0 W...3.6 kW

resonant frequency f_{res} is selected, such that the primary side referred output voltage $n \cdot V_{\mathrm{DC}-2}$ follows the input voltage $V_{\mathrm{DC}-1}$. This converter could e.g. be used as an isolation stage between the high-voltage battery and a non-isolated single-stage charger in an EV [8], according to the exemplary specifications summarized in **Tab. I**. Consequently, there are two possibilities to achieve ZVS of the power switches HB-1.a and HB-1.b in this converter: Either the magnetic energy stored in L_σ due to i_{load} is used to charge/discharge the C_{oss} of the power switches [6], or the magnetizing inductance is reduced and the resulting magnetizing current can be used to guarantee ZVS of the power switches [7]. Hence, for both methods, the power switches can be turned on with discharged output capacitors, whereby the voltage across the switches is almost zero and the switching operation can be assumed to be loss-less. Nevertheless, both of the aforementioned ZVS methods have their benefits and drawbacks, which will be discussed in the following.

In the first case, as the load current i_{load} is used for the ZVS transition, the Q_{oss} of the power switches is transferred to the secondary side as active power, which is why there are hardly any additional conduction losses induced for achieving ZVS. However, the required minimum peak current $i_{\sigma,\mathrm{pk}}$ at the beginning of the ZVS transition highly depends on the momentary DC-link voltage $V_{\mathrm{DC}-1}$, the employed series-resonant inductance L_σ and the nonlinear C_{oss} behavior and/or type of the employed power switches, as shown in **Fig. 2a** and **b** for an exemplary super-junction silicon MOSFET with an extremely non-linear $C_{\mathrm{oss}}(V_{\mathrm{ds}})$, and an exemplary GaN HEMT with a comparably flat $C_{\mathrm{oss}}(V_{\mathrm{ds}})$ curve. For this reason, either large inductance values L_σ have to be used, which are very difficult to achieve in PCB-integrated magnetics, or ZVS can only be achieved for the highest output power values, where sufficient i_{load} is available.

Alternatively, the magnetizing current can be used, which ensures ZVS independent of the output power. However, the magnetizing current is linearly increasing with the DC-link voltage, and for high switching frequencies, where short dead times t_{dead} need to be achieved, large magnetizing currents $i_{\mathrm{m,pk}}$ during the dead times are required (cf. **Fig. 2c** and **d**). Besides potential fringing losses around the additional air gap in the transformer core [9] (required for achieving a sufficient magnetizing current), the magnetizing currents yield significant additional conduction losses, as this current results in reactive power, which circulates on the primary side of the converter and does not contribute to the power transfer to the output. Furthermore, this concept can only be used efficiently in applications with a fixed switching frequency, as otherwise, ZVS would only be achieved for the lowest switching frequencies, since the amplitude of the magnetizing current decreases inversely proportional to the switching frequency.

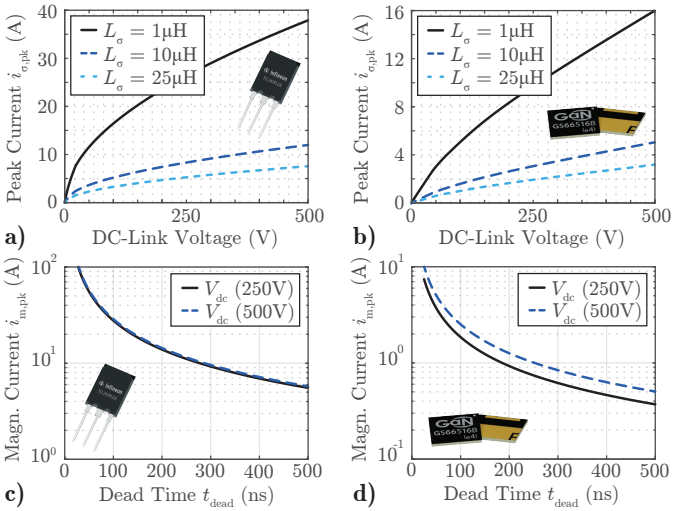


Fig. 2. a) Numerically calculated required peak currents to guarantee complete soft-switching of IPW60R018CFD7 silicon (Si) superjunction MOSFETs for three different series-resonant inductor values and **b)** the same currents for GS66516B gallium nitride (GaN) switches. **c)** Numerically calculated required magnetizing current to guarantee complete soft-switching within a certain dead time t_{dead} for the Si power transistor considered in **a)** and **d)** the same graphs for the GaN switch of **b)**.

In order to overcome these limitations, different possible alternatives have already been proposed in literature [10], [11], where auxiliary circuits are used to guarantee ZVS of the power semiconductors. However, most of the solutions which are based on passive components suffer from exactly the same issues as the approach, where the magnetizing current is used for ZVS. Thus, the reactive power, which is circulating in the auxiliary circuit, depends on the switching frequency and the converter port voltage and can therefore not be controlled. Consequently, significant conduction losses usually arise in applications with widely varying port voltages and/or switching frequencies. In contrast, most active ZVS auxiliary circuits guarantee load independent ZVS conditions and some of them can even operate with varying switching frequencies. However, they struggle to ensure ZVS conditions for the power switches in an efficient way, if a wide port voltage range needs to be covered, as in principle, they are based on the same idea as using the circulating magnetizing current in the transformer. Thus, they generate a controllable triangular or trapezoidal reactive current, which is used for charging/discharging the C_{oss} of the power switches. Furthermore, the active ZVS auxiliary circuits are often bound to one specific converter topology, as they rely on a certain way the main converter is controlled.

Consequently, a ZVS concept would be desirable, which can be operated with an arbitrary switching frequency, an arbitrary port voltage, works independent of the output power, only processes the absolutely necessary power to ensure ZVS, and ensures perfectly synchronized primary- and secondary-side switch-node voltages. The synchronization is important, such that only minimal voltage time areas across the series-

resonant inductor L_σ are applied, whereby this inductance can be extremely small and, in addition, a fast dynamic response of the DC-transformer is ensured. Fortunately, all this can be achieved by introducing a small ZVS auxiliary circuit as shown in **Fig. 1**, which comprises two additional small active switches T.a and T.b, a small auxiliary transformer T_{aux}, as well as two passive diodes D.a and D.b. Even though in this paper, the auxiliary circuit is explained based on the simple 1:1 DC transformer example, it can of course also be applied to converter systems with different topologies, different input to output voltage ratios and unequal primary and secondary side switches.

In **Section II**, the operating principle of the proposed auxiliary circuit is explained based on an exemplary switching transition. Subsequently, the impact of different semiconductor materials of the power switches on the performance of the auxiliary circuit is investigated in detail. Furthermore, in **Section III**, the arising losses in the proposed circuit are investigated based on simplified analytical calculations. Finally, the performance of the ZVS auxiliary circuit is experimentally verified in **Section IV** and the paper is concluded in **Section V**.

II. ZVS Auxiliary Circuit Operation

In order to explain the general idea and the operation of the proposed ZVS auxiliary circuit, an exemplary switching transition of the converter, shown in **Fig. 1**, is investigated in detail in the following section.

A. Exemplary ZVS Transition

Assuming an initial condition according to t_1 in **Fig. 3b**, where the voltages $v_{\text{HB}-x}, x \in \{1, 2\}$ across the switches are equal to V_{DC}, the Q_{oss} stored in the C_{oss} of HB-1.a needs to be transferred to the C_{oss} of HB-2.b, such that both, $v_{\text{HB}-1}$ and $v_{\text{HB}-2}$ drop to zero. Consequently, T.a needs to be turned on in order to apply $v_{\text{HB}-1}$ to the auxiliary transformer, whereby the resulting voltage difference between the applied voltage on the primary side of the transformer ($v_{\text{p}} = V_{\text{DC}}$) and the voltage on the secondary side of the transformer ($v_{\text{s}} = 0\,\text{V}$) initiates a current i_{ZVS} through the leakage inductance L_{ZVS} of the auxiliary transformer. This current then starts to discharge the C_{oss} of HB-1.a and to charge the C_{oss} of HB-2.b, as desired. It should be noticed, that the C_{oss} of the power switches of the primary and secondary side of the converter, together with the leakage inductance L_{ZVS} of the auxiliary transformer, form a resonant circuit, whereby no active control is required and the transfer of the Q_{oss} from the primary to the secondary side switches is inherently regulated by means of the circuit design. Therefore, as soon as the complete Q_{oss} of HB.1a is transferred to the secondary side and thus, $v_{\text{HB}-1}$ and i_{ZVS} drop to zero, the diode D.b would ideally start to block and $i_{\text{ZVS}}(t > t_2)$ would remain zero. Unfortunately, like every semiconductor device, the diode has a certain parasitic capacitance C_{diode}, which needs to be charged in order to build up the blocking voltage across the device. As a result, a current $i_{\text{C,diode}}$ is required for charging the C_{diode} of D.b from $0\,\text{V}$ to V_{DC}. At $t = t_3$, the voltage across D.b reaches

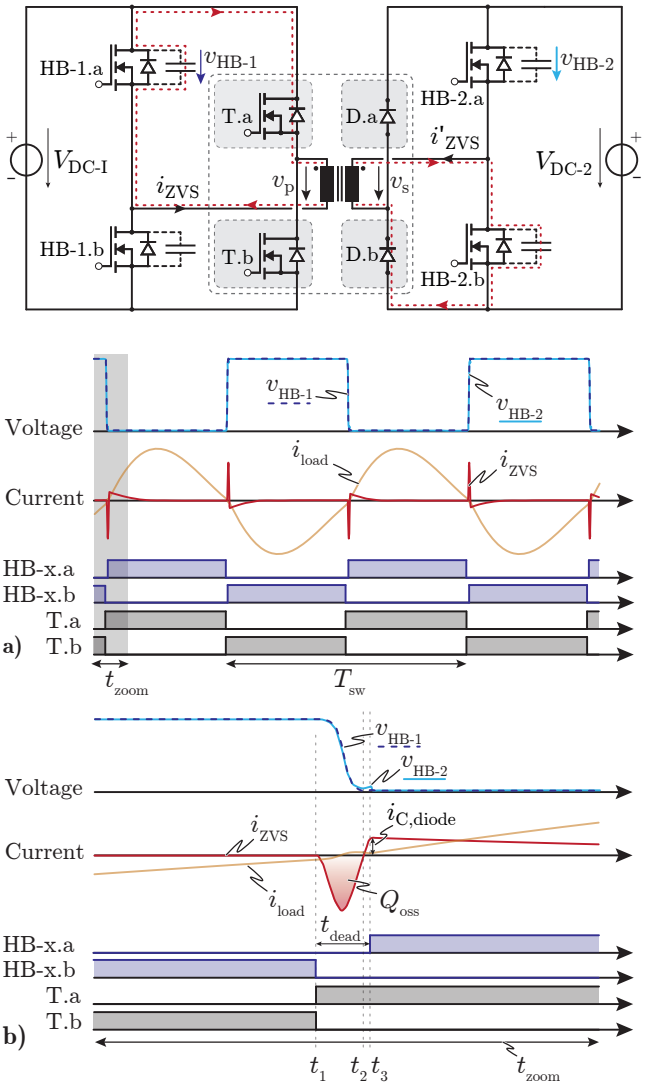


Fig. 3. Simplified converter topology, which is used for investigating the ZVS auxiliary circuit operation, where the capacitive voltage dividers, the leakage inductance L_σ, and the main transformer T_1 are not shown for the sake of clarity. **a)** Current and voltage waveforms as well as the gate signals of the SRC and the ZVS auxiliary circuit (cf. **Fig. 1**). **b)** Zoomed-in view of a single switching transition.

V_{DC} and i'_{ZVS} commutates from D.b to D.a. This current then circulates in L_{ZVS} and, as the voltage on both sides of the transformer is almost $0\,\text{V}$, its magnitude drops only slowly. As $i_{\text{ZVS}}(t > t_2)$ is not used for the ZVS transition and does only contribute additional conduction losses to the auxiliary circuit, diodes with minimum C_{diode} should be employed in order to minimize the required $i_{\text{C,diode}}$.

However, at $t = t_3$, the ZVS transition is theoretically completed and the next ZVS transition can be initiated after $T_{\text{sw}}/2$ by switching off T.a and turning on T.b.

B. Effect of Different Types of the Power Switches

In a real application, the aforementioned $L_{\text{ZVS}} - C_{\text{oss}}$ resonant circuit is nonlinear, as the output capacitance C_{oss} of semiconductors highly depends on the applied voltage and the employed type of switch (cf. **Fig. 4a**). Consequently, the

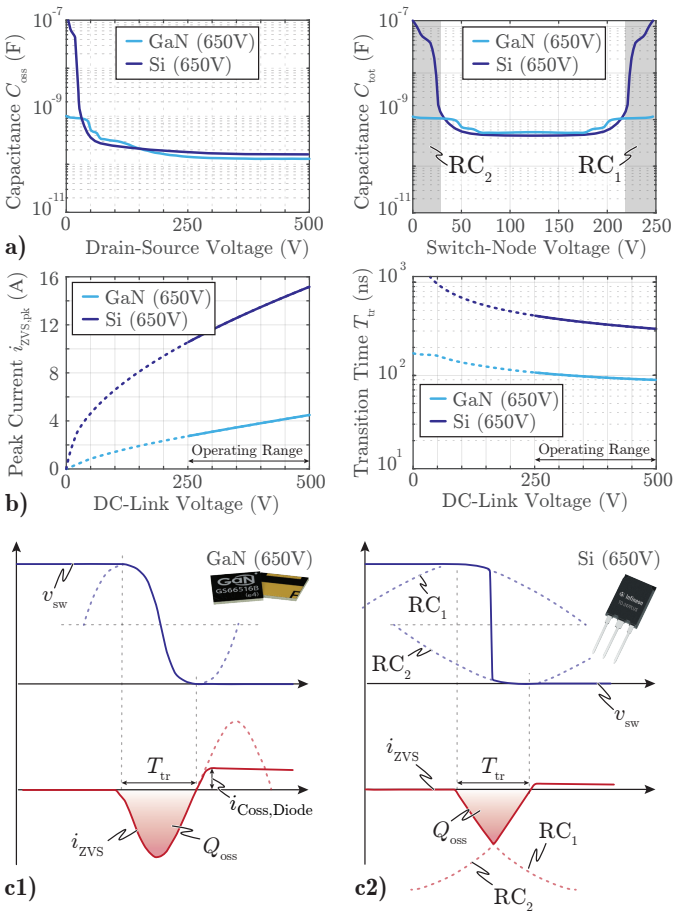


Fig. 4. a) C_{oss} and the total capacitance C_{tot} of a half-bridge for IPW60R018CFD7 Si superjunction MOSFETs [12] (cf. **Fig. 2a** and **c**) and GS66516B GaN switches [13] (cf. **Fig. 2b** and **d**). **b)** Peak values of i_{ZVS} and the transition times T_{tr} for a ZVS inductance L_{ZVS} of 3 µH for both aforementioned switches. **c)** Voltage and current waveforms during a switching transition for GaN (**c1**) and Si superjunction (**c2**) switches.

voltage-dependent effective capacitance $C_{tot}(v_{sw})$ of a half-bridge configuration can be calculated according to

$$C_{tot}(v_{sw}) = C_{oss}(v_{sw}) + C_{oss}(V_{dc} - v_{sw}), \qquad (1)$$

and is shown in **Fig. 4a** for two 650 V switches made of either silicon (Si) or gallium nitride (GaN). Due to the more linear behavior of the C_{oss} (and therefore C_{tot}) of GaN semiconductors, the voltage and current waveforms during a ZVS transition of these switches are of sinusoidal shape (cf. **Fig. 4c1**), whereas the waveforms for silicon switches look more like a voltage step resulting in a triangular current shape (cf. **Fig. 4c2**). This voltage step originates from the fact, that the C_{oss} of silicon switches for low voltages is orders of magnitude higher than for higher voltages. Hence, during the first half of the ZVS transition, almost all of i_{ZVS} flows into the C_{oss} of the upper MOSFET in order to charge this capacitance to a value of approximately 25 V. Thus, this C_{oss} forms the first resonant circuit with L_{ZVS} (cf. RC_1 in **Fig. 4c2**). As soon as v_{sw} reaches approximately $V_{DC} - 25\,V$, the C_{oss} of the upper switch drops significantly and, due to the large current and the small C_{tot}, the switch-node voltage

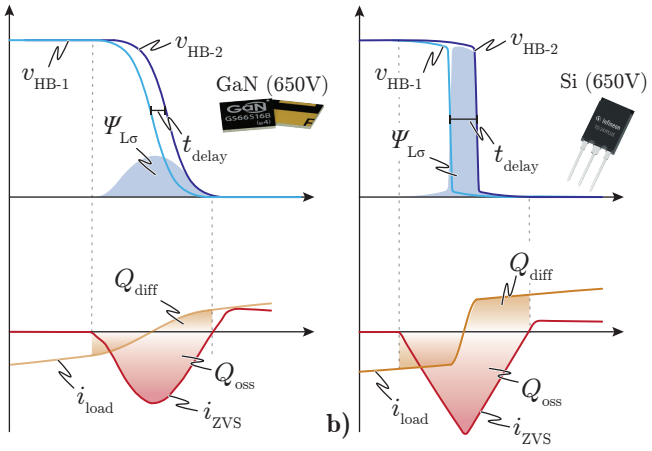


Fig. 5. Voltage and current waveforms of the delayed ZVS transition due to the load current i_{load} for **a)** GaN power switches and **b)** Si superjunction power MOSFETs.

drops to $v_{sw} \approx 25\,V$ almost immediately. As the C_{oss} of the lower MOSFET increases substantially for $v_{sw} < 25\,V$, this C_{oss} now forms a second resonant tank with L_{ZVS} (cf. RC_2), whereby v_{sw} drops to 0 V during the remaining $T_{tr}/2$.
The strong non-linearity of C_{tot} has the advantage, that the effective dead time T_{tr} of the circuit can hardly be seen based on the switch-node voltage, and that even during the dead time T_{tr}, the power flow through the main transformer continues. However, the load current i_{load} during the ZVS transition yields a charge imbalance in the auxiliary circuit, as i_{load} on the primary side of the converter assists the ZVS transition, whereas on the secondary side, i_{load} counteracts i_{ZVS} and therefore slightly delays the transition of the switch-node voltage of the secondary side (cf. t_{delay} in **Fig. 5**). Due to this delay, a large voltage time area $\psi_{L\sigma}$ is applied across the main inductor L_σ, which, depending on the inductance of L_σ, has a large impact on i_{load}. Consequently, T_{tr} should be chosen to be as short as possible for minimizing the L_σ inductance requirement. However, in order to be able to predict the impact of the length of the dead time T_{tr}, not only on L_σ, but also on the performance and the efficiency of the ZVS auxiliary circuit, the RMS values of the ZVS current i_{ZVS} need to be known, which is why they are calculated in the following section.

C. Simplified Analytical Calculations

In order to simplify the analysis of the ZVS auxiliary circuit, a charge-equivalent effective capacitance of a half-bridge configuration can be defined according to

$$C_{eff}(V_{DC}) = \frac{1}{V_{DC}} \int_0^{V_{DC}} C_{oss}(v_{sw}) + C_{oss}(V_{DC} - v_{sw}) \mathrm{d}v_{sw}. \qquad (2)$$

Using this equivalent capacitance, the peak currents and the transition times for both, sinusoidally shaped i_{ZVS} (as e.g. for GaN semiconductors) as well as triangular i_{ZVS} (as e.g. for Si superjunction MOSFETs), can easily be calculated according

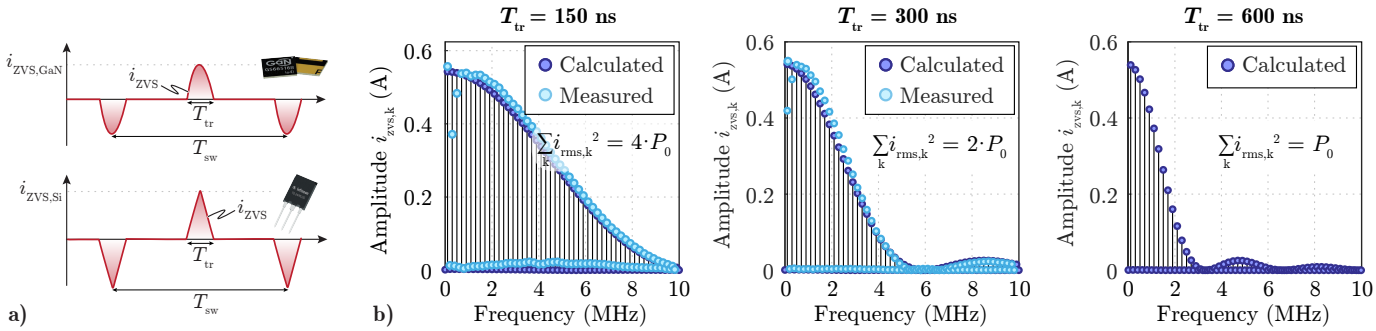


Fig. 6. a) Characteristic current waveforms for GaN and Si superjunction power switches and **b)** calculated (dark blue) and the experimentally measured (light blue) spectrum of the ZVS current i_{ZVS} for different transition times T_{tr}. Additionally, the calculated normalized conduction losses for a unity resistance are shown ($\sum_{\mathrm{k}} i_{\mathrm{rms,k}}^2$). Due to the neglected $i_{\mathrm{C,diode}}$ in the calculation of the current spectrum, there is a slight deviation between calculation and measurement.

to

$$i_{\mathrm{ZVS,pk,GaN}} = \sqrt{\frac{C_{\mathrm{eff}}}{2 \cdot L_{\mathrm{ZVS}}}} \cdot V_{\mathrm{DC}} \tag{3}$$

$$i_{\mathrm{ZVS,pk,Si}} = \sqrt{\frac{C_{\mathrm{eff}}}{L_{\mathrm{ZVS}}}} \cdot V_{\mathrm{DC}} \tag{4}$$

and

$$T_{\mathrm{tr,GaN}} = \pi \cdot \sqrt{\frac{C_{\mathrm{eff}} \cdot L_{\mathrm{ZVS}}}{2}} \tag{5}$$

$$T_{\mathrm{tr,Si}} = 2\sqrt{C_{\mathrm{eff}} \cdot L_{\mathrm{ZVS}}}. \tag{6}$$

The voltage-dependent $i_{\mathrm{ZVS,pk}}$ and T_{tr} are shown in **Fig. 4b** for two exemplary 650 V switches. As indicated in the figure, the transition time varies only slightly for DC-link voltages above 250 V and shows an almost linear dependency on V_{DC}. Thus, for GaN switches, a constant dead time t_{dead} of the power switches can be used, which ideally is chosen to be equal to the maximum expected transition time T_{tr} (occurring at the minimum V_{DC}, as shown in **Fig. 4b**), as T_{tr} only marginally varies with V_{DC}. For silicon superjunction switches, the variation of T_{tr} with V_{DC} is more pronounced, which is why the dead time t_{dead} is again set to be equal to T_{tr}, but this time it should be adapted to the momentary V_{DC} value according to the linear dependency of T_{tr} on V_{DC}. However, as the transition times T_{tr} are completely independent of the load current i_{load} and the switching frequency f_{sw} of the power switches, the dead time t_{dead} does not depend on i_{load} and f_{sw} either, which is why there is no need for any further control of the auxiliary circuit. Hence, no matter how large the C_{oss} of a certain semiconductor is, with an appropriately designed auxiliary circuit and a dead time t_{dead} selected according to equation (5) or (6), the required ZVS can be ensured under all operating conditions. Nevertheless, the capacitance of the C_{oss} has a major impact on the arising losses in the auxiliary circuit, as will be explained in the following.

In terms of system operation, an as small as possible T_{tr} and therefore L_{ZVS} would be desirable, in order to keep the ZVS transition as short as possible. However, from a loss perspective, a shorter transition time yields a higher harmonic content of i_{ZVS} and therefore significantly higher conduction losses in all components of the ZVS auxiliary circuit (cf. **Fig. 6**), according to

$$I_{\mathrm{RMS,Si}} = \sqrt{\frac{8}{3}} \cdot \frac{V_{\mathrm{DC}} \cdot C_{\mathrm{eff}}}{\sqrt{T_{\mathrm{tr,Si}} \cdot T_{\mathrm{sw}}}} \tag{7}$$

and

$$I_{\mathrm{RMS,GaN}} = \frac{\pi}{2} \cdot \frac{V_{\mathrm{DC}} \cdot C_{\mathrm{eff}}}{\sqrt{T_{\mathrm{tr,GaN}} \cdot T_{\mathrm{sw}}}}, \tag{8}$$

which have both been calculated based on the waveforms shown in **Fig. 6a** and the equations (5) and (6). Thus, the selection of T_{tr} yields a tradeoff between the overall system performance and the efficiency of the ZVS auxiliary circuit. In the following section, the individual loss components are investigated in detail, in order to simplify the design of the auxiliary circuit for a certain given set of power switches.

III. Arising Losses in the Auxiliary Circuit

The total arising losses of the ZVS auxiliary circuit can be divided into three main components: First, the switching losses of T.a and T.b, as their Q_{oss} is dissipated in the beginning of each ZVS transition; Second, the conduction losses in T.a, T.b, the auxiliary transformer, D.a and D.b; and third, the hysteresis losses in the C_{oss} of the power switches, as not all of the energy stored in C_{oss} can be recycled [14], [15]. However, this loss component is given by the internal power transistor structure and can hardly be influenced by the design of the auxiliary circuit. Nevertheless, the two other loss components strongly depend on the design, which is why they are investigated in detail in the following.

The switching losses in T.a and T.b can be calculated based on the datasheet values of their C_{oss} according to [5]

$$P_{\mathrm{ZCS,sw}} = 2 f_{\mathrm{sw}} V_{\mathrm{DC}} \cdot \int_0^{V_{\mathrm{DC}}} C_{\mathrm{oss}}(v) \mathrm{d}v. \tag{9}$$

Hence, in order to minimize the expected switching losses, an as small as possible C_{oss} should be targeted. For this reason, small GaN switches should be employed, as they feature an exceptional figure-of-merit ($C_{\mathrm{oss}} \cdot R_{\mathrm{DS,on}}$).

The second loss component is somewhat more difficult to calculate, as the conduction losses depend on the selection of T_{tr}. Thus, T_{tr} is considered as a degree of freedom for

system optimization, which is why the conduction losses are calculated for each T_{tr} individually.
The estimation of the conduction losses in T.a, T.b, D.a and D.b is straightforward according to

$$P_{\mathrm{cond,sw}} = R_{\mathrm{DS,on}} \cdot I^2_{\mathrm{RMS,x}} \tag{10}$$

and

$$P_{\mathrm{D}} = U_{\mathrm{F}} \cdot I_{\mathrm{avg}} + R_{\mathrm{D}} \cdot I^2_{\mathrm{RMS,x}}, \tag{11}$$

where the diode conduction losses can be approximated by $R_{\mathrm{D}} \cdot I^2_{\mathrm{RMS,x}}$, as this term is clearly dominating in this application. However, the limiting factor in the selection of appropriate diodes are usually not the conduction losses, but rather the allowable repetitive peak current of a certain device, which should correspond to the maximum peak current $i_{\mathrm{ZVS,pk}}(V_{\mathrm{DC}})$ in order to minimize the employed chip area and therefore the C_{diode} of D.a and D.b. For the application at hand, Schottky diodes made of silicon carbide (SiC) have been found to be the best solution due to their large ratio between the allowable repetitive peak current and their C_{diode} values.
However, in order to be able to calculate $i_{\mathrm{ZVS,pk}}$ and $I_{\mathrm{RMS,x}}$ (cf. (7) and (8)), the ZVS inductance L_{ZVS} needs to be known, which can be calculated for each T_{tr} based on (5) and (6) according to

$$L_{\mathrm{ZVS,GaN}} = \left(\frac{T_{\mathrm{tr}}}{\pi}\right)^2 \cdot \frac{2}{C_{\mathrm{eff}}} \tag{12}$$

$$L_{\mathrm{ZVS,Si}} = \left(\frac{T_{\mathrm{tr}}}{2}\right)^2 \cdot \frac{1}{C_{\mathrm{eff}}}. \tag{13}$$

In order to minimize the manufacturing costs and the AC resistance of this inductor, the inductance L_{ZVS} should be integrated as leakage inductance into the small auxiliary transformer, as the vertically aligned current flow in planar transformers reduces the proximity effect and therefore the high-frequency (HF) resistance of PCB windings as well [16]. This is especially important in this application, as otherwise, the high harmonic content of i_{ZVS} would lead to significant HF conduction losses.

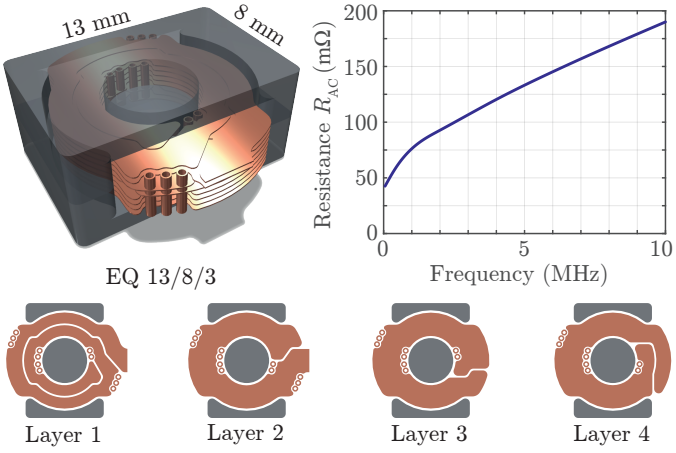


Fig. 7. ZVS auxiliary circuit transformer design with a turns ratio of 5:5, a leakage inductance L_{ZVS} of 256 nH and a total frequency-dependent winding resistance R_{AC} as illustrated.

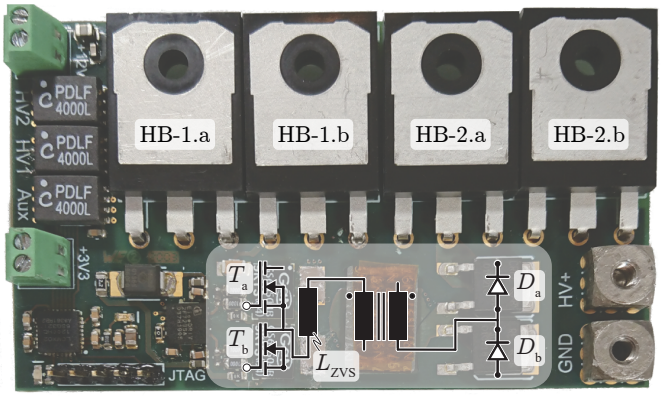
The leakage inductance between two PCB windings can be influenced by the geometrical arrangement of their turns (cf. **Fig. 7**) and in particular by the distance between the primary and secondary side windings. However, the calculation of the leakage inductance in planar transformers has already been discussed extensively in literature [17], [18], which is why it is not discussed any further in this paper.
The design of the transformer itself introduces again a large number of degrees of freedom (number of turns N, winding width b_{w}, core cross-section A_{C}, etc.) and is subject to an optimization with respect to efficiency and power density. This optimization is conducted based on the calculated winding current $i_{\mathrm{RMS,x}}$ (cf. (7) and (8)) and the peak flux linkage $\psi_{\mathrm{ZVS,pk}}$ given as

$$\psi_{\mathrm{ZVS,pk}} = \frac{1}{2} \max\left(V_{\mathrm{DC}}\right) T_{\mathrm{tr}}. \tag{14}$$

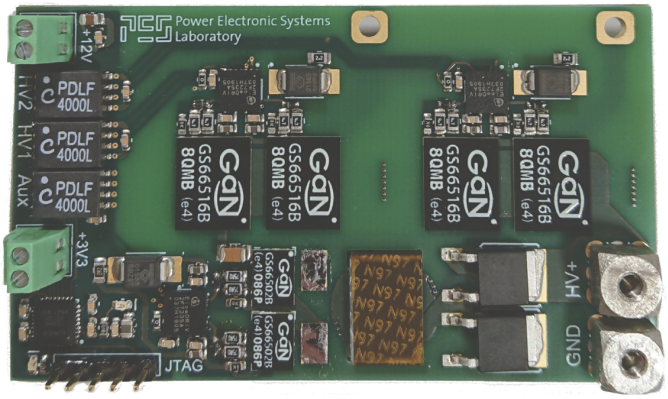
However, as this optimization is based on well-known formulas for calculating the winding [16], [19] and the core losses [20], it is not explained in detail here.
In **Fig. 7**, an exemplary ZVS transformer with a turns ratio of 5:5 and a leakage inductance L_{ZVS} of 256 nH is shown. Furthermore, the corresponding layer arrangement of one winding is illustrated, whereby the second winding is identical and mirrored with respect to the center of the eight-layer PCB. This transformer is finally used in the two hardware demonstrators, which will be introduced in the following.

IV. Experimental Verification

In order to verify the operating principle of the proposed ZVS auxiliary circuit, two hardware demonstrators have been built and measured (cf. **Fig. 8**). The ZVS auxiliary circuits are identical in both prototypes, but the power switches are either IPW60R018CFD7 Si superjunction MOSFETs from Infineon (**Fig. 8a**) or GS66516B GaN switches from GaN Systems (**Fig. 8b**). In order to be able to test the performance of the circuit for different L_{ZVS} and T_{tr} values, two SMD pads have been employed, to which different external inductors can be soldered to (L_{ZVS}). The auxiliary switches T.a and T.b are GS66502, the diodes D.a and D.b are C3D03060A SiC diodes from Cree and the transformer is the one shown in **Fig. 7** with an inherent leakage inductance of 256 nH. The whole circuit is controlled by means of a MachXO2 FPGA, which generates the required gate signals for the different switches.
Fig. 9 shows the experimentally measured waveforms during one switching transition for both hardware prototypes, a V_{DC} equal to 250 V and an external inductance of $L_{\mathrm{ZVS}} = 3\,\mu\mathrm{H}$. The dead times t_{dead} of the power switches were calculated as explained in **Section II-C** according to equations (5) and (6) to $t_{\mathrm{dead,GaN}} = T_{\mathrm{tr,GaN}}(250\,\mathrm{V}) = 115\,\mathrm{ns}$ and $t_{\mathrm{dead,Si}} = T_{\mathrm{tr,Si}}(250\,\mathrm{V}) = 428\,\mathrm{ns}$, respectively.
As expected, the shape of the measured waveforms as well as the T_{tr} and $i_{\mathrm{ZVS,pk}}$ values are in good agreement with the calculated values shown in **Fig. 4b**. The ringing of the switch-node voltage $v_{\mathrm{HB-2}}$ in **Fig. 9b** originates from the parasitic inductance of the TO-247 package of the power switches and cannot be avoided, as the nonlinear C_{oss} of Si MOSFETs yields huge di/dt-values within the switches during a ZVS

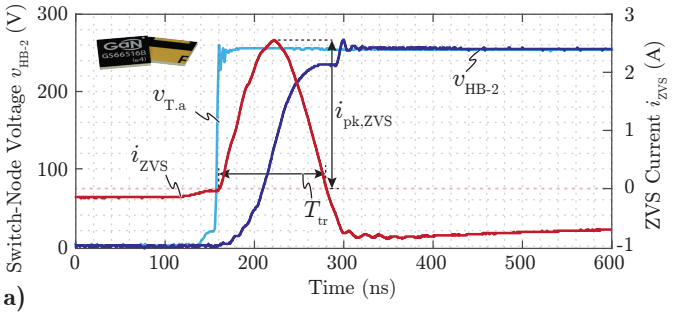


a) Si - Hardware Demonstrator

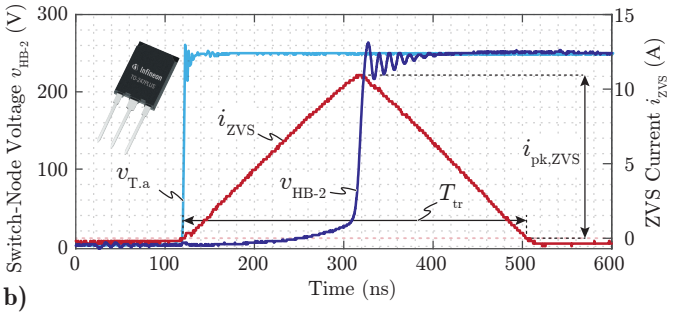


b) GaN - Hardware Demonstrator

Fig. 8. a) Hardware demonstrator for Si superjunction power switches and the proposed ZVS auxiliary circuit (grey-shaded) and **b)** the same ZVS auxiliary circuit, but with GaN power switches. The dimensions of both PCBs are given by 113 mm x 73 mm (4.44 in x 2.87 in).



a)



b)

Fig. 9. Experimentally measured voltage and current waveforms during a switching transition for the hardware demonstrator with **a)** GaN power switches and **b)** Si superjunction MOSFETs.

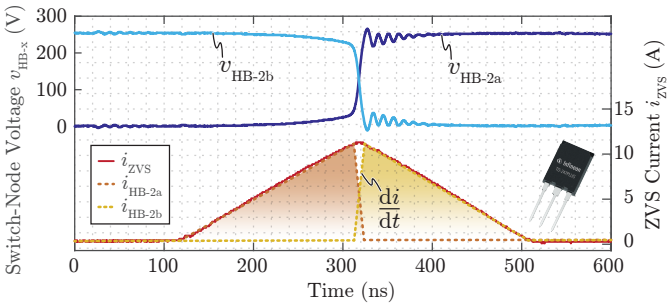


Fig. 10. Voltage and current waveforms of the Si hardware demonstrator with the indicated C_{oss} currents i_{HB-2a} and i_{HB-2b} in order to illustrate the large di/dt values during a ZVS transition.

transition (cf. **Fig. 10**). Hence, almost all of the ZVS current flows in the switch with the larger momentary C_{oss} value and the commutation from one switch to the other happens extremely fast.

In order to estimate the achievable benefit by utilizing the proposed ZVS auxiliary circuit, the total losses of the hardware demonstrator have been measured for a switching frequency of 100 kHz with (P_{ZVS}) and without (P_{ZCS}) active ZVS auxiliary circuit. Hence, without the auxiliary circuit (P_{ZCS}), the total Q_{oss} of the four power switches is dissipated by means of switching losses. This operating mode is required, if perfectly synchronous transitions of the switch-node voltages on the primary and the secondary side of the converter are important. The simultaneous transitions are crucial in applications where only a small L_σ is employed, as otherwise, the resulting voltage-time area $\psi_{L\sigma}$ results in a step in i_{load} and, worst case, in a destabilization of the resonant converter (cf. **Fig. 5**). If a larger L_σ would be employed, only the half-bridge on the primary side would need to be switched, as the secondary-sided half-bridge operates as a synchronous rectifier, thus is inherently operated under ZVS conditions. Consequently, only half of the aforementioned P_{ZCS} losses would be dissipated. However, as the ZVS auxiliary circuit targets applications with minimal L_σ requirements, the performance is compared to the first operating mode where all four switches are actively switched.

The results are shown in **Fig. 11** for different ZVS inductance values, where the loss saving ξ (solid lines) indicates the amount of the E_{oss} stored in the power switches which can be saved by operating the ZVS auxiliary circuit. Furthermore, the arising losses P_{ZCS} and P_{ZVS} are shown for a $L_{ZVS} = 250$ nH in **Fig. 11a** and $L_{ZVS} = 720$ nH in **Fig. 11b**, respectively. As expected based on (7) and (8), the losses are increasing for smaller L_{ZVS} and therefore shorter T_{tr}. However, while the loss saving in percentage of silicon switches is more or less constant for different DC-link voltages, the one of GaN switches is dropping significantly. This behavior originates from the dv/dt-dependency of the ZVS losses in GaN switches [21], [22], as the hysteresis losses are increasing significantly with the applied DC-link voltage (cf. **Fig. 12a**). In contrast, the hysteresis loss-percentage of Si superjunction switches is almost constant and for this specific

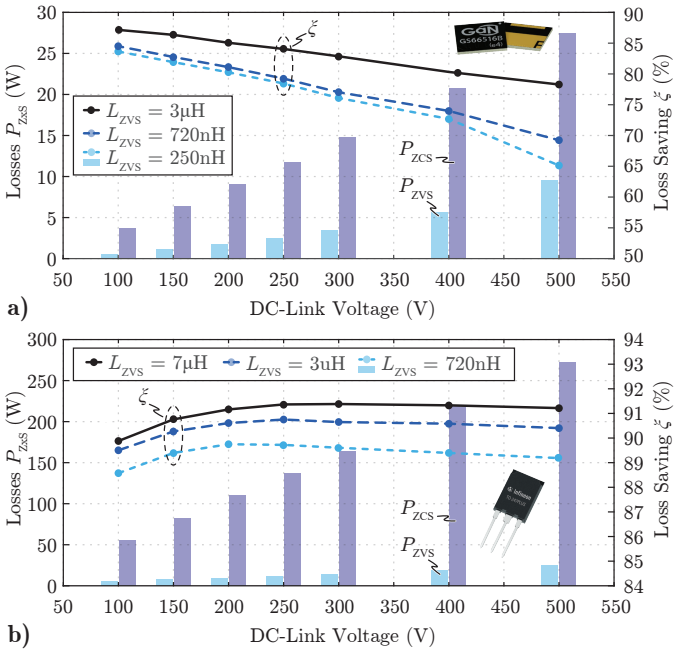


Fig. 11. Experimentally measured losses of the hardware prototypes with (P_{ZVS}) and without (P_{ZCS}) operating the ZVS auxiliary circuit in **a)** for GaN power switches and in **b)** for Si superjunction MOSFETs.

switch around 6 % (cf. **Fig. 12b**). However, the hysteresis losses strongly depend on the inner switch structure/design, i.e. manufacturer, device family, etc. [14], [15], [23], which is why they need to be measured for each device individually in

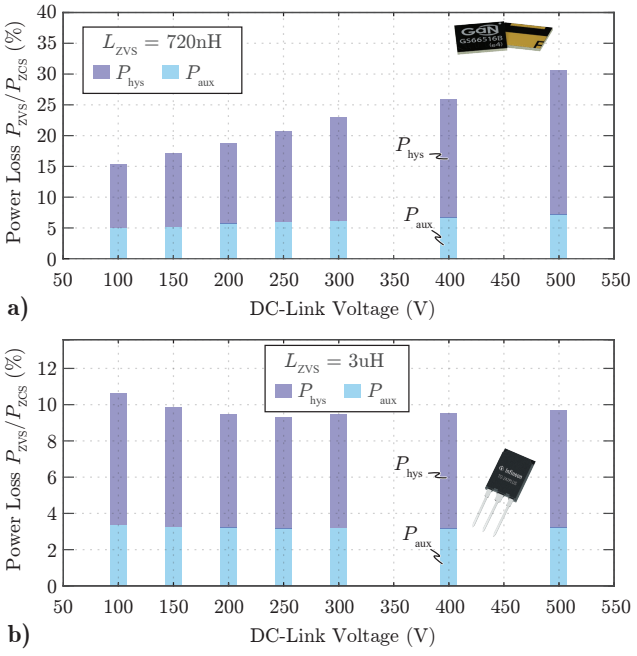


Fig. 12. Estimated distribution of the hysteresis losses P_{hys} and the total losses of the auxiliary circuit P_{aux} based on the total measured losses P_{ZVS}, the FFT of the measured i_{ZVS} and the measured AC resistances of the components for GaN switches (GS66516B) and an L_{ZVS} of 720 nH in **a)** and Si superjunction switches (IPW60R018CFD7) and an L_{ZVS} of 3 µH in **b)**.

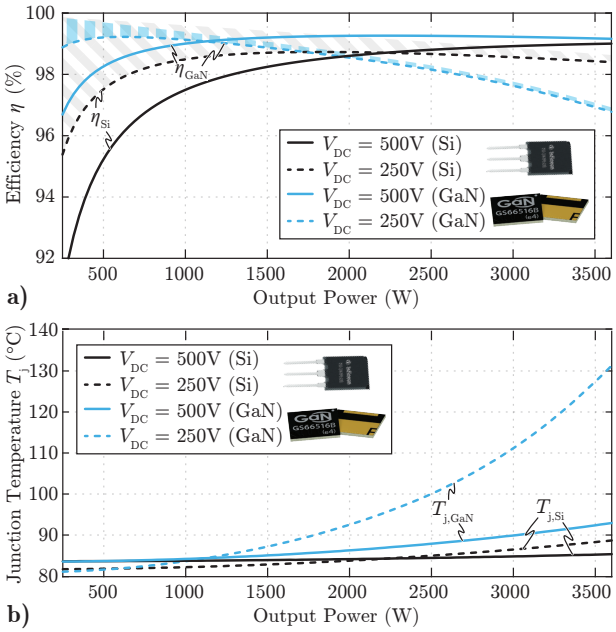


Fig. 13. a) Maximum achievable efficiency of the DC-transformer for two different power switches (Si = IPW60R018CFD7, GaN = GS66516T), a switching frequency of 100 kHz and DC-link voltages of 250 V and 500 V, where an ideal (loss-less) transformer is assumed. Furthermore, the hatched areas for V_{DC} = 250 V indicate the share of switching losses (incl. ZVS auxiliary circuit). **b)** The corresponding junction temperatures of the power switches for a water-cooled aluminum heat sink with a coolant temperature of 80 °C.

order to estimate the expected hysteresis losses. Nevertheless, as proven by means of the hardware demonstrators of **Fig. 8**, the utilization of the proposed ZVS auxiliary circuit allows for an efficient recycling of a large amount of the E_{oss} of power semiconductors. Thus, for a DC-link voltage of e.g. 500 V and a switching frequency of 100 kHz, the utilization of the ZVS auxiliary circuit increases the full-load (3.6 kW) efficiency of the overall converter system for GaN power switches by more than 0.5 %, and for Si superjunction MOSFETs by more than 6 %. Therefore, even Si superjunction MOSFETs can now be used for comparably high switching frequencies, without an excessive amount of additional circuitry.

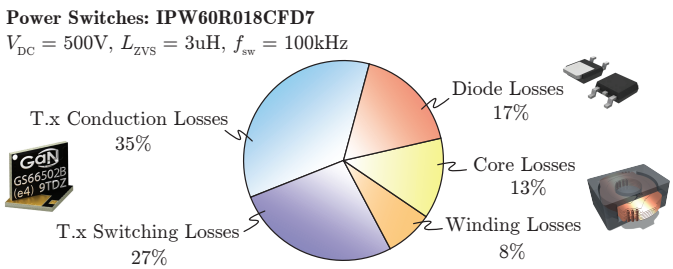


Fig. 14. Distribution of the arising losses within the ZVS auxiliary circuit, shown in **Fig. 8a**, with Si superjunction MOSFETs as power switches, a DC-link voltage of 500 V, a switching frequency of 100 kHz and an external ZVS inductance of L_{ZVS} = 3 µH (whose losses are not considered in this graph, as they would be much lower if L_{ZVS} would be fully integrated in the auxiliary transformer).

This is verified in **Fig. 13**, where the maximum achievable efficiencies of the DC-transformer example are shown for both, Si (IPW60R018CFD7) and GaN (GS66516T) power switches, a L_{ZVS} of $720\,\mathrm{nH}$, and a switching frequency of $100\,\mathrm{kHz}$, whereby only the losses in the power switches and the ZVS auxiliary switches are considered. Hence, the power transformer is assumed to be loss-less, as its design highly depends on the targeted converter efficiency and has no impact on the arising losses in the semiconductors. Thus, either an extremely power-dense transformer with high losses can be used, or a comparably large transformer with minimized conduction and core losses could be employed, whereby the efficiency of **Fig. 13a** can be approached. However, besides the additional transformer losses, all other loss components are considered, as will be discussed in the following.

The losses in the power semiconductors comprise two individual components: The switching losses, i.e. the hysteresis losses during the switching transitions (P_{hys}), and the conduction losses, which originate due to the sinusoidal transformer currents i_{load}. The switching losses are calculated based on experimental measurements (cf. **Fig. 11**), whereas the conduction losses are calculated based on the simulated i_{load} and the temperature dependent $R_{\mathrm{ds,on}}(T_{\mathrm{j}})$ of the power switches. The expected junction temperatures T_{j} are calculated iteratively based on the total losses in one semiconductor and a simple thermal model, which consists of the thermal resistance of the semiconductor package, the isolating thermal interface material ($\lambda = 6\,\mathrm{W\,m^{-1}\,K}$, thickness = $0.5\,\mathrm{mm}$) and a water-cooled aluminum heat sink with a coolant temperature of $80\,^{\circ}\mathrm{C}$, which is a common specification in automotive applications. The resulting calculated junction temperatures are shown in **Fig. 13b**, where it should be noted, that for full-load operation and $V_{\mathrm{DC}} = 250\,\mathrm{V}$, the GaN switches would be operated very close to their thermal limit, whereas the hot spot temperature in the Si switches never exceeds $90\,^{\circ}\mathrm{C}$.

Furthermore, in **Fig. 13a**, the hatched areas for the two efficiency curves $\eta_{\mathrm{Si,250V}}$ and $\eta_{\mathrm{GaN,250V}}$ indicate the amount of losses, which originate from the hysteresis losses P_{hys} and the auxiliary circuit P_{aux} alone, whereby the non-hatched area above the efficiency curves correspond to the conduction losses in the power semiconductors. It can be seen, that for the silicon MOSFETs, especially for partial-load operation, the switching losses $P_{\mathrm{hys}} + P_{\mathrm{aux}}$ have a huge impact on the achievable partial-load efficiency, whereby the conduction losses are almost negligible. In contrast, the switching losses of the GaN semiconductors are much lower and the conduction losses start to dominate the efficiency already at very low output power values. Hence, the GaN switches are very suitable for this application and the specified power level, whereby the Si MOSFETs are clearly under-utilized, as their junction temperatures are hardly increasing and they could be operated with much higher currents (at $P_{\mathrm{out}} = 6.6\,\mathrm{kW}$, $\eta_{\mathrm{Si,500V}}$ and $\eta_{\mathrm{Si,250V}}$ are still above $99\,\%$ and $97.5\,\%$, respectively).

Nevertheless, the full-load efficiencies for both semiconductor materials are almost identical, even though the cost for Si superjunction MOSFETs are significantly lower compared to the GaN HEMTs. Hence, by using the proposed ZVS auxiliary circuit, Si MOSFETs can be used with a similar full-load performance as GaN HEMTs up to comparably high switching frequencies.

In **Fig. 14**, the distribution of the arising losses in the ZVS auxiliary circuit is shown for one specific operating point. Due to the much higher AC resistance of the external inductor L_{ZVS} compared to a PCB-integrated equivalent, it has not been considered in this loss distribution in order not to distort the results. Hence, in a fully PCB-integrated solution with an L_{ZVS} of $3\,\mu\mathrm{H}$, the share of the winding losses would be slightly larger, in the range of $25\,\%$.

Despite ensuring ZVS conditions of the power switches, the ZVS auxiliary circuit can also be used to pre-charge the output capacitor of the secondary side, such that the power part of the circuit can start its operation with matching input and output voltages. Hence, L_{σ} does not need to be designed to withstand huge inrush currents, as it would be the case with a large initial voltage difference between the input and output voltage. As the auxiliary circuit is anyway designed in such a way, that the maximum energy which can be transferred within one switching cycle is the E_{oss} of the power switches, the initial voltage difference between the input and the output voltage does not matter and the peak value of i_{ZVS} is limited according to (3) and (4). Consequently, during each switching transition, the output capacitor C_{out} is charged due to i_{ZVS}, until it reaches the required output voltage $V_{\mathrm{out}} = V_{\mathrm{DC}}$. The corresponding simulated waveforms are shown in **Fig. 15**, where the (stepwise) charging of C_{out} can easily be observed. It should be noted, that the peak current $i_{\mathrm{ZVS,pk}}$ is independent of V_{out}, which is why the usage of this functionality has no impact on the design of the auxiliary circuit and it can be utilized "for free".

So far, the application of the ZVS auxiliary circuit has only been discussed for equal primary- and secondary-sided power switches. However, as previously mentioned, this concept can of course also be applied if different power switches are used, which is inevitable in converter systems with e.g. large input-to-output voltage ratios. In order to achieve the same ZVS behavior and synchronized switch-node voltages of the primary and secondary side half-bridges, it just needs to be ensured, that the primary-side referred effective capacitance of the secondary-sided power switches $C_{\mathrm{eff,sec}}/n_{\mathrm{ZVS}}^2$ equals the effective capacitance of the primary side power semiconductors $C_{\mathrm{eff,pri}}$. This can be achieved by increasing the smaller C_{eff} by means of additional ceramic capacitors, which are connected in parallel to the power switches. By doing so, the Q_{oss} of both half-bridges can be equalized and the ZVS auxiliary circuit can be operated in the same way as previously explained for equal power switches.

Until now, only the advantages of the proposed ZVS auxiliary circuit have been discussed. However, besides the topology-inherent benefits of unrestricted functionality with respect to the operating conditions, as e.g. DC-link voltage, switching frequency, and output power, there are of course also disadvantages of this topology. Thus, besides the increased

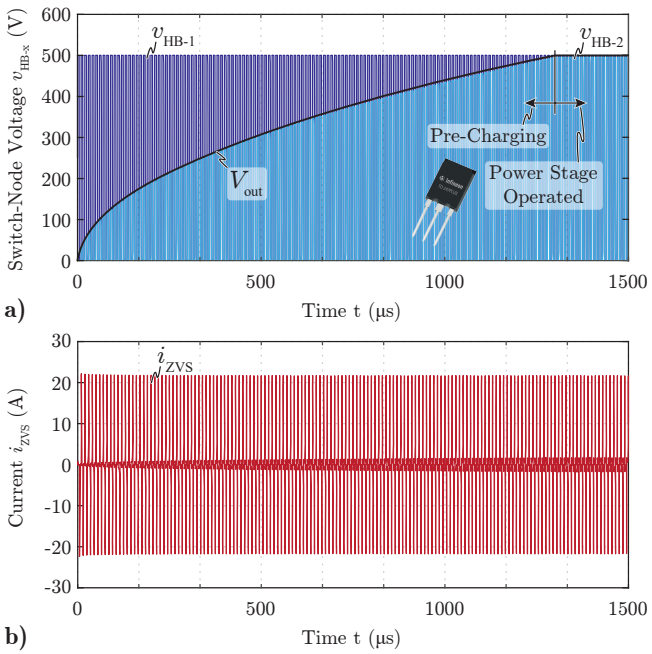


Fig. 15. a) Simulated switch-node voltages during a pre-charging sequence with initial input and output voltages of 500 V and 0 V, respectively. **b)** The corresponding simulated current i_{ZVS} during the pre-charging sequence.

system complexity due to the additional active circuitry and, therefore, lower reliability of the overall converter system, the suitability of the proposed concept for a certain application highly depends on the converter topology and the given specifications. Hence, if the output voltage range and/or the switching frequency range are not too wide, it could be more efficient to use an alternative, passive ZVS concept, as e.g. the magnetizing current of the main transformer, whereby there is no reason to use the more complex ZVS auxiliary circuit anymore. However, this can easily be estimated based on **Fig. 12**, where the distribution of the switching losses with the auxiliary circuit are shown.

Hence, assuming a certain given dead time t_{dead}, the hysteresis losses P_{hys} are approximately the same for all ZVS concepts and cannot be avoided. Consequently, the additional losses due to the ZVS auxiliary circuit alone are given by P_{aux}, which therefore need to be compared to the arising losses of an alternative ZVS concept (hereafter referred to as P_{alt}). In the example of using the magnetizing current i_{m} for achieving ZVS, P_{alt} would correspond to the additional conduction losses in the power switches and the main transformer T_1 due to i_{m}. Hence, if P_{aux} should be larger than P_{alt}, the alternative ZVS concept is the more promising solution and should therefore be used, especially if it is more reliable and/or more cost-effective than the proposed circuit.

Nevertheless, if an extremely small series-resonant inductance should be employed and, therefore, synchronous switch-node voltages are required, even a certain efficiency penalty due to the employment of the proposed ZVS auxiliary circuit might be acceptable, if in turn the power density and the efficiency of the main transformer T_1 can be improved.

Furthermore, the application of the proposed ZVS auxiliary circuit is of course not limited to the simple DC-transformer topology of **Fig. 1**. Moreover, it can be applied to all different kinds of topologies, where two half-bridges are operated synchronously. Thereby, it does not matter, whether the two half-bridges are both located in the same converter port or in different ports of the converter, as long as the Q_{oss} of one half-bridge can be directly transferred to a second half-bridge, which therefore needs to be switching at the same time. However, if the two half-brides are in the same converter port, the auxiliary circuit processes reactive power only, whereby the advantage of the pre-charging of the output capacitor is lost. Consequently, the arrangement where the two half-bridges are in different converter ports should be preferred if possible.

Generally, it can be stated that the proposed ZVS auxiliary circuit is most suitable in applications, where ZVS for a wide output voltage range and/or a wide switching frequency range needs to be ensured, without increasing the control effort of the actual converter system. However, if in a certain application an alternative, passive ZVS concept is equally efficient as the proposed active ZVS circuit, the passive concept should be preferred, as it is usually the more reliable and more cost-effective solution. Nevertheless, as in all operating conditions, only the absolutely necessary ZVS energy is processed by the proposed auxiliary circuit, it allows for utilizing cost-effective Si superjunction MOSFETs up to comparably high switching frequencies. This is an important advantage over conventional, passive ZVS concepts, where the large Q_{oss} of Si superjunction MOSFETs demands for large circulating reactive currents, such that ZVS is guaranteed under all operating conditions. These currents, however, yield significant conduction losses, reducing the achievable converter efficiency significantly, especially for low output power values.

V. Conclusion

In this paper, a simple auxiliary circuit has been proposed and analyzed, which ensures soft-switching of a series-resonant converter (SRC) by transferring the energy stored in the C_{oss} of the primary-side power switches to the C_{oss} of the secondary-side power transistors, by means of a resonant transition. Consequently, there is no need for stored magnetic energy in the main transformer, neither in the series-resonant inductance, nor in the magnetizing inductance, as ZVS is guaranteed by the proposed auxiliary circuit. Hence, an extremely small series-resonant inductance can be employed, which facilitates the design of the power converter with a very efficient PCB winding transformer, where the series-resonant inductor is integrated as leakage inductance. Furthermore, the structure of the ZVS auxiliary circuit inherently guarantees, that only the absolutely necessary amount of energy for ZVS is transferred from the primary to the secondary side, independent of the momentary output power and voltage level. This is a huge advantage compared to conventional approaches, where either the magnetizing current of the main transformer, or the load current in the series-resonant inductor is used to achieve ZVS of the power switches. Additionally, due to the resonant operating mode of the auxiliary circuit, there is hardly any additional control required, as the appropriate operation of the

circuit is ensured by means of circuit design.

The suitability and performance of the proposed auxiliary circuit have been tested and measured based on two hardware demonstrators for both, GaN and Si superjunction power switches. For both types of switches, a significant improvement in terms of efficiency could be observed, whereby especially for Si switches, a remarkable amount of switching losses can be saved.

Finally, it has been shown, that the auxiliary circuit can also be used for pre-charging the output capacitor of the power converter, in order to adapt the output voltage to the input voltage before starting the operation of the main power circuit.

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