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Accurate Transient Calorimetric Measurement of Soft-Switching Losses of 10 kV SiC MOSFETs and Diodes

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***Abstract*—The characterization of soft-switching losses of modern high-voltage SiC MOSFETs is a difficult but necessary task in order to provide a sound basis for the accurate modelling of converter systems, such as medium-voltage-connected Solid-State Transformers (SSTs), where soft-switching techniques are employed to achieve an improved converter efficiency. Switching losses, in general, are typically measured with the well-known double pulse method. In case of soft-switching loss measurements, however, this method is very sensitive to the limited accuracy of the measurement of the current and voltage transients, and thus is unsuitable for the characterization of fast switching high-voltage MOSFETs. This paper presents an accurate and reliable calorimetric method for the determination of soft-switching losses using the example of 10 kV SiC MOSFET modules. Measured soft-switching loss curves are presented for different DC-link voltages and switched currents. Furthermore, a deeper analysis concerning the origin of soft-switching losses is performed. With the proposed measurement method, it can be experimentally proven that the largest share of the soft-switching losses arises from charging and discharging the output capacitance of the MOSFET module and especially of the antiparallel junction barrier Schottky diode.**

***Index Terms*—Soft-switching losses, ZVS, 10kV SiC MOSFETs, calorimetric measurement, JBS diode**

I. Introduction

SOFT-SWITCHING techniques are widely used in power electronic converters for the reduction of switching losses (SL) and EMI distortions, especially in DC/DC applications [1]–[5] and also in AC/DC and DC/AC applications [6]–[9]. Although Wide Band-Gap (WBG) devices such as SiC MOSFETs offer superior switching behaviour compared to silicon devices [10]–[14], the soft-switching losses (SSL) of these devices (especially for high blocking voltages in the range of 10 kV) are not negligible. Therefore, it is very important to consider the SSL during the design process. However, most of the device datasheets only provide data for hard-switching losses which means that it is necessary to experimentally determine the SSL of the particular devices.

There are basically two types of switching loss measurement methods, namely electrical and calorimetric measurement methods. Electrical methods, such as the well-known double pulse test, feature the advantage of a rather short measurement time, since only pulse measurements have to be performed. Furthermore, with the same measurement setup both, the hard-switching losses and the SSL can be directly determined at different chip temperatures by electrically measuring the device voltage and current during a turn-on and a turn-off transient. However, due to the fast switching transients, the accuracy of the measured waveforms strongly decreases, thus the measured SL can be highly inaccurate. In [15], the error analysis for fast switching 10 kV SiC MOSFETs showed that, in case of SSL measurements, electrical measurement methods such as the double pulse test can be subject to measurement errors of more than 200 %. Hence, the double pulse method is unsuitable for the measurement of SSL.

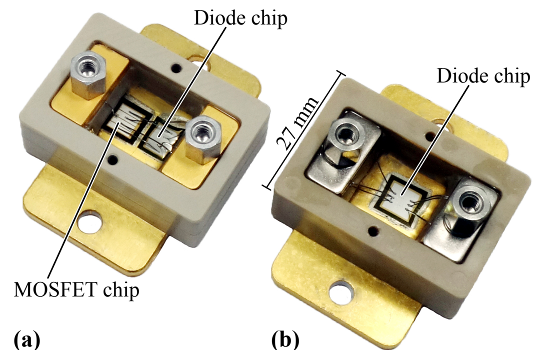

Fig. 1. Pictures of the 10 kV SiC devices: **(a)** Co-Pack module with a SiC-MOSFET chip and an antiparallel SiC JBS diode chip, **(b)** discrete packaged 10 kV SiC JBS diode.

In contrast to electrical measurements, with a calorimetric measurement setup, the semiconductor losses, i.e. the sum of the SL and the conduction losses (CL), are determined by measuring the dissipated power of the device under test (DUT) in continuous operation and, since no fast switching transients have to be measured, typically a higher measurement accuracy is achieved. However, the higher accuracy is reflected in a much longer measurement time due to the large thermal time constants of calorimetric measurement setups. There, the total semiconductor losses can be measured either in the thermal equilibrium or in the transient heat-up phase. For example, in [16], a half-bridge as part of a synchronous buck converter is operated continuously in a double chamber calorimeter until the thermal equilibrium is reached. The SSL of the half-bridge are finally obtained by subtracting the losses of the gate drives, the PCB and the DC-link capacitor from the total losses measured in the calorimeter. In order to reduce the measurement time of calorimetric measurements, in [17], a transient calorimetric method is presented, whereby a metal block is attached to the switches of a half-bridge circuit which is continuously operated. The metal block acts as a thermal

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capacitance which is heated up by the dissipated power of the switches, resulting in a certain temperature increase. Consequently, based on the resulting temperature slope, the dissipated power can be calculated. A further advantage of this method is that e.g. the gate driver and PCB losses do not have to be subtracted from the measured losses due to the low thermal coupling. Nevertheless, in both calorimetric measurement methods, the CL (which might be in the same range as the SSL) have to be subtracted from the total measured semiconductor losses, in order to obtain the pure SL. Hence, the accuracy achieved with calorimetric measurements strongly depends on the accurate determination of the CL. In principle, the CL can be calculated based on the DUT's on-state resistance $R_{\mathrm{DS,on}}$ given in the manufacturer's datasheet. However, the $R_{\mathrm{DS,on}}$ of the 10 kV SiC MOSFET examined in this paper (CPM3-10000-0350 from Wolfspeed, cf. **Fig. 1 (a)**), shows a strong dependency on the device current, the chip temperature, the current direction (above approximately 10 A, the antiparallel junction barrier Schottky (JBS) diode (CPW3-10000-Z020B from Wolfspeed, cf. **Fig. 1 (b)**) starts conducting) and even deviates from device to device by more than 20 %, because the MOSFETs at hand are prototype devices. In order to separate the CL and the SL directly in the measurement, a novel calorimetric SSL measurement method featuring a superior measurement accuracy is proposed in **Section II**. In **Section III**, this method is applied to the aforementioned 10 kV SiC MOSFETs. The obtained SSL for different DC-link voltages, currents and gate resistors are presented and can be utilized e.g. in the design optimization of medium-voltage converters [18]–[20]. Furthermore, even though the measured SSL are small, a deeper analysis concerning the origin of the SSL is performed, since they cannot be explained by the overlapping of the MOSFET voltage and MOSFET current during the switching transients. Therefore, it is assumed that the SSL are arising to a large extent from the charging and discharging of the parasitic output capacitances of the MOSFET and the antiparallel JBS diode, as also stated in [21], [22]. In **Section IV**, this assumption is experimentally verified with the proposed measurement method, which on the one hand allows to measure the charging/discharging losses, and on the other hand enables to allocate them to the MOSFET and the JBS diode. **Section V** finally provides a conclusion and an outlook.

II. Functional Principle of the Proposed Measurement Method

The basic idea of the proposed method for the measurement of SSL is on the one hand to measure the semiconductor losses calorimetrically and on the other hand to measure the SL and the CL separately. Therefore, as shown in **Fig. 2 (a)**, a third MOSFET S_0 is inserted in series to either the low-side switch S_2 or the high-side switch S_1 of the half-bridge. In the following it is assumed that S_0 is connected in series to the high-side switch S_1 since the cooling pad of the device under test (DUT) is connected to the drain potential of the MOSFET and thus in this configuration is fixed to a stable voltage. Furthermore, the MOSFET module S_0 is

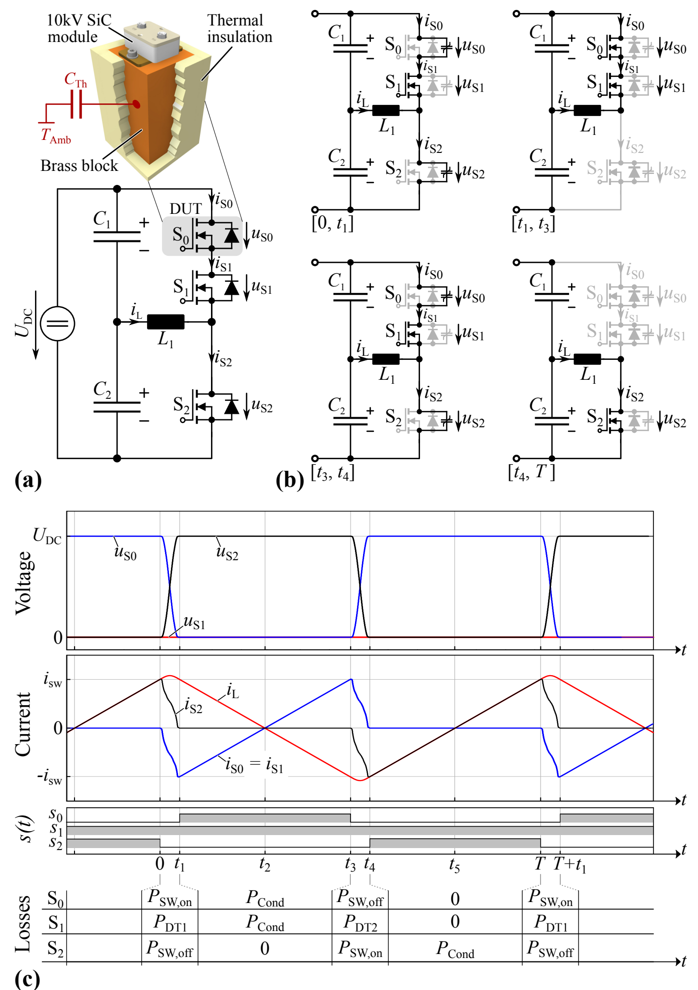

Fig. 2. **(a)** Circuit diagram with an additional MOSFET S_0 mounted on a thermally insulated brass block which acts as a thermal capacitance C_{Th}. **(b)** Circuit diagrams showing the current path during the specific time intervals; shaded symbols do not conduct current. **(c)** Ideal current and voltage waveforms as well as the gate signals of the three switches and the corresponding share of losses in each time interval.

mounted on top of a brass block, which absorbs the dissipated semiconductor losses and acts as a thermal capacitance C_{Th} (cf. **Fig. 2 (a)**). Brass is selected as heat sink material due to its high thermal capacitance per volume. In addition, the brass block is isolated with thermal insulation material in order to minimize the heat transfer to the ambient. Consequently, assuming a constant power dissipation in the semiconductor device S_0, the temperature of the brass block linearly increases over time, whereby the temperature slope is proportional to the dissipated power of S_0. Hence, the power dissipation of S_0 can be calculated as

$$P = \frac{C_{\mathrm{Th}} \cdot \Delta\vartheta}{\Delta\tau}, \tag{1}$$

where $\Delta\vartheta$ denotes the temperature difference and $\Delta\tau$ equals the measurement time. Based on (1), the dissipated power of S_0 can now be determined by operating the half-bridge continuously, and by measuring the time $\Delta\tau$ which is required to heat the insulated brass block by a certain temperature difference $\Delta\vartheta$, e.g. from 30 °C to 40 °C.

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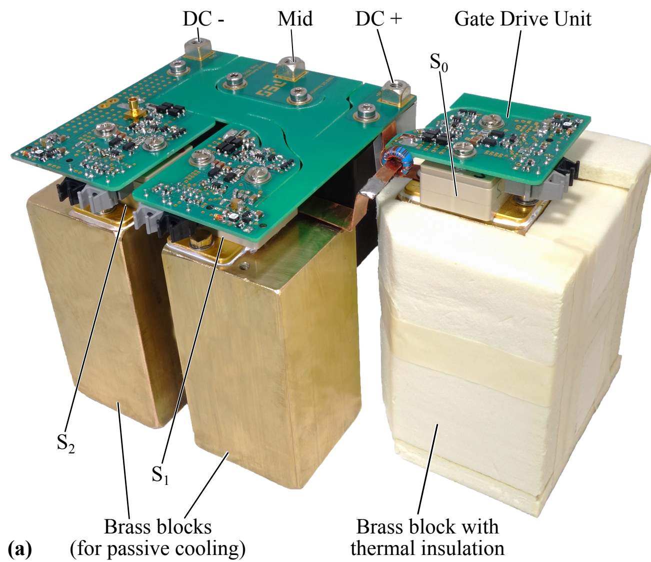

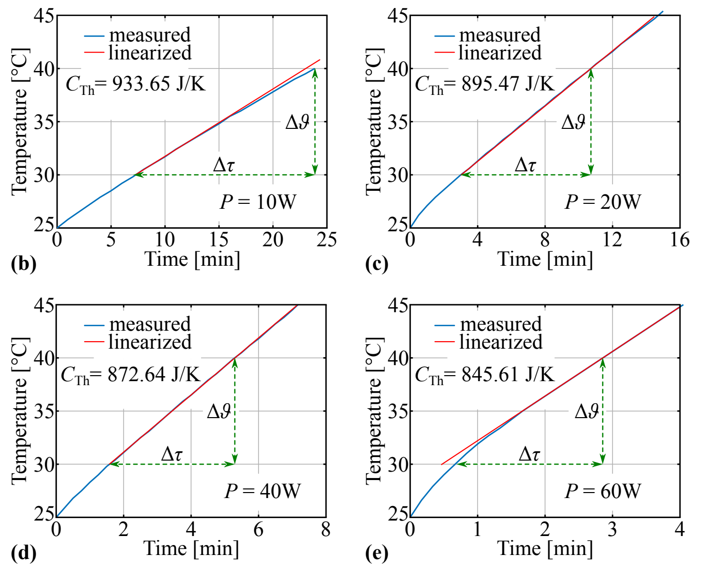

Fig. 3. **(a)**: 10 kV SiC half-bridge with the additional MOSFET S_0 on a thermally insulated brass block ($50 \times 50 \times 100$ mm). **(b)-(e)**: Thermal calibration measurements at constant DC power levels, **(b)** 10 W, **(c)** 20 W, **(d)** 40 W, and **(e)** 60 W. Each temperature profile is linearized around the measurement temperature range and the corresponding thermal capacitance is calculated for the given slope. A high linearity can be achieved in the temperature range from 30 °C to 40 °C and the power range from 20 W to 40 W. Thus, all the switching loss measurements are carried out in this power and temperature range.

For the basic operation of the modified half-bridge shown in **Fig. 2 (a)**, the series connection of S_0 and S_1 can be considered as one switch, where either S_0 or S_1 is permanently turned on, while the other is complementarily switched with S_2, i.e. the circuit behaves like a conventional half-bridge. Hence, in order to achieve soft-switching transitions in all switches, the half-bridge is continuously operated with a 50 % duty cycle resulting in a triangular current as shown in **Fig. 2 (c)**. As can be noticed, the shown section corresponds to a moment in time in which S_1 is permanently turned on, while S_0 and S_2 are complementarily switching. Consequently, due to the series connection of S_0 and S_1, the same current is flowing through both switches, which means that the CL in both switches are the same if equal on-state resistances $R_{\mathrm{DS,on}}$ are assumed. Furthermore, since only S_0 and S_2 are switching, the SSL are only generated in S_0 and S_2, while S_1 only generates CL. Accordingly, if one would separately measure the losses in both MOSFETs S_0 and S_1 based on (1), the SSL generated in S_0 could be directly extracted from the loss difference in the two semiconductor devices.

However, since the on-state resistance $R_{\mathrm{DS,on}}$ is strongly varying from device to device in this case, as already mentioned, the SL and the CL cannot be properly separated from each other. Therefore, instead of measuring the losses of two different devices S_0 and S_1 at the same time, in addition to the measurement M_1 discussed above, a second measurement M_2 is performed at the same operating conditions, i.e. the same switched current, DC-link voltage, dead time, switching frequency and temperature range. In measurement M_2, however, the MOSFETs S_0 and S_1 swap their roles such that S_0 is now permanently on and S_1 is complementarily switched with S_2. In this case, S_0 only generates CL ($P_{\mathrm{M2}} = P_{\mathrm{Cond}}$), while during measurement M_1 the MOSFET S_0 was generating both, SL and CL, i.e. ($P_{\mathrm{M1}} = P_{\mathrm{Cond}} + P_{\mathrm{SW}}$). Hence, the SSL of S_0 within one switching period can be found by subtracting P_{M2} from P_{M1} and dividing the difference by the switching frequency.

Unfortunately, even though in both measurements M_1 and M_2 the CL are measured in the same device for the same operating conditions, the CL are not exactly identical due to the dead time intervals $[0, t_1]$ and $[t_3, t_4]$, where the output capacitances of the switches have to be charged/discharged. In order to emphasize the importance of the dead time intervals in the calculation of the CL, in **Fig. 2 (c)** the switched current is chosen rather small, which means that the dead time intervals can occupy a significant part of a switching period. It should be noted that the length of the dead time intervals $[0, t_1]$ and $[t_3, t_4]$ is selected in such a way that the corresponding switch is turned on exactly at the moment when its drain-source voltage reaches 0 V, i.e. ideally the antiparallel JBS diodes are not conducting. Actually, since S_1 is connected in series to S_0, in the first measurement M_1 the MOSFET S_1 should only generate CL during the on-state interval of S_0. However, as shown in **Fig. 2 (b)**, during the dead time intervals $[0, t_1]$ and $[t_3, t_4]$, the current, which flows through the nonlinear output capacitance of S_0, also flows through the MOSFET channel of S_1, generating additional CL P_{DT1} and P_{DT2} in S_1 ($P_{\mathrm{DT}} = P_{\mathrm{DT1}} + P_{\mathrm{DT2}}$). Consequently, during the second measurement M_2 (S_0 permanently on, S_1 switching), the same additional CL P_{DT} arise in S_0 and thus have to be considered for the calculation of the SSL. As described in [15], the CL P_{DT}, which occur during the dead time, can be calculated as

$$P_{\mathrm{DT}} = h_{\mathrm{P}} \cdot P_{\mathrm{Cond}}, \text{ where} \tag{2}$$

$$h_{\mathrm{P}} = \frac{R_{\mathrm{DS,on}} \cdot \int_{0}^{t_1} i_{\mathrm{S0}}^2 \cdot \mathrm{dt}}{R_{\mathrm{DS,on}} \cdot \int_{\mathrm{t_1}}^{t_2} i_{\mathrm{S0}}^2 \cdot \mathrm{dt}} \approx \frac{\int_{0}^{t_1} i_{\mathrm{S0}}^2 \cdot \mathrm{dt}}{\int_{\mathrm{t_1}}^{t_2} i_{\mathrm{S0}}^2 \cdot \mathrm{dt}}. \tag{3}$$

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Thereby, h_{P} can be obtained by measuring the drain current of S_0 and by solving the given integrals for the corresponding time intervals.

As will be discussed in **Section III-A**, in order to achieve a high measurement accuracy, the SSL should account for the largest share of the overall power dissipation measured at the brass block, since in this case, the sensitivity of the SSL on calculation errors of h_{P} as well as on variations in the CL between the two measurements, e.g due to the temperature dependent $R_{\mathrm{DS,on}}$ of S_0, is very low. Accordingly, for the dimensioning of the brass block it is assumed that in the worst case, i.e. max. switched current of $15\,\mathrm{A}$, the CL should not exceed $50\,\%$ of the SSL, which in contrast to the CL can be adapted via the switching frequency and the inductance value. The $R_{\mathrm{DS,on}}$ of the $10\,\mathrm{kV}$ SiC MOSFETs at hand is around $0.35\,\Omega$ at room temperature, which in the worst case results in $13\,\mathrm{W}$ of CL, and according to this rule in a total power dissipation of $39\,\mathrm{W}$. Furthermore, in order to achieve a minimum relative accuracy of $\pm 1\,\%$ for the temperature measurement, the measurement range must be at least $\Delta\vartheta = 10\,\mathrm{K}$, if an absolute temperature measurement error of $\pm 0.1\,\mathrm{K}$ is expected. For the same reason of measurement accuracy, the minimum measurement time $\Delta\tau$ should be at least 2...3 minutes. Hence, the required thermal capacitance and therewith the size of the brass block ($50 \times 50 \times 100\,\mathrm{mm}$) can be calculated based on (1). A picture of the corresponding $10\,\mathrm{kV}$ SiC hardware setup with the thermally insulated brass block is shown in **Fig. 3 (a)**. It should be noted that the MOSFETs S_1 and S_2 are also mounted on separate brass blocks instead of heat sinks in order to not distort the measured temperature of the insulated brass block by any air stream.

In order to obtain the precise thermal capacitance of the brass block in the hardware setup, the value C_{Th} has to be calibrated by measurements. Therefore, a constant DC-power is fed into the MOSFET module by driving a feedback-controlled current through the device such that the constant power levels of $10\,\mathrm{W}$, $20\,\mathrm{W}$, $40\,\mathrm{W}$ and $60\,\mathrm{W}$ are reached. Thereby, the hardware configuration (including the copper bus-bars to the DC-link, the gate drive, and the thermal insulation etc.) must be exactly the same as it is later used for the SSL measurements. **Figs. 3 (b)-(e)** show the measured temperature profiles of the insulated brass block for the different power ratings. It can be seen that between $30\,^\circ\mathrm{C}$ and $40\,^\circ\mathrm{C}$ the measurements for $20\,\mathrm{W}$ and $40\,\mathrm{W}$ are nicely linear, whereas for $10\,\mathrm{W}$ and $60\,\mathrm{W}$ certain nonlinearities are measured in the temperature curves. Consequently, all SSL measurements are performed in the power range from $20\,\mathrm{W}$ to $40\,\mathrm{W}$ and in the temperature range from $30\,^\circ\mathrm{C}$ to $40\,^\circ\mathrm{C}$. Furthermore, as indicated in **Figs. 3 (b)-(e)**, the linearized thermal capacitance C_{Th} is slightly changing within the selected power range. Therefore, C_{Th} is interpolated iteratively from the calibration measurements for the purpose of obtaining the correct power dissipation.

Due to this limitation in the power range, now the problem of measuring only CL in measurement M_2 arises, since for small switched currents the CL are in the range of only 1...2 W. In order to overcome this problem, the operation principle of the half-bridge has to be modified in such a way

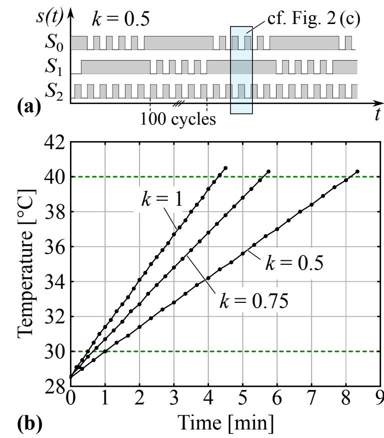

Fig. 4. **(a)** Gate signals of the three MOSFETs for the modified modulation scheme exemplarily shown for a switching cycle share of $k = 0.5$. **(b)** Measured temperature curves for $U_{\mathrm{DC}} = 8\,\mathrm{kV}$, $i_{\mathrm{Switched}} = 7.5\,\mathrm{A}$ and different values of k.

that also in the measurement M_2 higher losses are generated in S_0. Therefore, instead of permanently turning on S_0, S_0 and S_1 share the switching actions and therewith the SL among each other as indicated in **Fig. 4 (a)**. The share of the switching cycles, which is switched by S_0, is defined as the switching cycle share k. A value of $k = 1$ means that S_0 is switching continuously, while S_1 is permanently turned on. As an example, in **Fig. 4 (a)**, k is equal to 0.5 which means that S_0 and S_1 are alternatingly switching $50\,\%$ of the total switching cycles and are constantly turned on for the other $50\,\%$. For practical reasons, S_0 and S_1 are alternated for every 100 switching cycles. In **Fig. 4 (b)**, measured temperature profiles at $U_{\mathrm{DC}} = 8\,\mathrm{kV}$ and a switched current of $7.5\,\mathrm{A}$ are shown for different values of k. As can be noticed, the measurements follow a linear characteristic, which means that the thermal setup is operated in its linear region as desired.

Accordingly, depending on the selected switching cycle share k, the average losses P_{S0} of S_0 within one measurement can be brought into the optimum power range of $20\,\mathrm{W}$ to $40\,\mathrm{W}$ and can be expressed in general terms as

$$\begin{aligned} P_{\mathrm{S0}} &= k\,(P_{\mathrm{SW}} + P_{\mathrm{Cond}}) + (1-k)\,(P_{\mathrm{DT}} + P_{\mathrm{Cond}}) \\ &= k \cdot P_{\mathrm{SW}} + P_{\mathrm{Cond}} + (1-k)\,P_{\mathrm{DT}}, \end{aligned} \tag{4}$$

where $P_{\mathrm{SW}} = P_{\mathrm{SW,on}} + P_{\mathrm{SW,off}}$ and $P_{\mathrm{DT}} = P_{\mathrm{DT1}} + P_{\mathrm{DT2}}$. Hence, in the first measurement M_1 where $k = 1$, the power dissipated in S_0 is

$$P_{\mathrm{M1}} = P_{\mathrm{S0}}\,(k=1) = P_{\mathrm{SW}} + P_{\mathrm{Cond}}. \tag{5}$$

In the second measurement M_2 where $k < 1$, the dissipated power in S_0 is given as

$$P_{\mathrm{M2}} = k \cdot P_{\mathrm{M1}} + (1-k)\,(P_{\mathrm{Cond}} + P_{\mathrm{DT}}), \tag{6}$$

where $P_{\mathrm{SW}} = P_{\mathrm{M1}} - P_{\mathrm{Cond}}$ from (5) is used. Furthermore, based on (2), the dead time losses P_{DT} in (6) can be substituted by $h_{\mathrm{P}} \cdot P_{\mathrm{Cond}}$, thus the effective CL and SL are given as

$$P_{\mathrm{Cond}} = \frac{P_{\mathrm{M2}} - k \cdot P_{\mathrm{M1}}}{1 - k + (1-k) \cdot h_{\mathrm{P}}}, \tag{7}$$

$$P_{\mathrm{SW}} = P_{\mathrm{M1}} - P_{\mathrm{Cond}}, \tag{8}$$

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and only depend on the two measured losses P_{M1} and P_{M2} as well as on the selected switching cycle share k. For the SSL measurements of the $10\,\mathrm{kV}$ SiC MOSFETs, a switching cycle share of $k = 1$ has been chosen for measurement M_1, $k = 0.5$ for measurement M_2 and $k = 0.75$ for a third (verification) measurement, leading to stable and reproducible results. Finally, the SL per MOSFET and switching period can be determined as $E_{\mathrm{SW}} = P_{\mathrm{SW}}/f_{\mathrm{SW}}$.

III. Discussion and Experimental Results

The following section analyzes the accuracy of the proposed SSL measurement method and discusses possible limitations and sources of measurement errors. Finally, the measured SSL are presented and discussed.

A. Error analysis for the proposed soft-switching loss measurement method

Although calorimetric measurements are probably the most direct and accurate way of measuring power dissipations, there are several effects that have to be considered in order to obtain accurate results. First of all, an accurate and EMI robust measurement of the brass block temperature is required. Depending on the device package, the cooling terminal might be on drain potential of the MOSFET (which is the case for the $10\,\mathrm{kV}$ SiC MOSFETs at hand) such that the metal block including the temperature sensor is on (floating) potential and is possibly exposed to high $\mathrm{d}u/\mathrm{d}t$ values which could disturb the temperature measurement. Furthermore, the position of the temperature sensor on the metal block must be the same during the calibration and the switching loss measurements. Otherwise, measurement errors could arise due to a possibly inhomogeneous temperature distribution within the metal block. In the given setup, a thermocouple was attached to the top side of the brass block, next to the baseplate of the $10\,\mathrm{kV}$ SiC module. A better approach would be to use a fiber optic temperature sensor, which besides the EMI robustness also provides a galvanic isolation. Generally important for this measurement method is the thermal decoupling of the DUT and its brass block from the ambient (by applying thermal insulation material to the brass block) and especially from other heat sources contained in the hardware setup (such as the other switches) in order to prevent undesired heat transfers to the brass block. This is easily possible for the $10\,\mathrm{kV}$ SiC MOSFETs at hand due to the specific package design and the anyway required distances between the switch and other parts of the circuit for the reason of electrical isolation. The measured thermal time constant of the thermally insulated brass block together with the $10\,\mathrm{kV}$ SiC module is $\tau_{\mathrm{Block}} = 200\,\mathrm{min}$, which is a factor of 15 larger than the maximum measurement time. This shows that the undesired heat transfers to the ambient and other parts of the setup can be neglected in the given setup. For other device packages and especially lower voltage devices, however, the thermal decoupling of the DUT might be a problem, since a thermal decoupling goes hand in hand with an increase of the commutation loop inductance which could lead to voltage overshoots and ringing. For the employed $10\,\mathrm{kV}$ devices operated with DC-link voltages in the kilovolt range, the voltage overshoot caused by the additional inductance of the third switch is negligible and not even measurable.

TABLE I
Measured and calculated values for the case of low switched current ($7\,\mathrm{kV}$, $2.5\,\mathrm{A}$) and high switched current ($7\,\mathrm{kV}$, $15\,\mathrm{A}$).

Parameter	*Value for* $7\,\mathrm{kV}$, $2.5\,\mathrm{A}$	*Value for* $7\,\mathrm{kV}$, $15\,\mathrm{A}$
P_{M1}	37.50 W	38.54 W
P_{M2}	18.84 W	26.99 W
h_{P}	1.1883	0.0731
P_{Cond}	0.09 W	14.38 W
P_{SW}	37.41 W	24.16 W
P_{DT}	0.10 W	1.05 W
f_{SW}	200 kHz	100 kHz

Since the measurement method includes a measurement of a rather small temperature difference $\Delta\vartheta$ of $10\,\mathrm{K}$, the accuracy of the temperature measurement is the most critical parameter. Assuming a measurement error of $\Delta\vartheta = \pm 0.1\,\mathrm{K}$ (which corresponds to a relative error of $\pm 1\,\%$), a $\pm 2\,\%$ error in the thermal capacitance C_{Th} and a perfect time measurement (since time can be measured very precisely), the worst case error of a single power measurement is $\pm 3\,\%$ (cf. (1), $102\,\% \cdot 101\,\% \approx 103\,\%$). Hence, as a worst case estimation, if P_{M1} is measured $3\,\%$ too high and P_{M2} is measured $3\,\%$ too low, the relative errors in the SL are $5.8\,\%$ for the $7\,\mathrm{kV}$, $2.5\,\mathrm{A}$ case and $15.5\,\%$ for the $7\,\mathrm{kV}$, $15\,\mathrm{A}$ case, whereby measured values for P_{M1}, P_{M2} and h_{P} (cf. **TABLE I**) are inserted into (7) and (8) for the error analysis in order to give practical examples. Compared to the double pulse method, a 10 to 20 times higher accuracy can be achieved with the proposed calorimetric method [15]. Furthermore, in all of the performed measurements, the $k = 0.5$ and the $k = 0.75$ (reference) measurements match within $5\,\%$ error, which demonstrates that the worst case is not very likely to occur if the measurements are carried out carefully and indicates that the accuracy of the method is very high. As can be noticed, the measurement error increases with increasing switched currents, thus the SL should hold the largest share of the overall measured power dissipation in order to keep the measurement accuracy high. This can be managed by choosing a rather high switching frequency, which however is limited by certain constraints such as the gate drive power capability, the total generated losses on the metal block (which might be too high and result in a nonlinear temperature profile at some point) or the fact that with higher switching frequencies the dead time interval consumes a major part of the overall switching cycle. Another (limited) possibility to increase the measurement accuracy is to increase the temperature difference $\Delta\vartheta$. However, the temperature dependency of the MOSFET properties might start playing a role for higher values of $\Delta\vartheta$. For example, in the derivation of the SL from the two measurements M_1 and M_2, in equation (3) it is assumed that the on-state resistance $R_{\mathrm{DS,on}}$ is constant, however, this is not true, since the $R_{\mathrm{DS,on}}$ of the $10\,\mathrm{kV}$ SiC MOSFETs at hand depends on the temperature as well as on the direction and the value of the

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drain current. Hence, the $R_{\mathrm{DS,on}}$ does not completely cancel out in equation (3) and leads to a certain calculation error of h_{P}. However, the sensitivity of the SSL on calculation errors of h_{P} is very low. On the one hand, for low switched currents, the switching frequency is selected rather high (cf. **TABLE I**) in order to increase the SL until an optimal power dissipation between $20\,\mathrm{W}$ and $40\,\mathrm{W}$ on the brass block is achieved. In this case, the dead time indeed consumes a major part of the switching cycle ($h_{\mathrm{P}} \approx 1$), thus the corresponding losses P_{DT} are similar to the CL P_{Cond} (cf. **TABLE I**). Due to the low current rating, however, the SL P_{SW} are orders of magnitude higher than P_{DT} or P_{Cond}. Consequently, calculation errors of h_{P} hardly influence the SL. E.g. with the values given for the $7\,\mathrm{kV}$, $2.5\,\mathrm{A}$ measurement in **TABLE I**, the switching loss error stays below $0.012\,\%$, if for the determination of h_{P} a calculation error of $\pm 10\,\%$ is assumed. On the other hand, for high switched currents, the time to charge/discharge the output capacitances of the MOSFETs is short, i.e. $h_{\mathrm{P}} \approx 0$. Hence, errors in the calculation of h_{P} have a negligible impact on the SL. Assuming again an error of $\pm 10\,\%$ in h_{P}, for the case of $7\,\mathrm{kV}$, $15\,\mathrm{A}$ (cf. **TABLE I**), the switching loss error is below $0.41\,\%$.

Furthermore, a measurement error could potentially result due to the fact that the chip temperature and therewith the $R_{\mathrm{DS,on}}$ is not equal in the two measurements M_1 and M_2 since the generated losses P_{M1} and P_{M2} are different, which results in distinct junction temperatures. Therefore, the impact of this junction temperature difference on the measuring accuracy is analyzed in the following. As stated above, the influence of the dead time can be neglected ($P_{\mathrm{DT}} \approx 0$), thus with the simplified equations (5) and (6) and the assumption of equal average CL P_{Cond} within the two measurements, the SL P_{SW} can be immediately expressed by the difference of the two measured losses P_{M1} and P_{M2} as

$$\Delta P_{\mathrm{M12,ideal}} = P_{\mathrm{M1}} - P_{\mathrm{M2}} = P_{\mathrm{SW}}\,(1-k)\,. \tag{9}$$

Due to this difference in losses, however, the thermal resistance between the chip and the brass block R_{JB} leads to a higher junction temperature in measurement M_1 compared to M_2, even though both measurements are performed for the same brass block temperature range from $30\,°\mathrm{C}$ to $40\,°\mathrm{C}$. Assuming a thermal resistance of $R_{\mathrm{JB}} = 0.5\,\mathrm{K\,W^{-1}}$ (extracted from thermal FEM simulations) and exemplarily measured losses of $P_{\mathrm{M1}} = 30\,\mathrm{W}$ and $P_{\mathrm{M2}} = 20\,\mathrm{W}$, the chip temperature in M_1 would (ideally) pass through the temperature range from $30\,°\mathrm{C} + R_{\mathrm{JB}} \cdot P_{\mathrm{M1}} ... 40\,°\mathrm{C} + R_{\mathrm{JB}} \cdot P_{\mathrm{M1}} = 45\,°\mathrm{C} ... 55\,°\mathrm{C}$, whereby the chip temperature in M_2 passes through the temperature range of $40\,°\mathrm{C} ... 50\,°\mathrm{C}$, i.e. an average chip temperature difference of $5\,\mathrm{K}$. Consequently, since the on-state resistance $R_{\mathrm{DS,on}}$ of the employed $10\,\mathrm{kV}$ SiC MOSFETs features a temperature dependency of $\Delta R = 1\,\%\,\mathrm{K^{-1}}$, in this example the actual average CL in M_1 are $5\,\%$ higher than in M_2. Hence, considering a linear increase of the $R_{\mathrm{DS,on}}$ with temperature, (5) and (6) have to be adapted to

$$\begin{aligned} P_{\mathrm{M1}} &= P_{\mathrm{SW}} + (1+\beta)\,\alpha P_{\mathrm{SW}}, & (10)\\ P_{\mathrm{M2}} &= k \cdot P_{\mathrm{SW}} + \alpha P_{\mathrm{SW}}, & (11) \end{aligned}$$

with

$$\begin{aligned} \alpha &= \frac{P_{\mathrm{Cond}}}{P_{\mathrm{SW}}} \quad \text{and} & (12)\\ \beta &= R_{\mathrm{JB}} \cdot \Delta P_{\mathrm{M12,ideal}} \cdot \Delta R, & (13) \end{aligned}$$

where α is the ratio between the CL and the SL (which should always be kept as small as possible by properly choosing the switching frequency) and β is the relative increase of the MOSFET's $R_{\mathrm{DS,on}}$ depending on the loss difference between the two measurements M_1 and M_2. Subtracting (10) from (11) leads to

$$\begin{aligned} \Delta P_{\mathrm{M12,real}} &= (1 - k + \alpha\beta)\,P_{\mathrm{SW}}\\ &= \Delta P_{\mathrm{M12,ideal}} \left(1 + \frac{\alpha\beta}{1-k}\right). & (14) \end{aligned}$$

Now, the relative error $e_{\Delta\mathrm{T}}$ introduced by the junction temperature difference between P_{M1} and P_{M2} can be found as

$$e_{\Delta\mathrm{T}} = \frac{\alpha\beta}{1-k}. \tag{15}$$

It should be noted that this analysis is also valid for devices with a nonlinear dependency of the $R_{\mathrm{DS,on}}$ on temperature, since in this case, the $R_{\mathrm{DS,on}}$ can be linearized within the relevant temperature range of $10\,\mathrm{K}$ from e.g. $45\,°\mathrm{C}$ to $55\,°\mathrm{C}$ with a high accuracy. For the values given in **TABLE I**, equation (15) leads to a relative error $e_{\Delta\mathrm{T}}$ in the range of $0.05\,\%$ and $6.87\,\%$, which means that the worst case error for the measurements following in **Section III-B** is smaller than $7\,\%$. As can be noticed, the error increases with increasing current, since the ratio α between the CL and the SL increases. In order to keep the error small, the objective should be to achieve $\alpha \leq 1$ (which means $P_{\mathrm{M1}} - P_{\mathrm{M2}} \leq 20\,\mathrm{W}$ for the setup at hand). Nevertheless, if the exact values of R_{JB} and ΔR of the MOSFET are known, this error can be corrected in the loss calculation. Finally, it should be noted that the SSL do not or hardly depend on the junction temperature, as will be shown later.

B. Measurement results

In order to cover a wide range of applications in which the analyzed $10\,\mathrm{kV}$ SiC MOSFETs could be utilized, SSL measurements have been performed for different DC-link voltages, currents and gate resistors. **Fig. 5** shows the net measured SSL of the $10\,\mathrm{kV}$ SiC MOSFETs for DC-link voltages between $4\,\mathrm{kV}$ and $8\,\mathrm{kV}$ and switched currents between $2.5\,\mathrm{A}$ and $15\,\mathrm{A}$. Unless otherwise noted, the gate resistors are $R_{\mathrm{on}} = 20\,\Omega$ and $R_{\mathrm{off}} = 10\,\Omega$. It is clearly visible that the SSL depend mainly on the DC-link voltage and increase only slightly with increasing current. This behaviour will be discussed in more detail in **Section IV**. Compared to the hard-switching operation of these $10\,\mathrm{kV}$ SiC MOSFETs, cf. [23], almost a factor 100 lower SL can be achieved by applying soft-switching techniques, which enables higher switching frequencies, efficiencies and power densities. Comparing the three $7\,\mathrm{kV}$ curves with different turn-off gate resistors R_{off} in **Fig. 5**, it is evident that a turn-off resistor of $R_{\mathrm{off}} = 10\,\Omega$ leads to the lowest SSL. For the case of $R_{\mathrm{off}} = 15\,\Omega$, the dependency on the switched current shows a clear trend towards higher losses for higher switched

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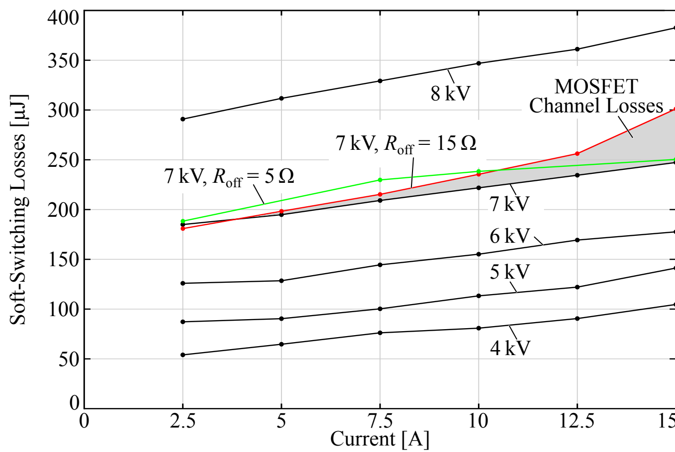

Fig. 5. Calorimetrically measured soft-switching losses (SSL) of the 10 kV SiC MOSFETs for different DC-link voltages, switched currents, gate resistors and a measurement temperature range of 30...40 °C. Unless otherwise noted, the turn-off gate resistor is $R_{\mathrm{off}} = 10\,\Omega$.

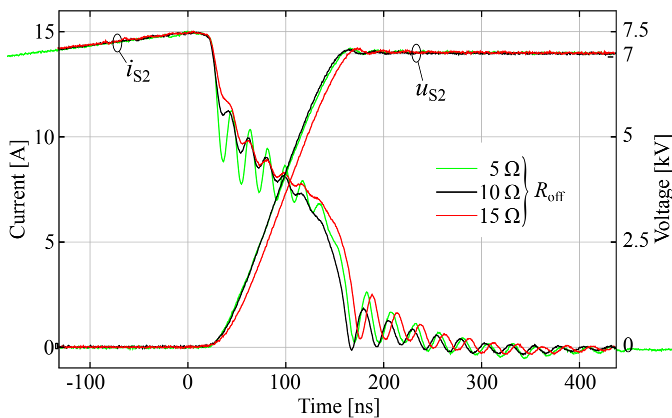

Fig. 6. Comparison of soft-switching transitions for different turn-off gate resistors at $U_{\mathrm{DC}} = 7\,\mathrm{kV}$ and $i_{\mathrm{Switched}} = 15\,\mathrm{A}$.

currents which is an indication for increased channel losses due to a larger overlapping of the voltage and current transients during turn-off. This behaviour can be explained by analyzing the soft-switching transitions given in **Fig. 6** for 7 kV and 15 A. While the switching transitions are almost equally fast for turn-off gate resistors of 5 Ω and 10 Ω, the switching transition for a gate resistor of 15 Ω is clearly slowed down. Hence, especially for higher switched currents, the higher gate resistor leads to a stronger overlapping of the MOSFET voltage and channel current transients and thus to higher SL. On the other hand, a low turn-off gate resistance of 5 Ω results in stronger oscillations in the drain current due to parasitic inductances introduced by the semiconductor packaging and thus causes higher SSL. Consequently, for the 10 kV SiC MOSFETs at hand, the optimum turn-off gate resistance is $R_{\mathrm{off}} = 10\,\Omega$, which could be probably slightly decreased if another package with lower parasitic inductances and/or with Kelvin source connection is used. However, even though the packaging can be improved, a substantial reduction of the SSL is not expected. Furthermore, it should be mentioned that the turn-on resistor does not or hardly influence the SSL.

IV. Output Capacitance Charging/Discharging Losses

In **Fig. 5**, it is clearly visible that the measured SSL are strongly depending on the DC-link voltage (with an approximately quadratic relation $E_{\mathrm{SW}} \sim U_{\mathrm{DC}}^2$) whereas the dependency on the switched current is linear with a rather flat and voltage-independent slope. Furthermore, the SSL curves do not pass through the origin, if they are extrapolated towards zero current. In contrast, the curves show a voltage-dependent offset, which means that there are voltage-dependent residual SSL which cannot be avoided. This indicates that a large share of the SSL might just arise from the charging and discharging of the parasitic output capacitances of the MOSFET and the antiparallel JBS diode, and only a minor share of the SSL is caused by the overlap of the MOSFET's voltage and channel-current transients. The loss mechanisms related to the charging/discharging of the nonlinear output capacitance have already been discussed for Superjunction MOSFETs [22], [24], where significant fractions (strongly depending on the device) of the stored energy in the output capacitance are lost during the charging/discharging process. (In [25], this effect is explained via a mixed-mode simulation of low-voltage Superjunction MOSFETs). In the following, an accurate calorimetric method to measure the charging/discharging losses (CDL) is presented. Furthermore, in order to identify to which component the CDL have to be allocated, i.e. the MOSFET or the antiparallel JBS diode, on the one hand the proposed method is applied to a module consisting of a 10 kV SiC MOSFET with an antiparallel JBS diode (cf. **Fig. 1 (a)**), and on the other hand to a module containing only a JBS diode (cf. **Fig. 1 (b)**).

A. Description of the charging/discharging loss measurement method

For the measurement of the CDL of the 10 kV SiC devices, the same measurement setup as for the determination of the SSL can be used. The DUT is still mounted on a thermally insulated brass block, however, instead of placing the DUT in series, it is now connected in parallel to the high-side switch (cf. **Fig. 7 (a)**), which means that the voltage across the high-side switch is also applied to the DUT. Since only

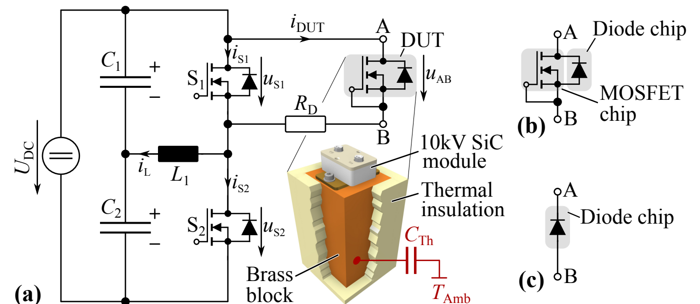

Fig. 7. **(a)** Circuit diagram of the charging/discharging loss (CDL) measurement setup. The DUT (permanently turned-off) is connected in parallel to the high-side switch via a damping resistor R_{D}. The two possible DUTs: **(b)** Co-Pack module consisting of a SiC-MOSFET chip and an antiparallel JBS diode chip and **(c)** discrete packaged JBS diode.

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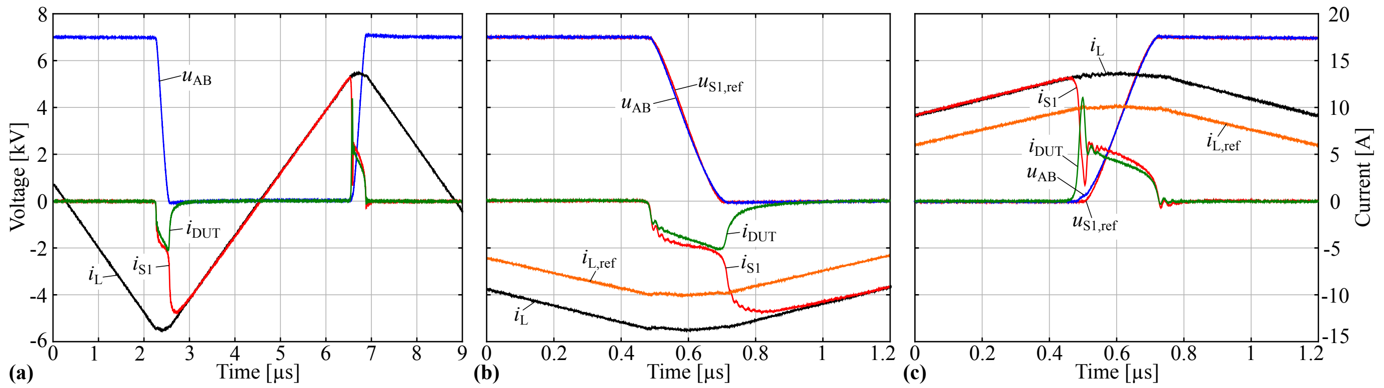

Fig. 8. **(a)** Current and voltage waveforms of the 7 kV, 10 A-equivalent CDL measurement. Detailed view of the waveforms **(b)** during the falling voltage transition and **(c)** during the rising voltage transition, where u_{AB} is matched to the voltage slope of $u_{\mathrm{S1,ref}}$, which was obtained from the 7 kV, 10 A SSL measurement.

the CDL should be measured, the DUT is permanently kept off by shorting the DUT's gate to the source terminal, thus the DUT only behaves like an additional nonlinear capacitor connected in parallel to the high-side switch. Due to the parasitic inductances of the module packages and the interconnections, a damping resistor R_{D} is added in series to the DUT, in order to avoid any ringing between the DUT and the high-side MOSFET during the switching transitions. In addition, during the on-state of S_1, R_{D} also prevents the DUT from reverse conduction, i.e. either through the body-diode of the SiC-MOSFET or the antiparallel JBS diode. As shown in **Fig. 8 (a)**, there is only a current i_{DUT} flowing through the DUT during the switching transitions, whereas during the conduction intervals of S_1 and S_2 the current i_{DUT} is zero.

The value of R_{D} was experimentally determined and is set to $R_{\mathrm{D}} = 20\,\Omega$. It should be noted that, due to the device's relatively high blocking voltage compared to its current rating, the voltage drop across R_{D} during the switching transition is negligible compared to the switched voltage, i.e. $u_{\mathrm{AB}} \approx u_{\mathrm{S1}}$. Hence, the voltage u_{AB} across the DUT closely follows the high-side MOSFET's voltage u_{S1} and the output capacitance of the DUT is entirely charged and discharged in each switching cycle. Accordingly, even though the voltage across R_{D} is comparatively small, depending on the switching frequency a significant amount of losses is dissipated in R_{D}. Therefore, R_{D} has to be thermally decoupled from the DUT in order not to influence the temperature measurement on the DUT's metal block.

Due to the parallel connection of the DUT to the high-side switch, the effective output capacitance of the half-bridge is increased, which means that compared to the SSL measurements for a given switched current the corresponding voltage slope, i.e. the $\mathrm{d}u/\mathrm{d}t$, is slowed down. In other words, for a given current, in this setup the charging current flowing through the DUT is lower compared to the current flowing through the MOSFET's parasitic output capacitance in the SSL measurements. However, in order to be able to properly assign the CDL to the correct SSL measurements, the DUT has to be tested under the same conditions. In this case, this means that the total switched current, i.e. the inductor current i_{L}, has to be increased in such a way that in both, the CDL measurement and the SSL measurement, the same $\mathrm{d}u/\mathrm{d}t$ is achieved. Consequently, based on $i = C \cdot \mathrm{d}u/\mathrm{d}t$, also the charging current in the DUT has to be the same. Exemplarily, **Figs. 8 (b) & (c)** show the measured waveforms during the two switching transients of the CDL measurement, which actually correspond to the SSL measurement carried out at $i_{\mathrm{L,ref}} = 10\,\mathrm{A}$. As can be noticed, in order to match the voltage slope u_{AB} to the corresponding voltage slope $u_{\mathrm{S1,ref}}$, the inductor current i_{L} has to be increased to $13.5\,\mathrm{A}$. This ratio between the reference current $i_{\mathrm{L,ref}}$ and the required current i_{L} slightly changes with the DC-link voltage and the current level due to the strong nonlinearity of the devices' output capacitances. However, as can be noticed, there is still a small deviation between u_{AB} and the reference voltage $u_{\mathrm{S1,ref}}$, which in consequence also leads to a slightly different charging current waveform. The reason is that, due to the parallel connection of the DUT and the high-side switch, the effective output capacitance of the high-side switch is larger than the one of the low-side switch and therefore the half-bridge is no longer symmetrical. This asymmetry can be compensated by also adding a DUT to the low-side switch, however, in this case the total output capacitance of the half-bridge is doubled. Consequently, for the SSL measurement at $i_{\mathrm{L,ref}} = 15\,\mathrm{A}$ (cf. **Fig. 5**) the corresponding CDL measurement would have to be performed at $i_{\mathrm{L}} = 30\,\mathrm{A}$, which is not possible with the given setup. Nevertheless, regardless whether one or two DUTs are used, the current pulses through the DUT are not equal for both transitions (cf. **Figs. 8 (b) & (c)**), since due to the nonlinear output capacitances of the devices, the inductor current i_{L} is not equally divided into the high and low-side switches during the switching transitions. **Fig. 9** shows the measured input (C_{iss}), reverse transfer (C_{rss}), and output capacitance ($C_{\mathrm{OSS,Co-Pack}}$) of the Co-Pack, as well as the measured output capacitance of the discrete JBS diode module (C_{Diode}) as a function of the applied bias voltage. Furthermore, the output capacitance of the MOSFET chip ($C_{\mathrm{OSS,MOSFET}}$), which has been obtained by taking the difference $C_{\mathrm{OSS,Co-Pack}} - C_{\mathrm{Diode}}$, is shown. It can be seen that the output capacitances of the MOSFET and the JBS diode are strongly nonlinear in the lower voltage range. Furthermore, it is evident that for higher voltages, the capacitance of the

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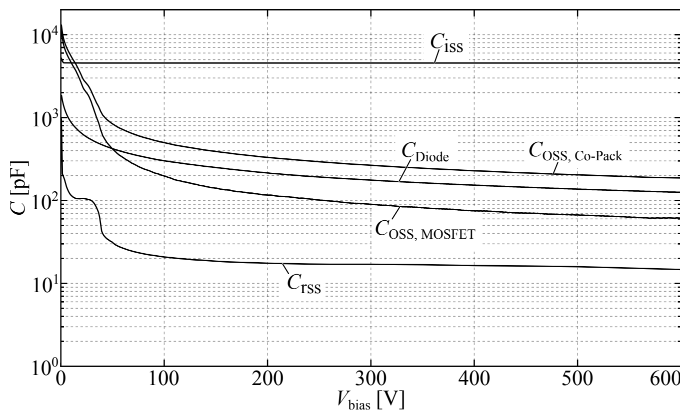

Fig. 9. Measured capacitances of the 10 kV SiC devices as function of the applied bias voltage V_{bias}. Note that the output capacitance of the MOSFET chip ($C_{\text{OSS,MOSFET}}$) is obtained by subtracting the measured output capacitance of the Co-Pack ($C_{\text{OSS,Co-Pack}}$) and the output capacitance of the JBS diode (C_{Diode}).

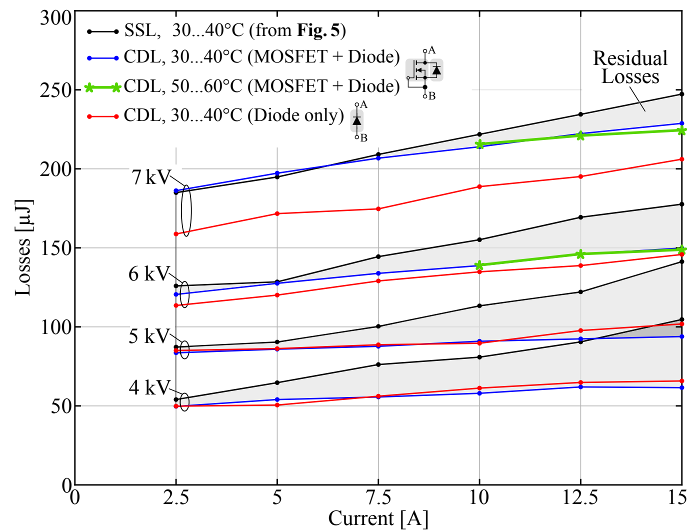

Fig. 10. Measured charging/discharging losses (CDL) of the Co-Pack module and the separate JBS diode together with the corresponding soft-switching loss (SSL) curves from **Fig. 5**. Note that measurements obtained at 30...40 °C and 50...60 °C are almost identical, i.e. the CDL are independent of the junction temperature.

JBS diode is twice as high as the output capacitance of the MOSFET chip.

Therefore, in **Fig. 8 (b)**, for example, the voltage u_{AB} across the DUT is initially at the DC-link voltage level, hence the output capacitance of the DUT and the switch S_1 is small compared to the one of S_2 and only a small part of the inductor current i_{L} is initially flowing through the DUT's output capacitance. On the other hand, when u_{AB} is small, the major part of i_{L} is charging the DUT's output capacitance, as shown in **Fig. 8 (c)**.

For the actual measurement of the CDL, the same measurement principle as described for the SSL measurements is used (cf. **Section II**). The DUT is mounted on a thermally insulated brass block and the measurement temperature range is again 30 °C...40 °C unless otherwise noted. However, in order to identify which component, i.e. the SiC-MOSFET or the JBS diode, is causing the CDL, two different types of modules, a Co-Pack module containing a SiC-MOSFET with a JBS diode and a module with only a JBS diode, are tested (cf. **Fig. 7 (b) & (c)** and **Fig. 1 (a) & (b)**).

B. Measurement results

In **Fig. 10**, the results of the CDL measurements obtained with the Co-Pack module (denoted as CDL, 30...40 °C (MOSFET + Diode)) are shown together with the results of the SSL measurements for DC-link voltages of 4...7 kV and currents between 2.5 A and 15 A. Surprisingly, at low currents the CDL and the SSL are almost identical and with higher currents, the losses drift apart from each other as indicated with the gray areas. This residual loss fraction, which is the loss difference between the SSL and the CDL, should actually correspond to the turn-off losses caused in the MOSFET-channel due to the overlapping of the voltage and current transients. Unexpectedly, the residual losses are increasing with decreasing DC-link voltage. Actually, the residual losses should be independent from the applied DC-link voltage, since on the one hand the MOSFET-channel losses are only generated in the initial period of the switching transition where the MOSFET-channel has not yet completely stopped conducting, and on the other hand the $\mathrm{d}u/\mathrm{d}t$ only depends on the switched current, which consequently results in the same overlapping of voltage and current transients. It is reasonable that the MOSFET-channel losses increase with increasing switched current, however, in this case typically the total SSL would not anymore increase linearly but rather disproportionally as shown in **Fig. 5** for a turn-off resistor of $R_{\text{off}} = 15\,\Omega$. Therefore, it is presumed that the deviation between the measured SSL and the CDL is caused by the introduced (and indispensable) damping resistor R_{D}, which on the one hand distorts the current waveform in the DUT - especially at higher current ratings or $\mathrm{d}u/\mathrm{d}t$-values - and on the other hand the voltage across R_{D} (worst case is $20\,\Omega \cdot 15\,\text{A} = 300\,\text{V}$) becomes more dominant at lower DC-link voltages. This means that, due to the linear slope of the SSL with respect to switched current and the fact that the CDL and the SSL are equal at low current, the two measurements should effectively be more or less equal at higher current ratings. Notwithstanding the above, the key message of the measurement results is that the SSL are almost exclusively originating from the charging/discharging of the DUT's output capacitance and not from the overlapping of the voltage and current transients. Consequently, the CDL constitute a lower limit for the SSL, independently of the gate driver performance and the packaging inductances of the device, which only affect the already comparably low turn-off losses.

Additionally, the CDL would also directly affect the performance of resonant DC-link inverters which achieve ZVS by forcing the drain-source voltage of the MOSFETs to zero during the current commutation by means of introducing a resonance to the DC-link capacitor [26]–[28]. Thereby, although the commutation of the load current within one MOSFET half-bridge is performed under zero voltage (and can be assumed as lossless), the output capacitances of the MOSFETs still have to be charged and discharged, leading to certain $\mathrm{d}u/\mathrm{d}t$-dependent

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CDL which have to be taken into account.

Furthermore, for the analysis of the temperature dependency of the CDL, the measurements were also conducted at a higher brass block temperature range of 50...60 °C (cf. **Fig. 10**, denoted as CDL, 50...60 °C (MOSFET + Diode)). As can be seen, the measurements obtained at 30...40 °C and 50...60 °C are almost identical. Hence, the CDL, and since these losses account for the majority of the SSL, also the SSL can be assumed to be independent from the chip temperature, as it is also the case for the hard-switching losses measured in [29]–[31].

In order to get a better idea about the resulting losses of the underlying application, the CDL, which in this case more or less correspond to the SSL, are set in relation to the stored energy in the parasitic output capacitance. For the tested 10 kV SiC Co-Pack modules, the SSL approximately correspond to $5\% - 10\%$ of the stored energy within the measured current and voltage range which underpins the outstanding switching characteristics of these 10 kV SiC devices and enables the use of comparably high switching frequencies in soft-switched applications.

It is now clear that the CDL of the 10 kV SiC Co-Pack modules at hand are responsible for the largest share of the SSL. However, the question in which component, i.e. the SiC-MOSFET or the JBS diode, the CDL are generated, remains. Therefore, besides the Co-Pack module also a separate discrete JBS diode in an identical package is tested (cf. **Fig. 7 (c)**). The corresponding CDL measurements are also shown in **Fig. 10** (denoted as CDL, 30...40 °C (Diode only)). For DC-link voltages of 4...6 kV, the CDL of the diode are more or less equal to the losses measured with the Co-Pack module. At a DC-link voltage of 7 kV, however, the measured CDL are slightly lower compared to the losses of the Co-Pack module, which means that the MOSFET starts to contribute to the CDL. Nevertheless, based on these measurements, the majority of the CDL, and consequently also of the SSL, have to be attributed to the JBS diode and surprisingly not to the SiC-MOSFET. Unfortunately, the CDL and their distribution among the JBS diode and the MOSFET cannot be estimated by the measurement of their output capacitances, since, although the capacitance of the JBS diode is only two times larger than the output capacitance of the MOSFET (cf. **Fig. 9** at higher voltages), almost the entire CDL are generated by the JBS diode. Therefore, it has to be assumed that the CDL loss mechanisms are not the same in the JBS diode and the MOSFET.

As a consequence, in order to strongly reduce the SL in converter systems employing soft-switching techniques, the JBS diode could be omitted and instead the body diode of the SiC-MOSFET could be used. Even though the body diode might have a much higher forward voltage drop, the additional CL in the short dead time interval are relatively small compared to the saved SSL. Unfortunately, since a module with a separate SiC-MOSFET was not available, the authors didn't have the opportunity to confirm this statement by experimental results.

V. Conclusion

In this paper, a novel accurate calorimetric method for the measurement of soft-switching losses (SSL) of a 10 kV SiC MOSFET is presented. As shown from literature, electrical measurement methods such as the double pulse test can lead to large measurement errors, and thus are unsuitable for the characterization of the considered 10 kV SiC MOSFET and other fast-switching devices. On the other hand, with calorimetric measurement methods, the total semiconductor losses can be measured accurately. However, the calorimetric methods presented in literature so far were not able to separate the switching losses (SL) from the conduction losses (CL) without calculations of e.g. the CL which could result again in certain measurement errors. This disadvantage is eliminated by the proposed measurement method, where an additional switch is introduced and which in combination with a novel modulation scheme enables to measure the CL and the SL separately. The error analysis for the proposed measurement method shows that the worst case error is 15 %, which is a factor of 10 to 20 more accurate than the accuracy obtained with the double pulse method. Based on the proposed measurement method, the SSL of the 10 kV SiC MOSFET are examined for different DC-link voltages, switched currents and gate resistors.

Additional charging/discharging loss (CDL) measurements revealed that the charging and discharging process of the output capacitances of the MOSFET and antiparallel JBS diode generate the largest part of the SSL. Furthermore, by testing a Co-Pack module (consisting of a 10 kV SiC-MOSFET in combination with a 10 kV JBS diode) and a separate 10 kV JBS diode module, it could be identified that the major part of the CDL and hence a major part of the SSL has to be attributed to the JBS diode and surprisingly not to the SiC-MOSFET.

Compared to the hard-switching losses, the SSL are almost 100 times lower, which enables a higher converter performance. However, the SSL are still relevant in comparison to the CL and therefore have to be considered in the converter design, especially for applications utilizing high switching frequencies.

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