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***Abstract*—The recently presented Dual Three-Phase Active Bridge (D3AB) converter integrates a three-phase Power Factor Corrected (PFC) rectifier and a DC–DC converter stage with galvanic isolation, originating from the Dual Active Bridge converter, in a single converter unit, and accordingly features low complexity, high efficiency, and high power density. This paper proposes a multi-objective optimization procedure that considers the objectives of low RMS transformer currents and/or switching losses in order to identify Pareto-optimal low-loss modulation schemes for the D3AB rectifier that meet given specifications, prevent power pulsation, and facilitate interleaved operation. From the obtained results, which are verified by means of detailed circuit simulations, an improved modulation scheme is selected, which, compared to conventional modulation, reduces the primary-side switching losses by 54 % and the total converter losses by 11 %. Due to the general nature of the presented method, the application to other three-phase rectifier/inverter topologies is directly feasible.**

I. Introduction

Recent research has shown numerous advantages of DC microgrids for a reliable and efficient integration of renewable energy sources (e.g., photovoltaics), DC loads (e.g., IT equipment), and energy storage devices (e.g., batteries) in residential applications, telecommunication systems, and data centers [2], [3]. DC microgrids are interfacing to the three-phase AC mains through bidirectional AC/DC power converters [2]. The recently proposed bidirectional Dual Three-Phase Active Bridge (D3AB) Power Factor Corrected (PFC) rectifier, depicted in **Fig. 1**, is a promising candidate for this application, since it features galvanic isolation, high efficiency, and high power density [1].

The conventional Single Phase-Shift (SPS) modulation scheme, used for the D3AB PFC rectifier in [1], operates the primary-side and secondary-side half-bridges of corresponding phases with same duty cycles, $D_1 = D_2$, and with constant phase-shift (also called load angle), φ, cf. Fig. 3 over the mains period, and achieves both, PFC functionality and isolated energy transfer. SPS features low complexity and is often employed for single- and three-phase Dual Active Bridge (DAB) converters without and with input-side boost inductors [4], [5], [6]. However, SPS may cause high conduction and switching losses.

TABLE I. Specifications of the D3AB PFC rectifier.

Nominal mains line-to-neutral voltage (rms)	$V_{\mathrm{ac}} = 230\,\mathrm{V}$
Mains frequency	$f_{\mathrm{m}} = 50\,\mathrm{Hz}$
Nominal dc port 1 voltage (non-isolated)	$V_{\mathrm{dc1}} = 800\,\mathrm{V}$
Nominal dc port 2 voltage (galv. isolated)	$V_{\mathrm{dc2}} = 400\,\mathrm{V}$
Nominal output power	$P_{\mathrm{out}} = 8\,\mathrm{kW}$

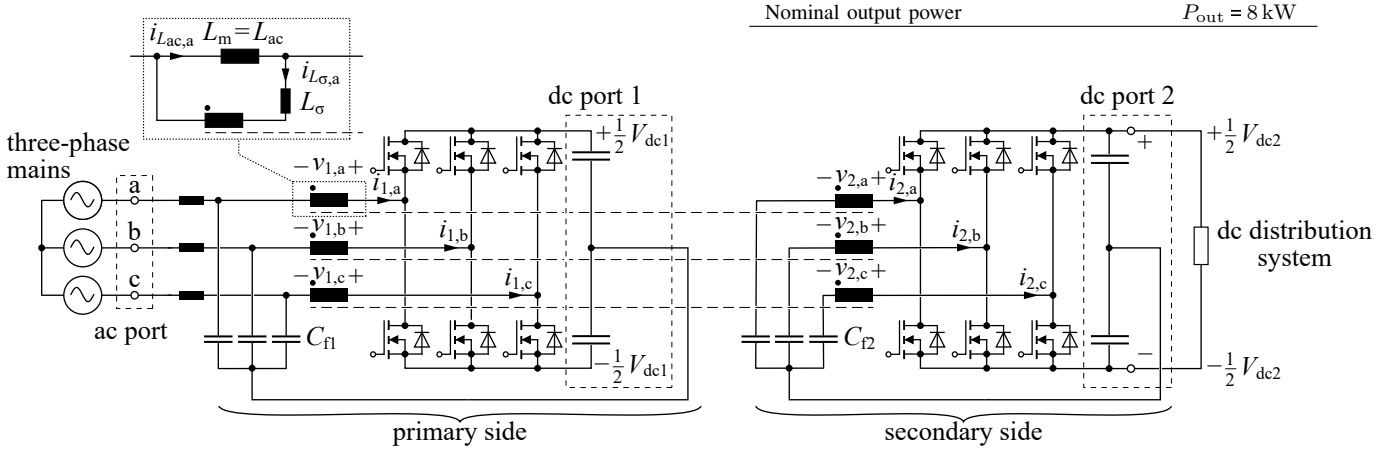

Fig. 1. Investigated converter topology (from [1]). The isolation stage of the topology behaves like three single-phase (half-bridge) DAB converters.

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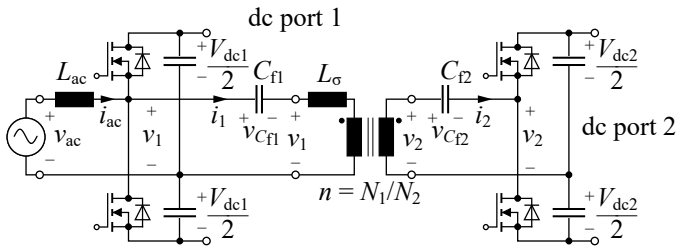

Fig. 2. Equivalent circuit of a single phase of the D3AB converter depicted in Fig. 1 with boost inductance L_{ac}, filter capacitors C_{f1} and C_{f2}, and isolating HF transformer (from [1]).

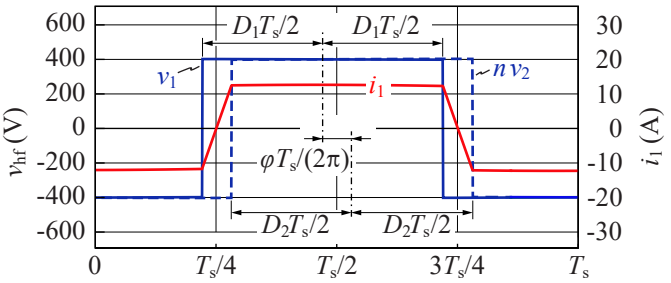

Fig. 3. Definition of D_1, D_2, and load angle φ (from [1]) with simulated waveforms over one switching period, T_s, with $f_s\,L_\sigma = 2\,\Omega$, $n = 2$, $V_{dc1} = 800\,V$, $V_{dc2} = 400\,V$, and $\varphi = 22°$.

Improvements are feasible with optimized modulation schemes, using different duty cycles on the primary and the secondary side, which are known for single-phase DAB converters, e.g., for minimal RMS transformer currents [7], and for three-phase DAB converters (minimal RMS currents [8], guaranteed Zero Voltage Switching (ZVS) over a wide load range [9], etc.).

Further numerical optimizations are shown in literature for the minimization of the total losses in single-phase DAB DC–DC [10], AC–DC [11], and three-phase DAB DC–DC [12] converters.

This paper presents a procedure, which automatically develops and evaluates modulation schemes for the grid-tied D3AB PFC rectifier to identify Pareto-optimal solutions that achieve the best trade-off between the RMS (transformer) currents and the switching losses, since previous investigations reveal that mainly the semiconductor losses (conduction, switching) and the transformer's copper losses contribute to the total converter losses. The paper is organized as follows. **Section II** describes the working principle and identifies the different degrees of freedom for the modulation of the converter shown in Fig. 1. **Section III** derives the High-Frequency (HF) equivalent circuit as well as the simplified loss models. The Pareto-optimal modulation schemes are derived in **Section IV**. **Section V** presents a possible implementation of a selected Pareto-optimal modulation scheme and a verification of the predicted improvements by means of circuit simulations, which consider detailed loss models.

II. Operating Principle

A. Single-Phase Model

The D3AB PFC rectifier can be analyzed as three single-phase converters. **Fig. 2** depicts the equivalent circuit for each phase [1]. Each single-phase converter consists of a boost rectifier and a DAB converter, using separated inductances L_{ac} and L_σ. The input voltage of each single-phase converter is equal to one mains phase voltage.

The primary-side half-bridge boosts the mains voltage to the nominal DC voltage, $V_{dc1} = 800\,V$, and ensures a sinusoidal current i_{ac}, that is in phase with the mains voltage to achieve unity power factor. At mains frequency, the impedance of the boost inductance, L_{ac}, is small and the corresponding Low-Frequency (LF) voltage drop across L_{ac} is negligible. Therefore, the local average value of the switched voltage, $\langle v_1 \rangle_{T_s}$, is considered to be equal to the mains voltage v_{ac}. Thus, the duty cycle of the primary-side half-bridge, D_1, has to be continuously varied to achieve constant DC-link voltage, V_{dc1}. The difference between switched voltages of the primary-side half-bridge and the (primary-side referred) secondary-side half-bridge, $v_1 - n\,v_2$, is applied across the stray inductance L_σ and, for $V_{dc1} = n\,V_{dc2}$, results in the typical trapezoidal DAB transformer current as illustrated in **Fig. 3**.

The turns ratio of the transformer is set to $n = 2 = {}^{V_{dc1}}/_{V_{dc2}}$ to achieve efficient operation of the DAB converter. The impedances of the inductances at switching frequency, f_s, are chosen according to the optimization carried out in [1], as $f_s\,L_{ac} = 6.8\,\Omega$ and $f_s\,L_\sigma = 2\,\Omega$. The filter capacitances C_{f1} and C_{f2} are in series with the transformer's primary and secondary winding, respectively, and prevent saturation by LF voltage components. The impedances of the filter capacitances at switching frequency are assumed to be zero.

B. Degrees of Freedom of the Three-Phase System Modulation

In total, the D3AB PFC rectifier features twelve degrees of freedom for the modulation, namely the switching frequency f_s of the half-bridges, the duty cycles of primary-side and secondary-side half-bridges ($D_{1,a}$, $D_{1,b}$, $D_{1,c}$, $D_{2,a}$, $D_{2,b}$, and $D_{2,c}$), the load angles between primary and secondary sides (φ_a, φ_b, and φ_c), and the phase-shifts at switching frequency between the phases (γ_{ab} and γ_{ac}).[1] For PFC operation, the mains phase-to-phase voltages define the differences between the local average voltages of the corresponding primary-side half-bridges, i.e.,

$$\begin{aligned} \langle v_{1,b} \rangle_{T_s} - \langle v_{1,a} \rangle_{T_s} &= v_{ac,b} - v_{ac,a}, \\ \langle v_{1,c} \rangle_{T_s} - \langle v_{1,a} \rangle_{T_s} &= v_{ac,c} - v_{ac,a}. \end{aligned} \tag{1}$$

Therefore, only the LF common mode voltage, defined as

$$v_{cm} = \frac{\langle v_{1,a} \rangle_{T_s} + \langle v_{1,b} \rangle_{T_s} + \langle v_{1,c} \rangle_{T_s}}{3}, \tag{2}$$

remains as a degree of freedom for the primary-side voltage, reducing the number of selectable primary-side duty cycles to

[1]The phase-shifts γ_{ab} and γ_{ac} refer to interleaving at the switching frequency, where γ_{ab} denotes the phase-shift between the centerlines of $v_{1,a}$ and $v_{1,b}$ and γ_{ac} the phase-shift between the centerlines of $v_{1,a}$ and $v_{1,c}$. Fig. 3 illustrates the definition of the (dash-dotted) centerlines in case of v_1 and v_2; same definitions apply to $v_{1,a}$, $v_{1,b}$, and $v_{1,c}$.

one. With, e.g., $D_{1,\mathrm{a}}$ selected, the other two duty cycles are given as

$$\begin{aligned} D_{1,\mathrm{b}} &= D_{1,\mathrm{a}} + \frac{v_{\mathrm{ac,b}} - v_{\mathrm{ac,a}}}{V_{\mathrm{dc1}}}, \\ D_{1,\mathrm{c}} &= D_{1,\mathrm{a}} + \frac{v_{\mathrm{ac,c}} - v_{\mathrm{ac,a}}}{V_{\mathrm{dc1}}}. \end{aligned} \tag{3}$$

Further, to achieve constant output power (prevent LF power pulsations), one of the load angles (e.g., φ_{c}) is defined for each operating point. Finally, with constant switching frequency operation and interleaving at the switching frequency ($\gamma_{\mathrm{ab}} = -2\pi/3$ and $\gamma_{\mathrm{ac}} = +2\pi/3$), only six degrees of freedom remain ($D_{1,\mathrm{a}}$, $D_{2,\mathrm{a}}$, $D_{2,\mathrm{b}}$, $D_{2,\mathrm{c}}$, φ_{a}, and φ_{b}), that completely define the operating point of the converter.

III. Calculation Model

To reduce the computational effort, the converter operation is evaluated at dedicated points in time that are evenly distributed over one mains period. Since the switching frequency is much higher than the mains frequency, $f_{\mathrm{s}} \gg f_{\mathrm{m}}$, converter operation during one switching period is practically the same as steady-state operation. Accordingly, steady-state converter analysis, which focuses on the HF components, i.e., at the switching frequency and multiples thereof, can be applied to determine the local RMS currents and switching losses. Important contributions from LF excitations, e.g., mains-side LF phase currents, are considered by means of superposition. The final RMS current and the switching losses over a mains period are obtained by averaging the squared values of the local RMS currents and the local switching losses, respectively.

Fig. 4 presents the derivation of the equivalent circuit of the D3AB converter used for steady-state analysis. In a first step, the voltage-source half-bridge converters are replaced by voltage sources with rectangular output voltages as shown in **Fig. 4(a)**. Each transformer is replaced by its equivalent circuit that is composed of stray inductance, magnetizing inductance,[2] and ideal transformer, shown in **Fig. 4(b)**; accordingly the circuit nodes A, B_1, B_2, and C, highlighted in Fig. 4, visualize the corresponding modifications in case of phase a. Node B_1 can be connected to B_2' without loss of generality; the ideal transformer of phase a can be omitted (remark: the modifier $'$ is used for secondary-side quantities that are transformed to the primary side). Furthermore, the HF components of the voltages across the filter capacitors C_{f1} and C_{f2} are approximately zero, thus, also the nodes corresponding to B_1 and B_2' in phases b and c can be connected together. This translates to the modifications depicted in **Fig. 4(c)** and, with the filter capacitors being replaced by short-circuits, the final equivalent circuit shown in **Fig. 4(d)**, which is used for the optimization.

[2]In the D3AB converter, the magnetizing inductance serves as PFC boost inductance.

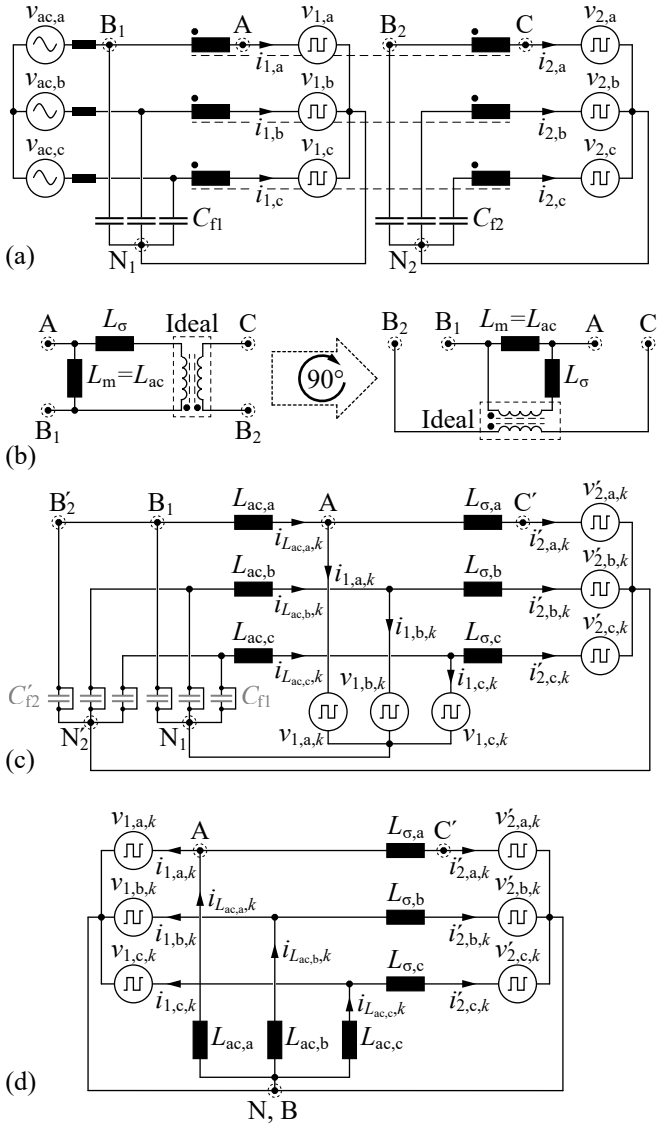

Fig. 4. Derivation of a simplified equivalent circuit suitable for the optimization of the modulation scheme: **(a)** voltage-source half-bridge converters being replaced by voltages sources with rectangular output voltages; **(b)** equivalent transformer circuit with magnetizing inductance $L_{\mathrm{m}} = L_{\mathrm{ac}}$, stray inductance L_σ, and ideal transformer; **(c)** HF equivalent circuit with transformers being replaced by their equivalent circuits and the ideal transformer being omitted (shorted filter capacitances in light gray); **(d)** final HF equivalent circuit, where all filter capacitors are replaced by short-circuits.

A. Loss Model

The optimization employs two cost functions, which represent conduction and switching losses of the converter, i.e.,

$$\xi_{\mathrm{rms}} = \sum_{p=\{\mathrm{a,b,c}\}} \left[I_{1,p,\mathrm{rms}}^2 + \left(I_{2,p,\mathrm{rms}}^{\prime} \right)^2 \right], \tag{4}$$

$$\begin{aligned} \xi_{\mathrm{sw}} = \sum_{p=\{\mathrm{a,b,c}\}} \Big\{ & \xi_{\mathrm{e}} \left[i_{1,p}(t_{1,p,\uparrow}) \right] + \xi_{\mathrm{e}} \left[-i_{1,p}(t_{1,p,\downarrow}) \right] \\ & + \xi_{\mathrm{e}} \left[i_{2,p}^{\prime}(t_{2,p,\uparrow}) \right] + \xi_{\mathrm{e}} \left[-i_{2,p}^{\prime}(t_{1,p,\downarrow}) \right] \Big\}, \end{aligned} \tag{5}$$

respectively, where the subscripts $\uparrow$ and $\downarrow$ denote instants with rising and falling edges of $v_{1,p}$ or $v_{2,p}$, respectively. Further-

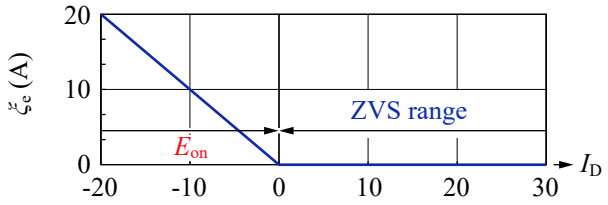

Fig. 5. Simplified, scalable switching loss function ξ_e considering a rising edge of the voltage at the switching node. Positive instantaneous current into the half-bridge, $I_D > 0$, results in soft switching and $\xi_e = 0$ applies. Negative current results in hard switching, with $\xi_e = |I_D|$.

more, ξ_e denotes a simplified representation of MOSFET's switching losses according to **Fig. 5** where hard switching losses are modeled proportionally to the switched current and soft switching losses are assumed to be zero. In the case of a duty cycle of 0 or 1, the corresponding half-bridge is not switching and the switching losses are set to zero.

B. Symmetry

Due to symmetry in the three-phase mains voltages, it is sufficient to consider one third of the mains period,

$$t_{\mathrm{m},1} = -\frac{T_\mathrm{m}}{6} \leq t_\mathrm{m} < t_{\mathrm{m},4} = +\frac{T_\mathrm{m}}{6}\,, \tag{6}$$

for the optimization as drawn in **Fig. 6**. During the second and the third part of the mains period, the values of the control variables, e.g., of phase a ($D_{1,\mathrm{a}}$, $D_{2,\mathrm{a}}$, and φ_a), are obtained with

$$\left.\begin{aligned} D_{1,\mathrm{a}}(t_\mathrm{m}) &= D_{1,\mathrm{c}}\left(t_\mathrm{m} - \tfrac{T_\mathrm{m}}{3}\right) \\ D_{2,\mathrm{a}}(t_\mathrm{m}) &= D_{2,\mathrm{c}}\left(t_\mathrm{m} - \tfrac{T_\mathrm{m}}{3}\right) \\ \varphi_\mathrm{a}(t_\mathrm{m}) &= \varphi_\mathrm{c}\left(t_\mathrm{m} - \tfrac{T_\mathrm{m}}{3}\right) \end{aligned}\right\} \forall\ t_{\mathrm{m},4} \leq t_\mathrm{m} < t_{\mathrm{m},4} + \frac{T_\mathrm{m}}{3}, \tag{7}$$

$$\left.\begin{aligned} D_{1,\mathrm{a}}(t_\mathrm{m}) &= D_{1,\mathrm{b}}\left(t_\mathrm{m} - \tfrac{2T_\mathrm{m}}{3}\right) \\ D_{2,\mathrm{a}}(t_\mathrm{m}) &= D_{2,\mathrm{b}}\left(t_\mathrm{m} - \tfrac{2T_\mathrm{m}}{3}\right) \\ \varphi_\mathrm{a}(t_\mathrm{m}) &= \varphi_\mathrm{b}\left(t_\mathrm{m} - \tfrac{2T_\mathrm{m}}{3}\right) \end{aligned}\right\} \forall \left\{\begin{aligned} &t_\mathrm{m} \geq t_{\mathrm{m},4} + \tfrac{T_\mathrm{m}}{3} \wedge \\ &t_\mathrm{m} < t_{\mathrm{m},4} + \tfrac{2T_\mathrm{m}}{3}, \end{aligned}\right. \tag{8}$$

respectively. For the variables of phases b and c, the same way of reconstruction is applied by using the values of the two other phases according to Fig. 6, where dash-dotted, dotted, and dashed line segments refer to the variables calculated for phases a, b, and c during $t_{\mathrm{m},1} \leq t_\mathrm{m} < t_{\mathrm{m},4}$, respectively.

C. Current Calculation

For simplicity, the required equations are only explained for phase a, since similar expressions apply to phases b and c. All voltages and currents of the converter are calculated in the frequency domain as introduced in [13]. The Fourier coefficients (e.g., $\underline{V}_{1,\mathrm{a},k} = a_{v_{1,\mathrm{a},k}} + \mathrm{j}\, b_{v_{1,\mathrm{a},k}}$) of the HF voltage sources are derived for K integer harmonics of the switching frequency, f_s. Using the superposition property, the expressions for the inductor currents, $\underline{I}_{L_{\mathrm{ac,a}},k}$ and $\underline{I}_{L_{\sigma,\mathrm{a}},k}$, are given by

$$\underline{I}_{L_{\mathrm{ac,a}},k} = -\frac{\underline{V}_{1,\mathrm{a},k}}{2\pi k f_\mathrm{s} L_{\mathrm{ac,a}}}, \tag{9}$$

$$\underline{I}_{L_{\sigma,\mathrm{a}},k} = \frac{\underline{V}_{1,\mathrm{a},k}}{2\pi k f_\mathrm{s} L_{\sigma,\mathrm{a}}} - \frac{\underline{V}_{2,\mathrm{a},k}}{2\pi k f_\mathrm{s} L_{\sigma,\mathrm{a}}}. \tag{10}$$

The input current of the secondary-side half-bridge and in the secondary-side transformer winding is equal to the current in the stray inductance, $\underline{I}'_{2,\mathrm{a},k} = \underline{I}_{L_{\sigma,\mathrm{a}},k}$ and the input current of the primary-side half-bridge and in the primary-side transformer winding is the difference of the current in the ac inductance and the stray inductance, $\underline{I}_{1,\mathrm{a},k} = \underline{I}_{L_{\mathrm{ac,a}},k} - \underline{I}_{L_{\sigma,\mathrm{a}},k}$.

The square of the RMS value of a current, used to determine ξ_rms, cf. (4), is calculated with

$$I^2_{1,\mathrm{a,rms}} = \sum_{k=1}^{K} \frac{|\underline{I}_{1,\mathrm{a},k}|^2}{2}\,,\quad \left(I'_{2,\mathrm{a,rms}}\right)^2 = \sum_{k=1}^{K} \frac{|\underline{I}'_{2,\mathrm{a},k}|^2}{2}. \tag{11}$$

For the switching cost function, the switched current in a half-bridge is calculated with an inverse Fourier transformation of the currents $\underline{I}_{1,\mathrm{a},k}$ and $\underline{I}'_{2,\mathrm{a},k}$, as

$$\begin{aligned} i_{1,\mathrm{a}}(t_{1,\mathrm{a},\uparrow\downarrow}) = &\sum_{k=1}^{K} |\underline{I}_{1,\mathrm{a},k}| \cos\left(2\pi k \frac{t_{1,\mathrm{a},\uparrow\downarrow}}{T_\mathrm{s}} + \angle\underline{I}_{1,\mathrm{a},k}\right) \\ &+ \begin{cases} +I_{\mathrm{m,a}} & \text{for rising edge,} \\ -I_{\mathrm{m,a}} & \text{for falling edge,} \end{cases} \end{aligned} \tag{12}$$

$$i'_{2,\mathrm{a}}(t_{2,\mathrm{a},\uparrow\downarrow}) = \sum_{k=1}^{K} |\underline{I}'_{2,\mathrm{a},k}| \cos\left(2\pi k \frac{t_{2,\mathrm{a},\uparrow\downarrow}}{T_\mathrm{s}} + \angle\underline{I}'_{2,\mathrm{a},k} + \varphi_\mathrm{a}\right), \tag{13}$$

and is only evaluated in the instants of rising, $\uparrow$, and falling edges, $\downarrow$, of $v_{1,\mathrm{a}}$ and $v_{2,\mathrm{a}}$. The instants are calculated from the primary-side and secondary-side duty cycles,

$$t_{1,\mathrm{a},\uparrow\downarrow} = T_\mathrm{s}\,\frac{1 \mp D_{1,\mathrm{a}}}{2}, \quad t_{2,\mathrm{a},\uparrow\downarrow} = T_\mathrm{s}\,\frac{1 \mp D_{2,\mathrm{a}}}{2}. \tag{14}$$

The constant current $I_{\mathrm{m,a}}$ represents the mains frequency component of the current in the boost inductor. Finally, with

$$P_\mathrm{tot} = \sum_{p=\{\mathrm{a,b,c}\}} \sum_{k=1}^{K} \frac{\Re\left(\underline{V}_{1,p,k}\,\underline{I}^*_{1,p,k}\right)}{2}, \tag{15}$$

the power transferred from primary to secondary side can be calculated.

IV. Optimization

To optimize the modulation scheme, the considered time interval, $t_{\mathrm{m},1} \leq t_\mathrm{m} < t_{\mathrm{m},4}$, is divided into N_m equally sized time steps, e.g., $t_{\mathrm{m},1}$, $t_{\mathrm{m},2}$, $t_{\mathrm{m},3}$, and $t_{\mathrm{m},4}$ as shown in Fig. 6. Furthermore, each of the four duty cycles and two load angles, representing the six degrees of freedom, is divided into N_D (e.g., $D_{1,\mathrm{a}} = \{0, 0.1, 0.2, \ldots, 1\}$) and N_φ equally sized steps, respectively. At each time, $t_{\mathrm{m},1}$, $t_{\mathrm{m},2}$, and $t_{\mathrm{m},3}$, all $N_D^4 \times N_\varphi^2$ operating points, are evaluated. For each operating point, the voltages and currents of the converter are calculated for one

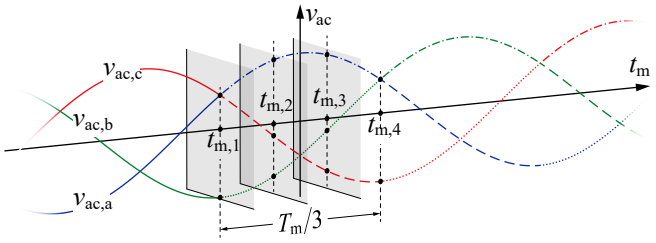

Fig. 6. Symmetries in the three-phase mains voltages allow for a reduction of the considered time interval. The times $t_{m,1}$, $t_{m,2}$, $t_{m,3}$, and $t_{m,4}$ are used in the course of the explanations presented in this paper. The dash-dotted, dotted, and dashed line segments refer to the phases a, b, and c during $t_{m,1} \leq t_m < t_{m,4}$, respectively.

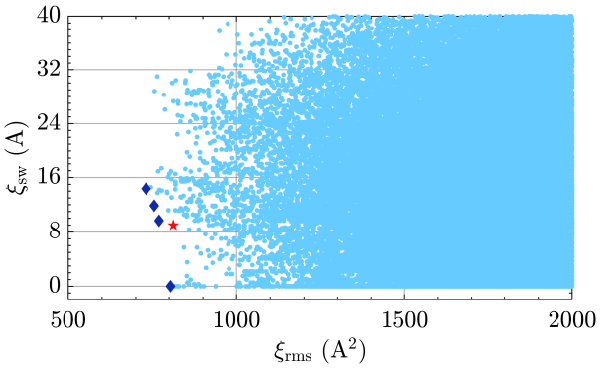

Fig. 7. Local Pareto plot of the cost functions ξ_{rms} and ξ_{sw} at $t_m = 0$; the diamonds (♦) mark the local Pareto-front and the star (⋆) denotes the operating point with the conventional modulation scheme used in [1].

full switching period, T_s. An exemplary result for $t_m = 0$ is shown in **Fig. 7** where the cost functions ξ_{rms} and ξ_{sw} are plotted on both axes, allowing a visualization of the existing trade-off between conduction and switching losses. Over the entire third of a mains period, up to $N_m \times N_D^4 \times N_\varphi^2$ operating points result, for which the cost functions are evaluated.

The calculated operating points are only valid in the temporal proximity of $t_{m,1}$, $t_{m,2}$, and $t_{m,3}$. To get a complete modulation scheme that is applicable to the whole mains period, one operating point in each time step can be successively connected to all reachable operating points at the next time step to create a path from $t_{m,1}$ to $t_{m,3}$ as illustrated in **Fig. 8**.[3] To close the path, the points at $t_{m,3}$ and $t_{m,4}$ are connected together, where the points at $t_{m,4}$ are obtained by considering symmetry as described in Section III-B. For the $N_m \times N_D^4 \times N_\varphi^2$ operating points, up to $\left(N_D^4 \times N_\varphi^2\right)^{N_m}$ paths exist, which already for small numbers of N_m, N_D, and N_φ leads to enormous computational effort that cannot be carried out in reasonable time with current computing power.

A. Reduction Functions

Reduction functions are introduced to reduce the number of possible paths in the optimization procedure. The reduction functions decrease the number of considered operating points in each time step of the path finding process, with the drawback that some optimal paths might be removed. In power electronic systems, however, optima are typically found to be relatively flat and therefore, only minor implications on the final results are expected if the reduction functions are carefully chosen.

[3]The presented procedure is similar to dynamic programming [14], however, the procedure in this paper differs in that it is specifically designed for PFC converters, allows for the optimization of a problem that does not have optimal substructure, and maintains the multi-objective characteristic for the results.

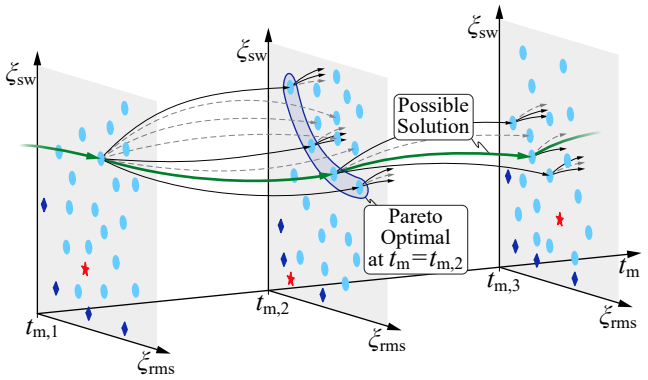

Fig. 8. Illustration of the path search procedure starting at $t_{m,1}$; solid arrows (→) indicate Pareto-optimal connections; dashed arrows (⇢) are disregarded; the bold arrows mark a possible solution.

First, sudden changes of the control variables between two subsequent instants, e.g., large sudden changes of the duty cycles, are limited to avoid HF components in the transformer currents, which would not be blocked by the filter capacitances, C_{f1} and C_{f2}, and could potentially saturate the transformer core. The corresponding limits, ΔD_{max} for the duty cycles and $\Delta\varphi_{max}$ for the load angles, are determined based on the approach explained below, in order to establish a configuration environment for the optimization that is independent of the number of time intervals, N_m. With regard to ΔD_{max}, the maximum rate of change of the local average voltage at the switching node of each primary-side half-bridge is considered, which occurs if one of the three phases of the primary-side rectifier is clamped, i.e., the local average voltage at one switching node is constant. In this case, the time derivatives of the local average voltages at the remaining primary-side switching nodes are equal to the time derivatives of the corresponding mains' phase-to-phase voltages, with a maximum voltage slope of $\left(\Delta V/\Delta t\right)_{max} = 2\pi f_m \sqrt{3}\sqrt{2} V_{ac}$. Since the duration of the time interval between two subsequent optimization points is $\Delta t = t_{m,2} - t_{m,1} = \left(3 N_m f_m\right)^{-1}$, the local average values of the switched primary-side voltages are subject to a maximum voltage change of

$$\Delta V_{max} = 2\pi f_m \sqrt{3}\sqrt{2} V_{ac} \times \Delta t. \tag{16}$$

Due to $\Delta D = {}^{\Delta V}/_{V_{dc1}}$ and with a safety factor of two, the final result for the tolerated step of each duty cycle is

$$\Delta D_{max} = \frac{4\pi\sqrt{2}\, V_{ac}}{\sqrt{3}\, N_m\, V_{dc1}}. \tag{17}$$

With regard to the load angles, a maximum rate of change of φ, $\left({}^{d\varphi}/_{dt}\right)_{max} = 2\pi\Delta f_{s,max}$, is defined, in order to facilitate the definition of a configuration variable that is independent

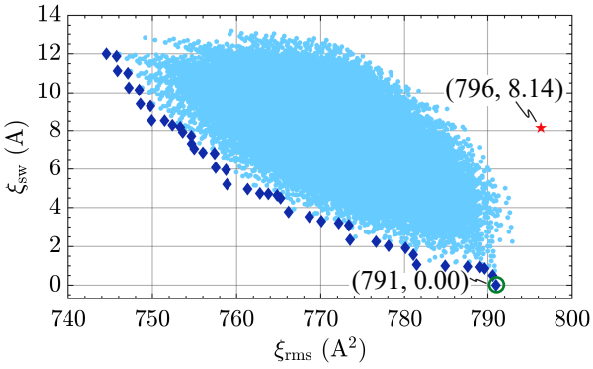

Fig. 9. Global Pareto plot of the total costs of possible paths representing complete modulation schemes; the diamonds (♦) mark the global Pareto-front and the star (⋆) denotes the conventional modulation scheme.

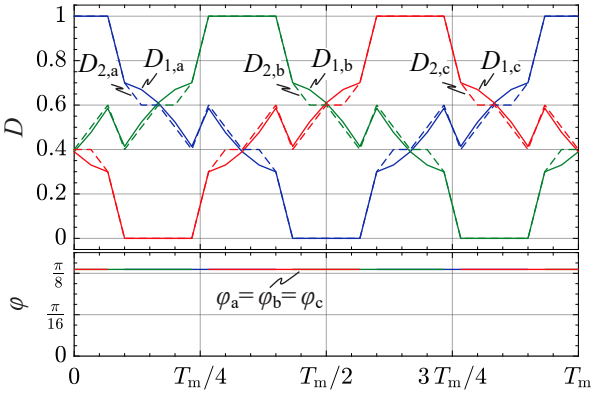

Fig. 10. Investigated optimization result (♦ in Fig. 9); similar duty cycles are determined on the primary side (solid line, ——) and the secondary side (dashed line, - - -); all load angles are constant, $\varphi_a = \varphi_b = \varphi_c \approx 0.4\,\mathrm{rad}$; each phase is clamped during one third of the mains period.

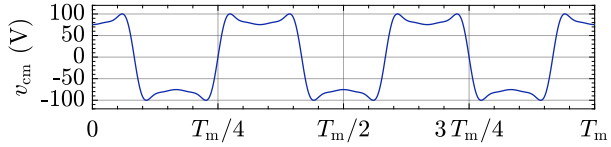

Fig. 11. Common mode voltage, which results with the investigated optimal modulation scheme (♦ in Fig. 9).

of N_m. The corresponding allowable change of each load angle between two subsequent optimization points is obtained by means of integration,

$$\varphi_{\max}(t+\Delta t) = \varphi(t) + 2\pi \int_{t}^{t+\Delta t} \Delta f_{\mathrm{s,max}}\,\mathrm{d}\tau$$
$$\Rightarrow \Delta\varphi_{\max} = \varphi_{\max}(t+\Delta t) - \varphi(t) = \frac{2\pi\,\Delta f_{\mathrm{s,max}}}{3\,N_\mathrm{m}\,f_\mathrm{m}}. \tag{18}$$

The calculation of all possible paths starts with all operating points on the plane at $t_\mathrm{m} = t_{\mathrm{m},1}$, as shown in Fig. 8. For each operating point at $t_\mathrm{m} = t_{\mathrm{m},1}$, the reachable points in the next instance, at $t_\mathrm{m} = t_{\mathrm{m},2}$, i.e., where the maximum allowed changes of the duty cycles and load angles are not exceeded, are considered, as shown with arrows pointing from the plane at $t_{\mathrm{m},1}$ to that at $t_{\mathrm{m},2}$ in Fig. 8. To further reduce the possible paths, only the Pareto-optimal subset of the reachable points is considered (solid arrows, →) while the other points are disregarded (dashed arrows, -→). From all the points that are Pareto-optimal in the first step, the same procedure is repeated to determine suitable paths from $t_{\mathrm{m},2}$ to $t_{\mathrm{m},3}$ and from $t_{\mathrm{m},3}$ back to $t_{\mathrm{m},1}$. To close the path, it is checked whether the point at $t_{\mathrm{m},1}$, where the search has started, is part of the Pareto-optimal subset that is reachable from $t_{\mathrm{m},3}$.

This procedure evaluates all possible paths that satisfy the reduction functions. Each path represents a complete modulation scheme valid for a full mains period. To enable a comparative evaluation of the different complete modulation schemes, the total costs of each path are defined as the mean values of the individual costs along the path.

B. Global Optimum

The discretization chosen for the optimization was selected such that a reasonable calculation time and sufficient calculation accuracy is achieved. The time discretization is set to $N_\mathrm{m} = 10$, what corresponds to a time resolution of $(3N_\mathrm{m}f_\mathrm{m})^{-1} \approx 0.67\,\mathrm{ms}$. For the discretization of the duty cycles, $N_D = 11$ is chosen, that allows duty cycle values of $D = \{0, 0.1, 0.2, \ldots, 1\}$ with a resolution of 0.1. Since small changes of the load angles are causing large changes of the transfered power [1], it is important to have high resolutions for the load angles. Therefore, the discretization is set to $D_\varphi = 61$, allowing load angle values of $\varphi = \{0, 0.105, 0.209, \ldots, 2\pi\}\,\mathrm{rad}$ with a resolution of $0.105\,\mathrm{rad}$ (6 °). The maximal load angle of $2\pi\,\mathrm{rad}$ is used as a placeholder, indicating a clamped secondary-side half-bridge. The calculations of the currents and voltages in the frequency domain consider $K = 30$ harmonics of the switching frequency. According to (17) and (18), a maximal change of the duty cycles of $\Delta D_{\max} \approx 0.3$ and a maximal load angle change of $\Delta\varphi_{\max} \approx 0.105\,\mathrm{rad}$ is allowed during the path finding process.[4] The resolutions of the duty cycles and the load angles are chosen such that they are integer parts of the corresponding limits $\Delta D_{\max}$ and $\Delta\varphi_{\max}$, which allows for an efficient implementation.

Fig. 9 depicts the total costs determined for $\approx 3\times10^5$ complete modulation schemes using these settings. The star (⋆) denotes the mean costs for the conventional modulation scheme, which is shown for reason of comparison. The results reveal a trade-off between conduction and switching losses, indicated with diamonds (♦), representing a global Pareto-front.

One very interesting result, which allows for very low switching losses, is marked with a circle (♦) in Fig 9. The duty cycles and load angles of this scheme are plotted in **Fig. 10** over a full mains period. The corresponding duty cycles on the primary side (solid line, ——) and the secondary side (dashed line, - - -) of each phase are similar and all three load angles

[4]The maximal change of the load angle is obtained for $\Delta f_{\mathrm{s,max}} = 25\,\mathrm{Hz}$, which is chosen such that $\Delta\varphi_{\max}$ is equal to the resolution of the load angle. A higher value, e.g., $\Delta f_{\mathrm{s,max}} = 100\,\mathrm{Hz}$, would lead to a more accurate result of the optimization, however, causes a substantial increase of the computational effort.

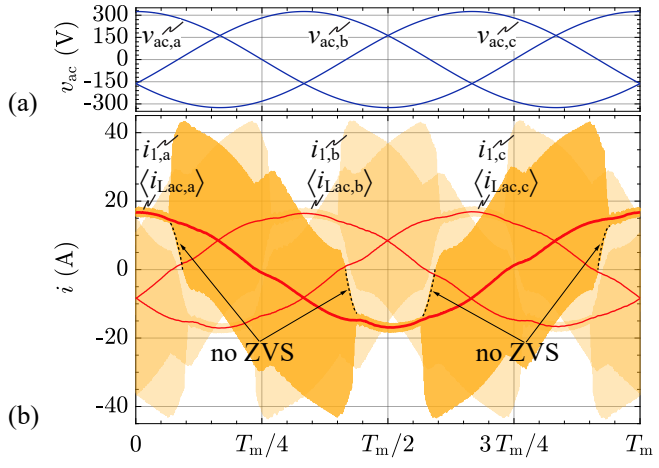

Fig. 12. Simulation results for the specifications given in Table **Table I** and the component values given in Table **Table II**: **(a)** Sinusoidal three-phase mains voltages; **(b)** filtered input currents and primary-side transformer currents; clamping of phase a occurs during $0 < t_m < {}^{T_m}/_{12}$, ${}^{5T_m}/_{12} < t_m < {}^{7T_m}/_{12}$, and ${}^{11T_m}/_{12} < t_m < T_m$; the THD values of the filtered phase currents are less than 3.5 %.

are constant and of same value.

This optimized modulation scheme mainly utilizes a LF common mode voltage, v_{cm}, to prevent hard-switching operation of the primary-side half-bridges by clamping the phase with the highest mains current, which is the main difference compared to the conventional modulation scheme. The calculated common mode voltage, as defined in (2), is shown for the optimized modulation scheme in **Fig. 11**. The conduction losses are similar to those of the conventional modulation scheme, even though only the two switching phases contribute to energy transfer between primary and secondary sides. This is reasonable, because the duty cycles of the switching half-bridges are close to 0.5, allowing efficient operations of the DAB converters.

V. Circuit Simulations

The calculation results of the optimization procedure are verified with detailed circuit simulations. The simulation employs three separate single-phase current PI-controllers, which ensure sinusoidal phase currents that are in phase with the mains voltages, and two voltage PI-controllers to stabilize the DC-link voltages. The first voltage controller regulates the DC-link voltage on the primary side, V_{dc1}, by adapting the amplitudes of the three-phase ac currents. The second voltage controller regulates the DC-link voltage on the secondary side, V_{dc2}, by adapting the load angles of all three phases, according to the operation principle of the D3AB converter [1].

This control structure is used to verify the conventional and the optimized modulation scheme. To realize the optimized modulation scheme, the calculated common mode voltage is added to the set voltages determined by the current controllers. Differences between primary-side and secondary-side duty cycles, shown in Fig. 10, are neglected.

The simulation uses the specifications given in **Table I** and the component values listed in **Table II**, which mainly

TABLE II. Component values of the D3AB PFC rectifier.

Switching frequency	$f_s = 35\,\text{kHz}$
Transformer turns ratio	$n = 2$
Magnetizing inductance	$L_{ac} = 195\,\mu\text{H}$
Stray inductance (on secondary side)	$L_\sigma = 14.5\,\mu\text{H}$
DC-link capacitance, primary side	$C_{dc1} = 24\,\mu\text{F}$
DC-link capacitance, secondary side	$C_{dc2} = 16.8\,\mu\text{F}$
Filter capacitance, primary side	$C_{f1} = 3.9\,\mu\text{F}$
Filter capacitance, secondary side	$C_{f2} = 22.5\,\mu\text{F}$

stem from the values derived in [1]. The result for the optimized modulation scheme is shown in **Fig. 12**. The filtered phase currents, $\langle i_{Lac,a} \rangle_{T_s}$, $\langle i_{Lac,b} \rangle_{T_s}$, and $\langle i_{Lac,c} \rangle_{T_s}$, of the simulation are sinusoidal[5] with a Total Harmonic Distortion (THD) less than 3.5 % and are in phase with the mains voltages; the resulting power factor is $\cos(\Phi) > 0.99$. The observed rapid changes of the primary-side current ripples occur at the beginning and the end of each time interval where the corresponding phase is clamped. Furthermore, **Fig. 12(b)** confirms that the phase with the highest current is clamped, since the input current of the clamped half-bridge features the smallest current ripple.

The evaluation of the loss model derived in Section III-A, using circuit simulation, results in $\xi_{rms} = 704\,\text{A}^2$ and $\xi_{sw} = 9.2\,\text{A}$ for the conventional and $\xi_{rms} = 725\,\text{A}^2$ and $\xi_{sw} = 3.3\,\text{A}$ for the optimized modulation scheme. The differences between the calculated and the simulated costs, ξ_{rms} and ξ_{sw}, cf. Fig. 9, are mainly attribute to the limited resolutions of duty cycles and load angles. A recalculation for the conventional modulation scheme with increased resolutions, $N_D = 100$ and $N_\varphi = 1000$, changes the estimated costs to $\xi_{rms} = 718\,\text{A}^2$ and $\xi_{sw} = 8.8\,\text{A}$, which is within a 5 % tolerance band compared to the simulation result. Furthermore, the simulation predicts a reduction of the switching losses by 63 % instead of 100 % predicted by the calculation. In the simulation, additional switching losses occurring during the transitions from switching to clamping and vice versa, indicated with a dashed line (- - -) in Fig. 12(b), are considered. These transitions cause hard switching operation of the primary-side half-bridges and are not considered in the calculation because of the limited time step resolution, N_m.

To further verify the correctness of the obtained solution, the more detailed loss model of [1], which includes skin and proximity effects, core losses, conduction losses, and switching losses, is applied to the simulation results. Compared to the conventional modulation scheme, the optimized modulation scheme enables a total loss reduction of 17 W or 11 %, as illustrated in **Fig. 13**. The loss savings mainly originate from reduced switching losses of the primary-side half-bridges, $P_{sw,prim}$ (from 30 W to 14 W or 54 %). The copper losses and the conduction losses remain approximately the same, what is in good agreement with the previously conducted estimation based on the current RMS cost function, ξ_{rms}.

[5]The observed deviation from the sinusoidal waveform is due to power pulsation on the primary-side DC-link. Related improvements are subject to future investigation.

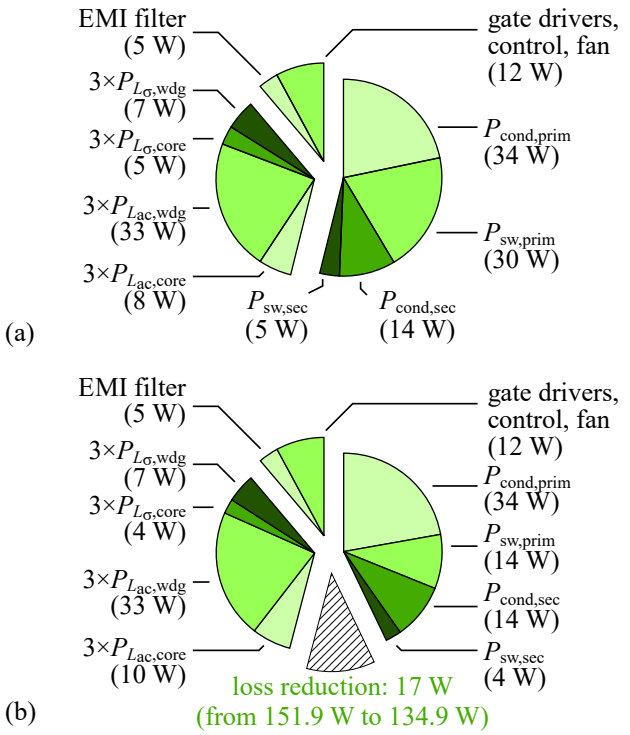

Fig. 13. Simulation results using the more detailed loss model presented in [1], for operation with rated power according to Tables **Tables I** and **II**: **(a)** conventional modulation scheme; **(b)** optimized modulation scheme, which enables a total loss reduction of 17 W or 11 % that mainly originates from reduced switching losses of the primary-side half-bridges, $P_{\mathrm{sw,prim}}$.

The result further reveals slightly increased core losses in the boost inductors, $P_{L_{\mathrm{ac}},\mathrm{core}}$, for operation with the optimized modulation scheme, even though reduced core losses may be expected since each phase is clamped during one third of the mains period. However, increased current ripples during periods with active switching operations cause an increase of $P_{L_{\mathrm{ac}},\mathrm{core}}$. The opposite effect is observed in case of the core losses in the stray inductances, $P_{L_\sigma,\mathrm{core}}$, where phase clamping leads to a slight decrease of the losses. Overall, similar total core losses of 13 W . . . 14 W are expected for both, the conventional and the optimized modulation scheme.

VI. Conclusion

This paper proposes an automated procedure to optimize the modulation scheme for a grid-tied D3AB PFC rectifier, with the objective to minimize copper, conduction, and switching losses. The optimization utilizes simplified loss models, circuit symmetry, and circuit calculations in the frequency domain to achieve a time-efficient computation of the loss characteristics of different modulation schemes. Circuit simulations serve for a thorough verification of the calculated results. The optimization identifies numerous different modulation schemes that are expected to feature lower losses than the conventional modulation scheme. From all these, one particularly promising result, which effectively lowers the losses resulting from hard switching, is selected for further analysis. The circuit simulation with detailed loss models, including skin and proximity effects, core losses, conduction losses, and switching losses, reveals a reduction of the primary-side switching losses by 54 % and a reduction of the total losses by 11 % as compared to the conventional modulation scheme.

Further research will be conducted towards a hardware implementation of the optimized modulation scheme to achieve an experimental verification of the predicted loss reduction. Additional improvements include the consideration of further loss mechanisms (e.g., core losses), implications on volume and losses of the Electromagnetic Interference (EMI) filter, and the investigation of alternative converter configurations.

Due to the generic nature of the presented procedure, its applicability is not limited to the D3AB converter topology. It is rather successfully demonstrated in this work that the automatic optimization of the operation of a power converter, as part of an overall converter optimization, is feasible with today's regularly available computational power. In this regard, the proposed procedure can be included into intelligent future automation systems in order to achieve a continuous optimization in the context of Industry 4.0.

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