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The Impact of Multi-MHz Switching Frequencies on Dynamic On-Resistance in GaN-on-Si HEMTs

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ABSTRACT Dynamic on-resistance (dR_{on}), where the on-resistance immediately after turn-on is higher than the DC resistance, increases the conduction losses in power converters with gallium nitride high-electron-mobility transistors (GaN HEMTs). There exist no direct dR_{on} measurements in the literature above 1 MHz, leaving designers unable to predict conduction losses in emerging multi-MHz applications. We address this literature gap by collecting the first on-state voltage dR_{on} measurements at multi-MHz frequencies, with a focus on the zero-voltage-switching conditions that are predominantly employed at high frequency. On the selected commercially-available HEMT with a breakdown voltage below 200 V, the dynamic contribution asymptotes above ≈ 2 MHz, a finding predicted by the slow time constants of the traps that cause dR_{on}. For the tested HEMT, we find a maximum dR_{on} increase over the DC resistance of $2\times$ in a multi-MHz, zero-voltage-switched application.

INDEX TERMS Dynamic on-state resistance, gallium nitride, power transistors, wide bandgap semiconductors.

I. INTRODUCTION

Increasing the switching frequency of power converters to the high-frequency (HF) range, between 3 MHz to 30 MHz, is an avenue to reduce passive component size, weight, and cost [1]. Gallium nitride high-electron-mobility transistors (GaN HEMTs) are an especially promising power semiconductor technology for this frequency range [2], but are known to suffer from "current collapse," or dynamic R_{on} (dR_{on}), where the on-resistance immediately after turn-on is noticeably higher than the nominal, steady-state value (R_{dc}) [3]. dR_{on} is caused by the trapping of electrons in the GaN HEMT structure, with two dominant mechanisms: off-state trapping (caused by drain-source and drain-substrate bias in the off-state) and hot electron trapping (caused by current-voltage overlap during the switching transition) [4]–[6]. With these electrons trapped in undesirable locations in the structure, the concentration of electrons in the 2-D electron gas (2DEG) must be proportionally reduced to maintain overall charge neutrality. During the finite time required to detrap these electrons, the device exhibits reduced drain-source current and consequently higher-than-expected on-resistance, or dR_{on}. In high-frequency applications, dR_{on} directly determines conduction losses since dynamic effects dominate the effective on-resistance for the entire conduction period, and the importance of accurate dR_{on} characterization is underscored by a recent dR_{on}-focused JEDEC standard [7].

This phenomenon is well-characterized at lower frequencies in commercially-available HEMTs [8], although with some discrepancy in methodology and reported values [9]. In the high-frequency range, however, there are no valid dR_{on} measurements in the literature to our knowledge, leaving multi-MHz-frequency power converter designers without a critical variable in determining semiconductor losses.

More tangibly, Ref. [10] uses an input power method to calculate dR_{on} in 600/650 V HEMTs, finding a $> 5\times$ increase of dR_{on} over R_{dc} at 3 MHz. For the same commercially-available devices, though, Refs. [11]–[14] use direct on-state voltage measurements to get increases over R_{dc} of 5%, 20%, 50%, and

70%, respectively, at 1 MHz. These discrepancies are partially a result of the prevalence of pulsed measurements (e.g. [7], [15], [16]), which may overestimate (if the blocking time is unrealistically long [17]) or underestimate (if traps accumulate over many switching cycles [18]) the true, *in-situ* effect of dR_{on} [9]. *Only* steady-state measurements accurately measure dR_{on}, especially when focused on the effect of frequency: as frequency increases, the blocking time and on-time both decrease, which have opposing effects on dR_{on} that are not captured by a pulsed test.

In this work, we start to fill this gap with the first continuous high-frequency dynamic on-resistance measurements, up to 5 MHz, on a commercially-available GaN-on-Si HEMT. In the HF range and beyond, zero-voltage-switched (ZVS) converters are preferred to mitigate frequency-dependent switching losses, and our dR_{on} measurements are therefore performed under ZVS conditions. The test method is validated on a Si MOSFET, which, as expected, shows no dynamic on-resistance compare Fig. 2(a) to Fig. 2(b). On the tested GaN-on-Si HEMT, the majority of the increase in dR_{on} occurs below 1 MHz, and, into the multi-MHz range, dR_{on}/R_{dc} asymptotes as the frequency is increased. A physical justification for this asymptote forms the foundation for extrapolating these findings to other GaN-on-Si HEMTs in MHz-frequency, ZVS power converters.

II. METHODOLOGY AND TEST SETUP

We measure dR_{on} on a commercially-available GaN HEMT (the device-under-test, or "DUT") with a breakdown voltage rating (BV_{ds}) of less than 200 V, with exact parameters hidden for anonymity. We use the on-state voltage measurement circuit (OVMC) from [11] (where the theoretical basis of this measurement circuit is given), with the 600 V SiC Schottky blocking diodes in [11] replaced with a 150 V Schottky (RB558VAM150 [19]) with less stored charge to speed the transient response to under 50 ns (see Fig. 1(b), with the key components listed in Table I). 12-bit resolution gives 0.4 mV per bit for a quantization error of less than 1%. Our measurements are taken in thermal steady-state after 3 minutes of continuous operation, substantially longer than the 100 s time constants of some underlying traps [6], [13], [18] to guarantee that the dynamic on-resistance has stabilized at the steady-state value that will be observed *in-situ*.

A range of circuit topologies could be employed to measure dR_{on} at multi-MHz frequencies, including the triangular current mode (TCM) technique employed in [11] or other resonant topologies [20], [21]. While these topologies are fully soft-switched, they suffer from high di/dt and a current zero-crossing during the on-time, complicating dR_{on} measurements [11]. At 5 MHz and 1 A_{pk} current in TCM, for example, di/dt = 20 A μs^{-1} and a single 1 nH of parasitic inductance in the current path will give an on-state voltage offset of 20 mV. Further, the on-time in this operating mode is only 100 ns, and with a transition time of 50 ns of our measurement circuit, an additional blanking time around the current zero-crossing would leave very little on-time for measurement

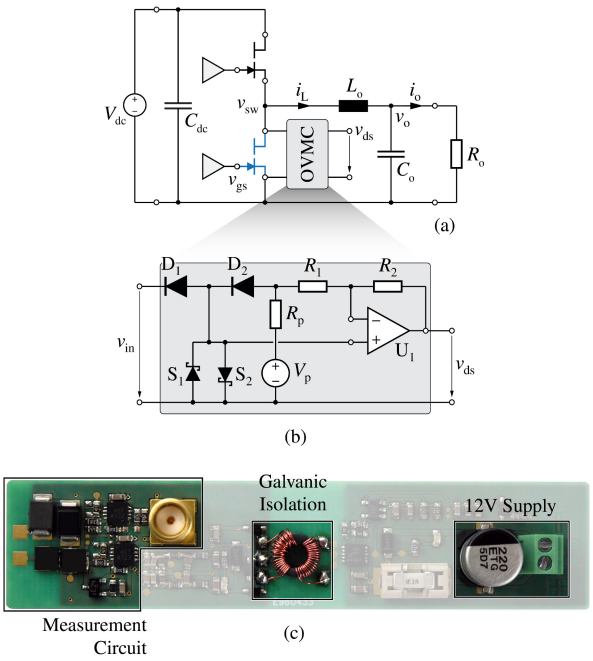

FIGURE 1. **(a) Buck converter test setup, with the low-side HEMT as the device-under-test (DUT) and highlighted in blue. This test configuration supports continuous operation and nearly-constant current for high-frequency dR_{on} measurements. (b) The on-state voltage measurement circuit (OVMC) from [11] is adapted for lower-blocking voltage and higher-frequency, with $D_{1,2}$ implemented with 150 V Schottky diodes and R_p decreased to speed the recovery from the blocking state. (c) Example OVMC implementation.**

TABLE I. **Key Components Utilized in the OVMC Circuit of Fig. 1**

Component	Value(s)
D_1, D_2	RB558VAM150
R_1, R_2	470 Ω
S_1, S_2	DFLS1200-7
V_p, R_p	10 V, 15 Ω
U_1	ADA4817

(and no meaningful "average current"). Instead, we select a simple buck topology Fig. 1(a), where the high-side switch is hard-switched but the DUT is under ZVS, as desired, and the current is nearly constant. This eliminates the concerns around di/dt, the zero-crossing, and average current determination, but the heating of the hard-switched high-side device does limit the achievable frequency range. This mode, further, only characterizes third-quadrant operation, but negative current is required for ZVS and is therefore the operating quadrant in the vicinity of turn-on for most multi-MHz converters.

Eight parameters must be controlled for valid dR_{on} trends [9], and these are given in Table II. The duty cycle of the low-side switch is set to 75 % to extend the available measurement time and reduce conduction losses in the high-side switch, which incurs hard-switching losses. Ideally, the device temperature would be fixed across all tests, but this is not easily achieved with a two order-of-magnitude sweep

TABLE II. Eight Controlled Parameters for Reported dR_{on} Measurements

	Parameter	Value(s)
V_{dc}	Blocking Voltage	0.33, 0.5, 0.67 BV_{ds}
f_{sw}	Switching Frequency	25 kHz to 5 MHz
d	Duty Cycle	75 %
$R_{g,ext}$	External Gate Resistance	0 Ω
v_{gs}	Gate Drive Voltage	+4.5 V, 0 V
T_j	Junction Temperature	32 °C < T_c < 75 °C
I_{sw}	Device Current	0.5 A, 1 A
	Switching Condition	Zero-Voltage

of switching frequency. Instead, we fix case temperature (T_c, which is within 4 °C of the junction temperature T_j at all test points, by $T_j - T_c = P_{diss}R_{\theta jc}$) for a subset of the measurements by varying fan speed, and report T_c for each test point.

Finally, we validate the measurements on a Si device (IRL100HS121 [22]), which, as expected, shows no dynamic on-resistance across the measurement range. These transient waveforms are shown in Fig. 2(a) and the full sweep results for this benchmark device are given in Fig. 3(a).

III. MULTI-MHz DYNAMIC ON-RESISTANCE MEASUREMENTS

Dynamic on-resistance is measured as the operating frequency is swept from 25 kHz to 5 MHz at two output currents, $I_{sw} = 0.5$ A and $I_{sw} = 1$ A. These steady-state dR_{on} values are reported for three input voltages in Fig. 3(a) and (b), with the Si benchmark measurements included in Fig. 3(a) to validate the technique and measurement circuit. We report the ratio of the dynamic on-resistance to the nominal DC resistance at the same T_c (directly measured for the particular DUT) as $dR_{on}(T_c)/R_{dc}(T_c)$.

For all voltages and currents, we observe that the dR_{on} does not materially increase between 2 MHz and 5 MHz for the DUT, with the majority of the dynamic penalty accruing below 1 MHz. For example, examining the $V_{dc} = 0.5\,BV_{ds}$ curve in Fig. 3(b), we measure $dR_{on}(T_c)/R_{dc}(T_c) = 1.17$ at 25 kHz, which increases to 1.73 at 1 MHz. At 5 MHz, though, the dynamic loss penalty only increases to 1.85, a small increase over the 1 MHz value. All of the measured curves obey this general trend.

Under ZVS conditions, we find that temperature has only a minor impact on dR_{on} [9], [23], as shown for select measurement points where only temperature is varied. For example, at $V_{dc} = 0.67\,BV_{ds}$ in Fig. 3(a), changes in T_c of 6 °C at 1 MHz and 10 °C at 2 MHz alter $dR_{on}(T_c)/R_{dc}(T_c)$ by less than 2%. With the small overall variation in T_c across our measurements, then, we can compare relative dR_{on} between curves (as in Fig. 4).

For the tested GaN-on-Si HEMT, in summary, the dynamic on-resistance under ZVS conditions is highly dependent on the blocking voltage and switched current, increases with frequency up to ≈ 2 MHz, and is asymptotic at higher MHz frequencies. In the next section, we survey the prior literature to find the physical origins of these trends to assess the extensibility to dynamic losses in other GaN-on-Si HEMTs.

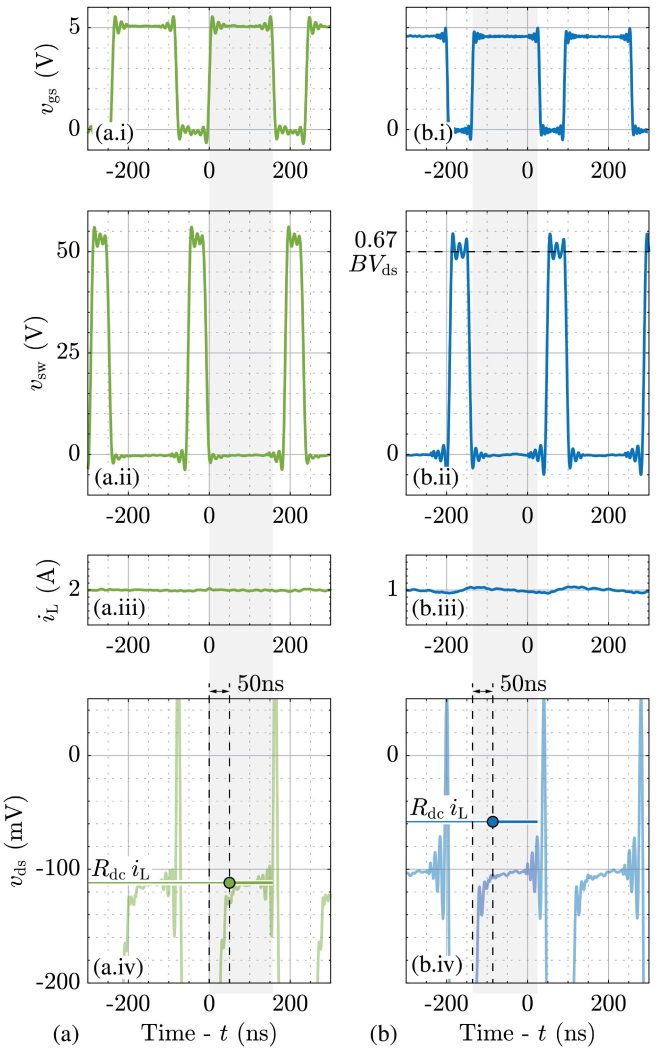

FIGURE 2. (a) Measured waveforms for the Si benchmark device at 4 MHz switching frequency and $V_{dc} = 0.5\,BV_{ds}$. Measured on-resistance matches $R_{dc}(T_c)$. (b) Measured waveforms for the BV_{ds} < 200 V GaN-on-Si HEMT under test at 4 MHz and $V_{dc} = 0.67\,BV_{ds}$. Measured on-resistance is 1.87 $R_{dc}(T_c)$. Labels referenced to Fig. 1. Both current scales are 200 mA/div. v_{sw}, v_{ds} scales not given for GaN HEMT for anonymity. The dynamic on-resistance measurement is valid within 50 ns of turn-on, and the reported on-resistance is the averaged on-resistance from 50 ns after turn-on to the turn-off time. In the tested buck converter of Fig. 1(a), the device current i_{ds} is equal to the measured inductor current i_L during the on-time (shaded for one cycle here).

IV. PHYSICAL ORIGINS

As highlighted in Section I, dR_{on} is attributed to the trapping of electrons at the surface, in the GaN channel, or in the buffer layers of the HEMT. To maintain net charge neutrality, the concentration of electrons in the 2-D electron gas (2DEG) is proportionally reduced, increasing the device on-resistance until the electrons are detrapped [3]. We review prior literature

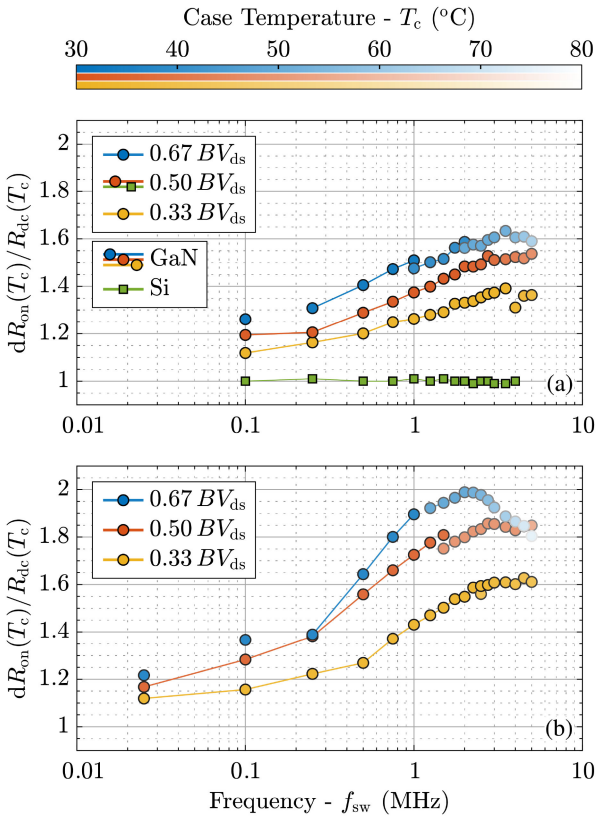

FIGURE 3. dR_{on} measurements from 25 kHz to 5 MHz, normalized by the DC resistance (R_{dc}) at the respective case temperature, $T_c \approx T_j$, $dR_{on}(T_c)/R_{dc}(T_c)$. Measurement parameters given in Table II. Solid lines join measurements at identical T_c. (a) GaN-on-Si HEMT measurements at $I_{sw} = 0.5$ A, with Si benchmark measurements at $I_{sw} = 2$ A to compare similar on-state voltages. (b) GaN-on-Si HEMT measurements at $I_{sw} = 1$ A.

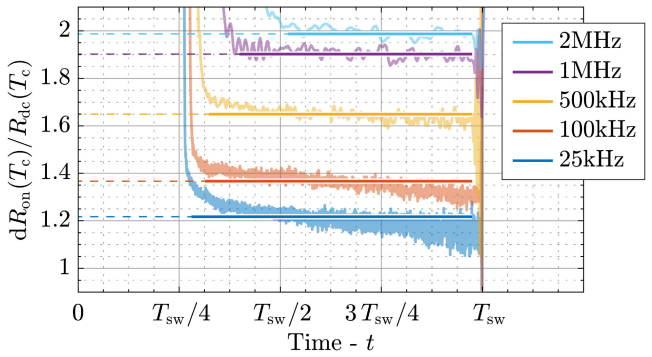

FIGURE 4. Measured transient waveforms and averaged $dR_{on}(T_c)/R_{dc}(T_c)$ at $V_{dc} = 0.67\,BV_{ds}$, $I_{sw} = 1$ A, $T_c = 38\,°C \pm 0.5\,°C$, except for the 2 MHz measurement, which is at $T_c = 50\,°C$, as the cooling system could not reach $T_c = 38\,°C$ with the higher switching losses at 2 MHz. Reduction of $dR_{on}(T_c)/R_{dc}(T_c)$ ratio during the on-time indicates detrapping of trapped electrons. Detrapping occurs during the on-time at 25 kHz and 100 kHz but does not occur at 1 MHz (on-time: 750 ns), indicating the detrapping time constant is on the order of 1 μs.

for the key trends found in Section III to highlight the physical origins of each.

- *Frequency asymptote:* dR_{on} increases up to 2 MHz for the tested HEMT, but does not materially increase at higher multi-MHz frequencies. Increasing the switching frequency shortens both the on-time, when detrapping occurs, and the off-time, when trapping occurs (note that the double-pulse test does not capture the shortening of the on-time with higher frequency). To understand this asymptotic behavior, we highlight the observed trapping dynamics of GaN-on-Si HEMTs in the literature and in the device tested here.
  Firstly, under ZVS conditions, there is a set of dominant trapping and detrapping time constants much slower than the switching frequency, on the order of 1 ms to 10 s [5], [6], [24]–[26]. Because these time constants are much slower than f_{sw}, the dR_{on} contribution associated with these traps will not change with switching frequency. These traps, however, do contribute to the baseline value of dR_{on} and underpin the importance of measuring dR_{on} only under steady-state conditions (after tens of seconds, and never with pulsed tests).
  Faster traps with time constants on the order of the switching frequency will trap and detrap during a switching cycle – until their time constants are also exceeded, and dR_{on} will, without any trapping and detrapping during a switching period, necessarily asymptote with frequency. In Fig. 4, we observe that the time constants in this particular HEMT are on the order of 1 μs, as measurable detrapping occurs during the on-time up to 500 kHz (on-time: 1.5 μs) but not at 1 MHz (on-time: 750 ns) and beyond. Detrapping time constants under ZVS conditions in a similar range (between 5 μs to 50 μs) were also measured in [9].
  In the characterized GaN-on-Si HEMTs, then, the fastest traps that measurably contribute to dR_{on} appear to have time constants on the order of μs. Once these μs time constants are exceeded, there is no further trapping or detrapping within a switching period, and we therefore can understand the observed lack of frequency dependence at multi-MHz frequencies.
- *Increase with blocking voltage:* dR_{on} increases monotonically with blocking voltage, V_{dc}, under all tested conditions. Charge storage in buffer traps is understood to be responsible for ZVS dR_{on}, with the buffer leakage current as the source of the charge [5], [24]. At higher voltages, the leakage current increases and traps more charge, increasing dR_{on}. Most literature finds an increase of dR_{on} with higher blocking voltage, although the relationship is more strongly monotonic under hard-switching (not considering unique device constructions that, for example, inject holes near the drain during hard-switching [14], [27]).
- *Increase with switched current:* dR_{on} increases between 0.5 A and 1 A switched current under all tested conditions. While other literature also finds an increase of dR_{on} with zero-voltage-switched, steady-state operation (e.g. [28], [29]), the current dependence is not deeply

explored, to our knowledge, in the physics literature for ZVS conditions. We identify two potential culprits.

Firstly, while hot electron trapping effects typically focus on the turn-on current-voltage overlap (when the device-under-test is gated on), this has been eliminated with zero-voltage switching. The turn-off transition (where the device-under-test is gated off, at the end of the shaded period in Fig. 2), however, is *not* a zero-current transition and therefore still includes an overlap of drain voltage and switch current, a much shorter overlap than at turn-on and one that is typically ignored in soft-switched converters. Increasing current is known, under hard-switching conditions, to increase hot electron trapping, and this could be occurring to a minor extent during this turn-off transition.

The second potential cause is the increase in dV/dt during the switching transition that occurs with higher current (at 1 A, the measured transition is $\approx 20\,\%$ faster than at 0.5 A). Higher dV/dt increases the displacement current through the parasitic capacitor between the drain and substrate, activating deep traps in the buffer layers [30], [31]. In GaN-on-Si HEMTs, these traps are one cause of soft-switching (or C_{oss}) losses [32], which are the losses that occur when the parasitic output capacitor is resonantly charged and discharged. These trap-based soft-switching losses are known to increase with dV/dt in GaN-on-Si HEMTs, and the same mechanism may also increase the buffer trapping that affects dR_{on}. We caution that these are hypotheses and the dependence of dR_{on} with current under soft-switching conditions needs to be further explored.

- *Minor temperature dependence:* Temperature has a very minor effect on dR_{on} in the tested HEMT. Under hard-switching conditions, higher temperature lowers dR_{on} because hot electron scattering is reduced at higher temperatures [23]. With ZVS transitions, which eliminate hot electron trapping (at least during turn-on), temperature has little impact on dR_{on} [9], [23]. While the time constants of the off-state traps change orders-of-magnitude with temperature, they remain much slower than the switching frequency and therefore do not substantially change dR_{on} here [5], [6].

V. CONCLUSION

We extend direct dynamic on-resistance measurements in GaN-on-Si HEMTs to the multi-MHz regime for the first time. Under zero-voltage-switching conditions, the dynamic on-resistance asymptotes around 2 MHz for the tested HEMT, an expected phenomenon when the switching frequency exceeds the relevant trapping and detrapping time constants. Although the exact frequency at which dR_{on} stops increasing will be device-specific, these findings indicate a substantial conduction loss penalty to increasing the switching frequency to ≈ 1 MHz but only a minor further penalty to scaling into the multi-MHz regime.

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