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***Abstract*—Solid-state transformers (SSTs) are considered for interfacing a medium-voltage (MV) ac grid to a low-voltage (LV) dc load in applications like high-power EV charging. This paper provides the first detailed analysis of a new modularized bridge rectifier (mBR) SST, which essentially consists of a three-phase diode rectifier with isolated dc-dc converters connected in parallel to the diodes, explains the operating principle, proposes a control method, and verifies the theoretical considerations with comprehensive circuit simulations. Finally, considering a 10 kV ac mains input, an 800 V dc output and a rated power of 1 MW, a comparative evaluation of the mBR SST against a state-of-the-art modular integrated-active-filter rectifier (mIAFR) SST indicates lower utilization of the mBR's dc-dc converters but practical advantages like the absence of direct series connections of transistors and the need for only a single type of power electronic building block (PEBB).**

***Index Terms*—Integrated active filter, modularized bridge rectifier, MVAC-LVDC, solid-state transformers.**

I. Introduction

Solid-state transformers (SSTs) have initially been proposed for traction applications and for future smart ac and dc grids. Whereas most SST topologies allow bidirectional power flow, prominent applications like high-power EV charging [4]–[7] (with fully rated industry prototypes demonstrated [8], [9]), datacenters [10], or electrolyzers [11] require only unidirectional power flow, i.e., high-power low-voltage (LV) dc loads must be supplied from the medium-voltage (MV) ac three-phase mains. Most SST topologies are phase-modular, i.e., each MV phase connects to an input-series, output-parallel (ISOP) arrangement of converter cells that consist of an ac-dc and an isolated dc-dc converter stage. Even when restricted to unidirectional power flow [12], each converter cell still processes single-phase power with an according fluctuation at twice the mains frequency.

Thus, a three-phase unfolder stage (comprising a three-phase diode rectifier bridge and phase selector switches (PSSs), see **Fig. 1a**), could be employed at the MVac input, which essentially improves the operating conditions for the cascaded converter cells arranged on the dc side, i.e., isolated dc-dc converters can be directly employed. **Fig. 1a** shows such a three-phase-unfolder-based MVac-LVdc SST topology, which has been proposed in [1] and later analyzed in [2]. As it is essentially an extension of the LV integrated-active-filter (IAF) rectifier [13] to MV input, the topology is referred to as *modular integrated-active-filter rectifier* (mIAFR) in the following and

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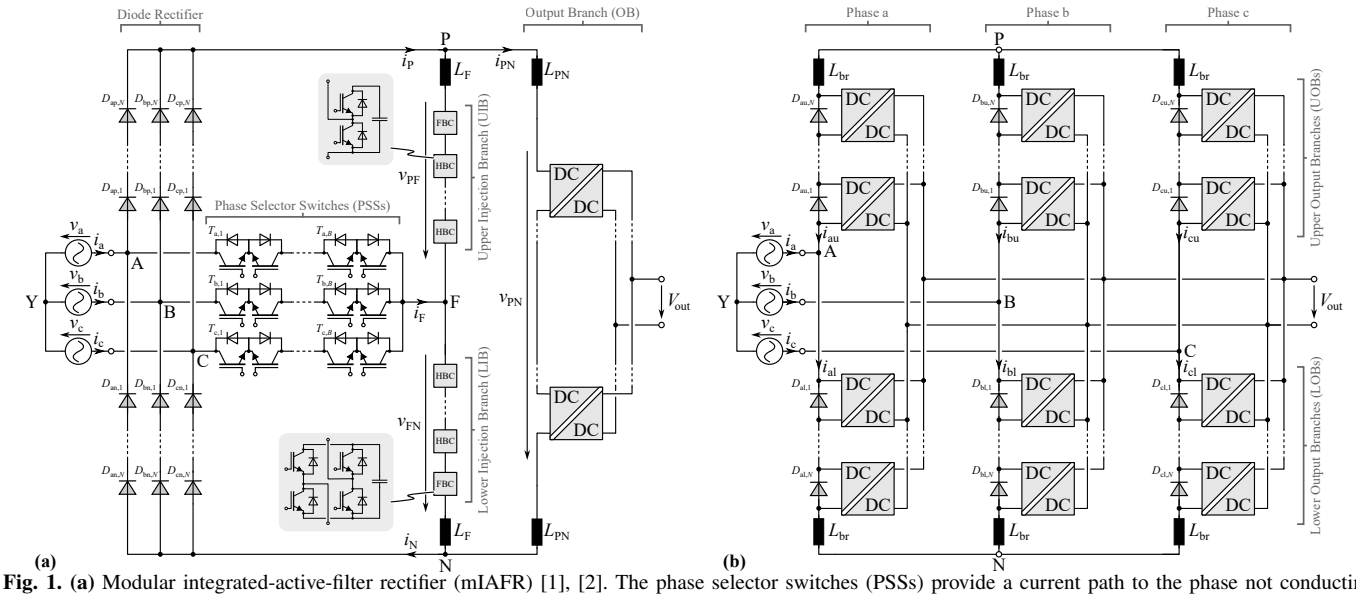


Fig. 1. (a) Modular integrated-active-filter rectifier (mIAFR) [1], [2]. The phase selector switches (PSSs) provide a current path to the phase not conducting current for conventional diode bridge operation, i.e., facilitate current injection and ultimately sinusoidal current consumption of all three phases. **(b)** Modularized bridge rectifier (mBR) topology proposed in [3], in which dc-dc converter modules parallel to blocking diodes transfer power to the system's output.

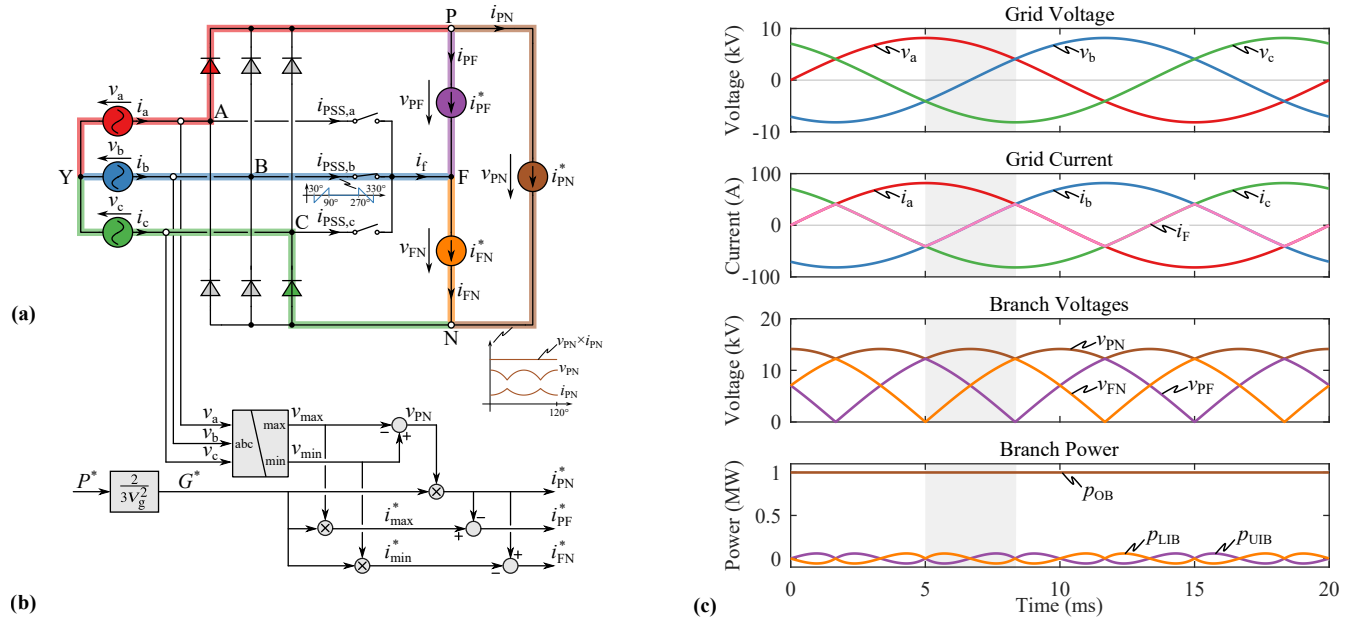


Fig. 2. Operating principle of the mIAFR from **Fig. 1a**. **(a)** Idealized equivalent circuit with current flows in an exemplary 60°-wide sector of the mains period; **(b)** block diagram for generating the branch current references; **(c)** simulated waveforms with the sector shown in (a) highlighted.

further discussed in **Section II** as a benchmark.

Alternatively, the isolated dc-dc converters could be directly integrated into the branches of a three-phase diode bridge rectifier: the voltages across blocking diode strings also can be utilized as unipolar supply voltages for cascaded converter modules. The resulting *modularized bridge rectifier* (mBR), which has been proposed by [3], is shown in **Fig. 1b**. The mBR essentially replaces the ac-dc stage found in converter cells of typical phase-modular SSTs by a single diode. In contrast to the mIAFR, a detailed analysis of the mBR's operating principle as well as control methods are missing in the literature. Therefore, **Section III** provides a detailed explanation of the mBR concept, discusses key design considerations and component stresses, and finally proposes a suitable control method. **Section IV** then provides a comparative evaluation of the mIAFR and the mBR, considering an exemplary 1 MW system interfacing the 10 kV (line-to-line rms) MVac grid to an 800 V LVdc output. **Section V** concludes the paper.

II. Modular Integrated-Active-Filter Rectifier

The mIAFR is a direct extension of the well-known IAF rectifier [13] to MVac input, as proposed in [1] and later analyzed in [2]. **Fig. 1a** shows the mIAFR power circuit, which is composed of a three-phase diode rectifier interfacing the MVac mains, phase-selector switches (PSSs), two injection branches (IBs), and the output branch (OB) that transfers the power to the LVdc load and provides galvanic isolation.

A. Operating Principle

The operating principle of the mIAFR is analyzed using the idealized equivalent circuit shown in **Fig. 2a**, where the IBs and the OB are substituted with equivalent current sources (CSs), and the PSSs are treated as ideal four-quadrant switches; **Fig. 2c** shows simulated key waveforms. In each 60°-wide sector of the grid period, the dc rails P and N are tied to the maximum (max) and minimum (min) grid voltage by two conducting rectifier diodes; the dc bus voltage v_{PN} thus shows the characteristic six-pulse shape corresponding to the maximum absolute value of the line-to-line voltages. The IBs inject a current into the mid phase (which otherwise would remain unloaded, resulting in discontinuous grid currents) through the corresponding PSS. Further, if the OBs transfer a constant power P to the load by shaping $i_{PN} = P/v_{PN}$, ohmic mains behavior with unity power factor results. The thus necessary current references i^*_{PN}, i^*_{PF}, and i^*_{FN} for the OB and the two IBs are calculated as in **Fig. 2b**, where P^* is the power reference from, e.g., an outer regulation loop for the dc output voltage V_{out}.

Table I
Exemplary specifications and design parameters used in the analysis.

Grid line-to-line rms voltage, V_{ll}	10 kV
Grid frequency, f_g	50 Hz
Load power, P_{load}	1 MW
DC output voltage, V_{out}	800 V
Semiconductor voltage rating	3300 V
Blocking voltage utilization	70%
OB dc-dc switching frequency	40 kHz
IB switching frequency	10 kHz
Voltage ripple on dc-dc capacitors (peak-to-peak)	5%
Current ripple on inductors (peak-to-peak)	1%
Peak flux density, B_{max}	120 mT
Winding current density, J_w	3.5 A/mm^2
Winding filling factor, k_{fill}	0.4

B. Design Aspects

In the following, key design considerations and resulting main component stresses are discussed based on the exemplary specifications and assumptions summarized in **Table I**.

1) Diode Rectifier: The diodes are stressed at maximum with the line-to-line grid voltage amplitude $V_{ll,pk} = 14.2$ kV; hence, a series connection of many individual devices is usually needed. Then, the current stresses are about 40 A rms and 23 A avg.

2) PSSs: The PSSs must provide bipolar voltage blocking and bidirectional current conduction capability, which can be implemented, e.g., using anti-series-connected transistors as in **Fig. 1a**. As the PSSs commutate at only twice the grid frequency, devices with optimized conduction characteristics and low cost like IGBTs are applicable. In nominal operation, the (maximum) blocking voltage stress is 12.2 kV and hence, again, typically a series connection of devices is needed, which implies a certain challenge regarding static and dynamic voltage sharing. The current stress of the PSSs is 14 A rms and 7 A avg.

3) OB: To handle MV on the input side and high currents on the LV side, the OB consists of an input-series, output-parallel (ISOP) arrangement of isolated dc-dc converters, which deliver a constant power to the output. The voltage rating of the OB is also defined by $V_{\mathrm{ll,pk}} = 14.2\,\mathrm{kV}$. Assuming realizations of the dc-dc converters with 3.3 kV SiC MOSFETs and a blocking voltage utilization of 70%, a minimum of $N_{\mathrm{OB}} = 7$ modules is needed. Thus, a dc-dc converter module power rating of 143 kW results. The input voltage on the MV side of each module fluctuates (six-pulse shape) in a relatively narrow range between 1750 V and 2020 V. On the MV side, the OB rms current is 74 A, and on the LV output side with $V_{\mathrm{out}} = 800\,\mathrm{V}$, each module contributes an output current of about 180 A.

The dc-dc converters could, for instance, be realized as dual-active-bridge (DAB) converters, whereby the relatively narrow range of the voltage transfer ratio facilitates full-range soft-switching operation with high efficiency. The input-side dc capacitors of the modules and the branch inductor L_{PN} form a low-pass filter, which should be designed such that the residual HF current ripple of i_{PN} is limited to low values; this limits the additional filtering effort at the mains terminals. Assuming a dc-dc converter switching frequency of $f_{\mathrm{sw}} = 40\,\mathrm{kHz}$ and, advantageously, interleaved operation of the N_{OB} converters, a module input capacitance of 2.7 µF is needed to limit the peak-to-peak voltage ripple to 5% and the total branch inductance of $2L_{\mathrm{PN}} = 2 \cdot 14\,\mu\mathrm{H}$ limits the HF current ripple to about 1% (peak-to-peak). The area product [14], $A_{\mathrm{c}}A_{\mathrm{w}} = I_{\mathrm{max}} I_{\mathrm{rms}} L/(k_{\mathrm{fill}} B_{\mathrm{max}} J_{\mathrm{w}})$, can be used as a proxy for the realization effort of the inductors, where A_{c} is the core cross section, A_{w} the winding window cross section, and $k_{\mathrm{fill}} B_{\mathrm{max}} J_{\mathrm{w}}$ (from **Table I**) is a technology-specific normalization factor that does not influence the comparison discussed later; $A_{\mathrm{c}}A_{\mathrm{w}} = 51\,\mathrm{cm}^4$ results for L_{pn}.[1] Similarly, the maximum stored energy $E_{\mathrm{C}} = 0.5\,CV_{\mathrm{C}}^2$ is a proxy for the MV-side capacitor volume; the total stored energy of all N_{OB} modules is 100 J.

4) IBs: In contrast to the OB, the IBs process only reactive power as can be seen in **Fig. 2c**, and can thus be implemented like a modular-multilevel-converter (MMC). In particular, each IB is composed of stacked half-bridge cells (HBCs) and at least one full-bridge cell (FBC) as shown in **Fig. 1a**; the latter is required to maintain controllability of the branch currents i_{PF} and i_{FN} even when the branch voltages v_{FN} and v_{PF} are close to v_{PN} [1], [2].

[1]Note that series connection of several converter modules also implies a certain stray inductance that can advantageously realize part of L_{pn}. As this is highly dependent on the actual physical realization, it is not considered further.

The voltage rating of each IB is identical to that of the OB, and therefore the same total module count is needed; specifically, each IB consists of 6 HBCs and 1 FBC, which process IB currents of up to $0.5 \cdot I_{\mathrm{g,pk}} \approx 41\,\mathrm{A}$, resulting in 15 A rms. Assuming again interleaved PWM operation with a lower switching frequency (not soft-switched) of 10 kHz, the branch inductances are $L_{\mathrm{F}} = 114\,\mu\mathrm{H}$, resulting in $A_{\mathrm{c}}A_{\mathrm{w}} = 41\,\mathrm{cm}^4$. **Fig. 2c** indicates that the IB modules process (low-frequency) LF power, which defines the module capacitances. Limiting the voltage ripple to 10% (peak) requires 30 µF per module, i.e., a substantial total stored energy of 1.1 kJ.

III. Modularized Bridge Rectifier

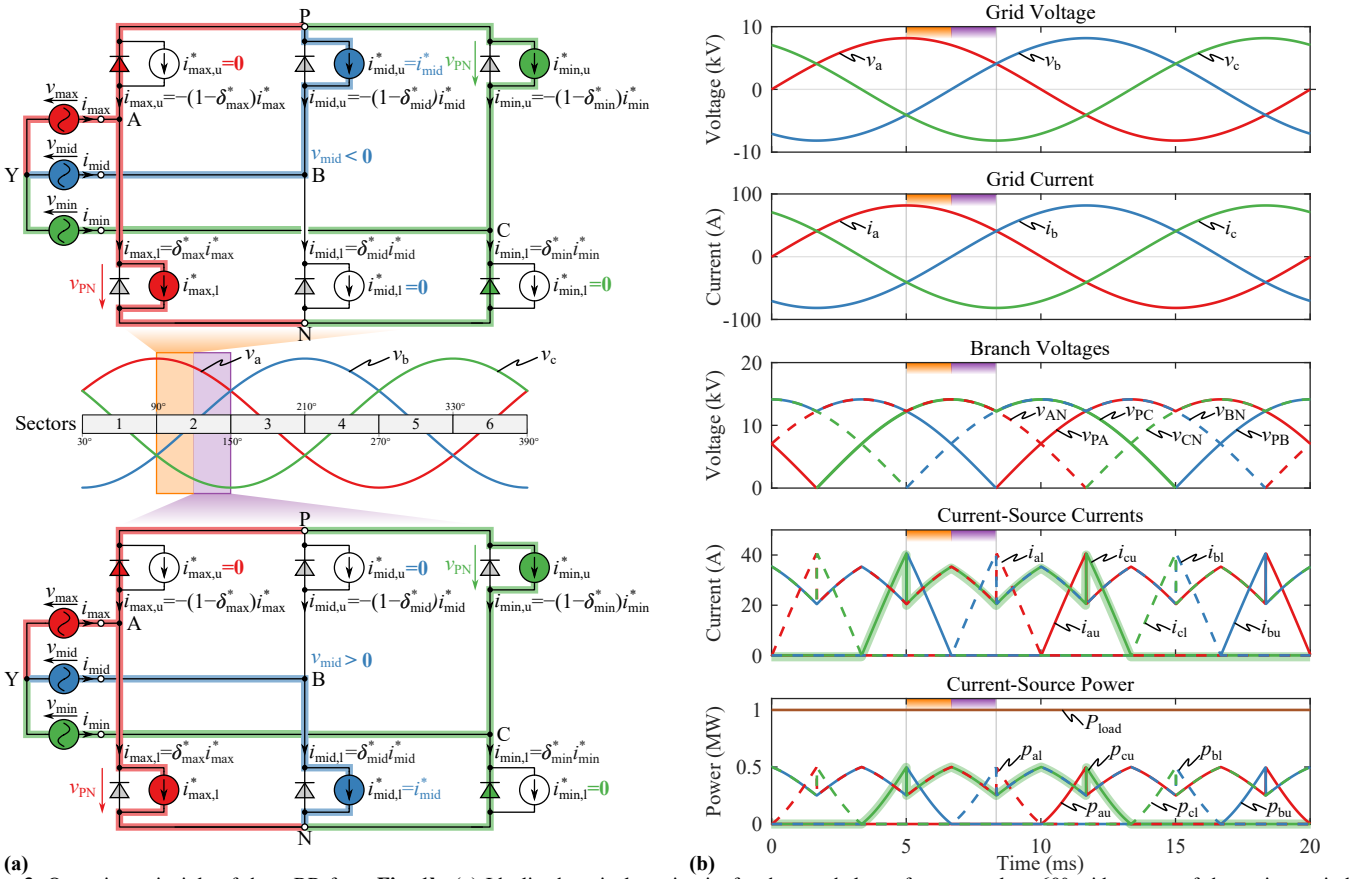
Fig. 1b shows the power circuit of the mBR [3]. Essentially, a three-phase diode rectifier is extended by isolated dc-dc converters that are connected in parallel to the rectifier diodes, thus forming an upper (u) and a lower (l) OB for each phase; advantageously, no PSSs or IBs are used. The upper and lower OBs are connected to the two ac-side star-points P and N, respectively. On the LV side, all dc-dc converters are connected in parallel (i.e., an ISOP arrangement is employed in each OB, like in the mIAFR); other configurations are possible [3] but not further discussed here.

A. Operating Principle

Again, the mBR's operating principle is best explained using the idealized equivalent circuit from **Fig. 3a**, where each OB is modeled as a diode in parallel with a controlled CS. As in any three-phase rectifier, the phase voltages define the conduction state of the rectifier diodes, i.e., the phase with the maximum (max) voltage v_{max} is connected to P whereas the phase with the minimum (min) voltage v_{min} is connected to N, and both diodes of the phase with the middle voltage v_{mid} are blocking; hence, $v_{\mathrm{PN}} = v_{\mathrm{max}} - v_{\mathrm{min}}$. Note that the roles of the phases a, b, and c with respect to v_{min}, v_{mid}, and v_{max} change in each of the six 60°-wide sectors of the mains period. Clearly, for a CS to absorb power (corresponding to power transfer through the dc-dc converter to the LVdc output), a positive voltage across the diode is required, i.e., only CSs in parallel to blocking diodes can participate in the power transfer to the output and in the shaping of the branch currents and thus ultimately of the mains currents.

For operation with unity power factor, grid currents i_{a}, i_{b}, and i_{c} that are proportional to the respective phase voltages and with amplitudes defined by the required output power are needed. It is convenient to discuss these currents also in terms of the max, mid, and min phases (defined by the phase voltages as discussed above), i.e., in terms of i_{max}, i_{mid}, and i_{min}. Each of the phase currents is split between the respective upper and lower branches, e.g., $i_{\mathrm{max}} = i_{\mathrm{max,l}} - i_{\mathrm{max,u}}$.

It is important to highlight that whenever a diode is blocking, the corresponding branch current is fully defined by the parallel CS according to a reference current (indicated with *, see **Fig. 3a**), e.g., $i_{\mathrm{max,u}} = i^*_{\mathrm{max,u}}$. If a diode conducts, the parallel CS (i.e., the dc-dc converters) should not operate as no power transfer is possible. Then, e.g., $i^*_{\mathrm{max,u}} = 0$ is used, which, however, does not imply $i_{\mathrm{max,u}} = 0$ due to the diode current.



(a) **(b)**

Fig. 3. Operating principle of the mBR from **Fig. 1b**. **(a)** Idealized equivalent circuits for the two halves of an exemplary 60°-wide sector of the mains period, and **(b)** simulated waveforms with the sector shown in (a) highlighted.

Thus, in a next step, the mapping of the desired phase current references i^*_{max}, i^*_{mid}, and i^*_{min} to the CS reference currents must be analyzed. To do so, δ^*_{max}, δ^*_{mid}, and δ^*_{min} are introduced to denote the share of the phase current that flows in the respective lower branch, e.g., for the max phase,

$$i^*_{\mathrm{max,l}} = \delta^*_{\mathrm{max}} i^*_{\mathrm{max}} \quad \text{and} \quad i^*_{\mathrm{max,u}} = -(1-\delta^*_{\mathrm{max}}) i^*_{\mathrm{max}}, \tag{1}$$

and similarly for the other phases as indicated in **Fig. 3a**. The δ parameters are linked by Kirchhoff's current law applied to the star points P and N as

$$\delta^*_{\mathrm{min}} i^*_{\mathrm{min}} + \delta^*_{\mathrm{mid}} i^*_{\mathrm{mid}} + \delta^*_{\mathrm{max}} i^*_{\mathrm{max}} = 0, \tag{2}$$

i.e., there are effectively only two degrees of freedom (DoF).

In the middle phase, both diodes are blocking and the voltages across the CSs in the upper and in the lower branch are positive and thus both could, in principle, draw power from the grid. However, this requires a positive branch current too, and hence the instantaneous direction of the middle phase current reference i^*_{mid} uniquely defines the current references of the upper and the lower branch CSs as

$$\begin{cases} i^*_{\mathrm{mid,u}} = i^*_{\mathrm{mid}} & \text{and} \quad i^*_{\mathrm{mid,l}} = 0 \quad \text{if} \quad i^*_{\mathrm{mid}} < 0, \\ i^*_{\mathrm{mid,u}} = 0 & \text{and} \quad i^*_{\mathrm{mid,l}} = i^*_{\mathrm{mid}} \quad \text{if} \quad i^*_{\mathrm{mid}} > 0. \end{cases} \tag{3}$$

As indicated in **Fig. 3a**, only one of the two CSs is active in each half of a sector. For unity power factor with $i^*_{\mathrm{mid}} \propto v_{\mathrm{mid}}$, we find $\delta^*_{\mathrm{mid}} = 0.5\,[1 + \mathrm{sgn}\,(v_{\mathrm{mid}})]$; substitution into (2) yields

$$\delta^*_{\mathrm{min}} i^*_{\mathrm{max}} + 0.5\,[1 + \mathrm{sgn}\,(v_{\mathrm{mid}})]\, i^*_{\mathrm{mid}} + \delta^*_{\mathrm{max}} i^*_{\mathrm{max}} = 0. \tag{4}$$

This clearly shows that one DoF remains (δ^*_{max} or δ^*_{min}) and can be used, e.g., to equalize the powers processed by the remaining two active CSs (one associated with the min and one with the max phase), i.e.,

$$\begin{aligned} p_{\mathrm{max}} &= p_{\mathrm{max,l}} = v_{\mathrm{PN}} i^*_{\mathrm{max}} \delta^*_{\mathrm{max}} \quad \text{and} \\ p_{\mathrm{min}} &= p_{\mathrm{min,u}} = -v_{\mathrm{PN}} i^*_{\mathrm{min}} (1 - \delta^*_{\mathrm{min}}), \end{aligned} \tag{5}$$

with $p_{\mathrm{max,u}} = p_{\mathrm{min,l}} = 0$ due to the conducting diodes (see **Fig. 3a**). In the mid phase,

$$p_{\mathrm{mid}} = p_{\mathrm{mid,u}} + p_{\mathrm{mid,l}} = \left[\delta^*_{\mathrm{min}} v_{\mathrm{PN}} + v_{\mathrm{mid}} - v_{\mathrm{max}}\right] i^*_{\mathrm{mid}} \tag{6}$$

does not depend on δ^*_{max} or δ^*_{min} as expected.

In case of unity power factor, the power balance $P_{\mathrm{load}} = p_{\mathrm{max}} + p_{\mathrm{mid}} + p_{\mathrm{min}} = \text{const.}$ can be satisfied with any pair of $\delta^*_{\mathrm{max}}, \delta^*_{\mathrm{min}} > 0$ for which (4) holds. Therefore, δ^*_{max} should be selected[2] such that the maximum power processed by the min and max CSs is minimized for any grid angle θ, which corresponds to requiring $p_{\mathrm{max}} = p_{\mathrm{min}}$, i.e.,

$$\delta^*_{\mathrm{max,opt}} = \underset{\delta^*_{\mathrm{max}}}{\mathrm{argmin}} \left(\max\{p_{\mathrm{max}}, p_{\mathrm{min}}\}\right) = \begin{cases} \frac{1}{2}, & v_{\mathrm{mid}} > 0 \\ -\frac{i^*_{\mathrm{min}}}{2 i^*_{\mathrm{max}}}, & v_{\mathrm{mid}} < 0 \end{cases}. \tag{7}$$

[2] An equivalent derivation could be made starting with δ^*_{min}.

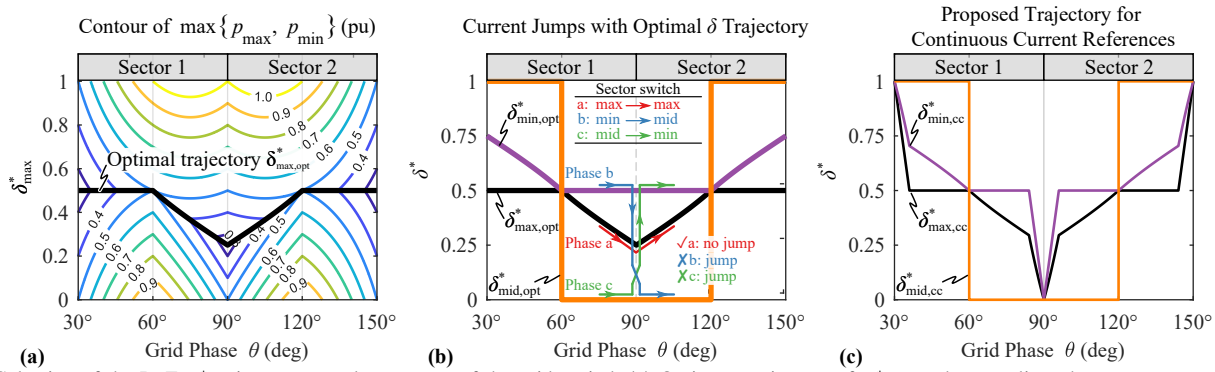


Fig. 4. Selection of the DoF $\delta^*_{\max}$ in two exemplary sectors of the grid period. **(a)** Optimum trajectory of $\delta^*_{\max,\mathrm{opt}}$ that equalizes the power processed by the min and max branch and hence results in minimum branch rms currents; the trajectory repeats in sectors 3/4 and then 5/6. **(b)** Shows the corresponding $\delta^*_{\min,\mathrm{opt}} = f(\delta^*_{\max,\mathrm{opt}})$ and $\delta^*_{\mathrm{mid,opt}}$ (which is not a DoF). The changing of the (a,b,c) to (min,mid,max) mapping at the sector boundaries causes discontinuities in the OB current references. **(c)** Modification of the optimum trajectory from (a) such that continuous OB current references result with $\delta^*_{\max,\mathrm{cc}}$ (see **Fig. 5**).

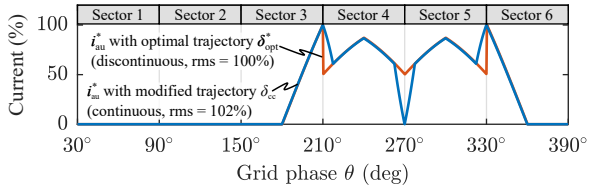


Fig. 5. Exemplary discontinuous OB current reference resulting with $\delta^*_{\max,\mathrm{opt}}$ from **Fig. 4a** and continuous variant with the modified trajectory $\delta^*_{\max,\mathrm{cc}}$ from **Fig. 4c**, which incurs a minor increase of the rms current by 2%.

Fig. 4a shows this optimal $\delta^*_{\max,\mathrm{opt}}$ as a function of θ; **Fig. 4b** also includes the corresponding $\delta^*_{\min,\mathrm{opt}}$ that follows with (4). With (1), the CS references follow as

$$i^*_{\max,\mathrm{l}} = i^*_{\min,\mathrm{u}} = \frac{1}{2}\min\left(i^*_{\max}, |i^*_{\min}|\right), \tag{8}$$

which are equal because the active CSs in the min and the max phase operate with the same voltage v_{PN} (see **Fig. 3a**). The resulting waveforms of current and power of the CSs are shown in **Fig. 3b**.

B. Design Aspects

As for the mIAFR in **Section II-B**, key design considerations for the mBR as well as the main component stresses are discussed, again with the specifications and assumptions from in **Table I**.

1) Diode Rectifier: The total diode blocking voltage stress is $V_{\mathrm{ll,pk}} = 14.2\,\mathrm{kV}$ as in the mIAFR, but a lower current stress of $I_{\mathrm{g,pk}}/(2\sqrt{3}) \approx 24\,\mathrm{A\,rms}$ ($I_{\mathrm{g,pk}}$ is the peak phase current) and 13 A avg results.

2) OBs: As for the mIAFR, each OB requires $N_{\mathrm{OB}} = 7$ stacked dc-dc converter modules, since the maximum applied voltage is again the peak line-to-line voltage $V_{\mathrm{ll,pk}} = 14.2\,\mathrm{kV}$; the rms voltage across an OB is $V_{\mathrm{ll,pk}}[1/3 + \sqrt{3}/(8\pi)]^{1/2} \approx 9\,\mathrm{kV}$. Whereas the OB voltage attains zero when the diode conducts, close inspection of **Fig. 3b** reveals that the dc-dc converters only process power when the OB voltage is higher than $0.5V_{\mathrm{ll,pk}}$. This results in a still comparably narrow input voltage range of the dc-dc converters of 1 kV to 2 kV. A peak current of $0.5\,I_{\mathrm{g,pk}}$ is drawn at an input voltage of 1750 V, resulting in a peak power rating of 72 kW for each module; the average power processed by each module is only 24 kW. Each module contributes a peak current of 90 A to the common LVdc output at 800 V. Finally, the dc-dc input rms current is $I_{\mathrm{g,pk}}\sqrt{1/8 \cdot (1 - 3/\pi)} \approx 19\,\mathrm{A\,rms}$. Similarly to the OBs of the mIAFR, considering DAB converters and interleaved operation, input capacitors of $C_{\mathrm{br}} = 2.7\,\mu\mathrm{F}$ and hence 39 J of stored energy per branch result (230 J in total). For a residual current ripple of about 1%, the branch inductances are $L_{\mathrm{br}} = 29\,\mu\mathrm{H}$ and carry the total branch current, i.e., the superposition of the diode and dc-dc input current; the area product is thus $A_{\mathrm{c}}A_{\mathrm{w}} = 43\,\mathrm{cm}^4$. Note further that L_{br} and the series connection of C_{br} form a resonance that is passively damped using an RL circuit in parallel to L_{br} according to [15]. Since the current components close to the resonance frequency are low, the volume and losses of the resulting dampers are negligible.

C. Proposed mBR Control Method

So far, **Section III-A** has described the operation of the mBR in terms of an idealized equivalent circuit with CSs representing the OBs. In reality, each OB consists of several dc-dc converters and passive elements (L_{br} and C_{br}) as outlined in **Section III-B**. This ultimately limits the achievable control bandwidth for the branch currents compared to ideal CSs, which is addressed by the control method proposed in the following.

1) Continuity of the Current References: Despite selecting $\delta^*_{\max}$ according to (7) results in optimum operation in the sense of minimizing peak power and rms current stresses, the resulting OB current references show discontinuities, see **Fig. 3b**. Therefore, a real implementation that is inherently bandwidth-limited cannot strictly follow these references, which would ultimately result in grid current distortions. The discontinuity in the OB current references is essentially caused by the fact that the mapping between (a,b,c) and (min, mid, max) changes at every sector boundary. As an example, **Fig. 4b** illustrates the change from sector 1 to sector 2, where phase b transitions from min to mid and phase c from mid to min. Since the two phase currents are equal at the sector boundary (unity power factor) but $\delta^*_{\min} \neq \delta^*_{\mathrm{mid}}$, the resulting OB current references are inevitably discontinuous.

Therefore, the $\delta^*_{\max,\mathrm{opt}}$ trajectory should be modified such that it remains as close as possible to the optimal one while still achieving continuous current references. Considering the

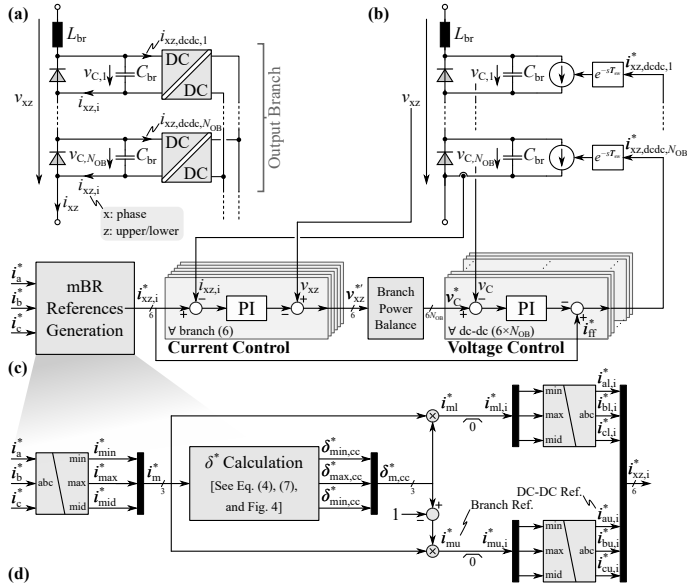


Fig. 6. Modeling and proposed control of the mBR. **(a)** Realization of a generic OB with isolated dc-dc converters that in **(b)** are modeled as CSs with an actuation delay of a switching period (e.g., typical for a DAB-type converter). **(c)** Block diagram of the proposed control method, including **(d)** the calculation of the OB current references.

instant of the change from an odd sector k to an even sector $k+1$, the continuity conditions are

$$\delta^*_{\mathrm{max},k} = \delta^*_{\mathrm{max},k+1}, \quad \delta^*_{\mathrm{mid},k} = \delta^*_{\mathrm{min},k+1}, \quad \delta^*_{\mathrm{min},k} = \delta^*_{\mathrm{mid},k+1}; \quad (9)$$

similar conditions exist for the change from an even sector. Then, (9) and (4) imply that all δ^* parameters must be equal at the instant of the sector change. The thus proposed modification of the ideal $\delta^*_{\mathrm{max,opt}}$ trajectory such that the resulting $\delta^*_{\mathrm{max,cc}}$ yields continuous OB current references is obtained with the following algorithm:

- If $v_{\mathrm{mid}} > 0$, then, starting at a predetermined fraction of the semisector (e.g., 25% or 7.5°), modify $\delta^*_{\mathrm{max,cc}} = \delta^*_{\mathrm{max,opt}} = 1/2$ to linearly reach 1 at the sector change; $\delta^*_{\mathrm{min,cc}}$ follows from (4);
- if $v_{\mathrm{mid}} > 0$, then, starting at a predetermined fraction of the semisector, modify $\delta^*_{\mathrm{min,cc}} = \delta^*_{\mathrm{min,opt}} = 1/2$ to linearly reach 0 at the sector change; $\delta^*_{\mathrm{max,cc}}$ follows from (4).

Fig. 4c shows the resulting $\delta^*_{\mathrm{max,cc}}$ and $\delta^*_{\mathrm{min,cc}}$ trajectories, and **Fig. 5** shows, as an example, the resulting continuous current references of the upper OB of phase a. The penalty in terms of rms current increase is only a few percent.

2) Modeling: **Fig. 6a** shows the hardware realization of a generic OB xz of phase x (z is u for upper, or l for lower), where the input capacitors of the dc-dc converters are explicitly shown. The voltages across these input capacitors can be controlled via the power flow through the dc-dc converters, and the sum of all capacitor voltages ultimately is used to regulate the current in the branch inductor L_{br}, i.e., the branch current, to the reference values derived above. Note that when the dc-dc converters are active (the diode is blocking), the branch current i_{xz} corresponds to the internal branch current $i_{\mathrm{xz,i}}$, i.e., the current provided by the dc-dc converters. Considering, e.g., DAB-type dc-dc converters, the power stage can be modeled in a first step as a controlled current source with a time delay of a switching period $T_{\mathrm{sw}} = f_{\mathrm{sw}}^{-1}$ as in **Fig. 6b**.

3) Control Scheme: Using this modeling approach, **Fig. 6c** shows the proposed control scheme. First, the phase current references (obtained from a higher-level regulator, e.g., of the mBR output voltage) i^*_{a}, i^*_{b}, and i^*_{c}, are mapped to the max/mid/min domain and the six continuous (using the trajectory $\delta^*_{\mathrm{max,cc}}$) OB current references $i^*_{\mathrm{xz,i}}$ are generated as shown in **Fig. 6d**. Then, a PI controller acts on the deviation of the measured OB currents from these references to calculate the required voltage across L_{br}. Further, a feed-forward of the measured branch voltage v_{xz} is used to generate the voltage references $v^{*'}_{\mathrm{xz}}$ to be tracked by the OB's dc-dc converters. In an ideal system, it would be sufficient to divide $v^{*'}_{\mathrm{xz}}$ equally among the dc-dc converters to obtain the references v^*_{C} for N_{OB} modules of the branch (i.e., $v^*_{\mathrm{C}} = v^{*'}_{\mathrm{xz}}/N$) but, in practice, a balancing system should be implemented to ensure equal power sharing among the dc-dc converters also for parameter deviations (e.g., among the C_{br}). Finally, inner control loops regulate the input capacitor voltages of the dc-dc converters by commanding the dc-dc converter input current references $i^*_{\mathrm{xz,dcdc}}$ (or, equivalently, the power transfer). Again, a feed-forward of the required OB current reference is used to improve the control dynamics. Finally, note that the dc-dc converters only process power once the voltage v_{xz} exceeds $0.5V_{\mathrm{ll,pk}}$; thus, the control of the dc-dc converters should only be activated once the diode blocks and v_{xz} approaches $0.5\,V_{\mathrm{ll,pk}}$.

4) Closed-Loop Simulation Results: Using the modeling approach from **Fig. 6b** with $N_{\mathrm{OB}} = 7$ and a digital implementation (40 kHz execution frequency) of the control scheme from **Fig. 6cd** yields the steady-state and transient (power reference step from 30% to 100%) simulation results shown in **Fig. 7** with a phase current THD of less than 1%.

D. Circuit Variants

Fig. 8a shows the OB configuration studied so far, where the blocking voltage of each diode is defined by the associated dc-dc converter's input voltage[3]; on the other hand, the branch inductor conducts both, the diode current and the dc-dc converter input current. Alternatively, the branch inductor could be distributed to the modules as shown in **Fig. 8b**, reducing its rms current stress. However, the (transient) blocking voltage sharing of the series-connected diodes is then not directly enforced by the dc-dc converters anymore. In any case, note again that the branch inductance can, at least partly, be provided with the inevitable stray inductances resulting from the physical assembly of the OB from several converter modules.

Further, the external diode could be omitted and the dc-dc converter input stage (e.g., as in **Fig. 9a**) be utilized as an (active) rectifier. This would reduce the component count but increase conduction losses of the dc-dc converter's input-stage devices.

Finally, whereas the basic mBR topology from [3] (see **Fig. 1b**) could provide reactive power operation (±30° phase

[3]This allows further to define the conduction state of the diodes through the dc-dc converter input voltage, which might be useful for certain advanced operating modes not considered here.

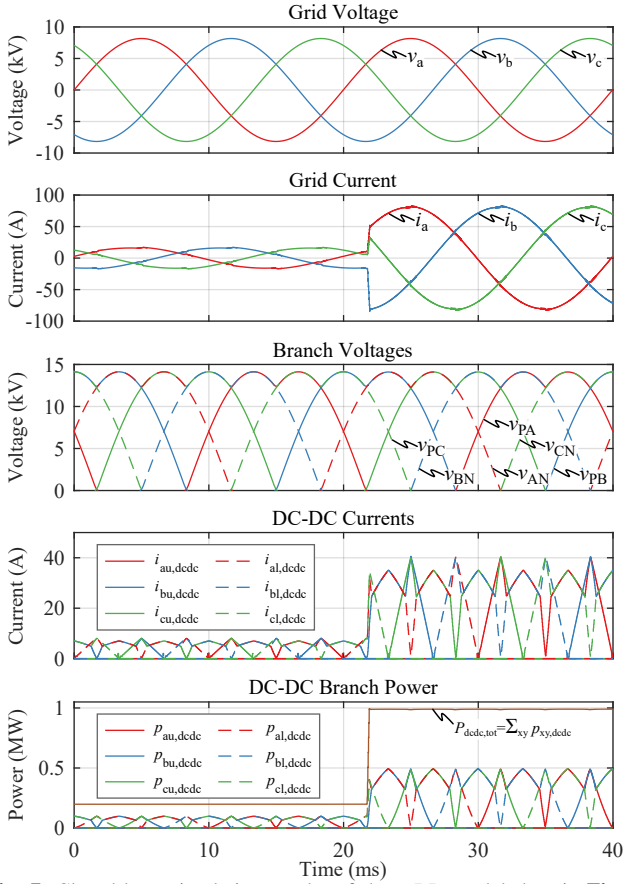


Fig. 7. Closed-loop simulation results of the mBR modeled as in **Fig. 3b** with $N_{OB} = 7$ an digital implementation (40 kHz execution frequency) of the controller from **Fig. 3cd**. After 22 ms, the power reference is increased from 30% to 100% of the nominal value.

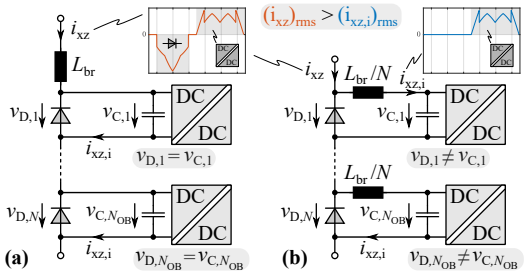


Fig. 8. Placement options of the mBR's branch inductor, i.e., **(a)** external (diode blocking voltage sharing ensured by the dc-dc converters, but higher rms current stress) or **(b)** internal (lower rms current stress but diode blocking voltage sharing not ensured by the dc-dc converters).

shift between mains voltage and current), which is not discussed further for the sake of brevity, the diode front-end prevents reverse power flow from the LVdc to the MVac side. Hence, **Fig. 9** shows how to extend the mBR for inverter operation: IGBTs, thyristors, GTOs could be arranged anti-parallel to the diodes as depicted in **Fig. 9b**, or, alternatively, the input stage of the dc-dc converter could be utilized (see **Fig. 9a**).

IV. Comparative Evaluation

The exemplary designs and component stresses discussed in **Section II-B** for the mIAFR and in **Section III-B** for the mBR facilitate a comparative evaluation of the realization efforts and a first performance estimate.

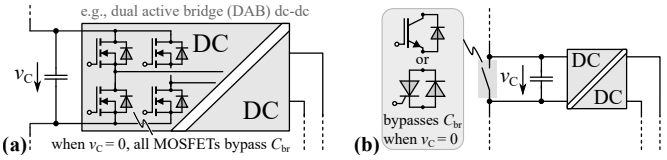


Fig. 9. Extension of the mBR concept to bidirectional power flow by **(a)** utilization of the dc-dc converter's input-stage transistors or **(b)** replacing the diodes with switches.

Fig. 10 compares the mIAFR and the mBR in terms of several high-level performance indicators. First, the realization effort of the main building blocks is characterized by the respective total VA ratings, i.e., the sum of the products of the respective maximum/rated voltage and maximum rms current of the constituent subunits, which is then normalized to the rated power of $P_{load} = 1$ MW: $S_{diodes,tot}$ relates to the rectifier diodes, $S_{PSS,tot}$ to the PSSs (mIAFR only) $S_{OB,tot}$ to the dc-dc converters of the OBs, and $S_{IB,tot}$ to the IB modules[4] (mIAFR only). Whereas the total VA rating of the mBR's OBs (i.e., dc-dc converters) is 60% higher than that of the mIAFR, there are no IBs, a 60% lower total VA rating of the rectifier diodes, and no PSSs, and hence no issues with voltage sharing among series connected transistors. Further, the floating capacitors of the mIAFR's IBs result in a roughly 5 times higher stored energy compared to the mBR. On the other hand, the sum of all inductor area products is higher for the mBR; yet, depending on geometry and, hence, the parasitic inductances of the physical branch realizations, no or much smaller dedicated branch inductors might be needed. Clearly, as each OB of the mBR has the same voltage rating as the single OB of the mIAFR, the mBR requires many more dc-dc converters and hence more medium-frequency transformers providing the high clearance and creepage distances needed when interfacing the MVac mains. This is a clear drawback, and points to the relatively low utilization of the dc-dc converters in the mBR (peak-to-average power ratio of 3 compared to 1 for the mIAFR, approximately), which is also reflected in the larger number of HF-operated transistors, and the higher numbers of sensors and communication links. On the other hand, the mIAFR requires 5 different types of power electronic building blocks (PEBBs), i.e., diode rectifier, PSSs, IB HBC, IB FBC, and OB dc-dc converters, whereas the mBR only requires a single type of PEBB (consisting of a diode and the dc-dc converter), which is beneficial due to economies of scale.

Finally, first-order estimates of the conversion efficiencies (at the rated output power of 1 MW) of the exemplary mIAFR and mBR designs are obtained using exemplary component datasheets and generic assumptions. Regarding the mIAFR, the rectifier is realized with 3.3 kV IXYS UGE0421AY4 diodes (2 in parallel), resulting in total losses of about 2.1 kW assuming a heat sink temperature of 100 °C. Similarly, the PSSs employ 3.6 kV IXYS IXBF20N360 IGBTs and contribute 700 W of losses. The IBs, in contrast, use 3.3 kV, 50 mΩ GeneSiC G2R50MT33K SiC MOSFETs, generating a total of 340 W of losses. Finally, the efficiency of the OB dc-dc converters that operate with a relatively narrow range of the voltage transfer

[4]The FBC is counted as two HBCs for simplicity.

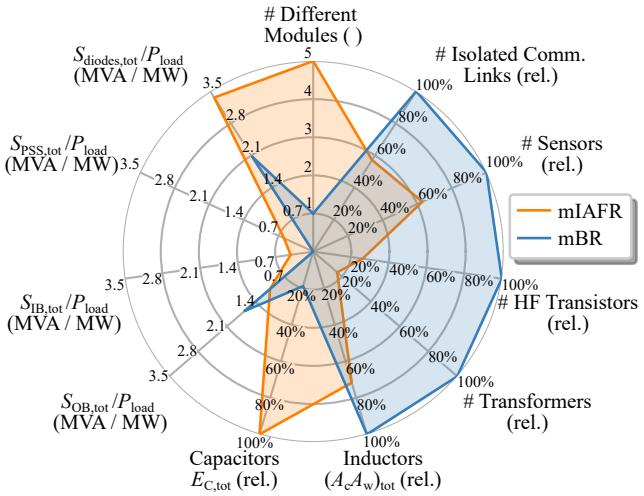


Fig. 10. Comparative evaluation of the mIAFR and the mBR regarding the realization effort; details are reported in the text.

ratio and with almost constant power, is assumed as 99% based on values reported in the literature, e.g., [16], [17], which implies 10 kW of losses. Thus, we estimate total mIAFR losses of 13 kW and hence an efficiency of 98.7%.

Similarly, the mBR's rectifier is realized with the same diodes (no paralleling), resulting in 1.3 kW of losses. The dc-dc converters in the mBR's OBs operate with a wider voltage transfer ratio and with a much wider power fluctuation than the mIAFR's; both are expected to result in lower (weighted) efficiency of the dc-dc converters. To achieve the same system-level efficiency as the mIAFR, the (weighted) dc-dc converter efficiency under the operating profile of the mBR would need to be at least 98.8%, which seems relatively high. Alternatively assuming that the mBR operating profile results in a 50% increase of the dc-dc converter losses compared to the more favorable conditions in the mIAFR, i.e., assuming a dc-dc converter efficiency of 98.5%, the overall mBR efficiency is still 98.4%. Despite the first-order approximations, these preliminary estimates still indicate that both topologies have the potential for achieving very high MVac-LVdc conversion efficiencies.

V. Conclusion

MVac-LVdc solid-state transformers (SSTs) with sinusoidal input currents can be realized by extending a B6 diode rectifier with additional circuitry, in particular with isolated dc-dc converters. This paper discusses two recently published examples, i.e., the modular integrated active filter rectifier (mIAFR) [1], [2] and the modularized bridge rectifier (mBR) [3]. Whereas the mIAFR has already been analyzed in the literature, this paper provides the first thorough analysis of the mBR. It further proposes a suitable control method that ensures minimum current stresses and achieves continuous branch current references to avoid grid current distortions, which is verified by detailed circuit simulations.

Considering an exemplary 1 MW system supplying an 800 V LVdc output from the 10 kV MVac mains, a quantitative and qualitative comparative evaluation of the mIAFR and the mBR indicates a lower utilization of the mBR's dc-dc converters and hence an overall higher realization effort. On the other hand, better modularity (only one type of PEBB) and the absence of direct series connections of transistors, in particular also for realization variants with bidirectional power flow capability, are interesting advantages of the mBR. Future work should extend the quantitative comparative evaluation and further include the concepts from [18], i.e., a three-phase unfolder front-end with PSSs but just two OBs, and from [19], which employs only three rectifier diodes connected to a common star point and with dc-dc converters in parallel; both require fewer dc-dc converters and hence better utilization is expected, but on the other hand the dc-dc converters must operate with a wide input voltage range down to zero input voltage.

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