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Swiss Competence Center on Energy Research FURIES - Overview and Contributions in the Area of Power Electronics and SmartGrids

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Keywords

HVDC, Multiterminal HVDC, Faults, Converter circuit, Renewable energy systems

Abstract

This paper introduces a special session on results of the Swiss competence center on energy research FURIES that has been established in coordination with the Swiss Energy strategy 2050 with the specific aim to develop, promote and deploy power grid-related innovative solutions toward the implementation of the Swiss Energy Strategy 2050. This contribution will report on activities within WP 3, "AC/DC multi-terminal grids and power electronics". This WP includes three subtasks with contributions from the major Swiss technical universities: Multi-terminal HVDC system design, fault detection and clearing in multi-terminal HVDC, enabling component and converter technologies and applications. The spectrum of the center's activities is briefly introduced and as an illustrative example, the contributions of the SCCER FURIES in relation with HVDC grids are summarized. These contributions include: new high power DC testing methods and laboratories, new DC breaker principles and fault location techniques, AC/DC grid resonance analysis and novel converter technologies.

Introduction

The Swiss federal government has implemented an energy strategy aiming at replacing the currently nuclear-based electricity generation share of approximately 40% with renewable energy by 2030. As a support to the extension of R&D capacities, several academic consortia are currently part-financed by Innosuisse. One of these is concerned with grids and grid components under the title "Future Swiss Electrical Infrastructure" (FURIES). The center is organized in four work packages: WP1 Regional multi-energy grids, WP2 Bulk multi-energy grids, WP3 Multi-terminal AC-DC grids and power electronics and WP4 Grid components. The activities in work package 3 are organized into three subtasks which are (1) multi-terminal HVDC system design, testing and operation, (2) fault detection and clearing in multi-terminal HVDC and (3) enabling component and converter technologies and applications.

This paper will illustrate the contributions of the SCCER FURIES WP3 to DC transmission and distribution. These technologies are of interest to the evolution of the Swiss power system: in transmission, there is an increasing interest in controllable load flows as well as underground solutions while in distribution, DC could provide a better integration of decentralized supplies, increase the capacity of existing infrastructure, reduce lines' visual impact and footprint and supply remote loads. VSC-HVDC

could be interesting for the additional features it can add the AC grid, also in light of Switzerland's role as a transit corridor within the interconnected European System. Finally, DC options might also be in a good synergy with improved hydro storage plants (e.g. variable speed pumped-storage), which will increase the dynamic requirements on the existing power system.

Development of converter technologies for DC applications

MMC-based MVDC converter technologies development within the SCCER FURIES

Modular Multilevel Converters (MMC) have emerged as highly efficient and flexible power electronics structures, allowing for easy voltage scalability meeting the applications needs. The basic topology of an MMC for AC-DC or DC-AC conversion consists of six branches where each is realized as series connection of multiple series connected sub-modules. The emergence of MVDC power distribution networks will require means to interface them with LVAC grids. Connection of DC terminals of the MMC to the MVDC network leads to MVAC output voltage at the AC terminals. The most obvious solution, is to connect line frequency transformer between the AC terminals of the MMC and the AC grid, and adjust voltage levels on the AC side. Instead, a different approach has been followed, considering that MMC already requires branch inductances and exploring possibility to realize them as part of transformer structure. In other words, integration of line frequency transformer into MMC is considered as viable approach to reduce number of components in the system.

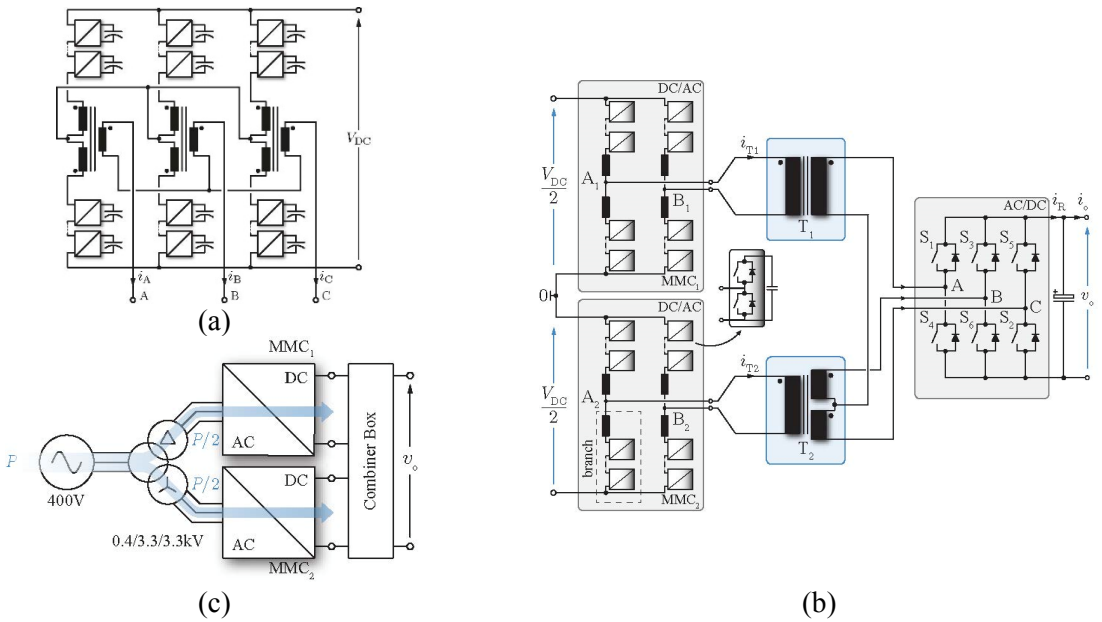


Fig. 1: (a) GIMC, featuring integrated magnetic structure into the MMC structure. (b) High-power DC-DC converter utilizing Scott transformer connection. (c) MMC-based MVDC amplifier.

This is illustrated in Fig. 1 (a), where a Galvanically Isolated Modular Converter (GIMC) is shown. It features three-phase transformers with three windings per phase, designed in such way to cancel flux contributions from DC currents present in each branch of the MMC [1]. Such a transformer structure essentially provides the function of branch inductances as well as galvanic isolation and voltage adaptation for the AC grid. Despite these hardware modifications positively impacting the size of the overall system, control principles of the MMC are preserved and without significant modifications, all the known control algorithms can be deployed, as discussed in [2]. Both half-bridge and full-bridge submodules can be used for the implementation. To address the needs to interface two MVDC grids of different voltage level, while providing galvanic isolation and ability to operate in case of partial loss of supply, the converter as shown in Fig. 1 (b) is proposed. It features Scott Transformer Connection (STC), for the first time operated at medium frequency and used for the DC-DC conversion. The STC, achieved by appropriate connection of two single-phase transformers, allows for creation of balanced three-phase voltage from set of in-quadrature single-phase, or vice versa. For those reasons, two MMC-based single-phase converters are connected to the STC on the high voltage side, while simple

six-step operated inverter is connected on the three-phase side, providing lower output voltage. Principles and details of the operation are discussed in detail in [3]. Important characteristic of the topology from Fig. 1 (b), is the ability to provide fault tolerant operation in case of loss of one pole in the MVDC grid (in case of bipolar network). Ability to perform in this operating mode has some implications to the converter sizing, as discussed in [3], but this is beyond the scope of this paper.

While increased interest into MVDC power distribution network requires developments of various conversion solutions, it also raises various questions related to stability of these systems and interactions between converters [4]. To be able to address these questions, high power high-performance equipment is needed providing great flexibility in testing of MVDC technologies. Fig. 1 (c) illustrates MMC-based MVDC amplifier, able to provide fast dynamic output voltage control on the DC side [5]. It is based on two MMC converters connected to separate windings of a 12-pulse transformer (3.3kVac) and providing ±5kVdc at output of each MMC. To achieve both polarities of output DC voltage full-bridge sub-modules are used for the implementation. DC outputs of two MMCs can be connected either in parallel (to double the current ratings) or in series to, effectively making it possible to achieve ±10kVdc at the output. Such MVDC amplifiers can be used either to emulate an MVDC grid, to supply other converters or serve the purpose of system identification by allowing injection of various test signals into the loads connected on the DC side.

SiC Super-Switch Intelligent Power Module

Context for the development of the intelligent power module

The realization of MV/LV DC–DC converters is commonly based on Dual Active Bridge (DAB) type converter topologies with or without MF resonant tank, featuring high achievable efficiency and power density, low component count, and bidirectional energy transfer capability.

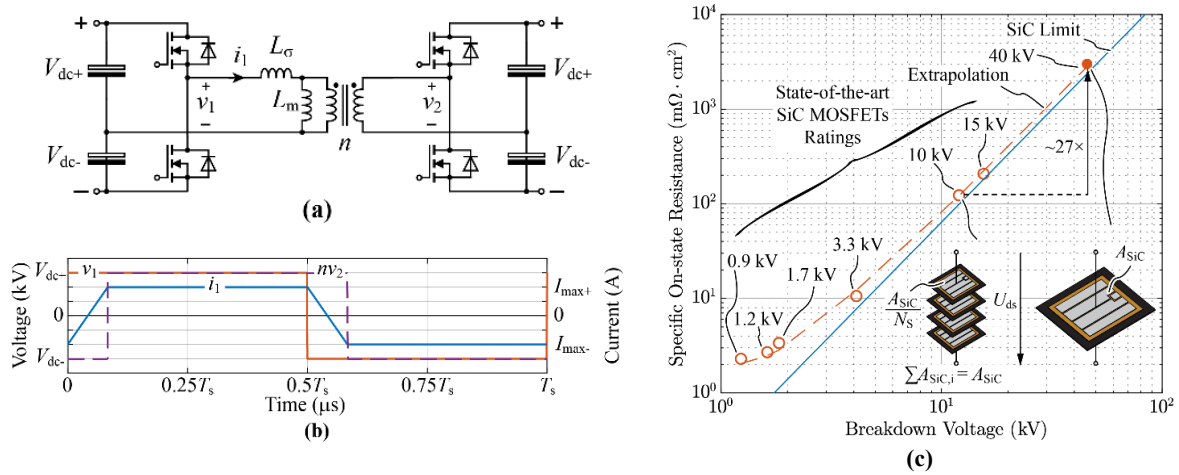


Fig 2: (a) DAB-type DC–DC converter employing a MV SiC half-bridge at the input side. (b) Simulated transformer primary and secondary side quantities (magnetizing current neglected). (c) Specific on-state resistance of SiC MOSFETs and SiC theoretical limit based on [7]. Bottom-right: starting point for the comparison of the specific on-state resistances of a considered 40 kV SiC MOSFET and four 10 kV SiC MOSFETs (N_S = 4, U_{ds} = 40 kV).

For higher power MV applications like EV charging, fast semiconductor switches with a voltage of 40 kV are required [6]. This exceeds the capabilities of current 10 kV and 15 kV SiC devices. Accordingly, converter topologies, multi-cell converter structures, or combinations thereof, are used to distribute the voltage to multiple semiconductors. Furthermore, a more effective utilization of the SiC chip area is achieved, if multiple MOSFETs are used instead of a single MOSFET since the minimum achievable specific on-state resistance, $R_{DS(on),spec,min}$, is increasing more than quadratically with the breakdown voltage. Fig. 2 (c) depicts the relation between minimum specific on-state resistance and breakdown voltage (based on [7]), a selection of reported values for $R_{DS(on),spec}$ for different SiC MOSFETs, and the expected minimum value of $R_{DS(on),spec,40kV}$ = 2.67 Ωcm² for a possible 40 kV SiC MOSFET (breakdown voltage of 48 kV considering a 20% margin). A direct comparison of the effective specific on-state resistances of the 48 kV MOSFET and four SiC MOSFETs with a breakdown

voltage of 12 kV (rated voltage of 10 kV) leads to approximately $4x4xR_{DS(on),spec,12kV} = 1.58\ \Omega cm^2$, lowering the conduction losses by 40% compared to a single 40 kV device (Multiplication by 4x4 for considering the series connection and the same chip area for both solutions). Series connected SiC MOSFETs however require circuitry to control the transient and steady-state voltage distribution [8]. A direct series connection of SiC JFETs (Supercascode) is reported in [9]-[10] for the realization of 5 kV and 40 kV power switches. This approach features a simple gate driver, however, the operation with balanced blocking voltages requires a passive network that is adapted to the parasitic capacitances of the SiC JFETs to ensure its proper operation [10]. Taking into account the limited number of JFET suppliers, solutions with MOSFETs featuring normally-off properties are thus preferred.

Alternatively, a cascode of converter cells, i.e., a multi-cell converter approach, as presented in the previous section and [11], could be employed, however requiring the use of a high number (and volume) of capacitors. Recent research therefore aims for circuit and control concepts that utilize multi-cell structures only to achieve a defined blocking voltage partitioning, by means of Quasi 2-Level (Q2L) operation, which minimizes capacitive energy storage requirements. In this context, [12] investigates the use of a Q2L-MMC as part of a DAB converter and considers staggered switching to achieve reduced average voltage slew rates. The work presented in this paper pursues Q2L operation for a multilevel Flying Capacitor Converter (FCC), which, compared to the Q2L-MMC requires only half of the power MOSFETs to achieve same voltage and current ratings. In addition, it features a lower total capacitor volume than the MMC, and enables the realization of a compact and versatile SiC Super-Switch Intelligent Power Module (SiC-SS-IPM) for Q2L applications (cf. Fig. 3 (a)).

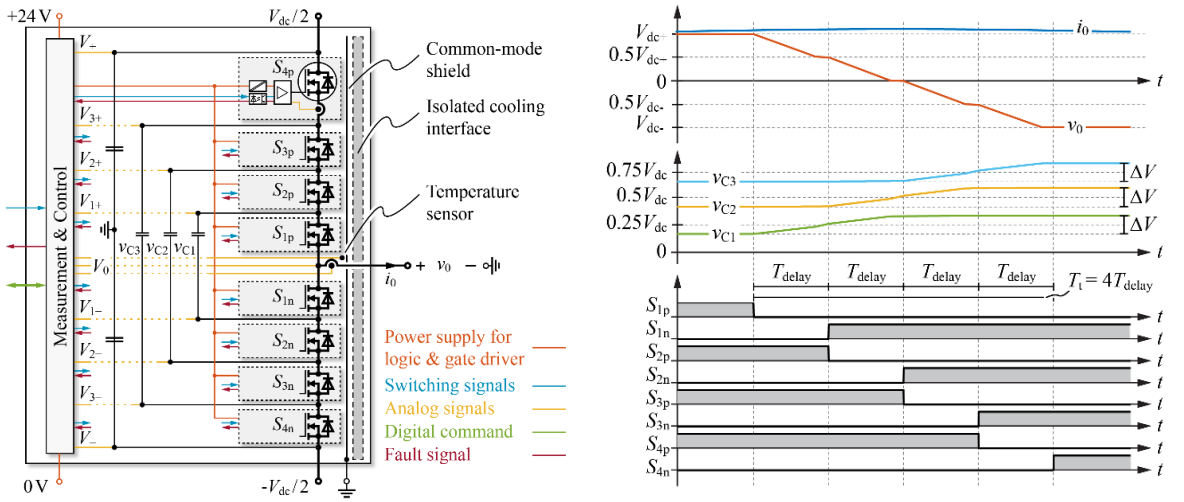


Fig. 3 (a) Proposed Flying Capacitor Q2L *SiC Super-Switch Intelligent Power Module* (SiC-SS-IPM) with 10kV SiC power MOSFETs [13]. (b) Simulation results for Q2L operation of a 5L-FCC bridge-leg: time intervals and simulated waveforms of output current i_0 and output voltage v_0, flying capacitor voltages v_{C1}-v_{C3}, and gate signals.

Description of the SiC Super-Switch Intelligent Power Module

To simplify the converter realization the investigated SiC-SS-IPM integrates all essential FCC bridge-leg components, i.e. semiconductors, capacitors, gate drivers, voltage balancing control, an isolated cooling surface, and a common-mode emission shield, cf. Fig. 3 (a). With this, a superordinate control system requires solely a single digital signal to control the Q2L commutations. The current research aims for a minimization of the total installed capacitor volume. In Q2L operation, charging and discharging of the flying capacitors only occurs during switching operations, which is presented in Fig. 3 (b) for a simulated switching operation related to a falling edge of v_0. For simplicity, MOSFETs are modelled as ideal switches with linear output capacitances. Fig. 3 (b) reveals substantial increases ΔV of the voltages v_{C1}-v_{C3} across the flying capacitors for durations of $2 \cdot T_{delay}$, i.e., the flying capacitors are subject to the output current or parts of it during this time. A corresponding analysis shows: $\Delta Q_{FC} = \pm T_{delay} \cdot I_{0,max}$, for the respective charge increment of each flying capacitor, where the switching sequence, i.e., S_{1x}–S_{2x}–S_{3x}–S_{4x} or S_{4x}–S_{3x}–S_{2x}–S_{1x}, determines the sign of ΔQ_{FC}. Thus, a minimization of

T_{delay} minimizes the required capacitance for a given ΔV. Still, a certain delay time between the turn-off of a switch and the turn-on of the complementary switch is required to achieve low switching losses, i.e., ZVS, which is considered with the gate signals $S_{xp,n}$ shown in Fig. 3 (b) (more details are given in [13]). Of particular interest is the investigation of the implications of the volumes of high voltage capacitors on the volume of a Q2L-MMC in comparison to a Q2L-FCC. For this analysis, off-the-shelf ultra-high voltage ceramic capacitors were considered for a Q2L 5L-MMC and a Q2L 5L-FCC. It was found that for a 40 kV/20 A half-bridge (ΔV = 1 kV, T_{delay} = 1µs) the total capacitor volume of the FCC (0.89 dm^3) is less than 20% of the capacitor volume of the MMC (4.7 dm^3). Consequently, this result confirms that the FCC concept is highly suitable for Q2L operation and integration into a SiC-SS-IPM. In the next step the SiC-SS-IPM will be designed with special focus on the insulation properties. Tests of a hardware demonstrator are scheduled for Q1/2020.

Fault-management in DC grids

DC circuit breakers

In two terminal HVDC, faults require a shutdown of the connection by interrupting the AC side of the converters. For multi-terminal networks, this approach is not feasible, as the failure of a single connection would require to shut down the complete grid. Consequently, for a safe and reliable operation of DC grids, HVDC circuit breakers are required. With no natural current zero crossings, mechanical circuit breakers are not sufficient for short circuit interruption in HVDC grids. The rise of fault current is limited by the system inductance and its steady state value by the parasitic resistance of the grid.

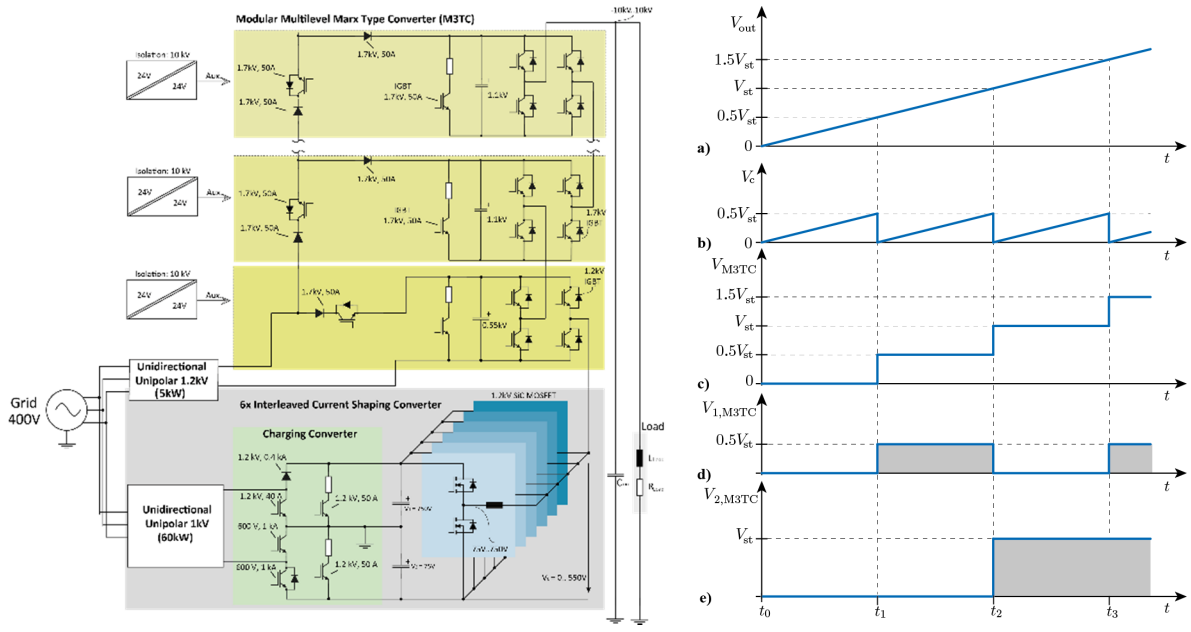
The basic functions of an HVDC circuit breaker (CB) are to build up a counter voltage using semiconductors or capacitors to revert the voltage drop across the system inductance and thus bring the fault current to zero. Current on-state losses of semiconductors still make them unsuitable for nominal current conduction in DC breakers [14]. Consequently, circuit breaker topologies for HVDC networks typically consist of three branches that split the tasks of nominal current conduction, counter voltage build-up and energy absorption. Currently established concepts for HVDC circuit breakers include: (i) Passive oscillation topologies are commonly used for metal return transfer switches [14], [15]; (ii) Current injection topologies [16], [17], where recent prototypes have interrupted peak fault currents of 16 kA without specified voltage (charged capacitor, [18]) and 9.2 kA at 160 kV (coupled inductor, [19]); and (iii) Hybrid breakers, combining mechanical and semiconductor switches [14], [20]. An 80 kV [20] and a 200 kV rated prototype [21] of the hybrid topology have been tested, reaching a peak fault current of 10 kA and 15 kA, respectively. Within SCCER FURIES, several projects in collaboration with ABB, GE, and Hyundai are addressing performance critical elements of HVDC breakers:

- A shortcoming of injection topology type HVDC circuit breakers is the need for several series connected vacuum breakers. SCCER FURIES work at ETHZ aims at improving the performance of gas circuit breakers by controlling the current gradient in the microseconds before current zero. If this is successful, a single unit CB could be used in this type of topologies.
- A second type of injection principle with improved current gradient control before current zero is in investigation at ETHZ. This concept is designed for single unit gas CB but the current gradient before current zero is controlled with IGBTs and the recovery voltage is limited by the use of diodes.
- In the area of switchgear using passive oscillation, another ETHZ project aims at optimizing the interrupter unit itself by controlling the voltage-current characteristic of the arc.
- The key performance limiting element of hybrid type HVDC is the mechanical ultra-fast disconnector, which are currently all operated by a Thomson coil actuator. SCCER FURIES research aims at providing a UFD technology with increased opening speed, minimum gap distance and low contact resistance in closed position.

Testing methods for breakers

In order to support the above developments with a hardware-in-the-loop testbench for DC CBs, by driving highly dynamic and arbitrary current waveforms through dynamic loads (e.g. DC arc), a flexible, modular high current source based on a 3–phase interleaved buck converter has been successfully demonstrated at 3 kV and 3 kA [22], [23]. Based on this, a novel topology with series or parallel stack modules for higher requirements has been introduced in [24], further improved in [25]. Fig. 4 (a)

shows a schematic of a single stack module of the topology, where a current-shaping converter, which controls the output current of the system, is used in series with a modular multilevel Marx-type converter (M3TC) in order to generate the required high output voltage. In [26], an advanced control system for the presented source is also discussed.



(a) (b)

Fig. 4: (a) Stack module of the current source, with 1.5kA nominal current and ±10kV output voltage per stack. The full-scale source consists of 20 parallel stacks with a nominal current of 30kA. (b) Basic operating principle of the investigated current source. a) Output voltage Vout. b) Converter output voltage Vc. c) M3TC voltage VM3TC. d) Voltage of the first stage of the M3TC. d) Voltage of the second stage of the M3TC [25].

Simulations confirm that the combination of an optimal design and a near-optimal control enables the use of the topology's full potential and ensures that the requirements are met without compromising the stability of the system. The current-shaping converter (a 6-phase interleaved buck-type converter) is responsible for controlling the current, shaping arbitrary current waveforms with a highly dynamic current. Additionally, the M3TC is responsible for generating a high staircase output voltage (with slow dynamics) by inserting or bypassing the pre-charged capacitors. For the M3TC converter, up to nine full-bridge modular multilevel converter stages are connected in series, constituting in principle a solid-state Marx-type generator.

The operating principle of the current source is illustrated in Fig. 4 (b). For generating, for example, a linearly rising output voltage V_{out}, first the converter output voltage V_c at t_0 is rising. At t_1, V_c reaches 0.5 V_{st}, which is the pre-charged value of the first stage of the M3TC. At that point, the first stage of the M3TC is turned on and VM3TC becomes $0.5V_{st}$, while V_c collapses to zero. As V_{out} continues to increase, V_c increases. At t_2, V_c reaches again to $0.5V_{st}$ and the first M3TC stage is turned off while the second stage, which is pre-charged to V_{st}, is turned on. Then, the voltage V_{M3TC} becomes equal to V_{st} and V_c collapses to zero. Likewise, at t_3, V_c reaches $0.5V_{st}$, the first M3TC stage is turned on, and VM3TC becomes $1.5V_{st}$. A complete stack module is expected to be fully developed and tested by 2020, including the 6-phase interleaved current shaping converter, 4 M3TC stages for a maximum output voltage of ±4.5kV, the charging system for the capacitor banks and the top level control of the system.

Fault location based on electromagnetic time reversal

Fault location in AC and DC networks has a significant influence on the security (in transmission networks) and quality of supply (in distribution networks). Current methods based on either phasors or

travelling waves have some drawbacks. Several challenges need to be addressed: (i) distributed generation units may have detrimental effects on the accuracy of fault location functions usually developed for passive distribution systems; (ii) overhead lines of distribution systems are often characterized by a significant asymmetry between the phases which refers to the lines' electrical parameters as well as to the lines' power flows; and (iii) the effect of the unknown fault impedance on the fault location accuracy can be significant. To address the above challenges, a promising technology that is able to find the accurate fault location in complex power networks using a single measurement point has been proposed in [27]. The technology is based on the theory of Time Reversal (TR), which was first proposed in acoustics [28]. It relies on the time reversal invariance property of wave equations and has been successfully applied to many areas [29]. Based on this theory an efficient method to locate faults in complex power network is proposed in [27]. It has been shown that the EMTR method can be equally applied to radial/meshed AC/DC power transmission or distribution networks, and compared to other TW-based methods, irrespective to the size and complexity of the network, it requires only a single measurement point. Furthermore, the accuracy of the method is robust against fault impedance and measurement noise [30]. In brief, the proposed method is based on the three steps:

1. Forward propagation phase: the transient voltage signals are recorded in a single measurement point.
2. Backward propagation phase: a number of guessed fault locations (GFL) are pre-defined. The recorded signals are reversed in time and back-injected into the simulated network model from the same measurement point where they have been measured.
3. Fault location characterization: the fault current at each GFL is calculated. According to the temporal and spatial correlation properties of the Time Reversal theory, the back injected signal will arrive in phase only when the GFL corresponds to the real fault location. Therefore, the fault current signal energy (FCSE) can be used as a metric to identify the real fault location.

By using the FCSE criterion, it has been shown that the EMTR process can be successfully applied for different types of power networks with inhomogeneous composition of lines (e.g., overhead and coaxial cables), radial distribution grids [27], series-compensated transmission lines [31], and multi-terminal HVDC networks [32]-[33]. A promising pilot test was performed on a live medium voltage distribution feeder. The tested distribution feeder is operated with a resonant neutral consisting of 11.9-km long double-circuit (overhead) lines operating at 18/60 kV and multiple 18 kV three-phase laterals branching from the main feeder. In order to accelerate the process, alternative methods in frequency domain using the argument of the voltage along the line [34] and using the mirrored minimum energy property [35] have been proposed. In these methods, the transverse branch representing the fault is removed in the backward propagation phase. Thus, the process can be applied using a single simulation of the back-propagation model.

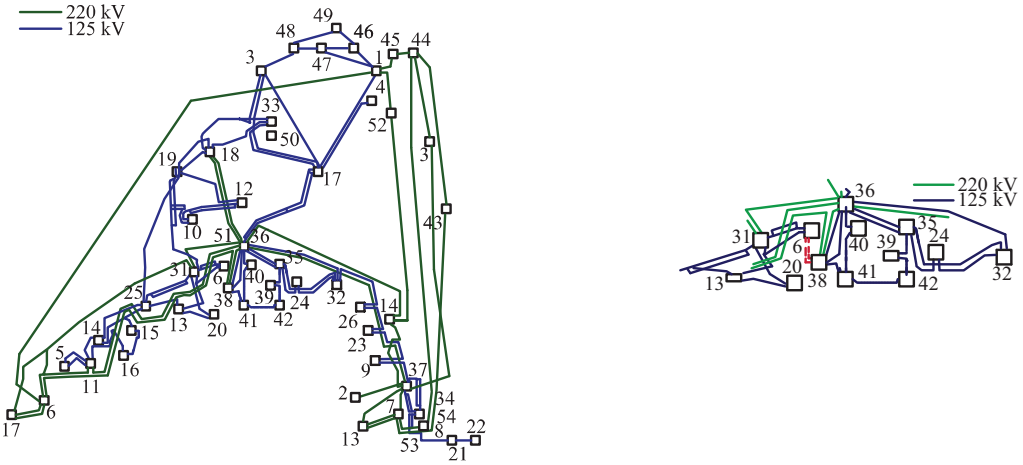
AC/DC system interactions: resonances

The number of grid-connected power electronic converters is increasing due to rising number of renewable energy sources (RES) and HV/MV DC lines [36]-[37]. The injected harmonics by these can lead to overvoltages and therefore damages. Within SCCER FURIES, the resonance behavior of current and expanded DSO networks has been studied (with AC and DC reinforcements), to predict possible resonance problems and to identify the origin of the resonance. A "grey-box" transformer model has been proposed where stray capacitances are taken into account: across each winding, between the primary and secondary windings and between the primary winding and the neutral of the transformer.

These models and methods are applied to an illustration example: the considered transmission (220 kV) and sub-transmission (125 kV) Geneva region networks (64 nodes and 99 lines) are presented in Fig. 5 (a). Power flow transits through the 125 kV network level are possible in case of congestions or outages in the 220 kV level. If line 31-36 is not available, power flows over unnecessarily long stretches of the 125 kV network may result. One of option to overcome this is to reinforce the 125 kV network by building a new HVDC line between nodes 6 and 38 (2.6 km), see Fig. 5 (b). Different operational topologies of the network are also investigated. Hence, the following case studies are performed:

- Case A: Current network, all switches are closed;

- Case B: Current network, switch in node 36 is opened;
- Case C: Current network with HVDC between nodes 6 and 38;
- Case D: Current network with HVDC between nodes 6 and 38, switch in node 36 is opened.



(a) (b)

Fig. 5: (a) Single line diagram of transmission and distribution networks of the Geneva region. (source: Romande Energie). (b) New line location.

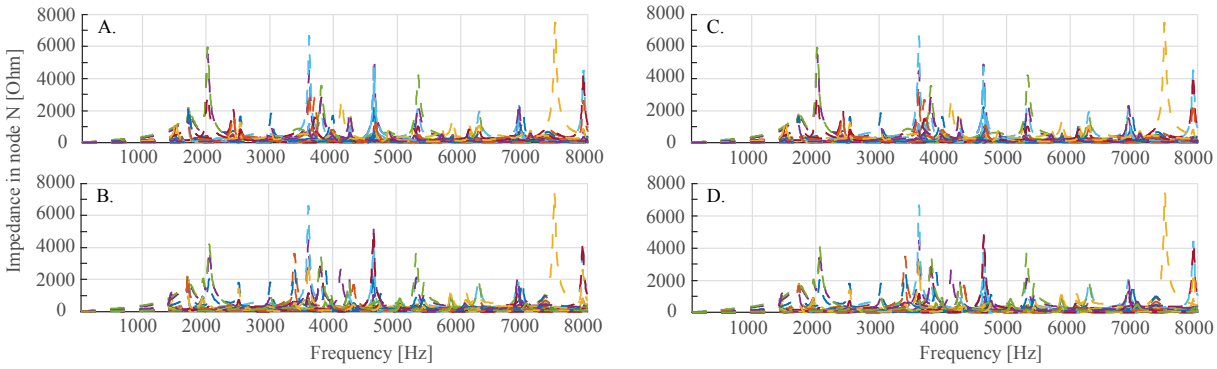


Fig. 6: Frequency scan, results for a phase: current network, current network with opened switch in node 36, the network with a HVDC link, the network with a HVDC link and with opened switch in node 36.

Table I: Changes in studied networks resonance behavior

		Changed switching mode		HVDC link re-inforce-ment	HVDC link reinforcement and changed switching mode	
Resonance amplitude decrement (Hz)		2543 4126		1730 4639	1730 2543	
Resonance peak appearance (Hz)		2059		-	2058	
Resonance peaks vanishing (Hz)		2420 5703		-	2424 5703	
Resonance peak shift (Hz)	Frequency at current network	1523	3382	-	1523	3384
	Frequency at link changed network	1465	3401	-	1465	3400

Fig. 6 shows the frequency scan results for the four studied cases. This example illustrates that the frequency scan study for each node impedance is not straightforward. Resonance mode analysis results described in more details in [38] are therefore needed in order to identify relevant resonance modes and contributing nodes. The considered network changes lead to resonance peaks vanishing, additional peaks appearance, resonance amplitudes decrease and peaks shift shown in Table I.

Concluding remarks

Even through there are currently no specific short-term plans for HVDC grids in Switzerland, HVDC could be interesting for the additional features they can add the AC grid, also in light of Switzerland's role as a transit corridor within the interconnected European System. DC options might also be in a good synergy with improved hydro storage plants (e.g. varspeed pumped-storage), which will increase

the dynamic requirements on the existing power system. Swiss manufacturers and vendors with manufacturing or research units in Switzerland are currently actively working in the HVDC area.

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