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Experimental Verification of the Efficiency/Power-Density (η - ρ) Pareto Front of Single-Phase Double-Boost and TCM PFC Rectifier Systems

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Abstract—Over the last decades, the converter systems performance has been substantially improved but the endeavor for highest possible performance, especially with respect to power density, efficiency, and costs remains the most important driver of present and future developments and research. In latest publications, comprehensive analytical models have been applied in optimization procedures to calculate the design parameters of single-phase AC-DC converter systems resulting in the highest performance concerning multiple objectives.

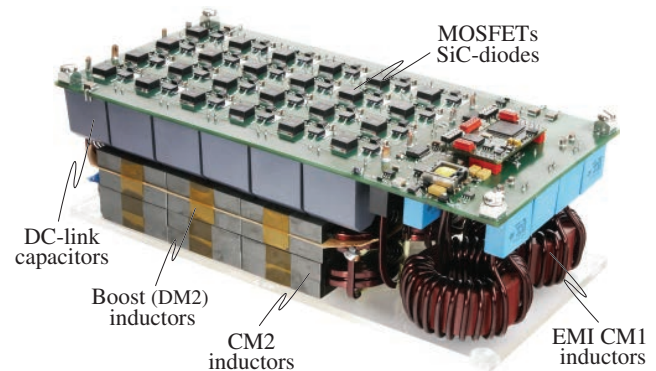
In this paper, an experimental validation of this analytical design approach is provided based on four prototype rectifier systems with Power Factor Correction (PFC) which result from the optimization with respect to power density or efficiency of the mature double-boost bridgeless Continuous Conduction Mode (CCM) and the recently published interleaved totem-pole-based Triangular Current Mode (TCM) rectifier topology. All design details, such as power component values and EMI-filter structure as well as volume and losses distributions, are provided and the measurement results regarding efficiency, EMI standards, and input current quality (power factor and total harmonic distortion) allow the direct performance comparison of the investigated rectifier topologies.

All four prototype systems comply with the EMI standard CISPR 22 class B and exhibit a high power factor and a low current THD. The recently published TCM-topology is beneficially applied to achieve a higher efficiency compared to the efficiency- and volume-optimized double boost CCM rectifier systems with a similar power density. With the loss-optimized TCM-prototype an extreme efficiency of 99.23 % at nominal input voltage and rated output power has been measured.

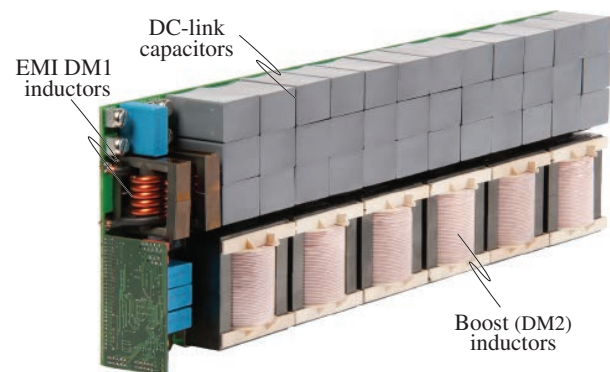
I. INTRODUCTION

In line with the miniaturization of electronic and micro-electronic systems, the development of power electronic systems has focused on the power-density enhancement, enabled by the advancements of semiconductor technology. High-density power supplies are particularly demanded in mobile applications, e.g. aircraft and automotive, as well as in data centers and telecom facilities, because of weight and space limitations. Severely increasing energy prices and the growing environmental awareness are resulting in a paradigm-shift towards efficiency as the today's most important physical performance index of power electronic converter system, while the achieved power-density level should be retained.

Because of the interdependently and multi-domain nature of the free design parameters of power electronic systems the system development towards a highest possible performance



(a) Efficiency-optimized double boost CCM rectifier;
 $\rho = 1.1 \text{ kW dm}^{-3}$ (18.0 W in^{-3}); $\eta_{\max} = 99.08 \%$;
 $85 \times 130 \times 275 \text{ mm}^3$ ($3.35 \times 5.12 \times 10.83 \text{ in}^3$).



(b) Efficiency-optimized sixfold-interleaved TCM rectifier;
 $\rho = 1.1 \text{ kW dm}^{-3}$ (18.0 W in^{-3}); $\eta_{\max} = 99.23 \%$;
 $50 \times 137.5 \times 440 \text{ mm}^3$ ($1.97 \times 5.41 \times 17.32 \text{ in}^3$).

Figure 1. Constructed 3.33-kW extremely efficient (a) double boost CCM and (b) sixfold-interleaved TCM bridgeless single-phase PFC rectifier.

index, e.g. efficiency, or multiple performance indices, e.g. efficiency in combination with a desired power density and costs, is challenging. Automatic optimization procedures based on comprehensive analytical models have been suggested, e.g. in [1]–[6], for computing values of the design parameters resulting in the desired system performance. The measurements taken from the prototype systems which are constructed based on the calculated design parameters enable the validation of the applied analytical models and the calculated performance.

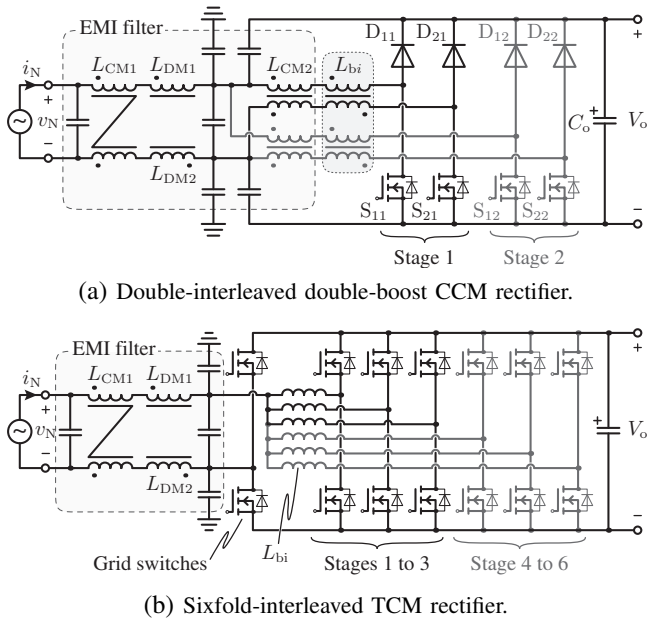


Figure 2. Schematic of the bridgeless (a) double-boost Continuous Conduction Mode (CCM) and (b) Triangular Current Mode (TCM) resonant transition single-phase PFC rectifier.

The knowledge of the design details furthermore allows the direct performance comparison of different systems, e.g. with respect to power density, efficiency and costs.

The area of high-power rectifier systems with Power Factor Correction (PFC) is a highly competitive and continuously increasing and highest performance is crucial in order to meet national regulations such as the Energy Star[®] requirements of computer servers [7], and to succeed in the market. In this paper, a review of two different state-of-the-art PFC rectifier topologies which have been designed and optimized for highest possible efficiency or highest possible power density is given. The design details, e.g. power circuit schematics, component materials and values as well as operation characteristics, and the resulting performance with respect to the power density and efficiency, i.e. losses and volumes distributions, are given in order to identify the feasible performance space in a efficiency–power-density plane (η – ρ plane). The presented performance space and the underlying design parameters allow the exploration of design trade-offs, the identification of the market position and the development of road maps for future rectifier systems.

The selected rectifier topologies, i.e. the bridgeless double-boost Continuous Conduction Mode (CCM) and the Triangular Current Mode (TCM) PFC system, cf. Fig. 2, are briefly reviewed in the following two subsections. In **Section II**, the design and measurement results for the two built power-density-optimized rectifier prototypes are presented. In **Section III** the two constructed extreme-efficiency prototype rectifier systems and the corresponding measurement results are presented. All four converter systems fulfill the international conducted EMI standard CISPR 22 class B due to the applied EMI filter circuits, cf. Fig. 8. In **Section IV**,

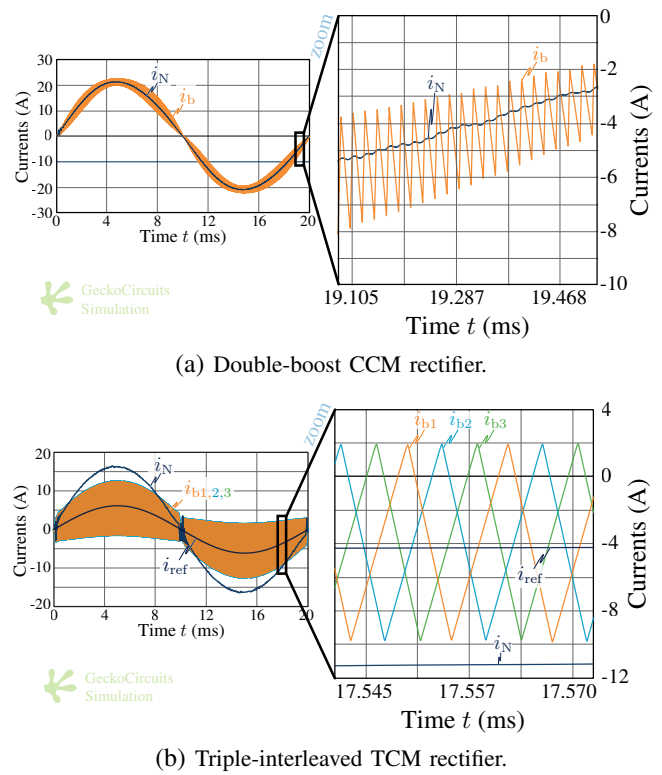


Figure 3. Typical waveforms of the boost inductor currents and the line currents of the (a) double-boost CCM and (b) TCM resonant transition single-phase PFC rectifier; (i_N line input current, i_{bi} boost inductor currents, i_{ref} current reference).

the prototype comparison with respect to the resulting power density and efficiency is given which identifies the feasible performance space and the Pareto Front, i.e. the boundary of the performance space concerning on simultaneous power-density and efficiency optimization.

A. Double-Boost PFC Rectifier

Conventional PFC-systems with a bridge rectifier as input stage suffer from high conduction losses as for each sine half-wave two rectifier diodes are located in the current conduction path. A higher efficiency can be achieved applying a bridgeless or double-boost topology as presented e.g. in [8], [9]. In Fig. 2(a) the schematic of the constructed double-boost PFC rectifiers is given. The double-boost rectifier topology, however, exhibits a considerably higher Common Mode (CM) noise, contrary to the conventional PFC rectifier topology, where always one of the bridge rectifier diodes is connected to neutral of the grid.

In order to enable smaller CM-filter components, two different topologies applying a bidirectional switch or two additional diodes connecting a phase of the mains to the negative output are described in [10].

In any case, the applied double-boost topology presented in this paper, where the DC-output terminals are connected via capacitors to the input lines in order to reduce the CM noise, cf. Fig. 2(a), requires by tendency a larger number of filter components than the below presented TCM resonant

transition single-phase PFC rectifier, cf. Fig. 2(b). A double-boost concept, i.e. two paralleled stages 1 and 2, was chosen to achieve a compact design and to provide the ability to deactivate one stage at part-load in order to increase the efficiency in the low output power range. The first filter stage (L_{CM1} , L_{DM1} , and the corresponding CM/DM filter capacitors) are shared by the paralleled rectifier stages of the ultra-compact prototype and for the highly-efficient prototype the first filter stage is paralleled for the above-mentioned reasons. The second filter stage consists again of the CM and the actual boost (DM) inductors.

The control of the systems and its complexity are comparable to conventional PFC control methods; line voltage and inductor current measurements are required. The high-frequency switching signal is commonly generated by comparing a constant-frequency triangular signal and the line-frequency reference signal calculated in the voltage/current control loop. (Note, that the operation with a frequency-jitter is possible in order to reduce peaks in the EMI spectrum). The resulting input (line) current i_n and the current in the boost inductor i_b are shown in Fig. 3.

The calculation of the component losses is based on the respective currents in the devices which are summarized in the following equations [11], assuming only one rectifier stage and that the MOSFET is turned off during the half period where the respective opposite bridge-leg is switched, i.e. the body diode of the inactive MOSFET is in the conduction path of the line-frequency current. The equations, however, can be easily adopted to the double-interleaved rectifier and different modulation schemes.

The modulation index M is defined by the peak value of the line voltage \hat{V}_N and the rectifier output voltage V_o ,

$$M = \frac{\hat{V}_N}{V_o}. \quad (1)$$

The average and RMS current in one MOSFET ($I_{S,avg}$ and $I_{S,rms}$) is determined with

$$I_{S,avg} = \left(\frac{1}{\pi} - \frac{M}{4} \right) \hat{I}_N \quad (2)$$

and

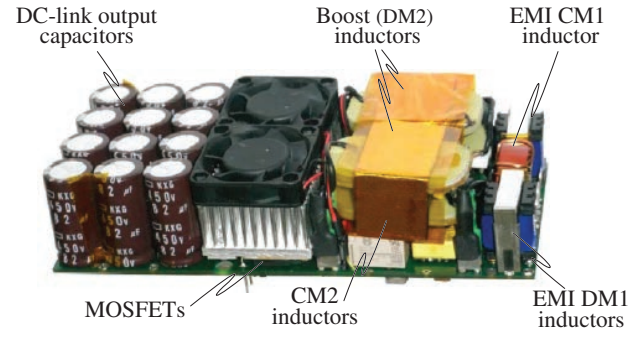
$$I_{S,rms} = \sqrt{\frac{1}{4} - \frac{2M}{3\pi}} \hat{I}_N \quad (3)$$

where \hat{I}_N is the peak value of the line current i_N . The average and RMS currents ($I_{SD,avg}$ and $I_{SD,rms}$) in the respective body diodes of the MOSFET are given by

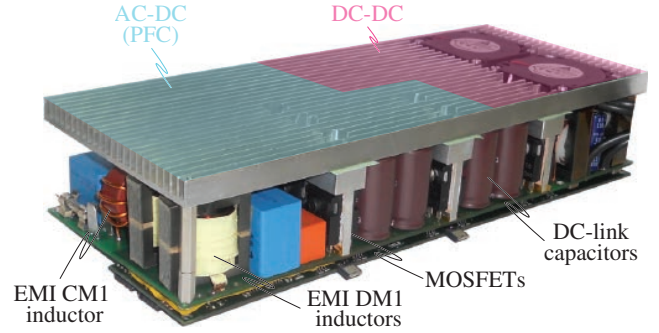
$$I_{SD,avg} = \frac{1}{\pi} \hat{I}_N \quad \text{and} \quad I_{SD,rms} = \frac{1}{2} \hat{I}_N. \quad (4)$$

In case that the MOSFET is turned on during the half period where the opposite bridge-leg is switched for boost-operation the current shares in (4) have to be included in (2) and (3). The average and RMS current stress ($I_{DF,avg}$ and $I_{DF,rms}$) in the two free-wheeling diodes of a single stage are determined by

$$I_{DF,avg} = \frac{M}{4} \hat{I}_N \quad \text{and} \quad I_{DF,rms} = \sqrt{\frac{2M}{3\pi}} \hat{I}_N. \quad (5)$$



(a) Volume-optimized double boost CCM PFC;
 $\rho = 5.09 \text{ kW dm}^{-3}$ (83.5 W in^{-3}); $\eta_{\max} = 95.8 \%$;
 $45 \times 83 \times 175 \text{ mm}^3$ ($1.77 \times 3.27 \times 6.89 \text{ in}^3$).



(b) Volume-optimized triple-interleaved TCM PFC;
 $\rho^* = 4.82 \text{ kW dm}^{-3}$ (78.9 W in^{-3}); $\eta_{\max}^* = 98.5 \%$;
 $54 \times 100 \times 250 \text{ mm}^3$ ($2.13 \times 3.94 \times 3.94 \text{ in}^3$).

Figure 4. Constructed 3.33-kW ultra compact (a) double boost CCM and (b) triple-interleaved TCM bridgeless single-phase PFC rectifier systems. (*Note, the given power density and efficiency in (b) corresponds to the PFC rectifier stage only.)

For each stage, the boost-inductor average and RMS current ($I_{b,avg}$ and $I_{b,rms}$) can be calculated with

$$I_{b,avg} = \frac{2}{\pi} \hat{I}_N \quad \text{and} \quad I_{b,rms} = \frac{1}{\sqrt{2}} \hat{I}_N. \quad (6)$$

In order to calculate the losses in the DC-link capacitors C_o , the RMS current stress $I_{Co,rms}$ is determined with

$$I_{Co,rms} = \sqrt{\frac{4M}{3\pi} - \frac{M^2}{4}} \hat{I}_N \quad (7)$$

assuming a constant load current. With the knowledge of the characteristic values of the employed components the power loss distribution in the main components can be calculated using (1) – (7).

B. TCM Single-Phase PFC Rectifier

Another boost-type rectifier topology providing low conduction losses is the totem-pole based AC-DC rectifier as presented e.g. in [12], [13] which consists of two bridge legs. Two stacked switches (hence the name totem pole) controlled with a high-frequency gate signal are employed in the first leg and two diodes in the second bridge leg commutated with the grid frequency. (Alternatively, the diodes can be replaced by active-switched semiconductor devices such as

Table I
MAIN COMPONENTS OF THE PRESENTED EXTREME EFFICIENCY AND EXTREME POWER-DENSITY PROTOTYPE SYSTEMS.

	Semiconductors			Capacitors DC-Link	Passive Components			Boost ind. DM 2 L_{b2}
	MOSFETs	Diodes	CM 1 L_{CM1}		DM 1 $L_{DM1,2}$	CM 2 L_{CM2}	Filter inductors	
ρ -optimized	4	4	12 x 82 μ F	1 x 637 μ H	2 x 10 μ H	2 x 830 μ H	2 x 100 μ H	
	CCM IPW60R045 45 m Ω	CSD10060 SiC, 10 A	Al-el. Nippon, KXG	VAC W409 2 x 7 turns	EF25 N87 14 turns	EILP38 N87 2 x 10 turns	EILP 38 N87 2 x 10 turns	
ρ -optimized	10	none	10 x 82 μ F	1 x 2.4 mH	2 x 25 μ H	none	3 x 100 μ H	
	TCM IPW60R041C6 41 m Ω	none	Al-el., Nippon, KXG	VAC W380 2 x 6 turns	ETD29 22 turns	none	E42/21/15 N87 33 turns	
η -optimized	24	24	36 x 15 μ F	2 x 1.44 mH	none	2 x 4 mH	2 x 700 μ H	
	CCM IPB60R099 99 m Ω	IDD08SG60C SiC, 8 A	foil AVX, FFB	VAC W565 2 x 12 turns	none	3 x EELP64 3C91 2 x 9 turns	3 x EELP64 3C91 2 x 9 turns	
η -optimized	24	none	36 x 20 μ F	none	2 x 25 μ H	none	6 x 300 μ H	
	TCM IPW60R041C6 41 m Ω	none	foil AVX, FFB	none	ETD39 N27 6 turns	none	ETD59 3C91 42 turns	

MOSFETs in order to further reduce the conduction losses as shown in Fig. 2(b) and considered in this paper.) Due to the connection of an output terminal with the grid during the whole mains cycle the totem-pole rectifier inherently exhibits a better CM noise behavior than the double-boost system. This rectifier topology, however, naturally suffers from significant reverse-recovery losses in the boost-switch leg if operated in Continuous Conduction Mode (CCM) and it is therefore commonly operated in boundary conduction or Discontinuous Conduction Mode (DCM). Consequently, the input current ripple is high and a large Differential Mode (DM) EMI filter is required.

By changing the control scheme of the boost-switches it is possible to achieve Zero Voltage Switching (ZVS) over the entire grid-period. This Triangular Current Mode (TCM) operation as e.g. discussed in [3], [4], [14], [15] is applied for the system depicted in Fig. 2(b). In order to decrease the current ripple and/or to ensure a low effort for EMI-filtering, multiple boost-bridge legs are paralleled and interleaved operation is used (for the compact prototype design three stages and for the extreme-efficiency rectifier six stages are paralleled). The gate control of the switches is, however, more complex compared to other PFC rectifier topologies, e.g. compared to the systems presented in Fig. 2(a) as the switches cannot be driven by the same signal and the zero-crossings of the boost-inductor currents have to be accurately detected. The control complexity is therefore higher compared to the CCM rectifier; furthermore, the switching frequency is varying during the mains period; however, the effort pays off as shown in the following sections.

For instance for positive mains voltage, the demagnetization of the boost inductor is always down to the negative current values in order to allow a resonant voltage transition from the upper to the lower MOSFETs and/or the achieve zero voltage switching. The operation scheme and the determination of the corresponding switching times, considering the non-linear output capacitance of the applied MOSFETs, is detailed in [3]. The sum of the inductor currents $i_{b1,2,3}$, cf. Fig. 3(b), closely correlates with the desired line current i_N ; the resulting

ripple current can be further reduced applying e.g. six instead of three interleaved stages as for the high-efficient converter prototype. As a result of the ZVS operation and a small current ripple, the EMI filter complexity can be reduced compared to the double-boost PFC rectifier shown in Fig. 2.

For calculating the losses in the rectifier system, one could refer to the equations provided in the following paragraph. The modulation index M is defined according to (1). The RMS current $I_{b,rms}$ in a boost inductor, if m stages are interleaved, can be approximated by

$$I_{b,rms} = \sqrt{\frac{8\pi \left(\frac{P_o}{m}\right)^2 - 8I_R \hat{U}_N \frac{P_o}{m} + \pi(I_R \hat{U}_N)^2}{3\pi \hat{U}_N^2}}, \quad (8)$$

where P_o is the output power and I_R is the necessary reverse (negative) current enabling ZVS operation. (The determination of I_R is given in [4]). With the knowledge of the boost-inductor current $I_{S,rms}$, the current in the power transistors in a bridge leg are provided by:

$$I_{S,rms} = \frac{1}{\sqrt{2}} I_{b,rms}. \quad (9)$$

The current stress $I_{Co,rms}$ in the output capacitor can be approximated with a second-order polynomial

$$I_{Co,rms} = \frac{4P_o}{\hat{U}_N} \left(0.348 - \frac{0.221}{M} + \frac{0.047}{M^2} \right). \quad (10)$$

Based on constructed extreme-efficiency and ultra-compact prototype systems the two bridgeless PFC topologies are compared regarding the resulting power density and efficiency in the following sections.

II. POWER-DENSITY-OPTIMIZED DESIGNS

Two topologies, i.e. a double-boost CCM with two interleaved stages and a triple-interleaved TCM bridgeless rectifier, cf. Fig. 2 have been designed with respect to minimum volume, whereas for the TCM rectifier additionally a minimum-efficiency of 98 % at half-load has been considered as a constraint. The constructed power-density optimized prototypes are shown in Fig. 4. In the double-boost CCM prototype

45-m Ω Infineon-MOSFETs IPW60R045 are applied in combination with a silicon carbide free-wheeling diode CSD1060 from Cree, as summarized in table I. Smaller packages with a higher on-resistance would result in a higher heat-sink volume and also paralleling of the devices would result in a higher volume even though the efficiency would increase. In the triple-interleaved TCM rectifier a newer-generation MOSFET (Infineon IPW60R041C6) has been applied, whose increased output capacitance has no drawback because of the ZVS-operation. The reduction of the semiconductor losses by using the TCM-topology, cf. Fig. 2(b), instead of the CCM-topology, cf. Fig. 2(a), is almost 40% as illustrated in Fig. 5, which consequently results in a decreased cooling effort. The absolute volumes of the semiconductor devices are, however, similar for both prototypes, cf. Fig. 6, which can be explained with the increased mounting space for the semiconductor devices.

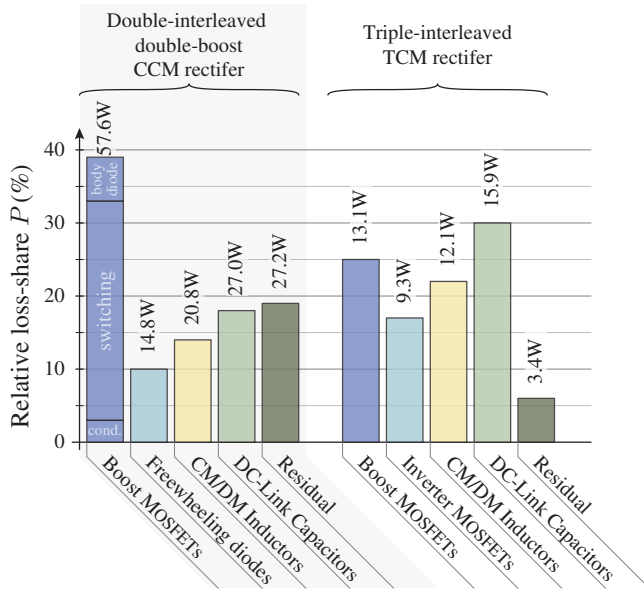


Figure 5. Calculated loss distribution for nominal input voltage ($V_{in}=230$ V) and output power ($P_{out}=3.33$ kW) of the power-density optimized double-interleaved double-boost CCM and triple-interleaved TCM bridgeless PFC rectifier system.

The boost inductors of the CCM-rectifier are constructed with planar EILP38 cores (EPCOS N87) and PCB-windings consisting of 2 x 6 pieces with ten turn each. In order to meet the efficiency constraints of the TCM rectifier, HF-Litz wires are applied on E-cores (EPCOS E42/21/15 N87) for HF-loss-reduced design. Additionally, because of the increased number of boost inductors, the inductors require 30% more volume in the TCM prototype; the losses, however, are decreased by 40%.

The reduced EMI noise of the TCM-concept allows a reduction of the EMI filter volume even though more bulky inductors have to be applied in order to meet the efficiency requirements. The total EMI filter (including the corresponding capacitors) is approximately 20% smaller compared to the

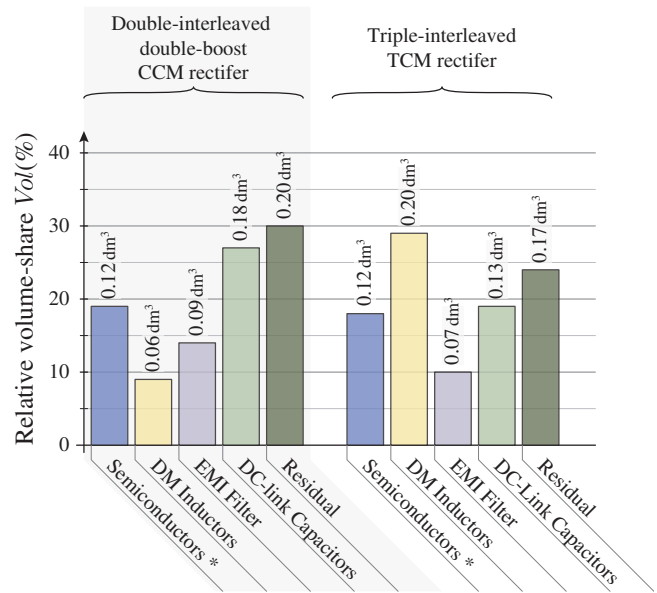


Figure 6. Volume distribution of the constructed compact double-interleaved double-boost CCM and triple-interleaved TCM bridgeless PFC rectifier system. (* The semiconductor volumes include the volume of the heat sink and fan.)

double-boost CCM rectifier.

The losses in the DC-link capacitors have a high share in the total losses which enables the high power density. The applied aluminum electrolytic capacitors exhibit a higher capacitance per unit volume (approx. factor 12 higher compared to the applied foil capacitors of the efficiency-optimized systems, if the net component volume is considered).

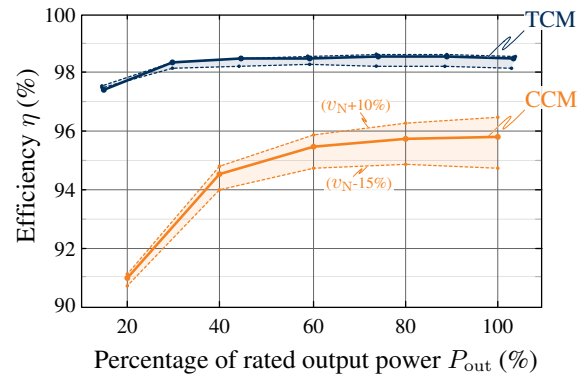


Figure 7. Measured efficiency as function of the output power of the ultra-compact double-interleaved double-boost CCM and triple-interleaved TCM single-phase PFC rectifier prototypes for different line voltages ($v_N = 230$ V -15% +10%).

The residual losses that include the losses in the auxiliary supply and the fans are reduced as a result of the drastically reduced losses in the compact TCM prototype. These almost load-independent losses which also include the reduced switching losses especially improve the part-load efficiency. This is clearly visible in the plots of the measured efficiency as function of the output power shown in Fig. 7. The maximum efficiency of the TCM rectifier has been furthermore increased

by 2.7 % compared to the CCM prototype and the full-load losses, for instance, are reduced by a factor of almost three, even though the volume is approximately similar (6 % higher volume of the TCM rectifier).

Both rectifier systems exhibit a low current THD and a high power factor as verified with measurements, cf. table II. The prototypes furthermore comply with the CISPR22 class B standard as shown in Fig. 8.

III. EFFICIENCY-OPTIMIZED DESIGNS

With the goal of achieving the highest possible efficiency two prototypes for each topology have been designed which are presented in Fig. 1. Both rectifier systems exhibit a similar power density of 1.1 kW dm^{-3} (18 W in^{-3}) and the resulting efficiency at the nominal input voltage is for both systems **above 99 %**, measured electrically and verified calorimetrically with high precision [16].

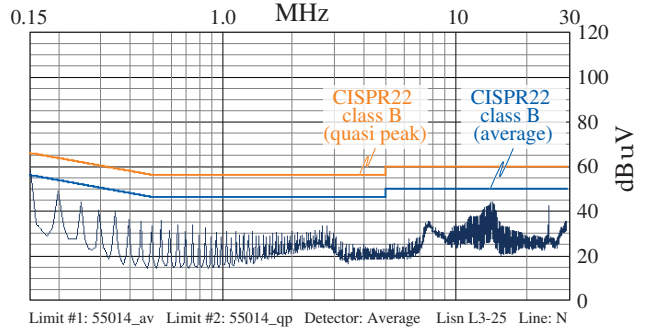
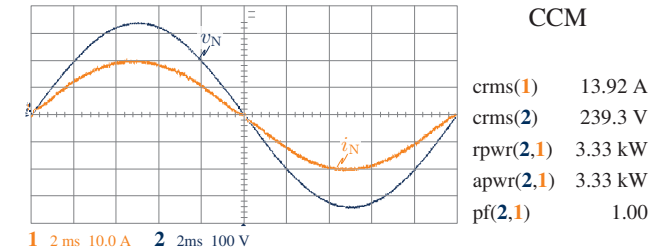
With the sixfold-interleaved TCM rectifier system an extreme efficiency of 99.23 % at nominal input voltage is achieved due to the massive deployment of semiconductors: 24 Infineon IPW60R041C6 MOSFETS ($R_{DS,on}=41 \text{ m}\Omega$) have been assembled in the system (two grid switches and two boost switches per stage). In the CCM rectifier 24 PCB-mounted Infineon IPB60R099 MOSFETs and 24 Infineon IDD08SG60C SiC free-wheeling diodes have been used, cf. table I. The losses in the boost MOSFETs of the CCM rectifier prototype could thereby be reduced by factor of seven (because of the small resulting on-resistance) compared to the ultra-compact design whereas the loss-reduction in the free-wheeling diodes is small because of the major dependency of the forward voltage drop. The switching losses and the frequency-dependent losses in general are furthermore reduced in both extreme-efficiency rectifier prototypes as the switching frequency is decreased from 450 kHz to 33 kHz (CCM rectifier) and from 56 kHz to 31 kHz (TCM rectifier), respectively.

The reduction of the switching frequency implies a necessary increase of the core volumes of the inductors keeping the same flux density. By further increasing the core volume and winding area, the core and winding losses can correspondingly be reduced. In the ultra-efficient CCM rectifier, three planar cores EELP64 (Ferroxcube 3C91) are assembled for a single boost inductor and each CM-inductor. In the ultra-efficient TCM rectifier six E-core based boost inductors are applied

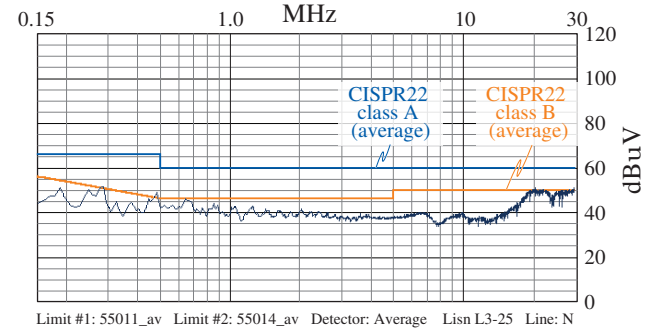
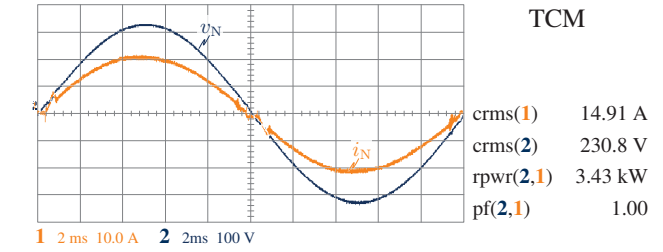
Table II

SWITCHING FREQUENCY f_{sw} , MEASURED POWER FACTOR λ , TOTAL HARMONIC DISTORTION THD_I OF THE INPUT CURRENT, AND EFFICIENCY η OF THE CONSTRUCTED PROTOTYPE SYSTEMS AT NOMINAL OUTPUT POWER $P_{out}=3.33 \text{ kW}$ AND NOMINAL INPUT VOLTAGE $v_N=230 \text{ V}$.

	ρ -optimized		η -optimized	
	CCM	TCM	CCM	TCM
Switching frequency f_{sw}	450 kHz	56 kHz	33 kHz	31 kHz
Power factor λ	99.8 %	99.8 %	99.9 %	99.1 %
Input current THD_I	4.6 %	3.21 %	1.77 %	*
Full-load efficiency η	94.70 %	98.51 %	99.07 %	99.23 %



(a) Double-Boost CCM rectifier



(b) Triple-interleaved TCM rectifier

Figure 8. Measured EMI spectrum and input current and input voltage waveform of the constructed ultra-compact (a) CCM and (b) TCM rectifier systems.

(ETD69, Ferroxcube 3C91). The volume of the boost inductors of the CCM rectifier consequently is increased by a factor of ten compared to the compact prototype, cf. Fig. 6 and Fig. 10. The resulting losses in the inductors could be reduced by a factor of 3.5, cf. Fig. 5 and Fig. 11. (The filter inductor volumes are similarly increased.) The losses in the magnetic components of the TCM rectifier are reduced by a factor of 2.5 with increasing the volume by a factor of six.

Instead of aluminum-electrolyte capacitors foil capacitors are employed in the DC-link. Because of the lower capacitance-per-volume ratio, the volume increases by a factor

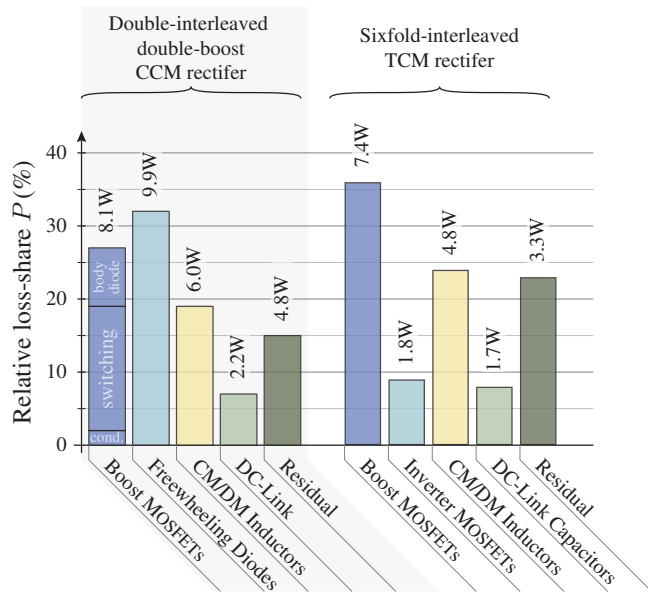


Figure 9. Calculated loss distribution for nominal input voltage ($V_{in}=230\text{ V}$) and output power ($P_{out}=3.33\text{ kW}$) of the ultra-efficient double-interleaved double-boost CCM and sixfold-interleaved TCM bridgeless PFC rectifier systems.

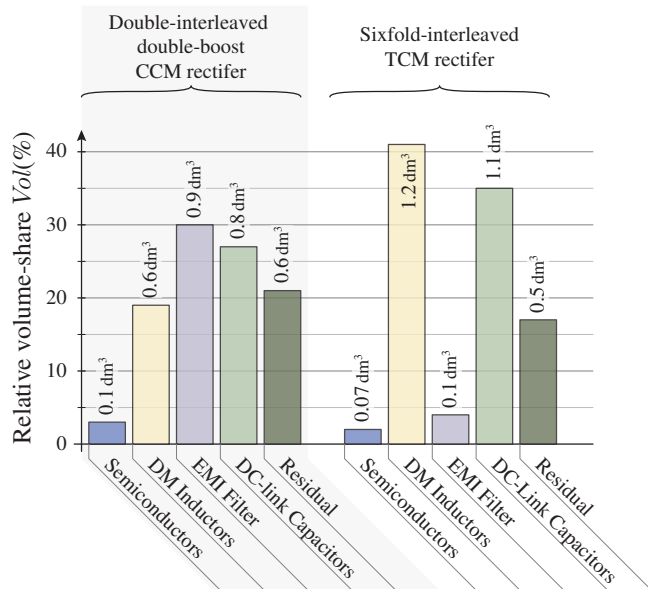


Figure 10. Volume distribution of the constructed ultra-efficient double-interleaved double-boost CCM and sixfold-interleaved TCM bridgeless PFC rectifier systems.

of 4.5 from 0.18 dm^3 to 0.8 dm^3 (CCM rectifier) and even by a factor of 8 from 0.13 dm^3 to 1.1 dm^3 (TCM rectifier), respectively. The DC-link capacitor losses, however, can be reduced by factor of approximately ten as a result of the reduced Equivalent Series Resistance (ESR) and the almost negligible leakage current of the foil capacitors.

The extreme efficiency is also enabled by a reduction of the residual losses which include e.g. the required power for control and cooling. Because of the reduced semiconductor losses natural convection is sufficient in the efficient prototypes

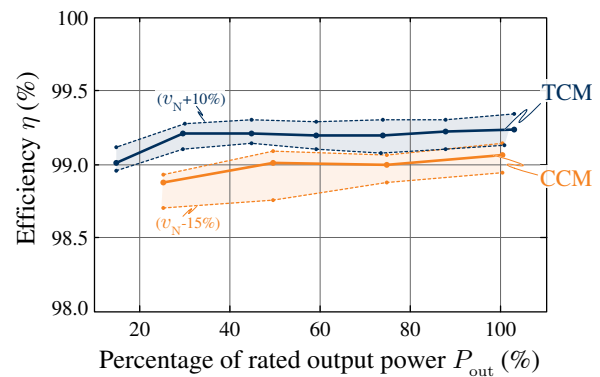


Figure 11. Measured efficiency of the extreme-efficiency systems as function of the output power for different line voltages ($v_N = 230\text{ V} -15\% +10\%$).

and fans are omitted. The control electronics are furthermore designed for highly-efficient operation by reducing the system clock frequency and applying low-power DSPs. The losses in the auxiliary power supply can be inherently reduced because of the decreased power demand.

A special attention with respect to efficiency and accuracy was paid to the boost-inductor current measurement. Applying a shunt resistor would result in low costs and volume; however, in order to have a sufficient resolution for the subsequent amplifier and A/D converter stage, the losses in the required shunts would be in the Watt-range resulting in a noticeable efficiency drop. An efficient option would be the placement of hall-effect latches in the air gaps of the boost inductor cores. The current resolution and the rise/fall time of the open collector output, however, are not sufficient for a highly accurate measurement. In terms of measurement bandwidth and efficiency a current transformer would be a suitable option; however, in order to detect the current direction, the 50-Hz mains frequency would have to be considered which would result in a high cross-section area of the current transformer core. A remedy is provided by applying a saturable current transformer which has been described e.g. in [4]. The efficiency and bandwidth of the saturable transformer remain on a high level as for a conventional current transformer; however, the volume can be drastically reduced.

Moreover, the interleaved structure of the TCM rectifier allows the turn-off of the stages during light-load operation which results in an improved part-load efficiency as shown in Fig. 7; the measured efficiency at the nominal input voltage is above 99% even below 20% of the rated output power (an efficiency of 88% is proposed for 20% load in the EnergyStar[®] program requirements for computer servers for single-output power supplies above 1000 W [7]).

Similarly as for the compact systems, the extreme-efficient systems show an excellent measured power factor and input-current THD, cf. table II. The CISPR 22 class B standard was confirmed with measurements as well.

IV. CONCLUSION

The main contribution of this paper is the comparison of two PFC rectifier topologies based on constructed prototype

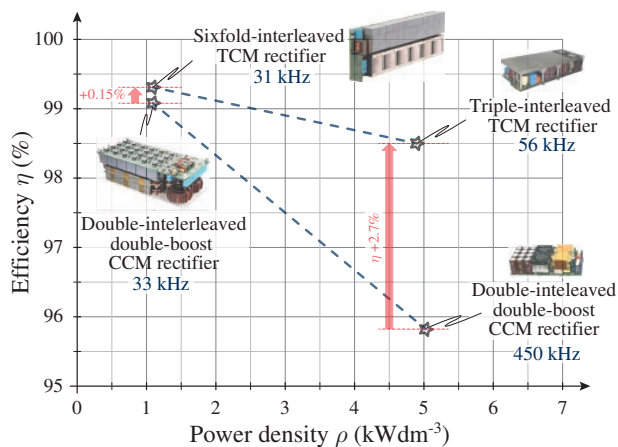


Figure 12. Efficiency–power-density (η – ρ) plane of the presented extreme-efficient and power-density optimized prototype system.

systems with performances as plotted in the η – ρ plane in Fig. 12. With the underlying knowledge of the design provided in the previous sections, researchers and design engineers can validate the own market position and have information on the performance limits. Furthermore, the performance plot allows an estimation of the design parameters such as switching frequency, inductor size, and of the amount of semiconductors for multi-objective design purposes, i.e. for reaching a specific efficiency, power-density or cost target.

As shown in Fig. 12 the totem-pole based sixfold-interleaved TCM rectifier, cf. Fig. 2(b), offers the opportunity to increase the efficiency compared to the double-boost CCM rectifier system with similar power density. The measured efficiency-gain of 0.17 % at full load operation is equivalent to a loss-reduction of 18 %, from 31.42 W to 25.76 W total converter losses ($P_o=3.33$ kW, $V_o=230$ V). The efficiency gain of the ultra-compact prototype systems is even more pronounced; with the only 6 % bigger TCM-rectifier the maximum efficiency could be improved by 2.7 %. At full-load operation ($\eta_{CCM}=94.7$ %, $\eta_{TCM}=98.5$ %) the efficiency-increase of 3.8 % is equivalent with to the loss-reduction by a factor of 3.7.

The design for extreme efficiency results in a significant decreased power density; for the double-boost CCM rectifier prototype a full-load efficiency increase of almost 4.4 %, i.e. a loss-reduction by a factor of almost six, is enabled by the power-density reduction by a factor of 4.6. The efficiency margin of the presented TCM rectifier systems is smaller; the reduction of the losses by a factor of ≈ 2 (efficiency-improvement of 0.73 %) is enabled by almost the same severe power-density reduction as for the CCM-rectifier system (approximately a factor of 4.4).

The extreme efficiency is mainly enabled by the massive employment of semiconductors and the increase of the inductor volume. For the extreme-efficiency CCM-rectifier the number of semiconductors is six times higher (the chip area of the MOSFETs is approximately three times higher) and in the extreme-efficiency TCM-rectifier the number of semiconductors has more than doubled compared to the ultra-compact sys-

tem. The volume for the filter components and boost inductors is ten times higher in the extreme efficiency system compared to the ultra-compact double-interleaved double-boost CCM-rectifier system (approximately a factor of five for the TCM-rectifier prototypes).

The increase of the purchasing costs is approximately proportional to the semiconductor device-count and the volume of the magnetic components. This results in a high initial price to be paid for extreme-efficiency power conversion.

REFERENCES

- [1] J. W. Kolar, J. Biela, and J. Miniboeck, "Exploring the Pareto front of multi-objective single-phase PFC rectifier design optimization - 99.2 % efficiency vs. 7 kW/dm³ power density," in *Proc. of the 6th IEEE International Power Electronics and Motion Control Conference (IPEMC)*, 2009, pp. 1–21.
- [2] U. Badstuebner, J. Biela, and J. W. Kolar, "An optimized, 99 % efficient, 5 kW, phase-shift PWM DC-DC converter for data centers and telecom applications," in *Proc. of the International Power Electronics Conference (ECCE Asia - IPEC)*, Jun. 2010, pp. 626–634.
- [3] C. B. Marxgut, J. Biela, and J. W. Kolar, "Interleaved triangular current mode (TCM) resonant transition, single-phase PFC rectifier with high efficiency and high power density," in *Proc. of the IEEE/IEEJ International Power Electronics Conference (ECCE Asia)*, Sapporo, Japan, Jun. 2010, pp. 1725–1732.
- [4] J. Biela, D. Hassler, J. Miniböck, and J. W. Kolar, "Optimal design of a 5 kW/dm³ / 98.3 % efficient TCM resonant transition single-phase PFC rectifier," in *Proc. of the IEEE/IEEJ International Power Electronics Conference (ECCE Asia)*, Sapporo, Japan, Jun. 2010, pp. 1709–1716.
- [5] M. Hartmann, "Ultra-compact and ultra-efficient three-phase PWM rectifier systems for more electric aircraft," Ph.D. dissertation, ETH Zurich, Nov. 2011.
- [6] U. Badstuebner, J. Biela, D. Christen, and J. W. Kolar, "Optimization of a 5 kW telecom phase-shift DC-DC converter with magnetically integrated current doubler," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 10, pp. 4736–4745, Oct. 2011.
- [7] Energy Star[®]. (2009, May) Energy Star[®] Program Requirements for Computer Servers. [Online]. Available: <http://www.energystar.gov/>
- [8] D. M. Mitchell, "AC-DC converter having an improved power factor," U.S. Patent 4 412 277, 1983.
- [9] B. Lu, R. Brown, and M. Soldano, "Bridgeless PFC implementation using one cycle control technique," in *Proc. of the 20th IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 2, 2005, pp. 812–817.
- [10] L. Huber, Y. Jang, and M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1381–1390, May 2008.
- [11] R. D. Greul, "Modulare Dreiphasen-Pulsleichrichtersysteme (in German)," Ph.D. dissertation, ETH Zurich, Switzerland, 2006.
- [12] J. C. Salmon, "Circuit topologies for PWM boost rectifiers operated from 1-phase and 3-phase ac supplies and using either single or split dc rail voltage outputs," in *Conference Proceedings of the 20th IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 1, 1995, pp. 473–479.
- [13] L. Huber, B. T. Irving, and M. Jovanovic, "Closed-loop control methods for interleaved DCM/CCM boundary boost PFC converters," in *Proc. of the 24th IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2009, pp. 991–997.
- [14] F. Musavi, W. Eberle, and W. G. Dunford, "A high-performance single-phase bridgeless interleaved PFC converter for plug-in hybrid electric vehicle battery chargers," *IEEE Transactions on Industry Applications*, vol. 47, no. 4, pp. 1833–1843, 2011.
- [15] B. Su, J. Zhang, and Z. Lu, "Totem-pole boost bridgeless PFC rectifier with simple zero-current detection and full-range ZVS operating at the boundary of DCM/CCM," *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 427–435, Jan. 2011.
- [16] D. Christen, U. Badstuebner, J. Biela, and J. Kolar, "Calorimetric power loss measurement for highly efficient converters," in *Proc. of the IEEE/IEEJ International Power Electronics Conference (ECCE Asia)*, Sapporo, Japan, Jun. 2010, pp. 1438–1445.