Highly Compact Isolated Gate Driver With Ultrafast Overcurrent Protection for 10 kV SiC MOSFETs

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***Abstract*—Silicon Carbide (SiC) semiconductor technology offers the possibility to manufacture power devices with unprecedented blocking voltages in the range of 10…15 kV and superior switching characteristics, enabling switching frequencies beyond 100 kHz. To drive these 10 kV SiC devices, the power supply and the gate signal of the (high-side) gate driver require an appropriate galvanic isolation featuring a low coupling capacitance and a high du/dt ruggedness. Since at the moment no commercially available gate drivers for these specifications exist, a customized isolated gate driver is developed, which, in order to simplify the use of the high-voltage SiC devices, is intended to be integrated into a future intelligent MV SiC module. For this purpose, a highly compact isolated gate driver with an isolation voltage rating of 20 kV is implemented and tested. The realized isolation transformer of the isolated power supply shows a volume of only 3.1 cm^3 and a coupling capacitance of only 2.6 pF, and has been successfully tested at 20 kV DC. Furthermore, an ultrafast overcurrent protection (OCP) circuit is implemented to protect the expensive SiC modules from destruction due to overcurrents, which e.g. could result from false turn-on of both transistors of a bridge-leg or from short circuits of the load. The OCP circuit reacts within 22 ns to a fault and measurements prove that it can successfully clear both, a hard switching fault (HSF) and even a flashover fault (FOF), where one of the two switches of a bridge-leg configuration is subject to a flashover, in less than 200 ns for a DC-link voltage of 7 kV.**

***Index Terms*—10 kV SiC MOSFET, isolated gate driver, isolation transformer, overcurrent protection, short circuit.**

I. Introduction

MEDIUM-VOLTAGE (MV) SiC devices with blocking voltages of 10…15 kV have gained significant interest in the recent years [1]–[9], since they enable the simplification of MV-connected power electronics by reducing the number of switches and associated isolated gate drivers compared to modular MV converters based on lower voltage devices [10], [11]. Therefore, possible applications for MV SiC MOSFETs and IGBTs are, besides HVDC, e.g. Solid-State Transformers (SSTs) for future data center power supplies [12]–[14], high-power electric vehicle battery charging facilities [15], [16], traction applications [17], [18], naval or marine on-board MV-AC or MV-DC distribution systems [19], [20] or even future all-electric aircrafts [21]. However, these MV SiC devices such as the one shown in Fig. 1 feature extremely fast switching speeds with dv/dt values of up to 100 kV/µs and, in the case of SiC MOSFETs, extremely low soft-switching losses, which allow switching frequencies beyond 100 kHz for DC link voltages in the 5…10 kV range [22]. Consequently, standard isolated gate driver ICs as well as standard isolated gate driver power supplies and optocouplers are not applicable for the power and signal transmission to the high-side switches, since their isolation voltage rating and dv/dt ruggedness are not sufficient. For these reasons, a customized gate driver circuit with a very low coupling capacitance, an isolation voltage in the range of 20 kV for the signal and the power path, and a high dv/dt ruggedness is required to guarantee a reliable operation. Furthermore, in case of a fault, an overcurrent protection (OCP) circuit for the highly expensive SiC devices is desired.

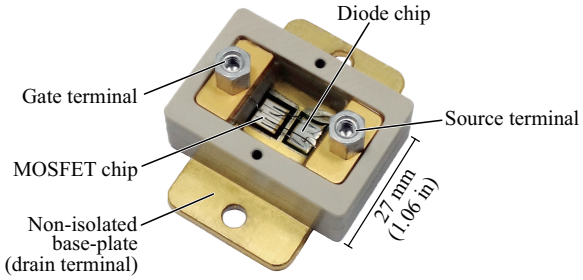

Fig. 1. Basic non-isolated 10 kV SiC module containing a MOSFET chip and an antiparallel SiC JBS diode chip [23], [24].

Concerning the electrical performance, the isolated gate driver should in future be integrated into the SiC module, since this enables a reduction of the gate loop inductance and/or enhances the switching performance of the SiC MOSFET, as it is already reported for 650 V GaN and 1200 V SiC devices [25]–[27]. Moreover, the integration of the isolated gate driver and the OCP into an MV SiC module allows to significantly simplify the design process of MV converters, since the high voltages then only occur at the power terminals of the module, whereas the gate signals and the auxiliary power can be supplied to the module without any additional external isolation measures. Besides the simplification of the MV converter design, this also allows a substantial increase of the MV converter power density, especially by avoiding the large required creepage and clearance distances in air, which can be minimized using a proper insulation material in the isolation transformer and an

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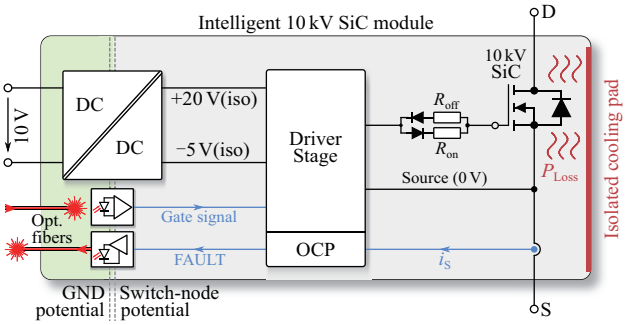

Fig. 2. Concept of a future intelligent 10 kV SiC module which also contains the isolated DC/DC converter for the supply of the (high-side) gate driver stage and a fiber optic receiver for the gate signal. Furthermore, an overcurrent protection (OCP) circuit is integrated, which in case of a fault safely turns off the MOSFET and sends an optically isolated FAULT signal to the supervisory control.

according insulation coordination. Furthermore, in the case of multi-level converters where the auxiliary power is e.g. drawn from the submodule capacitors [28], the integrated isolated power supply can significantly reduce the complexity of the required external auxiliary power supply circuitry.

Fig. 2 shows a schematic drawing of a possible future intelligent 10 kV SiC MOSFET module featuring an integrated isolated DC/DC converter for the generation of the +20 V/−5 V driving voltages, a fiber optic receiver and transmitter for the reception of the gate signal and the transmission of the FAULT signal, and the driver stage with an OCP circuit, which measures the device current and safely turns off the MOSFET in case of a fault. Advantageously, the heat is extracted via an isolated cooling pad, which could be realized with e.g. an aluminum nitride plate featuring a high thermal conductivity while at the same time providing electrical insulation. For the integration of the gate driver, the individual components must be highly compact, which is especially important for the isolated power supply, since the gate driver volume is mainly defined by the volume of the isolation transformer. Consequently, the volume of the isolation transformer V_{trans} has to be minimized, which is one of the main objectives of the following considerations.

In literature, most commonly air or tape-insulated transformers with discrete windings [29]–[34] or PCB windings [35] are used to isolate the power supplies of gate drivers employed in MV SiC applications. In some cases however, these transformers are up to 10 times larger than the 10 kV SiC module shown in Fig. 1. This can be explained by the large creepage distances required in air (40 mm for 10 kV according to the International Standard IEC 60950-1 [36]). Furthermore, these isolation transformers must be placed in safe distance from other converter circuit components in order to not risk creepage currents, partial discharges or even dielectric breakdowns. In [37] a relatively compact current-transformer-based solution with a common AC-bus has been presented and is intended for the supply of several gate drivers at the same time.

Another possibility to realize the galvanically isolated gate driver power supply is to use inductive power transfer (IPT) coils [38]–[41]. However, since the electric breakdown field strength of air is comparably small, a large air gap and large creepage paths are necessary, i.e. the overall IPT system will be large and hence is not suited for an integration in a highly compact module.

A further method to supply electric energy to a floating gate driver circuit is to use an optical fiber [42]. Thereby, a powerful laser (e.g. 3…10 W optical power) feeds an optical fiber, which is connected to the laser receiver on the gate driver side converting the laser power back into electric energy. The advantage of this concept is the theoretically infinite dv/dt immunity, since apart from the remaining intrinsic capacitance of the physical components, the coupling capacitance of the optical fiber is basically zero. Furthermore, no creepage distances to the laser receiver are required, such that compact gate driver circuits could be realized with this concept. However, it has to be mentioned that the laser transmitter is very large (e.g. 220 mm × 197 mm × 143 mm (8.66 in × 7.75 in × 5.63 in) for 3…20 W optical power, cf. [43]) and thus is difficult to accommodate. The low receiver efficiency of only 25% and the high costs are further disadvantages.

Therefore, a highly compact and cost-effective solution for the galvanically isolated power supply of the high-side gate driver circuits for 10…15 kV SiC MOSFETs must be developed, which could be integrated in a future intelligent MV SiC power module.

Furthermore, the gate driver circuit should be equipped with an OCP in order to protect the 10 kV SiC devices (*Wolfspeed CPM3-10000-0350*) from destruction due to overcurrents and/or short circuits. A typical fault scenario is the shoot-through of a bridge-leg configuration, i.e. both switches are erroneously turned on, e.g. due to incorrect or distorted gate signals. For the switch turning on while the complementary switch is already in on-state, this type of fault is called hard switching fault (HSF). In contrast, the switch which is already in the on-state experiences a so-called fault under load (FUL) [44], [45]. However, in MV applications, faults due to isolation and/or flashover failures are especially critical due to their extremely fast transients. These so-called flashover faults (FOF) are much more challenging to handle, and to also protect the MV SiC MOSFETs in this worst-case scenario, an OCP with FOF clearing capabilities is developed.

The most common method for the implementation of an OCP is a desaturation detection circuit, which measures the device on-state voltage and compares it to a certain threshold voltage [42]. However, since during the turn-on transition a large blanking time is required until the device is in full on-state, the fault detection time is relatively high and potentially hazardous for the 10 kV SiC devices due to the high instantaneous power dissipation in the chip during e.g. an FOF. Furthermore, the drain voltage has to be sensed and blocked by several series-connected diodes, which have to be separated from the rest of the gate driver circuit by a certain creepage distance, which increases the gate driver volume [46]. As an alternative, the current could be measured with a shunt in the source path, or, if a Kelvin source contact is available (which is not the case for the 10 kV SiC modules at hand, cf. Fig. 1), the voltage

drop across the parasitic inductance between Kelvin source and power source can be measured and integrated to obtain the device current [47]. Unfortunately, both methods do not offer galvanic isolation, which potentially could lead to undesired CM distortions due to the extremely fast fault transients. Alternatively, the device current could be measured galvanically isolated with a Rogowski coil [48], which is, however, sensitive to external electric and magnetic fields and could therefore lead to false triggering.

In order to avoid the disadvantages of the mentioned OCP methods and to ensure a highly robust and fast protection, an air-gapped current transformer in the source path of the MOSFET is used, which features galvanic isolation, a high bandwidth, and does not require a connection to the drain potential. The measured current is subsequently processed by a high-speed analog circuit, which reacts to a fault within 22 ns and safely turns off the device.

In the following, first the galvanically isolated power supply and the realization of the isolation transformer with minimum volume and coupling capacitance will be discussed (Section II). Subsequently, the ultrafast OCP circuit is described in Section III and it is experimentally proven that it is able to safely clear both, an FOF and a HSF for a DC-link voltage of 7 kV. Finally, conclusions of the main findings are drawn in Section IV.

II. The Isolated Power Supply

The isolated power supply has to provide electric energy to the driver circuit of the power MOSFET, which in the case of the high-side switch is referenced to the switch-node potential, i.e., in the case of 10 kV SiC MOSFETs to a floating rectangular voltage of e.g. 7 kV with a frequency of > 100 kHz, and dv/dt values of up to 100 kV/µs. Therefore, besides providing the isolated +20 V/−5 V driving voltages, the power supply needs to feature a sufficient electrical isolation voltage rating. Furthermore, the common-mode (CM) currents through the parasitic isolation transformer coupling capacitance C_{CM} must be kept sufficiently low in order not to disturb the proper operation of the gate driver and the protection circuits. Commercially available isolated power supplies, e.g. for 3.3 kV and 6.5 kV IGBTs, feature coupling capacitances in the range of 20…25 pF and a size of typically 50 mm × 50 mm × 20 mm [49], [50], whereby MV IGBTs are switching with rather low dv/dt values in the range of 10 kV/µs [51], which is 10 times slower than in the case of 10 kV SiC MOSFETs. Consequently, in a 10 kV SiC MOSFET-based converter, C_{CM} must be reduced by roughly a factor of 10 in order to keep the peak CM current in the same range as in an Si IGBT-based converter. Although there are devices such as [52] featuring an insulation voltage of 12 kV (for one minute) and a coupling capacitance of only 3 pF, the actual allowed operating voltage according to [36] is only 7.2 kV and due to the missing dv/dt and CM frequency ratings, also these devices are unsuitable for MV SiC MOSFET applications. Therefore, a customized isolated power supply featuring appropriate insulation ratings has to be realized. However, with standard isolation transformer designs, a low coupling capacitance can only be realized by large distances between the windings and between the windings and core, whereas on the other hand a significant downsizing is necessary for the integration of the transformer (cf. Fig. 2). To achieve both, a special transformer concept must be developed (cf. Section II-B).

TABLE I
Specification of the Isolated Power Supply

Property	Symbol	Value
Output voltages	U_{DC1} , U_{DC2}	+20 V , − 5 V
Max. output power	P_{max}	2 W
Max. coupling capacitance	$C_{CM,max}$	3 pF
Isolation voltage	U_{iso}	20 kV

The power consumption of the gate driver circuit at hand is 600 mW at most during operation (including the optical fiber transceivers). In order to provide a sufficiently large margin (e.g. if several 10 kV SiC MOSFETs should be operated in parallel), the isolated power supply is rated for a power of P_{max} = 2 W. TABLE I lists the specifications of the power supply as a basis for the design.

A. Isolated Power Supply Topology

Due to the high isolation voltage requirement of 20 kV, a certain isolation distance is required between the transformers' primary and secondary windings. Consequently, a comparably low magnetic coupling factor k and hence a relatively large leakage inductance results, which, if not compensated, leads to a load-dependent voltage drop and hence to a load-dependent output voltage of the gate driver supply. To still obtain a stable secondary-side voltage, a feedback-control would be necessary, which would, however, require an isolated transmission of the measured output voltage signal across the isolation barrier, i.e. additional effort which would further increase the risk of failure of the supply.

To overcome this problem, a topology with a load-independent voltage transfer ratio, namely the series-series compensated resonant converter shown in Fig. 3 is selected. It consists of an H-bridge inverter, a 1 : 1 isolation transformer (i.e. $L_p = L_s$), the resonance capacitors C_{r1} and C_{r2}, and a voltage doubler rectifier generating 20 V DC for the positive gate bias of the 10 kV SiC MOSFET. Thereby, the transformer leakage inductance is compensated by the resonance capacitors and the system is operated at the unity-gain operating point where the output voltage is independent of the load [53]. Furthermore, soft-switching of the primary-side full-bridge (realized with a *MAX13256* IC) can be achieved, enabling a high switching frequency and therefore a more compact design. Furthermore, in this operating point, the transformer currents are sinusoidal and hence beneficial in terms of low high-frequency (HF) losses due to skin-effect and proximity-effect, since no higher current harmonics are present.

According to [53], if only the resistances of the primary and the secondary windings are considered, the highest efficiency (i.e. the lowest rms currents) of the resonant system is achieved when the impedance of the secondary-side is matched to the load impedance. For a maximum output power of P_{max} = 2 W, a given secondary-side inductance L_s and a secondary-side

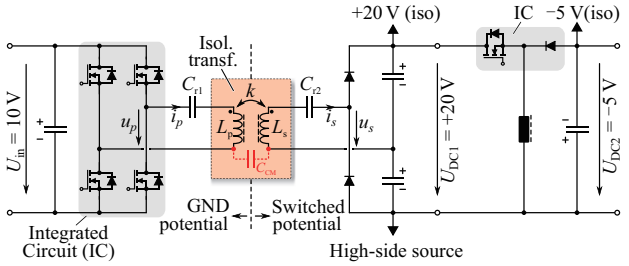

Fig. 3. Schematic diagram of the isolated power supply. The isolation transformer is operated in a series-series compensated configuration whereby $L_p = L_s$ and $C_{r1} = C_{r2}$. The subsequent voltage doubler rectifier generates +20 V DC, from where a buck-boost converter generates −5 V DC, which is used for the supply of the analog and logic ICs as well as for the negative biasing of the gate in the off-state of the 10 kV SiC MOSFET.

voltage of $u_s = U_{DC1}/2 = 10$ V (half the DC output voltage U_{DC1} due to the voltage doubler rectifier, cf. Fig. 3), the optimum operating frequency f_0 in order to fulfill the load matching condition at full load is given as

$$f_0 = \frac{8}{\pi^2} \cdot \frac{u_s^2}{2\pi\sqrt{2}\, L_s k P_{max}}, \tag{1}$$

with k as magnetic coupling factor between the transformer's primary-side and secondary-side. To achieve a load-independent voltage transfer ratio, the resonance capacitors have to be dimensioned as [53]:

$$C_{r1} = C_{r2} = \frac{1}{(2\pi f_0)^2 L_s (1-k)}. \tag{2}$$

In this operating point (which is slightly above the resonance), the phase angle of the input impedance seen by the full-bridge is

$$\varphi(Z_{in}) = \arctan(\sqrt{2}) = 54.7° \tag{3}$$

and hence guarantees ZVS operation of the MOSFETs due to the inductive behavior [53]. Furthermore, due to this particular compensation method, the primary-side rms current is independent of the inductances, the magnetic coupling, and the operating frequency, and can be calculated as

$$i_{p,rms} = \sqrt{\frac{3}{8}} \cdot \pi \cdot \frac{P_{max}}{u_s} = 384\,\text{mA}. \tag{4}$$

The secondary-side current is ideally in phase to the rectangular voltage applied from the rectifier and its rms value can be calculated as

$$i_{s,rms} = \frac{P_{max}}{u_s} \cdot \frac{\pi}{2\sqrt{2}} = 222\ \text{mA}. \tag{5}$$

B. Isolation Transformer

In conventional isolation transformers, the primary and the secondary windings are placed on the same magnetic core and are galvanically isolated from each other by means of insulation material between the primary winding and the core, the secondary winding and the core, and between the primary and secondary windings. In the case of the application at hand, the differential mode voltage applied to both transformer windings is < 50 V and hence, no further isolation between the primary winding and the core (which in this case would be tied to GND potential) would be necessary. However, the secondary winding would have to be isolated from both, the core and the primary winding since it is floating on the switched potential of e.g. 7 kV. Consequently, the winding window and therewith the size of the entire magnetic core has to be chosen sufficiently large, such that the secondary winding can be separated from the core and from the primary winding by approximately 1.6 mm of insulation material thickness to each side, if an (average) electric field strength of 4.5 kV/mm is allowed and the transformer is potted in a suitable insulation material. Since the transformer's power rating is only $P = 2$ W but the isolation distances do not scale with the power but are defined by the isolation voltage, the required winding window would be large compared to the dimensions of a typical 2 W HF transformer without MV isolation and hence, this transformer concept is not suitable for achieving a low volume.

To overcome this limitation and to minimize the volume of the isolation transformer, as many isolation barriers as possible have to be omitted. Therefore, the primary winding and the secondary winding are wound on separate ferrite E-core halves without any isolation distance between the winding and the core. Fig. 4(a) shows a drawing of one of the core halves with its corresponding winding. Thereby, the core consists of several stacked E-cores to achieve the desired form factor. The two core halves with their respective windings are then separated by a certain distance $d = 1.6$ mm to keep the average electric field strength below 4.5 kV/mm in the case of 7 kV CM voltage, similar to the air gap in a conventional transformer [54], [55]. The isolation distance between the two core halves is ensured by mounting them in a 3D-printed enclosure as shown in Fig. 4(b). In operation, the primary winding is on GND potential, whereas the secondary winding floats on the switch-node potential. To also define the potential of the ferrite cores, they are connected to one end of the corresponding winding as shown in Fig. 4(c) and are covered with a thin layer of semiconductive graphite spray (cf. Fig. 4(d)) to tie the surface of the entire core halves to the potential of the respective winding. The surface resistance of the graphite spray (*Kontakt Chemie Graphit 33*) is < 2000 Ω/sq, which is sufficiently low to define the potential of the surface and at the same time is sufficiently high such that no significant eddy current losses are generated by the magnetic field [56]. As an alternative, semiconductive tape could be used to create an equipotential surface.

Consequently, this transformer arrangement can be regar-ded as plate capacitor from an electric field point of view, which allows to estimate the coupling capacitance of the transformer as

$$C_{CM} = \frac{\varepsilon_0 \varepsilon_r A}{d}, \tag{6}$$

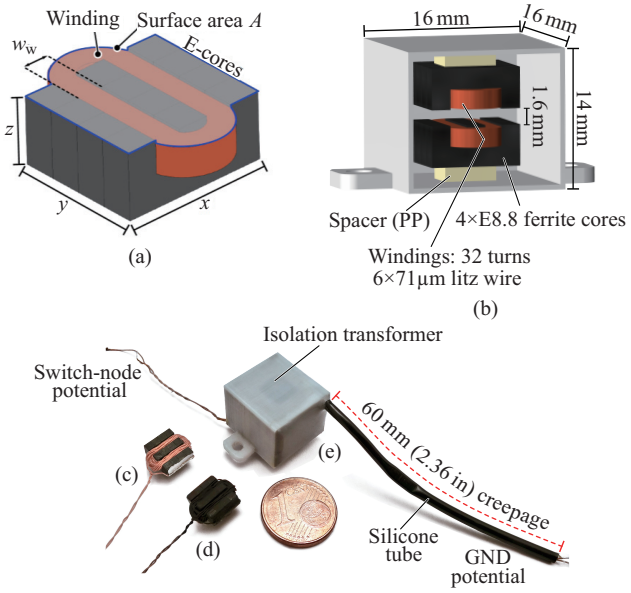

Fig. 4. (a) Ferrite core half (consisting of several stacked E-cores) with its corresponding winding. (b) CAD model of the isolation transformer (outer dimensions 16 mm × 16 mm × 14 mm, i.e., 0.63 in × 0.63 in × 0.55 in) showing the two windings on the ferrite cores, which are separated by a 1.6 mm gap. The 3D-printed housing is then filled up with a special silicone which provides the electrical insulation. (c) Picture of the winding (32 turns of 6 × 71 µm litz wire) on four stacked E8.8 ferrite cores. One end of the winding is electrically connected to the stacked cores with the help of conductive silver paint (silver color). (d) The whole arrangement is then coated with a semiconductive graphite layer (black color) to define an equipotential surface. (e) Picture of the realized silicone-encapsulated isolation transformer. The necessary creepage distance is provided by the silicone tube.

where A is the surface area of the core halves and the windings (cf. Fig. 4(a)) and d is the separation distance between the core halves. Since d is already fixed to d = 1.6 mm, the remaining geometry parameter to minimize the coupling capacitance is the surface area A. With a relative permittivity of ε_r = 4.12 of the selected insulation material (cf. Section II-B1), the surface area must be lower than 132 mm^2 to keep the coupling capacitance below the desired value of $C_{CM,\,max} < 3$ pF, which is roughly 10 times lower than the coupling capacitance of commercially available isolation transformers. To fulfill this condition, four stacked E8.8 ferrite cores (material *N30*) are used (x = 9 mm (0.35 in), y = 8 mm (0.31 in), z = 4.1 mm (0.16 in), cf. Fig. 4(a)), which results in an almost square-shaped form factor of the core surface, a surface area of A = 108 mm^2 (including the winding heads), and a theoretical coupling capacitance of C_{CM} = 2.5 pF.

In order to analyze the electric field in the isolation transformer, a FEM simulation has been implemented and the simulated electric field distribution is shown in Fig. 5. As can be seen, the windings are field-free due to the shielding effect of the graphite coating. Furthermore, a high electric field only occurs between the limbs of the ferrite cores and is slightly lower between the windings (due to the slightly larger distance). To decrease the maximum electric field strength, the edges and corners of the ferrite cores have been rounded off and the maximum value of the electric field (6 kV/mm) is still

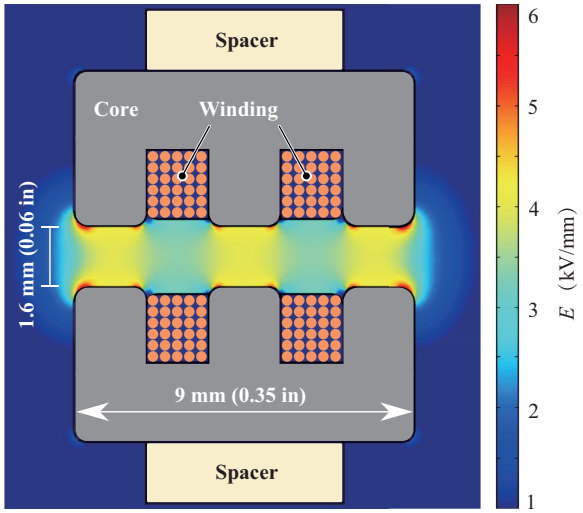

Fig. 5. Simulated electric field strength in the isolation transformer. The maximum occurring electric field strength (6 kV/mm) is still lower than the breakdown field strength of the used insulation material (24 kV/mm) by a factor of four.

a factor of four lower than the breakdown field strength of the used silicone encapsulant and therefore uncritical.

As can be noticed from the dimensions of the cores, the isolation gap is comparably large and hence, a rather low magnetic coupling factor k will result. Thus, the transformer acts similar to a pair of inductive power transfer (IPT) coils. Thereby, larger primary-side and secondary-side inductance values are beneficial for ensuring a higher quality factor [57] and lower magnetization current, and for this reason the number of turns wound on the two core halves should be as high as possible while the thermal limit has to be considered at the same time. Therefore, a maximum current density of J_{max} = 15 A/mm^2 is defined. In order to keep the high-frequency losses due to the skin and proximity effect to a moderate level, litz-wire has to be employed for the primary and secondary windings. For a maximum expected operating frequency of f_{max} = 1 MHz, a skin-depth in copper of δ_{Cu} = 65 µm results. Hence, as a compromise between the copper filling factor and the HF losses, a strand diameter of d_s = 71 µm is selected and with an assumed total copper filling factor of 25% (i.e. 50% litz-internal and a 50% ratio between the winding area and the available core window area), the maximum achievable number of turns is 34. For practical reasons, a 6 × 71 µm litz wire and N = 32 turns is selected, resulting in a DC-resistance of R_{DC} = 620 mΩ.

To check the feasibility of the transformer design, the magnetic flux density in the ferrite core is determined, whereby it is assumed that the operating frequency is in the range of $[f_{min}, f_{max}]$ = [100 kHz, 1 MHz]. Furthermore, due to the series-series compensation of the leakage inductance, the peak value of the sinusoidal voltage applied to the magnetizing inductance of the transformer is approximately equal to the fundamental component of the rectangular voltage applied from the primary-side, i.e.

$$\hat{u}_\mathrm{m} = \frac{4}{\pi} \cdot u_\mathrm{p} \ . \tag{7}$$

Consequently, with the magnetic cross section area A_m of the core, the peak magnetic flux density can be calculated as

$$\hat{B} = \int_0^{\frac{1}{4f}} \frac{\hat{u}_\mathrm{m}}{N \cdot A_\mathrm{m}} \sin(2\pi f t) \cdot \mathrm{d}t = \frac{2u_\mathrm{p}}{\pi^2 N A_\mathrm{m} f} \ , \tag{8}$$

resulting in $\hat{B}$ = 3.2 mT…32 mT for the assumed frequency range, which indicates that the ferrite cores are operated far below the saturation limit and hence the design is feasible from a magnetic perspective.

1) Thermal Model & Selection of the Insulation Material:

For a prediction of the temperature distribution inside the transformer and especially in the insulation material which plays a central role for the transformer at hand, a thermal FEM simulation is conducted. As a basis for the simulation, the different loss components, i.e. winding losses, core losses, and dielectric losses are calculated first.

For an estimation of the worst case winding losses, the AC winding resistance at the highest expected transformer operating frequency (f_max = 1 MHz) is calculated. Considering the skin-effect and the proximity effect, the winding losses can be calculated according to [58] as

$$P_\mathrm{Cu} = R_\mathrm{DC} (F_\mathrm{R} \hat{I}^2 + G_\mathrm{R} \hat{H}^2) \ , \tag{9}$$

where F_R and G_R are the factors describing the skin-effect and the proximity-effect, and $\hat{H}$ depicts the temporal peak value of the magnetic field, which shows a triangular spatial distribution across the winding window width w_w = 1.65 mm (cf. Fig. 4(a)) and a spatial rms value of [59]

$$\hat{H}_\mathrm{srms} = \frac{N\hat{I}}{\sqrt{3}\, w_\mathrm{w}} \ . \tag{10}$$

By combining (9) and (10), the ratio between the effective AC resistance R_AC and the DC resistance R_DC can be derived [58]. For f_max = 1 MHz, this factor is $R_\mathrm{AC}/R_\mathrm{DC}$ = 4.5, i.e., the effective AC resistance is R_AC = 2.8 Ω for each of the two windings. With the calculated primary-side and secondary-side currents (cf. Section II-A), the highest expected winding losses are $P_\mathrm{p,Cu}$ = 415 mW and $P_\mathrm{s,Cu}$ = 138 mW.

Furthermore, a calculation of the core losses with the Steinmetz parameters for *N30* ferrite (k_c = 15.88, α = 1.31, and β = 2.45 [60]) and the determined values for the magnetic flux density leads to 4 mW at f = 100 kHz and 0.3 mW at f = 1 MHz, respectively, i.e. the core losses can be neglected.

Due to the comparably high electric field in the isolation transformer and the high switching frequency of the 10 kV SiC MOSFET bridge, the insulation material between the two core halves is exposed to a high dielectric stress and therefore, dielectric losses might become significant and would have to be considered. According to [61], the dielectric losses generated in a capacitance C_CM by a rectangular voltage with bottom value 0 V, top value U_DC, frequency f_sw and 50% duty cycle can be calculated as

$$P_\mathrm{d} \approx \tan\delta \cdot C_\mathrm{CM} U_\mathrm{DC}^2 \cdot \frac{2f_\mathrm{sw}}{\pi} \ln\left(\frac{2e^\gamma f_\mathrm{c}}{f_\mathrm{sw}}\right), \tag{11}$$

where $\gamma \approx 0.57$ is the Euler-Mascheroni constant, and

$$f_\mathrm{c} = \frac{\ln\left(\frac{0.9}{0.1}\right)}{2\pi t_\mathrm{rise}} \tag{12}$$

is the corner frequency (cf. [61]). Furthermore, t_rise is the 10 %…90 % rise time of the switch-node voltage. Thereby, it is important to note that not only the fundamental frequency component of the switch-node voltage but also the higher order harmonics contribute to the dielectric losses. (11) already includes the effect of the harmonics and as can be seen, the total dielectric losses are proportional to the dissipation factor tan δ, the switching frequency f_sw, and the square of the voltage, or the electric field, respectively. To show that it is important to select a suitable insulation material, the dielectric losses are first calculated for a typical epoxy-based insulation material, e.g. *Damisol 3418* whose dissipation factor is strongly frequency and temperature dependent [61] and is assumed to be tan δ = 1.2% for the following calculations. With a switch-node voltage of 7 kV, a switching frequency of f_sw = 125 kHz and a rise time of t_rise = 100 ns, dielectric losses of P_d = 430 mW occur in the insulation material, which is very high compared to the rated power of the isolation transformer. Furthermore, epoxy resins typically feature a rather low thermal conductivity (0.3 W/(m K) in this case), which means that the extraction of the heat generated by the dielectric losses is impeded and therefore could lead to a thermal runaway.

Fig. 6(a) shows the simulated temperature distribution inside the isolation transformer in the case of epoxy resin as insulation material and a fixed housing temperature of 50 °C. As can be seen, due to the dielectric losses in the insulation material and the low thermal conductivity of the epoxy resin, a hot spot between the two core halves and a temperature rise of 44 K occurs. Since epoxy resins typically show a significant increase of their dielectric dissipation factor tan δ which can reach values of tan δ > 25% at higher temperatures in the region of their glass transition temperature [61]–[63], a thermal runaway is very likely to happen (especially when a higher surface temperature of the isolation transformer is considered, e.g. the baseplate temperature of 100 °C of a SiC module, which also integrates the transformer, cf. Fig. 2) and therefore, epoxy resins are unsuitable for MV MF applications.

In contrast, silicone composites typically feature a very low and stable tan δ up to temperatures beyond 200 °C. However, pure silicone rubber typically shows only a low thermal conductivity, which would potentially lead to an undesired heat accumulation similar to Fig. 6(a). To increase this value, thermally conductive micro or nanoparticles can be added to the pure silicone, which, on the other hand, leads to an

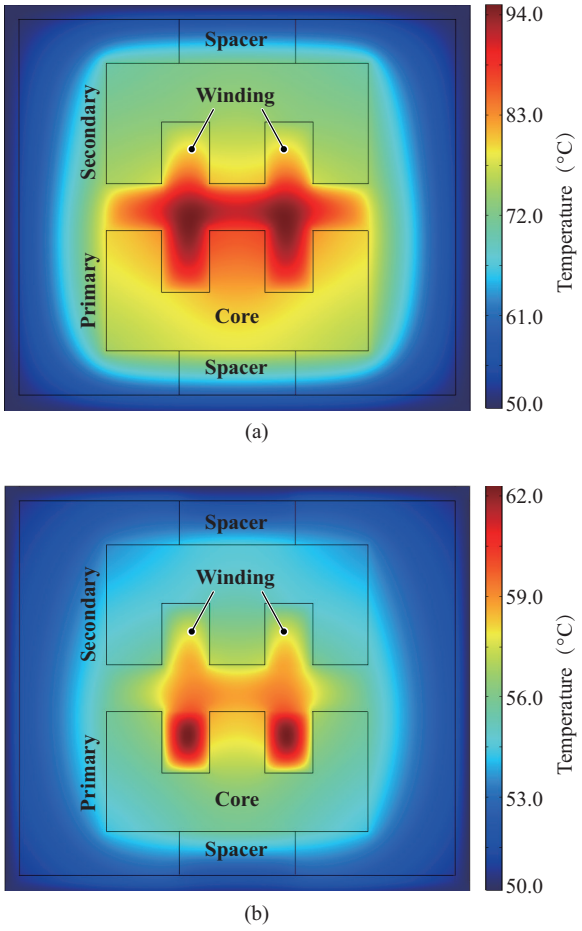

Fig. 6. (a) Thermal FEM simulation of the temperature distribution inside the isolation transformer in the case of epoxy resin as insulation material and a boundary condition of 50 °C at the transformer housing surface. The dielectric losses dominate over the winding and core losses and a temperature increase of 44 K occurs in the insulation material between the core halves. (b) Temperature distribution in the case of silicone (*Dow Corning TC-4605 HLV*) as insulation material. Due to the much lower dissipation factor and the higher thermal conductivity, the temperature increase is only 12 K in this case.

TABLE II
PROPERTIES OF THE UTILIZED SILICONE *DOW CORNING TC 4605 HLV*

Property	Value
Dielectric strength	24 kV/mm
Dielectric constant ε_r	4.12@100 kHz
Dissipation factor tan δ	0.63%@100 kHz
Thermal conductivity	1 W/(m K)
Operating temperature	− 45 . . . 200 °C

increasing dielectric dissipation factor [64]. Therefore, a compromise between a low tan δ and a high thermal conductivity has to be made. The utilized material for the encapsulation of the isolation transformer at hand is the two-component silicone compound *Dow Corning TC-4605 HLV* and the properties of this material are listed in TABLE II. With this insulation material, the dielectric losses are only P_d = 300 mW. Fig. 6(b) shows the associated temperature distribution inside the isolation transformer and as can be seen, the temperature increase in the hot spot, which is now located inside the primary-side winding, is only 12 K due to the lower dielectric losses and the higher thermal conductivity. This shows that the selection of a proper insulation material is crucial for the functionality of a highly compact isolation transformer and consequently, with the selected material, the isolation transformer can be operated inside an intelligent 10 kV SiC module with an assumed baseplate temperature, i.e. transformer surface temperature of 100 °C, which would lead to a hot spot temperature of 112 °C inside the transformer.

For a reliable operation of the isolation transformer, the insulation material must be free of air-cavities or other impurities, which could lead to partial discharges and a degradation of the material over time. Therefore, a vacuum pressure potting (VPP) process is used, i.e. the silicone is devolatilized and the transformer is potted under vacuum (30 mbar) before the pressure is increased again to compress possible air or vacuum cavities. The still liquid silicone compound is then cured at a temperature of 120 °C for several hours. More details on the VPP process and the insulation material are given in [14].

In order to provide a sufficiently large creepage distance between the primary-side and secondary-side litz wires at the outside of the transformer, a silicone tube is covering the primary-side litz wire (on GND potential) and is also potted in the silicone insulation material such that there is no other creepage path than the one along the silicone tube. The finalized isolation transformer is shown in Fig. 4(e).

2) Determination of the Transformer Properties:

Besides the inductances and the magnetic coupling factor k, which are required to determine the optimum operating frequency, also the parasitic coupling capacitance C_{CM} between the primary-side and the secondary-side is measured. For this purpose, a *HP 4294A Precision Impedance Analyzer* is used.

The measured value of the coupling capacitance is C_{CM} = 2.6 pF, which matches very well with the calculated value of 2.5 pF. Considering the small transformer dimensions, this capacitance value is very low and ensures that the parasitic CM currents stay in a reasonable range even in the case of high dv/dt values of up to 100 kV/µs.

The measurement of the primary-side and the secondary-side inductances leads to L_p = 23.7 µH and L_s = 23.4 µH and together with a measured leakage inductance of L_σ = 22 µH, the magnetic coupling factor (referenced to the primary-side) can be calculated as

$$k = \sqrt{1-\frac{L_\sigma}{L_p}} = 0.27. \tag{13}$$

With these values, the optimum operating frequency f_0 = 713 kHz, and the values of the resonance capacitors $C_{r1} = C_{r2}$ = 2.88 nF, can be determined with (1) and (2), respectively.

C. Experimental Verification of the Isolated Power Supply

For the experimental verification of the isolated gate driver power supply, different stress tests have been performed. To test the DC isolation rating of the designed transformer, a

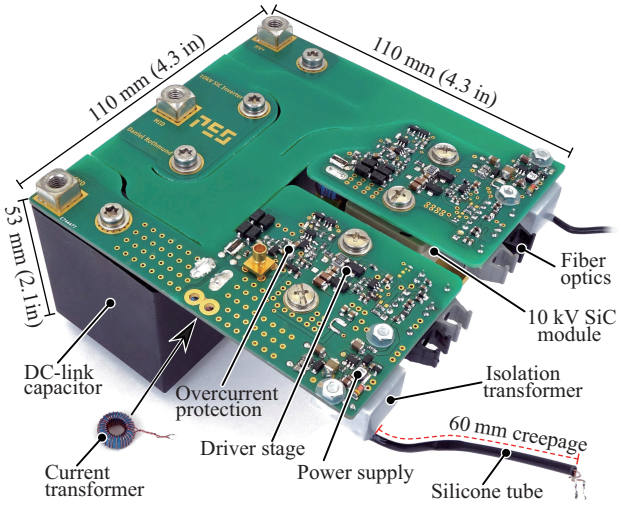

Fig. 7. Picture of the 10 kV SiC-MOSFET half-bridge. Due to the encapsulated isolation transformers, no additional isolation distances are required, enabling a highly compact design of the gate driver circuit and the half-bridge. The 10 kV SiC MOSFETs and the current transformers (cf. Section IV) are mounted below the PCB.

20 kV DC voltage (which is almost three times higher than the maximum operating voltage of 7 kV) has successfully been applied between the transformer's primary and secondary windings for one hour without breakdown, temperature increase or measurable current flow through the isolation. This proves that the isolation concept is properly working and well overdimensioned to guarantee a long lifetime.

Furthermore, to also test the complete gate driver circuit and the isolation transformer under real operating conditions, a 10 kV SiC-MOSFET-based half-bridge inverter has been designed as shown in Fig. 7. It consists of a PCB which incorporates the low-side and the high-side MOSFETs together with their respective gate driver and isolated power supply circuits. As can be seen, the isolation transformers are placed on the bottom side of the PCB and enable the construction of a highly compact half-bridge due to their small dimensions. As already mentioned, the silicone tube provides a 60 mm creepage distance to the primary-side driving circuit of the isolation transformer (not shown), which only consists of a *MAX13256* H-bridge IC, an adjustable clock generator IC, and two ceramic DC buffer capacitors.

To expose the isolation transformer to a very high stress, the half-bridge has been operated with a DC-link voltage of 7 kV and a switching frequency of 125 kHz for one hour. Thereby, an inductor has been used as load to enable ZVS and therewith to minimize the switching losses of the 10 kV SiC MOSFETs [22]. During this test, the CM current of the high-side isolation transformer has been measured. The corresponding circuit diagram and the according voltage and current waveforms during a rising voltage transition are shown in Fig. 8. It can be seen that a dv/dt of 82 kV/µs leads to a peak CM current of 300 mA. To obtain this peak current from the measured voltage slope, a coupling capacitance of 4.1 pF (which is 1.5 pF larger than the measured coupling capacitance of the isolation

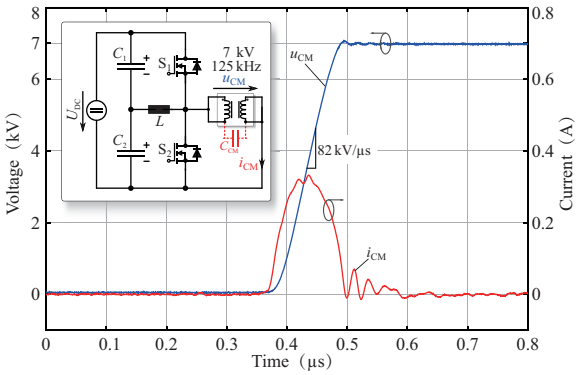

Fig. 8. Measured CM voltage u_{CM} across the isolation transformer together with the measured capacitive current i_{CM}.

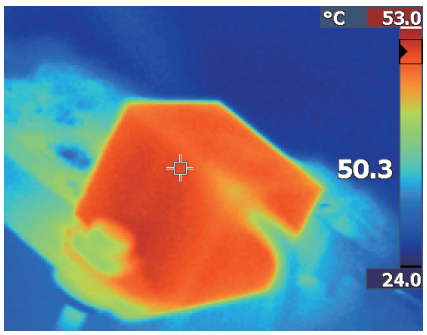

Fig. 9. Thermal image of the isolation transformer under operation with a 2 W load and a CM voltage stress of 7 kV, 125 kHz. The average steady state surface temperature reaches 50 °C under natural convection.

transformer) must be present. The additional capacitance can be explained by parasitic capacitances of the connection of the PCB to the isolation transformer and/or additional cable capacitances.

During the 7 kV, 125 kHz operation of the entire circuit with a load of 2 W, the steady-state surface temperature of the isolation transformer (cf. Fig. 9) reaches 50 °C (at an ambient temperature of 25 °C and for natural convection cooling), and as already shown by the thermal FEM simulation in Fig. 6(b), the hot spot temperature is estimated to be around 62 °C.

III. Ultrafast Overcurrent Protection (OCP)

In MV applications, it is highly recommended to implement an overcurrent and/or short circuit protection for the MV semiconductors due to the high voltages and the corresponding high energies in e.g. the DC-link capacitors, which could lead to serious damage of the hardware in case of a fault. Furthermore, MV SiC devices with blocking voltages of 10…15 kV are still very expensive and are up to now only available as prototype devices.

It is shown in [65] that single 10 kV SiC MOSFETs can survive approximately 8.5 µs under a full short circuit with 6 kV DC-link voltage. However, in [66], a clear relation between the degradation of the MOSFET-chip (i.e. increased $R_{DS,on}$) and the short circuit duration is apparent, since the degradation is an effect of the high temperature of the chip and its metallization

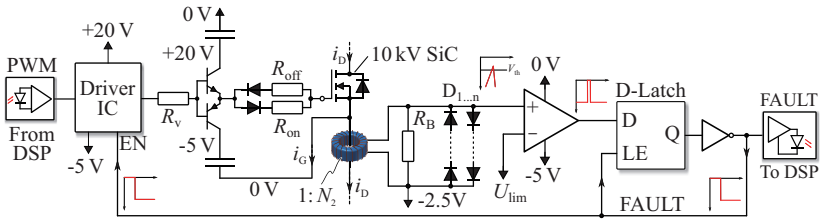

Fig. 10. Circuit diagram of the driver stage and the overcurrent protection. The drain current i_D of the MOSFET is measured via a 1 : N_2 = 1 : 30 air-gapped current transformer and the subsequent burden resistor R_B = 1 Ω. Once the threshold U_{lim} is exceeded, the comparator and consequently also the D-latch changes state and latches the FAULT state. This signal is fed back to the enable input EN of the driver IC (*UCC27531-Q1* from *TI*), leading to a turn-off of the 10 kV SiC MOSFET. The delay of the logic is approximately 22 ns. Furthermore, the FAULT signal is optically transmitted back to the supervisory control.

during a short circuit. Additionally, in the case of 10 kV, 100 A SiC MOSFET modules, a short circuit withstanding time of only 3.5 µs at 6 kV has been observed [67]. Therefore, the goal is to realize an ultrafast overcurrent protection (OCP) with a very short reaction time in order to keep the thermal stress on the 10 kV SiC MOSFET chips as low as possible.

In literature, two major types of faults are described, namely the hard switching fault (HSF), where a MOSFET turns on onto a short circuit, and the fault under load (FUL), where a short circuit occurs while the MOSFET is in on-state. In this case, however, the current and voltage slopes are mainly and significantly limited by the switching speed of the turning on MOSFET, whereas in MV applications, flashovers can occur (due to insulation failures of e.g. the silica gel in MV semiconductor modules or the insulation material e.g. in the transformer employed in a DC/DC converter) and show extremely fast voltage and current transients, which are much more critical to handle for an OCP. Therefore, the standard HSF and FUL tests are the only measure for the quality of an OCP circuit, since they do not test the worst case scenario, namely an arc flashover across one of the MOSFETs in a bridge-leg configuration while the complementary MOSFET is turned on. Therefore, the term flashover fault (FOF) is introduced and an FOF is applied to a 10 kV SiC MOSFET bridge-leg by using a gas discharge tube (GDT) of type *Bourns SA2-7200-CLT-STD* in the high-side position, which internally ignites a low-ohmic plasma (i.e. a solid short circuit) when the applied voltage exceeds its breakdown voltage, while the low-side switch is in on-state and has to clear the fault.

A. Functional Principle of the OCP

For the detection of a fault, the device current is measured by means of an air-gapped current transformer in the source path of the 10 kV SiC MOSFET as shown in Fig. 10. Thereby, the air gap avoids the saturation of the core material due to the DC current component and compared to e.g. a current measurement shunt, the current transformer provides galvanic isolation of the measurement signal and improves the immunity against CM distortions. In the following, the fundamental functionality of the OCP circuit is explained, assuming that the drain current can be measured with a sufficient accuracy with the 1 : 30 current transformer. The details on the design of the current transformer can be found in the Appendix.

In the configuration shown in Fig. 10, the current transformer is placed below the gate and source contacts of the driver stage, which ensures that only the drain current i_D is measured. The secondary-side of the current transformer is connected to a burden resistor R_B = 1 Ω and the entire circuit is powered from the 0 V/ −5 V rails. Since the drain current of the 10 kV SiC device can also be negative, one terminal of the current transformer is connected to a locally generated −2.5 V potential, allowing a voltage swing of ±2.5 V across R_B, which corresponds to a drain current of ±75 A. In case of a fault, where much higher currents can occur, the diodes $D_{1...n}$ start conducting and clamp the voltage across R_B in order to protect the input of the subsequent comparator from overvoltages. The advantage of diode strings compared to a single TVS or zener diode per direction is the steeper characteristic of pn diodes, i.e. the clamping voltage is less current dependent. The type and the number of serial diodes is selected such that a clamping voltage of 2.5 V results.

For the detection of an overcurrent, the voltage at the upper rail of R_B is compared to the threshold voltage U_{lim} = −2.5 V + 1 V = −1.5 V (for an overcurrent threshold of 30 A, R_B = 1 Ω and N_2 = 30) by an ultrafast comparator. Once the threshold is exceeded, the comparator sets its output to HIGH (0 V) and the subsequent D-latch changes state and latches its output state when LE is LOW (−5 V). This FAULT signal (cf. Fig. 10) is connected to the enable input EN of the gate driver IC *UCC27531-Q1* from *TI*), which then initiates a turn-off of the 10 kV SiC MOSFET. The delay caused by the logic ICs and the gate driver IC adds up to T_{react} ≈ 22 ns between the detection of the overcurrent and the reaction of the gate voltage. Since the gate driver IC does not provide a sufficiently high gate current (but undervoltage lockout, which is the reason to use an IC at all), a BJT totem-pole stage is used to provide a sufficiently high gate current. The gate resistors for turn-on and turn-off are R_{on} = 20 Ω and R_{off} = 10 Ω , respectively, according to [22]. Alternatively, a soft turn-off circuit could be implemented, which, in case of a fault, turns off the device with a larger gate resistor as it is done for IGBTs to limit the voltage overshoot. Furthermore, the FAULT signal is also transmitted back to the supervisory control via an optical fiber (30 ns delay) in order to turn-off all devices in the converter system in the case of an overcurrent in one of the 10 kV SiC devices. Accordingly, when a fault is detected, after 22 ns, the inner fault loop initiates the turn-off of the device which detected the overcurrent, and after approximately 100 ns, the gate voltages of all other 10 kV devices react. It should be noted that alternatively a direct

feedback path to the gate could be implemented for a further reduction of the reaction time.

B. Flashover Fault Simulation

Before the OCP is tested in hardware and has to prove that it is able to safely clear a HSF and an FOF at 7 kV DC-link voltage, a simulation is carried out in order to predict the behavior of the circuit under these extreme conditions. Fig. 11(a) shows the simulation model of the bridge-leg in the case of an FOF, where an ideal switch is located in the high-side MOSFET position and the low-side MOSFET is replaced by a simple equivalent circuit consisting of a voltage controlled current source, the nonlinear parasitic MOSFET capacitances, the antiparallel body diode, and the package inductances [20]. The current source is controlled by the internal gate voltage $u_{GS,int}$ across the gate-source capacitance C_{GS} via

$$i_{D,0} = g_m(u_{GS,int} - U_{th}), \tag{14}$$

where U_{th} is the threshold voltage of the MOSFET and g_m is its transconductance. In the simulation, the ideal switch is closed at $t = 0$ while the low-side MOSFET is already turned on, i.e., $u_{Driver} = 20$ V. Furthermore, it is assumed that the overcurrent protection will react 30 ns after the fault and will force the driver output voltage u_{Driver} to −5 V within another 15 ns.

Fig. 11(b) shows the simulated waveforms under these assumptions. Initially, the drain current i_D rises with a very high di/dt, which in turn induces a high positive voltage $u_{LS} \approx 140$ V across the source inductance L_S. The relatively large gate-source capacitance C_{GS} however keeps its voltage $u_{GS,int}$ constant and therefore, the external gate-source voltage u_{GS} closely follows the induced voltage u_{LS} with a 20 V offset, while the effect of the gate inductance L_G can be neglected in this case. Since also the driver voltage u_{Driver} is still clamped to 20 V, the difference of $u_{GS} - u_{Driver} \approx 140$ V peak is applied to the turn-off gate resistor $R_{off} = 10\ \Omega$, forcing a part of the MOSFET channel current through C_{GS} and leading to a negative gate current of $i_G = (u_{GS} - u_{Driver})/R_{off} = -14$ A peak (when the gate inductance L_G is neglected). The reader should note that the gate resistors and the diodes should be well dimensioned to withstand the high peak current. Consequently, C_{GS} is discharged (i.e. $u_{GS,int}$ decreases) and according to (14), the MOSFET channel current $i_{D,0}$ decreases again, as can be seen in the figure. Although the channel current decreases, the series inductances L_S, L_D, and L_σ try to keep the current constant and hence, a part of the drain current i_D commutates to the output capacitance C_{DS}, resulting in a rapid increase of the drain-source voltage u_{DS} and an inductive overshoot. At the same time, the drain current effectively decreases, and the complete process until this point takes place without any action from the gate driver and is therefore referenced as "self turn-off" of the MOSFET. However, at this point, the decreasing drain current leads to a positive gate current due to the negative induced voltage across L_S, such that the MOSFET partly turns on again. Now, the induced voltage is applied to $R_{on} = 20\ \Omega$, which is twice the value of R_{off} and therefore, the increase of the drain current is only small and the oscillation is damped. Furthermore, it is assumed that the OCP detects the overcurrent within 30 ns and switches the driver voltage u_{Driver} to −5 V, thereby actively turning off the remaining drain current. Depending on the application, a higher turn-on gate resistor might be selected to dampen the oscillation even more.

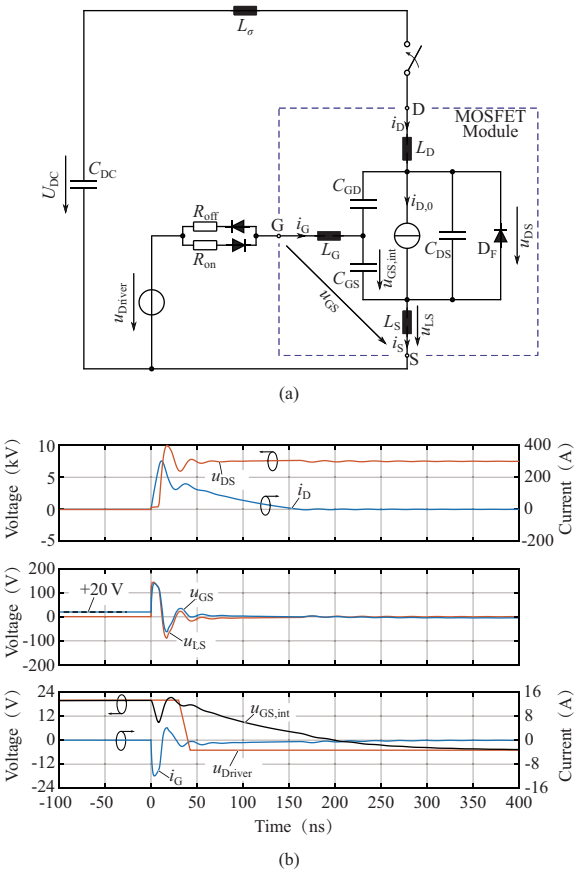

Fig. 11. (a) Schematic diagram of the MOSFET bridge-leg during a flashover fault (FOF), i.e., flashover across the high-side MOSFET during the on-state of the low-side MOSFET. For the simulation, the low-side MOSFET is replaced by a simple equivalent circuit consisting of a gate-source voltage controlled current source and the nonlinear MOSFET capacitances. (b) Simulated waveforms during a 7.6 kV FOF. The fault is cleared successfully and although the gate-source voltage u_{GS}, measured at the module terminals, reaches 140 V, the chip-internal gate-source voltage $u_{GS,int}$ is almost unaffected (voltage drop mostly occurring along the parasitic gate inductance and the gate resistor) and the MOSFET is not endangered.

As can be seen in Fig. 11(b), due to the self turn-off mechanism and the short reaction time, the OCP is able to clear the FOF within 200 ns, whereby a peak drain current of 320 A is reached. Furthermore, it can be noted that the chip-internal gate-source voltage u_{GS} barely exceeds 20 V and hence stays within the absolute maximum ratings, i.e., the MOSFET chip is not endangered.

C. Experimental Results

1) FOF Experiment

Since the results from the FOF simu-lation show that the OCP is able to successfully clear an FOF in theory, this situation is also tested in real hardware. Thereby, as shown in

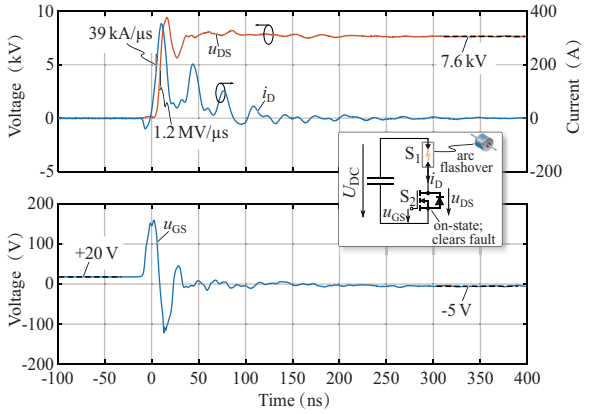

Fig. 12. Measured waveforms in the case of a flashover fault (FOF) for a DC-link voltage of 7.6 kV. S_2 is in the on-state while S_1 fails to short, e.g. due to an isolation breakdown, which is reproduced with a flashover in a gas discharge tube (GDT) of type *Bourns SA2-7200-CLT-STD*. The current rises with a slope of 39 kA/µs and reaches its peak of 350 A. Due to the self turn-off mechanism, the MOSFET turns itself off and the drain-source voltage rises to the DC-link level within 6 ns, i.e. an unprecedented dv/dt of 1.2 MV/µs. After the reaction delay of approximately 22 ns, the gate driver actively brings the gate voltage to −5 V and the fault is cleared within 150 ns.

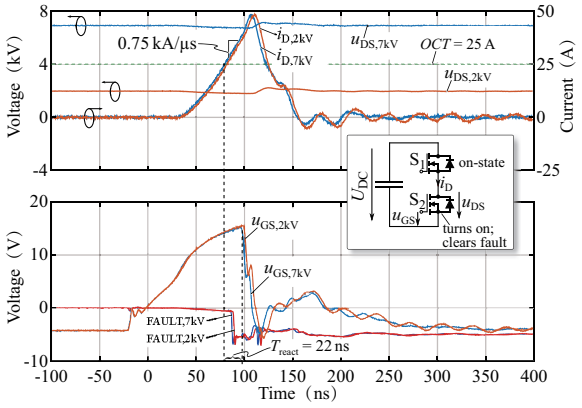

Fig. 13. Measured waveforms for a hard switching fault (HSF) for $U_{DC} = 2$ kV and $U_{DC} = 7$ kV. S_1 is in the on-state when S_2 turns on. 22 ns after drain current reaches the overcurrent threshold (OCT), the gate voltage reacts and S_2 is safely turned off within 150 ns. Almost independently of the DC-link voltage level, the current reaches a maximum of 48 A.

the schematic in Fig. 12, the low-side MOSFET is permanently turned on while the high-side MOSFET is substituted by a gas discharge tube (GDT) of type *Bourns SA2-7200-CLT-STD* and the DC-link voltage is increased until the GDT ignites. Fig. 12 shows the measured drain-source voltage u_{DS}, the gate-source voltage u_{GS}, and the drain current i_D during an FOF test with a 7.2 kV GDT, which ignited at 7.6 kV (due to tolerances). As can be seen, the waveforms are similar to the simulation, i.e., also in real hardware a self turn-off occurs. Thereby, the drain current reaches a value of 350 A and the drain-source voltage rises in 6 ns to the DC-link level with an unprecedented dv/dt of 1.2 MV/µs (which is close to the 100 MHz bandwidth limit of the used voltage probe). The OCP then actively clears the fault within 150 ns and the successful FOF test proves the proper functioning of the OCP under the most extreme conditions. Compared to the simulation, the measured waveforms show more oscillations in the drain current, which can be explained by the fact that the simulation model does not include all parasitics and nonlinear effects in the MOSFET. Furthermore, in the experiment, only the external gate-source voltage can be measured and reaches a value of 150 V peak. However, the simulation shows a very similar external gate-source voltage, which solely occurs due to the inductive voltage drop across the source inductance L_S, whereas the gate-source voltage directly on the MOSFET chip does not exceed 20 V during the FOF, which is therefore also assumed for the real FOF experiment.

If the 10 kV SiC module featured a Kelvin source contact, the MOSFET would not be subject to a self turn-off during an FOF, since the gate loop would be decoupled from the power loop. However, according to [66], the maximum short circuit current (in the case of a usual FUL or HSF) of similar 10 kV SiC MOSFETs from *Wolfspeed* is self-limited by the MOSFET channel to 270 A for a DC-link voltage of 6 kV and therefore, the presented OCP would also work for modules featuring a Kelvin source contact.

2) HSF Experiment

The schematic in Fig. 13 shows the situation for the HSF test, where the high-side MOSFET S_1 is in the on-state when the low-side MOSFET S_2 turns on. The measured waveforms of the drain current i_D, the drain-source voltage u_{DS}, the gate-source voltage u_{GS}, and the FAULT signal are shown for a HSF at 2 kV and 7 kV, respectively. With the increasing gate-source voltage, also the drain current increases and once it reaches the threshold (25 A in this case), after a short delay the internal FAULT signal, which is connected to the enable signal of the driver IC, changes state. The gate driver IC then switches its output to −5 V and the gate-source voltage decreases after the IC's propagation delay has passed. Almost independently of the DC-link voltage, a peak current of 48 A peak is reached and the OCP safely clears the HSF in less than 200 ns. The total reaction time from the point where the current threshold is reached until the gate voltage reacts is $T_{react} = 22$ ns in this case. It should be noted that a successful HSF experiment alone does not mean that the OCP can protect the switch comprehensively. Only in combination with a successful FOF experiment, it can be stated that the OCP is able to protect the device also in worst case fault situations.

IV. Conclusion

In this paper, a highly compact isolated gate driver for 10 kV SiC MOSFETs with ultrafast overcurrent protection is presented. A main challenge for medium-voltage (MV) gate drivers is the galvanic isolation of the gate driver power supply and the isolated low propagation delay signal transmission. In order to obtain a highly compact gate driver circuit, which could be integrated into future MV SiC modules, an encapsulated isolation transformer employed in a resonant converter topology is designed and constructed. Thereby, in contrast to classical transformers with both windings on the same

magnetic core, the primary winding and the secondary winding are wound on separate ferrite core halves, which are separated by a small gap that is filled with a silicone insulation material featuring a low dielectric dissipation factor and a high thermal conductivity to ensure a sufficient heat transport from the windings to the surface of the transformer. The dimensions of the realized transformer are 16 mm × 16 mm × 14 mm and the coupling capacitance is only 2.6 pF. The transformer isolation has been successfully tested for 1 hour with a 20 kV DC voltage and for one hour with a 7 kV, 125 kHz switching-node voltage, which proves the functionality of the designed MV isolation transformer.

Furthermore, in order to protect the 10 kV SiC devices from overcurrents and a possible destruction by short circuits, an ultrafast overcurrent protection (OCP) circuit is implemented. Thereby, the drain current of the device is measured via a gapped toroidal current transformer. The measured signal is subsequently compared to a predefined threshold by an ultrafast comparator whose output signal is latched in case of a fault and fed back to the enable input of the gate driver IC, which then initiates the turn-off of the 10 kV SiC device. The delay between the crossing of the overcurrent threshold and the reaction of the gate voltage is only ≈ 22 ns. Measurements prove that the realized OCP is also able to successfully clear a flashover fault (FOF) and a hard switching fault (HSF) at a DC-link voltage of 7 kV within less than 200 ns. Furthermore, during the FOF experiment, an unprecedented dv/dt of 1.2 MV/µs has been observed.

Acknowledgment

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Appendix
Design of the Current Transformer

For the measurement of the drain current of the 10 kV SiC MOSFETs, the current transformer has to be designed for a high bandwidth, such that fast overcurrent transients can be measured accurately. Furthermore, the current transformer should not add a significant signal delay to the protection circuit. Consequently, the leakage inductance and capacitance have to be kept small, which can be achieved by choosing a low number of secondary-side turns equidistantly wound on a toroidal ferrite core. As shown in Fig. 10, the secondary winding is connected to a burden resistor $R_B = 1\ \Omega$ where a current-proportional voltage is measured. If a voltage of 1 V across R_B is desired for an overcurrent threshold of $OCT = 30$ A, a turns ratio of $1 : N_2 = 1 : 30$ results, i.e. the number of secondary turns on the current transformer is $N_2 = 30$. To operate the ferrite core material in its linear region, the maximum magnetic AC flux density is set to $B_{max,AC} = 75$ mT and for an assumed rectangular drain current with 50% duty cycle, a minimum converter switching frequency of $f_{min} = 30$ kHz, a bottom value of 0 A, and an amplitude of $i_{d,max} = 30$ A, a core cross section of $A_m = 7.4\ mm^2$ is required. Therefore, a R10 × 6 × 4 ferrite core (N30 material) with a magnetic cross section area of 7.83 mm^2 is selected.

As the drain current of the switches is not a pure AC current but rather a superposition of an AC and a DC current, the current transformer has to be designed appropriately, such that the DC component does not lead to saturation of the magnetic core. Therefore, an air gap is inserted in the ferrite core. For limiting the magnetic DC flux density to $B_{max,DC} = 125$ mT, the required air gap length is

$$\delta = \frac{\mu_0 \cdot i_{D,DC}}{B_{max,DC}} = 150\mu m \tag{15}$$

for a maximum DC current component of $i_{D,DC} = 15$ A.

The air gap, however, causes the magnetizing inductance of the current transformer to drop significantly, which increases the AC magnetizing current. For the current transformer at hand, the peak magnetizing current for $f_{min} = 30$ kHz and 30 A, 50% duty cycle is 7% of the measured current value, which does not influence the detection of a HSF or an FOF due to the usually large resulting fault currents. For the sake of completeness, it should be noted that the current transformer represents a high-pass system (corner frequency $f_c = 17$ kHz) and is not able to measure DC currents, since the DC component only occurs as magnetizing current on the primary-side.

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