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Modeling the Output Impedance of a T-Type Power Converter

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Letters

Modeling the Output Impedance of a T-Type Power Converter

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***Abstract*—The impact of operating point dependent switching time delays on the output characteristic of a T-type half-bridge is investigated for dc–dc operation. It is found that a series connection of operating point dependent components, i.e., a differential resistance and a voltage source, can accurately reproduce the implications of these switching time delays on the response of the output current of the half-bridge to a step of the duty cycle. This letter details the calculation of these components and verifies the derived expressions by means of experimental results.**

***Index Terms*—Circuit modeling, control, delay effects, dynamic response, MOSFETs, resistance, stability.**

I. Introduction

In the course of the optimization of different control structures for a controllable ac voltage source (CVS), presented in [1], [2], measurements of the step response of a single phase of the output stage, depicted in Fig. 1(a), reveal an unexpected result: a slight change of the duty cycle, here from 50% to 56% at $V_{\mathrm{dc}} = 700\,\mathrm{V}$ and $t = 0$ in Fig. 1(b) and (c), leads to a measured inductor current which experiences a much stronger damping than the simulated current, even though the simulation considers the MOSFET's channel resistances ($40\,\mathrm{m\Omega}$ for each MOSFET) and a constant loss resistance of $R_L = 50\,\mathrm{m\Omega}$ in series to L. Since the results of the optimization of the control structures of [1], [2] are only meaningful if the dynamic model of the power stage is known and verified, a thorough investigation of this discrepancy has been conducted.

The examination of different measurement results and the inspection of corresponding simulation results reveal that the difference between the waveforms shown in Fig. 1(b) and (c) originates from the switches' time delays. The observed effect is related to the impact of time delays on the output voltage that has been intensively investigated for inverter topologies [3]–[11]. Early investigations determine the error of the output voltage if only the dead time is considered and disregard the additional turn-on and turn-off delays [3], [4]. Subsequent publications, beginning with [5] and [6], include the contributions of turn-on and turn-off delays and the implications of the current ripple on the effective time delays [7]–[9]. The voltage drop at the output of the inverter is found to depend on the output current, e.g., in [10]. Furthermore, for inverter operation and in the d-q-frame, a corresponding effective average resistance is determined in [11]. The existing literature focuses on inverter applications, dead time compensation, and quality improvement of the output voltage rather than the investigation of the implications of delay times on the dynamic model at a particular operating point and dc–dc mode of operation.

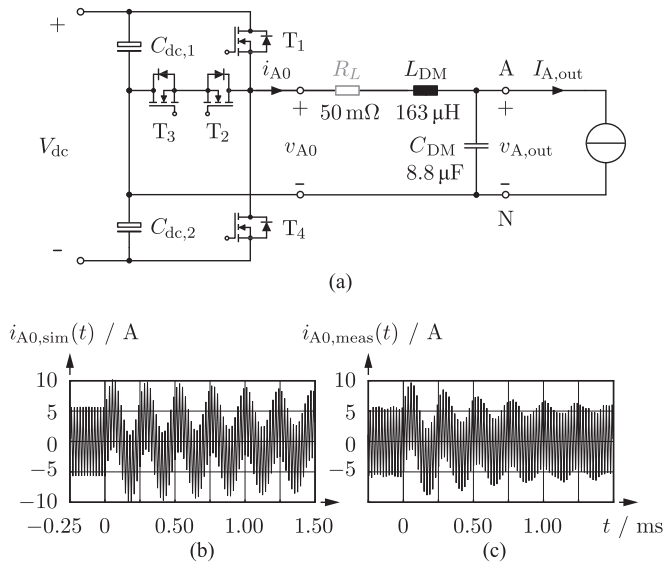

Fig. 1. (a) Phase A of the considered CVS: T-type half-bridge circuit and single-stage output filter. (b), (c) Initially simulated and measured output currents for $I_{\mathrm{A,out}} = 0$, $V_{\mathrm{dc}} = 700\,V$, and $T_{\mathrm{s}} = 20.8\,\mu\mathrm{s}$ if the duty cycle immediately changes from 50% to 56%.

This letter revisits the measurement of switching time delays in Section II and employs the related and known deviations between theoretical and practical values of the average output voltages in order to identify the output-side dynamic properties of a T-type half-bridge circuit in Section III in presence of dc–dc operation. The resulting model contains operating-point dependent components, i.e., voltage source and differential resistance, which, in Section IV, are shown to accurately reproduce the measured waveforms.

II. Current Dependent Time Delays

The time delays are measured on the hardware realization of one phase of the considered CVS, depicted in Fig. 1(a), however, with the output filter being omitted ($L_{\mathrm{DM}} \to 0$, $C_{\mathrm{DM}} \to 0$) and with the current source being replaced by an inductor with sufficiently large inductance, such that i_{A0} remains approximately constant during the total duration of the measured switching operation. Fig. 2(a) depicts the gate signals that are used to measure

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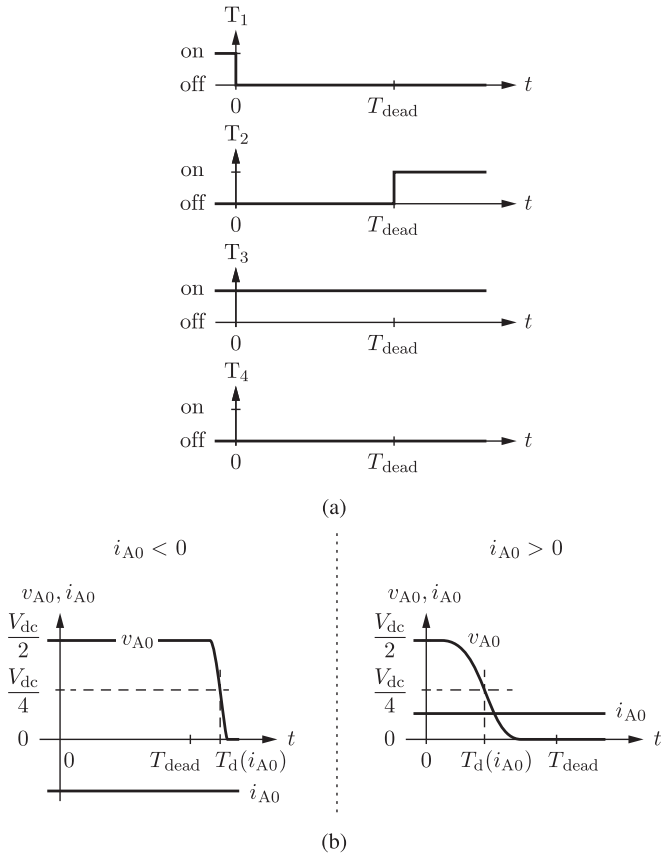

Fig. 2. Measurement of the time delay introduced by the power semiconductor switches of the T-type half-bridge depicted in Fig. 1(a): (a) gate signals used to determine T_d for positive output voltages and definition of $t = 0$, (b) illustration of how the time delay characteristic depicted in Fig. 3 has been measured.

the time delay, T_d, for positive output voltages (T_3 remains in the on-state and T_4 in the off-state) and Fig. 2(b) illustrates the method for obtaining T_d. The preceding pulse sequence, used to generate the desired output current for a given output inductor, is not shown. Please note that this letter only considers positive output voltages of the T-type half-bridge $v_{\mathrm{A0}}(t) > 0$. Similar results are obtained for negative output voltages, due to the symmetry of the circuit.

According to Fig. 2(a) the microcontroller turns OFF T_1 at $t = 0$ and turns ON T_2 at $t = T_\mathrm{dead}$. This switching operation causes the output voltage, v_{A0}, to change from $V_\mathrm{dc}/2$ to zero. The actual instant when this change happens, however, depends on the value of the output current i_{A0} cf., Fig. 2(b).

1) For $i_{\mathrm{A0}} < 0$, the body diode of T_1 conducts during the dead time interval $0 < t < T_\mathrm{dead}$, and, thus, the change of the output voltage happens after the turn-on of T_2.
2) For $i_{\mathrm{A0}} > 0$, the body diode of T_1 blocks at $t > 0$, the output current charges or discharges the parasitic effective output capacitances of the power semiconductors involved in the switching process, and the change of the output voltage can take place immediately after the turn-off of T_1.

The time delay T_d is measured from the instant when the microcontroller turns OFF T_1 until the time when the output voltage reaches $V_\mathrm{dc}/4$, which is half of the final output voltage. This procedure allows for a simplified measurement of T_d; it, however, accepts minor errors at low positive output currents, i.e., at output currents that are too small to completely charge or discharge the MOSFETs' effective output capacitances during the dead time. A refined method for a more accurate measurement of T_d is based on the identification of equal voltage-time-areas of measured and idealized switching transients of v_{A0} and is illustrated in Fig. 8 in [8].

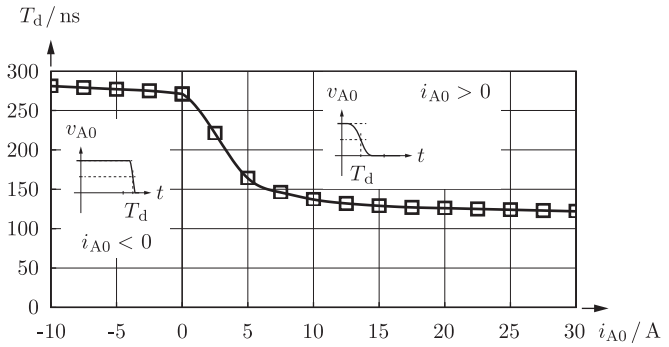

Fig. 3. Time delays for different output currents, i_{A0}, and constant dead time, $T_\mathrm{dead} = 180\,\mathrm{ns}$, measured at an ambient temperature of $25\,^\circ\mathrm{C}$. The rectangles denote actual measurement results.

Fig. 3 depicts the measurement results obtained for $T_\mathrm{dead} = 180\,\mathrm{ns}$, $V_\mathrm{dc} = 700\,\mathrm{V}$, and at an ambient temperature of $25\,^\circ\mathrm{C}$. The time delay decreases for increasing output current, since the discharging and charging of the parasitic effective output capacitances proceeds faster for higher currents, and reaches values of less than $130\,\mathrm{ns}$ for $i_{\mathrm{A0}} > 15\,\mathrm{A}$. The negative gradient of $T_\mathrm{d}(i_{\mathrm{A0}})$, $\mathrm{d}T_\mathrm{d}(i_{\mathrm{A0}})/\mathrm{d}i_{\mathrm{A0}} < 0$ is even present for negative output currents, since the turn-on delay slightly increases for increasing MOSFET turn-on currents, i.e., for decreasing values of i_{A0}. The maximum time delay of $280\,\mathrm{ns}$, thus, occurs for the minimum negative output current of $-10\,\mathrm{A}$.

III. Improved Dynamic Model of the Power Stage

During normal operation, each T-type half-bridge of the CVS generates a rectangular output voltage with a certain duty cycle. Without time delays of the switching operations, the relation between duty cycle and the theoretically present output voltage of, for example, phase A is given with

$$D^*_{\mathrm{A0}}(kT_\mathrm{s}) = \frac{\langle v^*_{\mathrm{A0}}(kT_\mathrm{s})\rangle_{T_\mathrm{s}}}{V_\mathrm{dc}/2},\ k \in \mathbb{Z} \tag{1}$$

where $\langle x(t)\rangle_{T_\mathrm{s}}$ denotes the average of $x(t)$ over one switching period $T_\mathrm{s} = 1/f_\mathrm{s}$. In a practical set-up, however, the current dependent time delays of the switching operations cause a difference between the theoretically and the actually present duty cycles D^*_{A0} and D_{A0}

$$D_{\mathrm{A0}} = D^*_{\mathrm{A0}} + D_{\mathrm{A0,d}} \tag{2}$$

with

$$D_{\mathrm{A0,d}} = \frac{-T_{\mathrm{d}\uparrow}(i_{\mathrm{A0,min}}) + T_{\mathrm{d}\downarrow}(i_{\mathrm{A0,max}})}{T_\mathrm{s}} \tag{3}$$

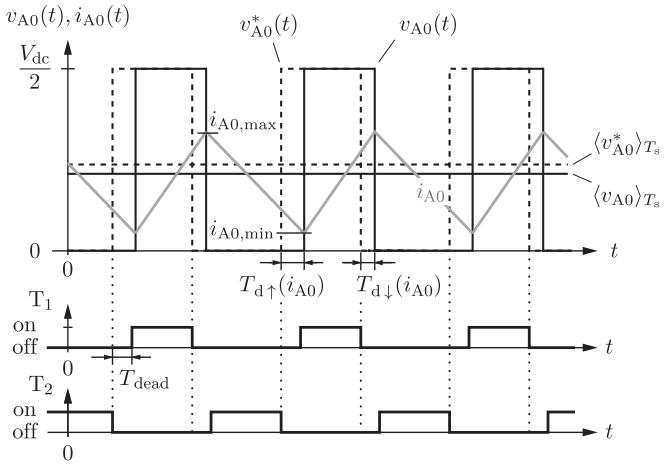

Fig. 4. Qualitative representation of effective (gray curve) and ideal assumed (dashed black curve) half-bridge output voltage v_{A0} for a positive output current i_{A0} and corresponding gate signals (T_3 and T_4 remain in the on- and off-states, respectively; the delay times have been exaggerated for the purpose of a better illustration).

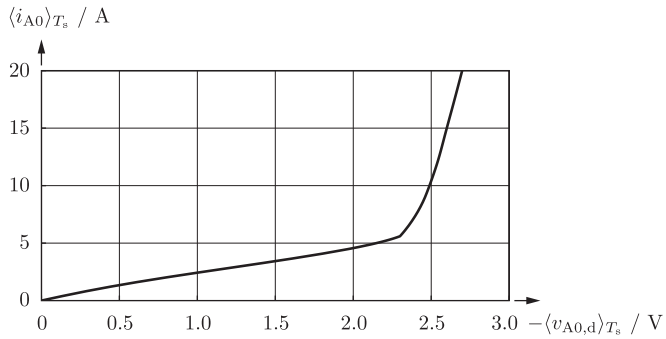

Fig. 5. Output current–voltage drop characteristic of the considered T-type half-bridge, determined with (7) for the time delay of Fig. 3, $\Delta I = 11.2\,\mathrm{A}$, $V_{dc} = 700\,\mathrm{V}$, and $T_s = 20.8\,\mu\mathrm{s}$.

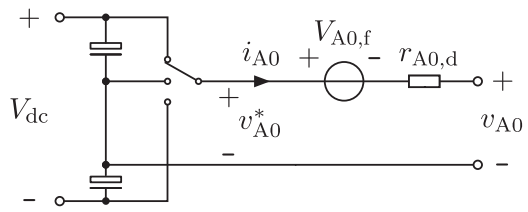

Fig. 6. Linearized converter network: $r_{A0,d}$ and $V_{A0,f}$ are valid for dc–dc operation at a dedicated operating point and model the implications of the current dependent delay times (during switching) on the output voltage.

where $T_{d\uparrow}(i_{A0,min})$ and $T_{d\downarrow}(i_{A0,max})$ denote the time delays in the events of rising and falling edges of $v_{A0}(t)$, cf., Fig. 4 and [7]. $T_{d\downarrow}(i_{A0,max})$ is directly obtained from the time delay function plotted in Fig. 3

$$T_{d\downarrow}(i_{A0,max}) = T_d(i_{A0,max}). \tag{4}$$

Since the considered hardware prototype realizes all four switches in Fig. 1(a) with same MOSFET devices (SiC-MOSFETs with a blocking voltage of 1.2 kV), similar time delays are expected for the complementary switching operation

$$T_{d\uparrow}(i_{A0,min}) = T_d(-i_{A0,min}). \tag{5}$$

Expression (5) evaluates T_d at $-i_{A0,min}$, in order to take the altered sequence of turning the MOSFETs OFF and ON into account: different to Fig. 2(a), T_2 is first turned OFF and, after the dead time, T_1 is turned ON in the event of a rising edge of v_{A0}.

The difference between D^*_{A0} and D_{A0} leads to an average output voltage that deviates from the theoretically expected value

$$\langle v_{A0}\rangle_{T_s} = \langle v^*_{A0}\rangle_{T_s} + \langle v_{A0,d}\rangle_{T_s}. \tag{6}$$

The voltage error that occurs during each switching period $\langle v_{A0,d}\rangle_{T_s}$ can be calculated with (3)

$$\langle v_{A0,d}\rangle_{T_s} = D_{A0,d}\frac{V_{dc}}{2} = \frac{V_{dc}}{2}\frac{[-T_{d\uparrow}(i_{A0,min}) + T_{d\downarrow}(i_{A0,max})]}{T_s} \tag{7}$$

and requires the values of $i_{A0,min}$ and $i_{A0,max}$. In this letter, the minimum and maximum inductor currents are determined based on the peak-to-peak current ripple ΔI, which is considered to be constant during the investigated small-signal transient

$$i_{A0,min} = \langle i_{A0}\rangle_{T_s} - \frac{\Delta I}{2} \text{ and } i_{A0,max} = \langle i_{A0}\rangle_{T_s} + \frac{\Delta I}{2}. \tag{8}$$

The results obtained from (7) are in accordance to the results obtained with the expressions obtained in [9]. However, [9], evaluates the time delays based on analytical approximations and this work employs measured time delays to calculate $\langle v_{A0,d}\rangle_{T_s}$.

Fig. 5 depicts the result of (7), evaluated for the time delays depicted in Fig. 3 and for $\Delta I = 11.2\,\mathrm{A}$. The authors decided to depict $i_{A0}(-\langle v_{A0,d}\rangle)$ instead of $\langle v_{A0,d}(i_{A0})\rangle$ in order to unveil the characteristic of a (nonlinear) internal resistance of a non-ideal voltage source in Fig. 5. At a dedicated operating point this nonlinear resistance can be linearized with a series connection of differential resistance $r_{A0,d}$ and a forward voltage at zero current $V_{A0,f}$

$$r_{A0,d} = \frac{\mathrm{d}\langle -v_{A0,d}\rangle}{\mathrm{d}\langle i_{A0}\rangle} = \frac{V_{dc}}{2}\frac{1}{T_s}\left[\frac{\mathrm{d}T_{d\uparrow}(i_{A0,min})}{\mathrm{d}\langle i_{A0}\rangle} - \frac{\mathrm{d}T_{d\downarrow}(i_{A0,max})}{\mathrm{d}\langle i_{A0}\rangle}\right] \tag{9}$$

$$V_{A0,f} = \langle -v_{A0,d}\rangle - \langle i_{A0}\rangle\, r_{A0,d}. \tag{10}$$

Fig. 6 depicts the corresponding converter model.

It is to be noted that this equivalent circuit model is lossless; the physical explanation is that the energy absorbed by this resistor is not converted to heat but transferred back to the dc-link capacitors. The electrical powers calculated for $V_{A0,f}$ and $r_{A0,d}$ do not increase the total losses and do not decrease the converter's efficiency provided that the process of transferring energy back to the dc-link capacitors has a negligible impact on the losses and the dc-link voltage. Furthermore, the model of Fig. 6 is obtained by means of averaging and is intended for use at frequencies well below the switching frequency. The implications of a transient change of the dc-link voltage on the output current are neglected.

TABLE I
OPERATING POINTS SELECTED FOR THE EXPERIMENTAL VERIFICATION AND CORRESPONDING PARAMETERS $V_{\mathrm{A0,F}}$ AND $r_{\mathrm{A0,D}}$ OF THE CONVERTER MODEL DEPICTED IN FIG. 6 (CALCULATED FOR $\Delta I = 11.2\,\mathrm{A}$, $V_{\mathrm{DC}} = 700\,\mathrm{V}$, $T_{\mathrm{S}} = 20.8\,\mu\mathrm{s}$, $T_{\mathrm{DEAD}} = 180\,\mathrm{ns}$, AND THE CURRENT DEPENDENT TIME DELAY CHARACTERISTIC OF FIG. 3)

Op. pt.	D (before and after step)	$I_{\mathbf{A0}}$	$V_{\mathbf{A0,f}}$	$r_{\mathbf{A0,d}}$
1	$50\% \rightarrow 55.7\%$	0	0	$340\,\mathrm{m\Omega}$
2	$50\% \rightarrow 55.7\%$	2 A	$-0.15\,\mathrm{V}$	$470\,\mathrm{m\Omega}$
3	$50\% \rightarrow 55.7\%$	5 A	$0.61\,\mathrm{V}$	$310\,\mathrm{m\Omega}$
4	$50\% \rightarrow 55.7\%$	10 A	2.2 V	$27\,\mathrm{m\Omega}$

IV. EXPERIMENTAL VERIFICATION

The converter prototype presented in [12], with only a single-stage output filter according to Fig. 1(a), is used to verify the model derived in Section III at the four operating points listed in Table I. The employed converter prototype is operated with a switching frequency of $48\,\mathrm{kHz}$ and a dc supply voltage V_{dc} of $700\,\mathrm{V}$. The current source depicted in Fig. 1(a) is realized with the series connection of a $100\,\mathrm{mH}$ inductor and a suitable load resistor (depending on the inspected operating point). For all experiments the power hardware is operated in open loop and the duty cycle changes immediately from 50% to 55.7% at the reference time $t = 0$. This change of the duty cycle corresponds to a change of the average output voltage from 175 to 195 V. Table I also lists the parameters $V_{\mathrm{A0,f}}$ and $r_{\mathrm{A0,d}}$ determined for the corresponding operating points, using the time delay characteristic depicted in Fig. 3. According to these results, elevated values of $r_{\mathrm{A0,d}}$ result at low output currents. Thus, the oscillations in the inductor currents, triggered by the immediate change of the duty cycle, are expected to experience more effective attenuations at operating points 1–3 than at operating point 4.

Fig. 7 compares the measured output currents to calculated output currents. In Fig. 7(b)–(e) the measured inductor currents are post-processed with a moving average filter in order to facilitate a direct comparison to the analytical results calculated with the averaged model network depicted in Fig. 8, which, besides $V_{\mathrm{A0,f}}$ and $r_{\mathrm{A0,d}}$ listed in Table I, also considers the copper resistance of the inductor coil, $R_L = 50\,\mathrm{m\Omega}$, and summarizes the on-state resistances of the relevant power semiconductor switches in the effective loss resistance $R_{\mathrm{T,eff}}$. This effective loss resistance is determined based on the conduction losses and for the CVS being operated with positive output voltage $v_{\mathrm{A0}}(t) \geq 0$

$$P_{\mathrm{cond}} = R_{\mathrm{DS,on,T_1}}\, D I_{\mathrm{A0,rms}}^2 + (R_{\mathrm{DS,on,T_2}} + R_{\mathrm{DS,on,T_3}})\, (1-D) I_{\mathrm{A0,rms}}^2 = R_{\mathrm{T,eff}} I_{\mathrm{A0,rms}}^2 \tag{11}$$

and is evaluated for $D = 50\%$ and $R_{\mathrm{DS,on,T_1}} = R_{\mathrm{DS,on,T_2}} = R_{\mathrm{DS,on,T_3}} = 40\,\mathrm{m\Omega}$.

The measured and the calculated waveforms depicted in Fig. 7 match very well. Increased attenuation can be observed in Fig. 7(a)–(d), due to comparably great values of $r_{\mathrm{A0,d}}$. Fig. 7(e) presents the result for $I_{\mathrm{A,out}} = 10\,\mathrm{A}$ where a low value of $r_{\mathrm{A0,d}}$ ($= 28\,\mathrm{m\Omega}$) is present and, accordingly, the oscillation of the inductor current experiences less attenuation.

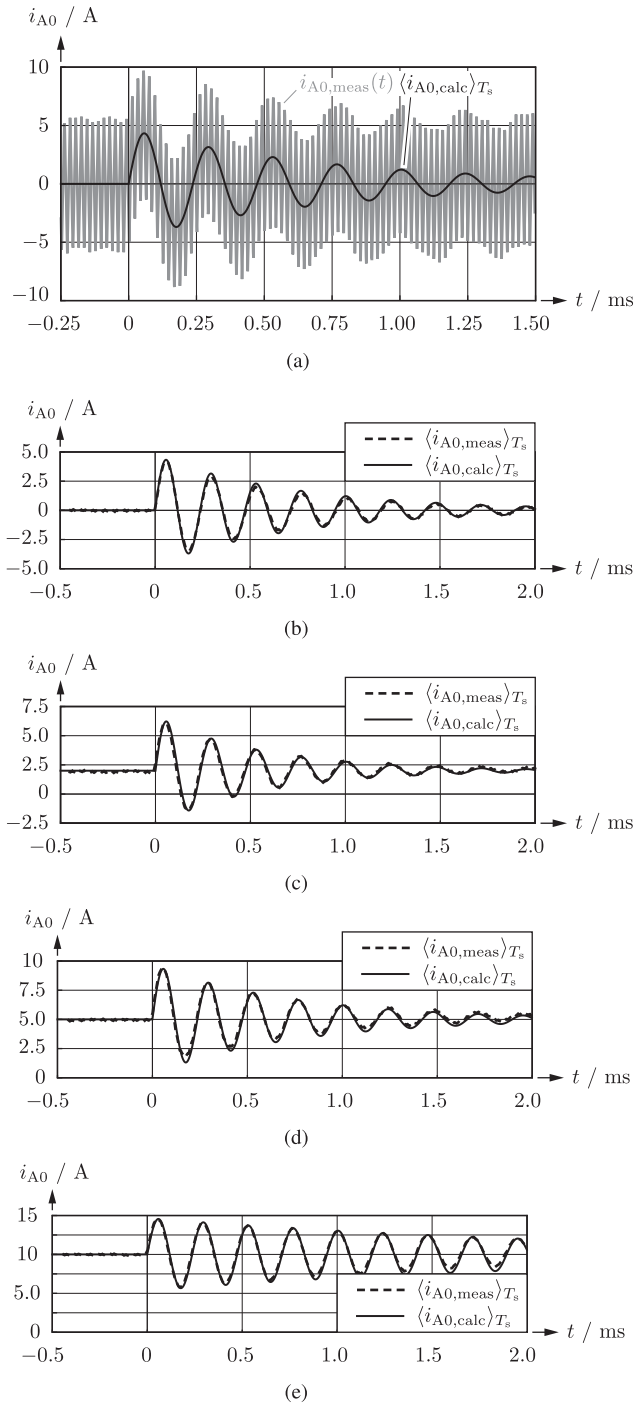

Fig. 7. Comparison of measured inductor currents [post-processed by means of a moving average (MA) filter in Fig. (b)–(e); the notch in the MA filter's frequency response effectively eliminates the ripple] and inductor currents calculated with the network of Fig. 8 for the operating points listed in Table I: (a) and (b) $I_{\mathrm{A,out}} = 0$ (c) $I_{\mathrm{A,out}} = 2\,\mathrm{A}$ (d) $I_{\mathrm{A,out}} = 5\,\mathrm{A}$ and (e) $I_{\mathrm{A,out}} = 10\,\mathrm{A}$.

The presented model facilitates in-depth knowledge on the effective damping of the output filter, which, for example, can be utilized in the context of controller design [2]. For this reason, and in order to assess the achieved accuracy of the proposed model, Table II compares estimated (from measurement and simulation results) to calculated damping coefficients, ζ, of

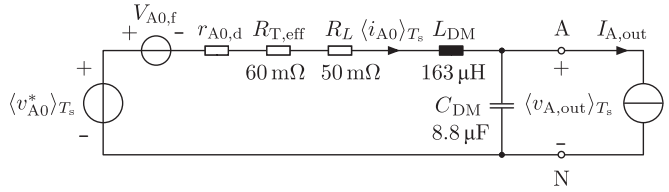

Fig. 8. Averaged model network used to calculate the transient response depicted in Fig. 7.

TABLE II
DAMPING COEFFICIENTS OF SECOND-ORDER TRANSFER FUNCTIONS DETERMINED FOR MEASURED, SIMULATED, AND CALCULATED CURRENT STEP RESPONSES AT THE OPERATING POINTS LISTED IN TABLE I (RELATIVE ERRORS, WITH RESPECT TO THE CALCULATED RESULTS, IN PARENTHESIS)

Op. pt.	ζ_{meas} (e_{meas})	ζ_{sim} (e_{sim})	ζ_{calc}
1	54.6×10^{-3} (5%)	62.6×10^{-3} (20%)	52.1×10^{-3}
2	65.5×10^{-3} (-4%)	67.2×10^{-3} (1%)	68.2×10^{-3}
3	53.1×10^{-3} (8%)	42.1×10^{-3} (-13%)	48.8×10^{-3}
4	18.8×10^{-3} (17%)	16.2×10^{-3} (0.7%)	16.0×10^{-3}

a second-order transfer function, $G(s) = g/[1 + 2\zeta(s/\omega_0) + (s/\omega_0)^2]$ (gain g, resonance frequency ω_0, and damping ζ). In case of measurements and simulations the parameters of this transfer function have been fitted to the step responses of the filtered inductor currents, cf., Fig. 7(b)–(e), by means of least mean square optimization (due to the weak damping the resonance frequency is almost equal to the frequencies of the oscillations seen in the step responses). For comparison reasons, the listed relative errors are determined with respect to the calculation results and are within -13% and $+20\%$, which, in view of ζ being relatively sensitive to the considered operating point, confirms a good matching between measured, simulated, and calculated results.[1] Further operating points have been assessed by means of simulation, for a reduced duty cycle step of 1%. Table III summarizes the corresponding results.

According to the results listed in Tables II and III $\zeta \in \left[15.5 \times 10^{-3}, 121 \times 10^{-3}\right]$ applies for the considered operating points. The lower boundary of this interval is, thus, found to be close to the minimum damping defined by the parasitic resistances of the output stage and the filter inductor, $\zeta_{min} = 10.5 \times 10^{-3}$. The results, furthermore, reveal that the value of ζ depends on the average output current, I_{A0}, and the duty cycle, D, due to its impact on $i_{A0,min}$ and $i_{A0,max}$. In accordance to (9), increased values of ζ are observed for operating points where increased gradients $\mathrm{d}T_{d\uparrow}(i_{A0,min})/\mathrm{d}\langle i_{A0}\rangle$ and / or $-\mathrm{d}T_{d\downarrow}(i_{A0,max})/\mathrm{d}\langle i_{A0}\rangle$ occur, which is particularly the case for operating points with I_{A0} equal to 0 or 2 A. In case of large-signal excitations a circuit simulator may be preferred, since the inductor current (average and ripple values) experiences great changes in the course of the excited oscillation, rendering the small-signal approximation (9) inaccurate.

[1]The employed circuit simulation models each power semiconductor with a series connection of an ideal switch and an (on-state) resistances of $40\,\mathrm{m}\Omega$ and delays the switching event by the delay time determined with the time delay function of Fig. 3.

TABLE III
COMPARISON OF DAMPING COEFFICIENTS ζ OF SIMULATED AND CALCULATED CURRENT STEP RESPONSES AT FURTHER OPERATING POINTS (REL. ERRORS, WITH RESPECT TO THE CALCULATED RESULTS, ARE GIVEN IN PARENTHESIS)

D	I_{A0}	$\zeta_{sim}(e_{sim})$	ζ_{calc}
$12.5\% \rightarrow 13.5\%$	0	121×10^{-3} (4%)	116×10^{-3}
$12.5\% \rightarrow 13.5\%$	2 A	87.8×10^{-3} (7%)	82.0×10^{-3}
$12.5\% \rightarrow 13.5\%$	5 A	24.6×10^{-3} (3%)	23.8×10^{-3}
$12.5\% \rightarrow 13.5\%$	10 A	20.0×10^{-3} (5%)	19.0×10^{-3}
$25\% \rightarrow 26\%$	0	103×10^{-3} (4%)	98.7×10^{-3}
$25\% \rightarrow 26\%$	2 A	79.9×10^{-3} (5%)	76.4×10^{-3}
$25\% \rightarrow 26\%$	5 A	25.0×10^{-3} (2%)	24.5×10^{-3}
$25\% \rightarrow 26\%$	10 A	17.7×10^{-3} (-0.6%)	17.8×10^{-3}
$50\% \rightarrow 51\%$	0	55.3×10^{-3} (6%)	52.1×10^{-3}
$50\% \rightarrow 51\%$	2 A	71.0×10^{-3} (4%)	68.2×10^{-3}
$50\% \rightarrow 51\%$	5 A	45.0×10^{-3} (-8%)	48.8×10^{-3}
$50\% \rightarrow 51\%$	10 A	15.5×10^{-3} (-3%)	16.0×10^{-3}

V. CONCLUSION

This letter derives a dynamic model for the T-type half-bridge circuit if dc–dc operation applies and if the implications of a transient change of the dc-link voltage on the output current can be neglected. Detailed investigations reveal that switching time delays, which depend on the instantaneous output currents at the switching operations, lead to a current dependent output voltage characteristic of the explored half-bridge circuit. The corresponding converter model developed in this work, thus, considers operating point dependent components, i.e., a constant forward voltage source and a differential resistance, at the output port of the half-bridge circuit. Due to the modeled differential resistance, a weakly dampened *L–C* output filter may, in the event of a transient change of the duty cycle the half-bridge circuit is operated with, provide a damping that is considerably greater than the damping that would be expected by reason of the inductor's and the power semiconductors' copper and conduction losses. The computed transient voltage and current waveforms, determined with the forward voltages and differential resistances calculated according to this work, are successfully verified by means of experimental results.

The presented dynamic model features the simple and accurate modeling of each T-type half-bridge circuit of the investigated CVS and can be used to improve the accuracy of the results obtained in the context of controller optimization, e.g., according to [1] and [2]. The investigation of different operating points reveals a great dependence of the damping coefficients of corresponding second-order transfer functions on the considered operating point. The presented model predicts [and the experimental result obtained at operating point 4, cf., Fig. 7(e), confirms] the existence of operating points with low damping, close to the minimum damping by reason of parasitic resistances, which typically denotes the worst-case scenario that is to be considered for the controller design.

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