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Ultra-High-Bandwidth Power Amplifiers: A Technology Overview and Future Prospects

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ABSTRACT Testing of power electronic converters can advantageously be carried out in power-hardware-in-the-loop (P-HIL) environments that emulate the behavior of power grids, electric motors, etc. The interface between the model and the device under test requires a power amplifier whose bandwidth ultimately limits the accuracy of the emulation. Hence, there is a need for general-purpose AC power amplifiers with ultra-high power bandwidth. This paper first provides a comprehensive review of amplifier concepts proposed over the past decades, i.e., linear power amplifiers, switch-mode amplifiers, including advanced variants such as multilevel (parallel-interleaving) and multicell (series-interleaving) topologies, as well as hybrid approaches that, e.g., combine analog and switch-mode stages. Based on this review, the two key concepts (parallel-interleaving of bridge-legs and cascading of converter cells) that facilitate high efficiency and ultra-high power bandwidth are identified and discussed, covering also suitable isolated mains interfaces and control considerations. Finally, we present a three-phase amplifier system that uses six cascaded converter cells per phase to realize an effective switching frequency of 3.6 MHz. The prototype thus achieves a measured power bandwidth of 100 kHz at the nominal phase output voltage of 230 V rms, and an output power of up to 10 kW per phase.

INDEX TERMS Power-hardware-in-the-loop (P-HIL), grid emulation, motor emulation, power amplifier topologies, switch-mode power amplifier, ultra-high-bandwidth power amplifier.

I. INTRODUCTION

Power amplifiers are a key component of power-hardware-in-the-loop (P-HIL) test environments, where they act as interfaces between a virtual system model (e.g., of a power grid or of a load) and a device under test (DUT, e.g., an inverter stage) [1]. A typical example is the emulation of power grids, including transient phenomena and disturbances (e.g., unbalanced voltages, voltage dips, harmonics) [2]–[4], and possibly also the grid impedance characteristics [5], [6], to facilitate comprehensive testing of grid-connected converters such as PFC rectifiers or PV inverters. The authors of [7] provide an up-to-date overview on grid-emulation concepts. Similarly, multi-area power system dynamics can be investigated using test benches with multiple grid and load emulators [8]–[11]. The emulation of electrical motors is another important field where P-HIL testing can advantageously enable flexible and fast analyses of motor drive inverter systems [12]–[17], whereby various coupling networks between amplifier and DUT inverter can be employed [18]. Considering, e.g., automotive drive trains, also the emulation of batteries [19] is of interest. Further applications for power amplifiers include injecting test signals into electric systems that can be characterized by their frequency-dependent impedance, e.g., impedance spectroscopy of batteries [20] and measurements of the grid impedance to accurately assess the control-loop stability of grid-connected converters [21]. Finally, gradient amplifiers for magnetic-resonance imaging (MRI) systems share similar requirements of high power, highly dynamic voltage adaption, and bandwidth [22], [23].

In general, the accuracy of emulated phenomena such as grid transients or slot effects in electric motors is ultimately limited by the bandwidth of the power amplifier. Also, as the switching frequencies of DUTs increase, e.g., due to the spread of wide-bandgap (WBG) power semiconductors, so must the bandwidths of amplifiers used in P-HIL

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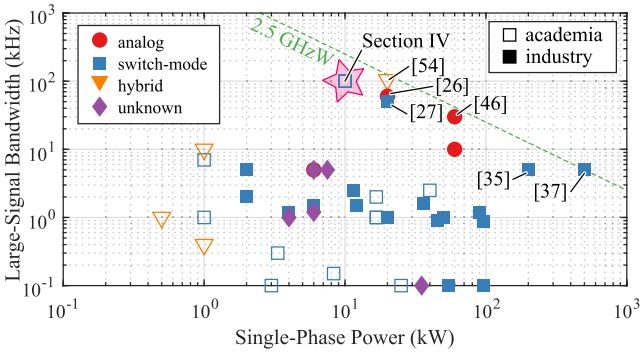

FIGURE 1. Large-signal bandwidth (maximum output frequency at nominal voltage) vs. single-phase power (of a single unit, i.e., without paralleling of multiple units) of typical AC power amplifier systems that can generate a single-phase output rms voltage of at least 230 V, as reported in literature by industry [26]–[46] and academia [12]–[14], [38], [47]–[55]. The category "unknown" applies to industry systems of which the topology could not be determined from publicly available information. The systems closest to the indicated (empirical) performance boundary as well as the ultra-high power bandwidth (UH-PBW) amplifier system proposed in this work (see **Section IV**) are highlighted.

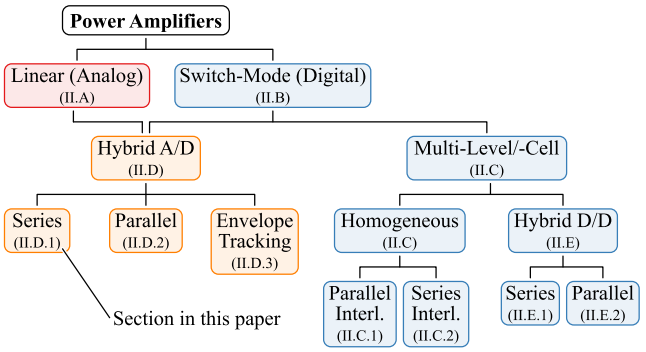

FIGURE 2. Classification of power amplifier realization options as used in Section II; small identifiers refer to the corresponding subsections; the color coding corresponds to that used in Fig. 1.

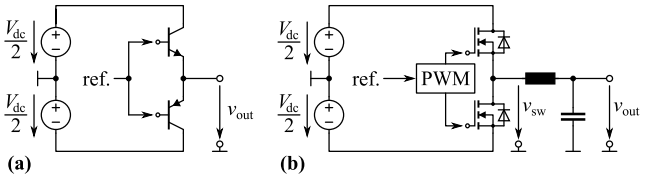

FIGURE 3. Basic amplifiers with controlled output voltage. (a) Linear (analog) class B amplifier. (b) Digital (switch-mode) two-level amplifier with low-pass output filter to remove switching harmonics (exemplary single-stage LC filter shown).

systems [24] to still accurately capture the corresponding interactions between DUT and emulated environment. Similarly, considering, e.g., future aircraft onboard grids with grid frequencies of up to 1 kHz, or high-speed motors with similar or even higher fundamental frequencies, there is a need for power amplifiers that not only provide a high small-signal bandwidth, but that can also provide full voltage and power at high output frequencies of up to 50 kHz to 100 kHz [25].

Fig. 1 gives an overview of power amplifier systems reported by industry and academia. Typically, analog amplifiers need to be employed if ultra-high power bandwidths (UH-PBWs), i.e., higher than a few kilohertz, should be reached. However, the advent of WBG power semiconductors and the increasing computing power of digital control hardware, which facilitate higher switching frequencies and advanced (e.g., interleaved) converter topologies, enables switch-mode amplifiers to achieve *quasi-analog* amplifier performance and much higher efficiencies. The focus of this paper is thus on the hardware realization options for such next-generation power amplifiers. As a starting point, **Section II** provides a comprehensive review of analog, switch-mode, and hybrid power amplifier topologies reported in the literature. Based on this, we identify the most promising approaches for next-generation UH-PBW power amplifiers, which we then discuss in **Section III**. Finally, **Section IV** demonstrates the achievable performance of a modular switch-mode power amplifier system that employs one such approach—cascading of multiple converter cells—to realize a 10 kW phase module of a three-phase system with an UH-PBW of 100 kHz and 230 V rms output phase voltage.

II. TYPES AND ARRANGEMENTS OF POWER AMPLIFIERS

To provide a basis for identifying the most promising concepts and topologies for future power amplifiers that can meet the UH-PBW requirements outlined in the introduction, this section gives a comprehensive overview and a classification (see **Fig. 2**) of power amplifier concepts described in the literature. Whereas the focus of this paper is on AC power amplifiers with output voltages in the range of 230 V rms (single-phase) and output power levels in the order of several kilowatts to several tens of kilowatts, the following discussion considers also other examples with lower or higher output voltage and power capabilities as far as necessary to comprehensively cover all conceptually different solutions.

Note further that we use the terms "large-signal bandwidth", "power bandwidth", and "maximum output frequency" interchangeably to refer to the maximum frequency at which an amplifier can provide full-scale output voltage and current (i.e., power). Similarly, the publications summarized below do not all employ a consistent definition of the "small-signal bandwidth". Unless specifically mentioned otherwise, we therefore use a generic definition as a maximum frequency where only a small fraction (e.g., 10 %) of the full-scale output voltage or current can be provided.

A. LINEAR (ANALOG) POWER AMPLIFIERS

Linear power amplifiers (LPAs) operate power transistors (see **Fig. 3a**) in the linear range and hence can achieve very high bandwidths, high slew rates and low output impedances [56]. **Fig. 1** reflects these desirable characteristics and indicates that still many commercial high-bandwidth power amplifiers are of analog type. However, as known from electronics textbooks such as [57], the maximum efficiency of an analog class-B amplifier is given by

$$\eta_{\max,\text{Class B}} = \pi/4 \approx 78.5\,\%, \tag{1}$$

which it achieves only at the maximum output voltage ($\hat{v}_{\text{out}} = V_{\text{dc}}/2$) and with resistive load. The efficiency degrades in

direct proportion to the output voltage amplitude and also scales with the power factor $\cos\varphi$. This efficiency characteristic is an inherent property of the topology and can not be improved, e.g., by employing larger transistors. Class AB amplifiers achieve better linearity (reduced distortions around the output voltage zero crossing) by introducing a quiescent current that flows through both output-stage transistors and hence further reduces the efficiency. Similarly, operation with reverse power flow, i.e., as an active load, results in extreme power dissipation as then the sum of the supply power and of the power fed back from the DUT is dissipated in the linear amplifier's transistors [56]. All in all, these low efficiencies, which imply high losses and correspondingly high cooling effort, render conventional purely analog concepts unsuitable for future UH-PBW power amplifiers.

For the sake of completeness, note that there is ongoing research on improving the efficiency of analog amplifiers. Following essentially the same approach discussed in **Section II-C** below for switch-mode amplifiers, i.e., cascading of building blocks consisting of low-voltage (LV) power semiconductors and individual DC power supplies, [58] proposes a diode-clamped linear inverter. The system replaces the n-type and the p-type transistors of a class-B amplifier with series connections of n-type and p-type LV MOSFETs and a network of clamping diodes. Depending on the output voltage, at any point in time only a single LV MOSFET operates in the linear region, whereas all other LV MOSFETs are either fully turned-on or fully turned-off. Therefore, the efficiency increases with the number of series-connected LV devices to values exceeding 95 % for more than 20 series devices (e.g., using 40 V MOSFETs for a total DC-link voltage of 800 V). However, the losses are not equally distributed among the power devices. A further improvement can be achieved if the DC voltages are not split equally but asymmetrically [59]. Similarly, [60] employs a flying-capacitor approach to ensure equal blocking voltages for the LV MOSFETs. Both systems feature unity *voltage* gain and hence require a high-voltage reference signal. The concepts have been proposed and tested for filter-less motor drives with sinusoidal output voltages or rectifier applications with a few kilowatts of power. However, so far no performance evaluation focusing on UH-PBW operation has been reported.

B. SWITCH-MODE (DIGITAL) AMPLIFIERS

The term "switch-mode amplifier" has been coined as early as in the 1950s [61]–[63], initially for inverters targeting applications such as servo drives and later for audio applications (Class D). By not operating the transistors in the linear range but only either in the off-state or in the fully turned-on state (digital behavior), i.e., in switch-mode operation, amplifiers with significantly higher efficiencies could be realized. Importantly, their efficiencies do not depend strongly on neither the output voltage amplitude nor on the power factor, which is in stark contrast to LPAs.

As shown in **Fig. 3b** for the simplest case of a single half-bridge stage, switch-mode (digital) amplifiers employ pulse-width modulation (PWM) to generate a switched output voltage whose local average value follows a reference signal. Considering naturally sampled PWM with a triangular carrier and a purely sinusoidal reference signal, the spectrum of the switched voltage, v_{sw}, contains harmonics at multiples of the carrier frequency, i.e., at nf_{s}, and sidebands at $nf_{\mathrm{s}} \pm 2f_{\mathrm{out}}$ (and $\pm 4f_{\mathrm{out}}$, etc., which are, however, already significantly lower in amplitude), where f_{s} denotes the switching frequency and f_{out} denotes the fundamental frequency of the (filtered) output voltage, v_{out} [64]. Thus, a low-pass output filter is required to separate the desired local average of the switched output voltage from the switching-frequency harmonics (see also **Fig. 4a** and the in-depth discussion in **Section III-A**). To do so, even with an ideal low-pass filter the maximum output frequency is limited to $f_{\mathrm{out}} \leq f_{\mathrm{s}}/3$, because otherwise the relevant sideband harmonic at $f_{\mathrm{s}} - 2f_{\mathrm{out}}$ would be in the filter's passband. According to [56], in practice only lower maximum output frequencies (for a given switching frequency) are feasible, i.e., typically $f_{\mathrm{out}} \leq f_{\mathrm{s}}/10$, taking into account characteristics of real filters with finite slopes such as the exemplary single-stage LC-filter with -40 dB/dec shown in **Fig. 4a**.

The switching losses even of modern WBG SiC and GaN power semiconductors still limit f_{s}, if certain efficiency targets should be achieved and/or maximum cooling system volumes are limited. Nevertheless, in parallel to the development of power electronic inverter systems (drives, UPS, etc.), two-level topologies have found and are finding widespread application as power amplifiers in applications where the achievable output frequencies / bandwidths are sufficient, e.g., for the emulation of 50 Hz grids. Thus, before discussing more advanced topological variations, i.e., multilevel and multicell topologies, that facilitate increasing the *effective* switching frequency and by doing so shift the fundamental limit discussed above to significantly higher frequencies, we give a brief overview on recent applications of two-level switch-mode amplifiers as AC power amplifiers.

Typical systems based on standard two-level (IGBT-based) inverters feature switching frequencies of around 10 kHz and power levels in the range of about 10 kVA to 50 kVA, achieve small-signal control bandwidths in the order of 1 kHz and are typically employed for applications with fundamental frequencies of up to 100 Hz [2], [8], [9], [12], [14], [15], [17], [65], [66]. Higher fundamental output frequencies can be achieved by employing special modulation patterns, as, e.g., reported in [13] for a 120 kVA machine emulator system that supports a maximum output frequency of 2.5 kHz with a switching frequency of 10 kHz only. Moving from silicon IGBTs to WBG power semiconductors facilitates higher switching frequencies above 100 kHz and correspondingly also higher small-signal bandwidths of up to several 10 kHz [5], [51], [67]. Special techniques such as synchronizing the amplifier's modulation to the PWM of the DUT inverter allows the emulation of motor current harmonics at the switching frequency of a DUT inverter (10 kHz) [24]. Note that when only lower output voltage levels are required,

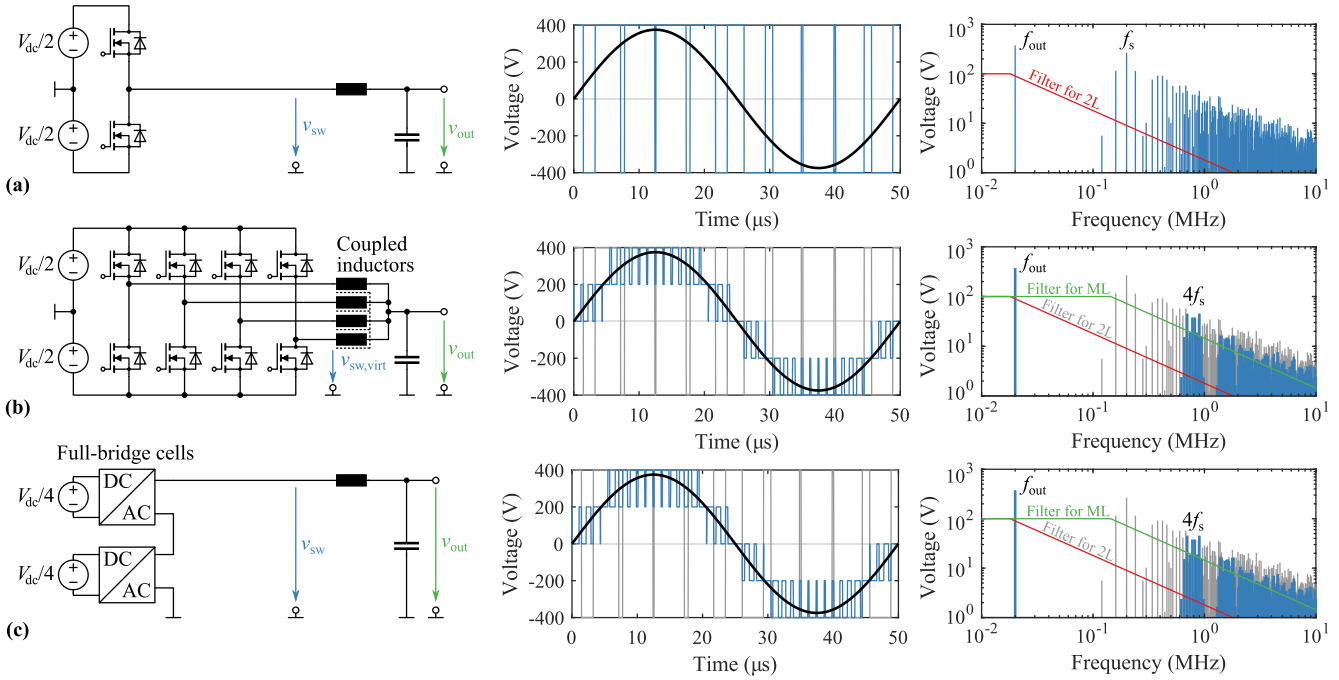

FIGURE 4. Basic topologies of digital amplifiers with exemplary waveforms of the switched voltages and the corresponding spectra, considering $V_{dc} = 800$ V, $f_{out} = 20$ kHz, and a device switching frequency of $f_s = 200$ kHz. The cutoff frequency of the LC output filter is selected to limit the maximum peak-to-peak voltage ripple of the output voltage, v_{out}, to $0.02 \cdot V_{dc}/2$ in all cases. (a) Two-level bridge-leg. (b) Parallel-interleaving of $N_{HB} = 4$ two-level bridge-legs, which results in a cancellation of all switching-frequency harmonics below $f_{s,eff} = N_{HB} f_s$, i.e., an N_{HB}-times higher effective switching frequency at roughly the same switching losses as occurring for (a), and enables a significantly higher filter cutoff frequency. Compared to a single bridge-leg, the current stress of the power semiconductors is reduced. Note that $v_{sw,virt}$ is the sum of the four bridge-legs' individual switch-node voltages divided by N_{HB}. (c) Series-interleaving of two full-bridge cells with in total again $N_{HB} = 2N_{cell} = 4$ bridge-legs, which thus achieves identical harmonic performance. Note the dedicated (isolated) power supplies of the cells, and the lower DC voltage switched by the cells' bridge-legs (reduced voltage stress). We discuss the operating principle of these concepts in detail in Section III-A. Note: the solid black waveform is $v_{sw,(1)}$, i.e., the switched voltage's fundamental component that corresponds to the reference voltage.

significantly higher large-signal bandwidths can be achieved such as 50 kHz for a 45 V DC system reported in [68], because the employed LV power semiconductors allow much higher switching frequencies (e.g., 700 kHz) without excessive switching losses. These considerations already indicate that a further increase of the achievable bandwidths could be facilitated by either paralleling of multiple bridge-legs or by stacking multiple converter cells realized with LV power semiconductors.

C. MULTILEVEL/-CELL DIGITAL AMPLIFIERS

In order to increase the bandwidth of switch-mode power amplifiers, ultimately the cutoff frequency of the output low-pass filter must be increased. If the output voltage quality should not be compromised, this implies that the harmonic content of the switched waveform must be shifted to higher frequencies. There are two basic strategies to achieve this without increasing the switching frequency of the power semiconductors: series-interleaving and parallel-interleaving, which is comprehensively explained in, e.g., [69]. Please note that we provide a detailed technical analysis of multilevel and multicell amplifier scaling laws later in **Section III-A**, whereas here the focus is on providing an overview of corresponding examples found in the recent literature to give an impression of the use cases and achievable performance:

1) PARALLEL INTERLEAVING

In the widest sense, the constant power flow of a three-phase power system [70] can be understood as a result of parallel-interleaving. As pointed out in [56], parallel operation of multiple systems to increase the effective operating frequency is known since 1916 from mercury-arc valve rectifiers with DC-side interphase reactors [71]. More specifically, as known since the early 1970s [72], [73], two or more bridge-legs can be operated in a parallel-interleaved manner to generate a multilevel output voltage waveform with $N_{HB} + 1$ voltage levels with N_{HB} denoting the number of parallel bridge-legs. The first switching-frequency harmonics occur around the *effective* switching frequency $f_{s,eff} = N_{HB} \cdot f_s$ (see **Fig. 4b**). Therefore, it can be shown (see **Section III-A**) that a single-stage LC filter's maximum cutoff frequency $f_{0,max}$ required to ensure a given maximum output voltage ripple increases (implying higher possible bandwidth) with the number of bridge-legs, N_{HB}, over the baseline (required cutoff frequency $f_{0,max,2L}$ in case of a single two-level bridge-leg) as

$$f_{0,max} = N_{HB}^{3/2} \cdot f_{0,max,2L}, \tag{2}$$

whereby the switching frequency of each transistor (device switching frequency) is kept constant, see also **Fig. 5**. The power semiconductors still need to block V_{dc}, but the output current is shared among the bridge-legs. Thus, also compared

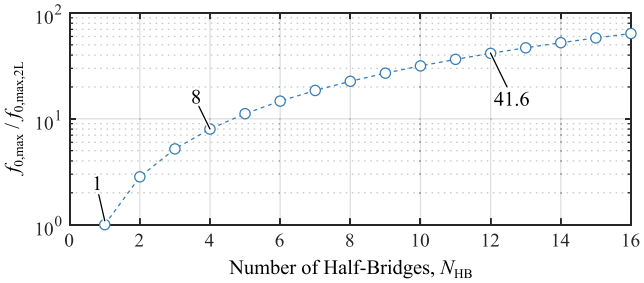

FIGURE 5. Possible increase of a single-stage LC filter's cutoff frequency by adding additional half-bridges to a simple two-level topology (parallel or series interleaving, see Fig. 4), for otherwise identical parameters (device switching frequency, allowed voltage ripple, etc.), see (2). Note that the 8 times higher cutoff frequency obtained for $N_{HB} = 4$ can be observed also in the examples shown in Fig. 4.

to simply increasing the semiconductor current rating (i.e., the chip area) of a single bridge-leg to reach higher power levels, interleaved operation of several bridge-legs is advantageous.

The concept has thus also been employed for digital amplifiers already in the 1990s [74], e.g., for driving MRI gradient coils [22]. More recently, high-power systems have been described, where even with the use of IGBTs relatively high effective switching frequencies and hence small-signal and large-signal bandwidths have been achieved. For example, [75] demonstrates tracking of a 1 kHz reference signal with a "LinVerter" operating from a 320 V DC bus at up to 10 A output current. Similarly, [52] employs a full-bridge configuration with two times six interleaved IGBT bridge-legs switching at 20 kHz each (i.e., achieving an effective switching frequency of 240 kHz) to realize a 50 kVA (three-phase) amplifier with a bandwidth of 1 kHz for grid emulation applications. Parallel interleaving has also been used in industrial systems. For example, [35] and [76] describe a 200 kVA emulation system that achieves a large-signal bandwidth of 5 kHz and a small-signal bandwidth of 15 kHz using six parallel amplifier modules with six interleaved IGBT bridge-legs each, operating from an 800 V DC bus. Even higher power ratings can be achieved by paralleling more amplifier modules. Similarly, [37] and [38] describe a high-power industrial motor emulator system with an overall output current rating of up to 1600 A rms at a fundamental frequency of up to 5 kHz, which is facilitated by an effective switching frequency of 800 kHz. It can be assumed (based on the high performance and the high effective switching frequency) that also a digital amplifier that became available recently as a product [27] employs a parallel-interleaved topology to achieve an effective switching frequency of 1 MHz and thus the ability to provide a large-signal bandwidth of 50 kHz at an output power of up to about 20 kW. Finally, recent work [77] targeting lower output voltages (45 V) and making use of state-of-the art 150 V GaN transistors' capability of switching at up to a megahertz to reach an effective switching frequency of 4 MHz (four interleaved bridge-legs) demonstrates extreme performance in terms of bandwidth by reaching large-signal amplification of reference signals with a bandwidth of up to 350 kHz.

Another recently proposed concept specifically targeting motor emulation for testing three-phase two-level inverters uses parallel bridge-legs with individual LC output filters to generate four voltage levels, and four AC-switches to alternately connect one voltage level to the emulator's phase terminal [78], [79]. Whereas the concept avoids introducing additional (very small) current ripple as compared to a parallel-interleaved alternative, the hardware effort (number of switches) as well as the control complexity are significantly higher.

2) SERIES INTERLEAVING (CASCADING OF CONVERTER CELLS)

Several full-bridge converter cells can be connected in series at their AC terminals to form a cascaded H-bridge (CHB) converter, which has been proposed in 1971 [80]. Again, interleaved operation of these converter cells results in a multilevel output voltage waveform with $2N_{cell} + 1$ levels, where N_{cell} is the number of cascaded converter cells. The first group of switching-frequency harmonics occurs around $f_{s,eff} = N_{HB} \cdot f_s$ (see **Fig. 4c**, and [81] for a formal analysis), where N_{HB} again denotes the number of bridge-legs and, considering full-bridge cells, $N_{HB} = 2 \cdot N_{cell}$ holds. CHB-based solutions require dedicated, i.e., isolated, power supplies for each of the cascaded cells. The topology thus inherently features galvanic isolation. It is furthermore fully modular, which facilitates scaling of output voltage or power ratings to higher levels by increasing the number of cells. In contrast to parallel-interleaved topologies, the blocking voltage of the cells' power semiconductors is reduced to $V_{dc}/(2N_{cell})$ (note that V_{dc} always refers to the total DC voltage of an equivalent parallel-interleaved or non-interleaved amplifier, see **Fig. 4**), which advantageously allows to employ devices with lower blocking voltages and hence lower switching losses. In case of MOSFETs, devices with lower blocking voltage ratings advantageously also feature lower specific on-state resistances (which scales roughly with $V_B^{-2.5\cdots-2}$) [82].

Even though known for a long time and successfully applied especially in high-power and medium-voltage applications, the CHB structure has first been introduced to switch-mode amplifiers only shortly after the turn of the millenium [83]. Later, [84] described a system with grid-level output voltage ranges and a 2 kW power rating, which could achieve a closed-loop large-signal bandwidth of 5 kHz using six cascaded cells switching at 25 kHz each (effective switching frequency of 300 kHz). Similar results have also been reported in [50] or, for lower output voltages, in [85].

The scalability of the CHB concept renders it suitable also for applications with higher voltages such as gradient amplifiers for MRI systems [23] and medium-voltage grid simulation, as indicated by, e.g., a 6 MVA, 50 Hz system that can provide 35 kV output voltage (with a step-up transformer) [86]. Recently, [87] and [4] have introduced a 1 MVA system with five cascaded cells and a total DC voltage of 6 kV, which achieves a small-signal bandwidth of 7 kHz. Series-interleaving has also been employed for special

applications, e.g., with low power but high voltage as for supplying plasma reactors with a 15 kV (peak) square wave voltage at 5 kHz [88]. Fully utilizing the benefits of the CHB concept, [89] describes an amplifier for medical application (electroporation) that consists of 20 cascaded cells with 60 V DC each. Making use of 80 V GaN devices and a combination of staircase modulation and PWM operation of one cell with a switching frequency of 1 MHz, the amplifier can generate bursts of a 500 kHz sinusoidal output voltage with an amplitude of up to a about 1 kV at 7 A rms load current. A similar system described in [90] employs asymmetric cell voltages to optimize the trade-off between switching losses and output voltage quality.

Series-interleaving of cascaded converter cells is an extremely powerful concept for future UH-PBW systems. Therefore, we will discuss this approach in more detail in **Section III-A** and demonstrate the performance of a single-phase 10 kW prototype with a large-signal bandwidth of 100 kHz in **Section IV**.

3) SERIES INTERLEAVING (MULTILEVEL BRIDGE-LEGS)

Multilevel bridge-legs such as neutral-point clamped (NPC) structures (patent filed in 1979 [91], also described in 1981 [92]) or flying-capacitor converter topologies (proposed in 1992 [93]) consist of power semiconductors that only require a blocking voltage rating that is lower than the total DC bus voltage, and advantageously generate an output voltage with multiple levels and a higher effective switching frequency, i.e., they can be seen as a non-modular variant of the series-interleaved multi-cell topology discussed above. Therefore, the approach has been selected for certain digital power amplifiers discussed in the literature.

For example, [94] employs a five-level diode-clamped bridge-leg structure to realize a 7.5 kW (three-phase) amplifier with a switching frequency of 10 kHz and a filter cut-off frequency of 2 kHz. Similarly, but now making use of SiC power semiconductors, [48], [95], [96] propose a 10 kW three-phase AC power source based on three-level T-type bridge-legs [97] that operate with a switching frequency of 48 kHz, achieving a small-signal bandwidth of 7.1 kHz. The effective large-signal bandwidth is limited to about 300 Hz by the capacitive current consumption of the employed two-stage LC filter; paralleling of bridge-legs would thus become necessary to increase the maximum output frequency.

Recently, [98] demonstrated an arbitrary voltage waveform generator with an eight-level flying-capacitor bridge-leg using GaN transistors that switch at 200 kHz. The prototype is rated at only 500 W and operates with a relatively low DC-bus voltage of 200 V, and it achieves a very high closed-loop bandwidth of 50 kHz that facilitates large-signal output waveforms with fundamental frequencies of up to 40 kHz.

Modular multilevel converter (MMC) structures [99] are a fully modular alternative for realizing bridge-legs with a single DC-side interface: in contrast to CHB topologies, the converter cells of an MMC bridge-leg do not need dedicated

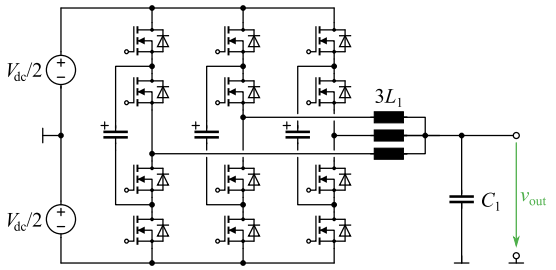

FIGURE 6. Example for a combination of (flying-capacitor) multilevel bridge-legs and parallel interleaving as proposed in [25].

power supplies, i.e., the local DC capacitor voltages are maintained via appropriate control, and a single DC supply for the digital amplifier stage is sufficient. MMC-based grid emulators have been proposed in [100] and later, targeting emulation of grid faults and unbalanced conditions, with a delta-wye coupling transformer [101] or in a transformer-less three-phase four-wire configuration [102]. Recently, a MMC topology has been proposed as an arbitrary waveform generator for dielectric testing of high-voltage grid assets; the full-scale system shall provide an output voltage of up to 100 kV and 10 kW of power with a large-signal bandwidth of 500 Hz [103]. Note, however, that MMC topologies are not suitable for operation with DC or very *low* output frequencies due to the increased energy exchange with the modules' floating capacitors [104].

4) COMBINATION OF SERIES AND PARALLEL INTERLEAVING

Of course, it is possible to parallel-interleave several multilevel bridge-legs, thereby combining the advantages of both concepts (current sharing, lower blocking voltage) in a single converter stage. An early reference from the year 2000 combines several multilevel bridge-legs—realized with gate-turn-off thyristors (GTOs) switching at the fundamental frequency—in a parallel-interleaved manner to realize an arbitrary waveform generator [105]. More recently, [39] proposed a motor emulator that consists of three parallel-interleaved three-level NPC bridge-legs operating from an 800 V DC bus, which allows to use 600 V or 650 V silicon MOSFETs. The emulator realizes output currents of more than 50 A rms at a fundamental frequency of up to 2.5 kHz. Instead of three-level NPC bridge-legs, also multilevel flying-capacitor bridge-legs can be parallel-interleaved, as recently proposed in [25], [53]. This design shown in **Fig. 6** uses three three-level flying-capacitor bridge-legs operating from an 800 V DC bus, which are realized with 600 V GaN transistors. This facilitates a switching frequency of 800 kHz and hence an effective switching frequency of 4.8 MHz. The system will achieve a large-signal bandwidth of 100 kHz at the rated power of 10 kW (single-phase).

D. HYBRID ANALOG/DIGITAL AMPLIFIERS

Generally speaking, analog amplifiers tend to achieve near-ideal behavior regarding the dynamic performance but suffer from high losses, whereas the opposite is true for digital amplifiers. Therefore, already in the 1980s combinations

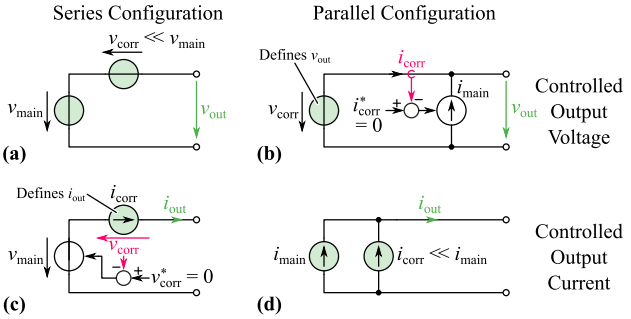

FIGURE 7. Generic classification (introduced by Yundt in 1983 [107], [108]) of hybrid amplifier concepts. For concepts (a) and (d), the main amplifier (index $_{main}$, i.e., the stage that provides the bulk power to the load) approximates the desired output as closely as possible and the correction amplifier (index $_{corr}$) compensates any remaining deviation; the output quantity (voltage or current) is the sum of both stages' contributions. In contrast, in case of concepts (b) and (c) the correction amplifier defines the output quantity directly and the main amplifier is controlled to adjust the load impedance seen by the correction amplifier (e.g., in case (b), the main amplifier is controlled such that the correction amplifier's output current is minimized and ideally zero).

of analog and digital amplifiers to form *hybrid* amplifiers have been proposed [106] and classified into two main categories as shown in **Fig. 7** [107], [108]. Note that typical AC power source applications require a controlled voltage output. Hence, in the following we focus only on these topologies even though **Fig. 7** shows the equivalent arrangements for amplifiers with a current-source output characteristic, too.

Note that the correction amplifier stage, which for A/D hybrid amplifiers is realized with an analog amplifier, could also be realized with a low-power / low-voltage digital amplifier with correspondingly higher bandwidth than the main amplifier. Such D/D hybrid amplifiers will be discussed below in **Section II-E**. First, however, we will give a brief overview on the different A/D hybrid amplifier concepts, including a third concept (envelope-tracking power supply) not shown in the classification from [107], [108] and **Fig. 7**. The interested reader finds a more detailed review of hybrid amplifier concepts published before 2011 in [109].

1) SERIES CONFIGURATION

In a series configuration (see **Fig. 7a**) of a main digital amplifier stage and an analog correction amplifier stage, the output voltage is the sum of the two amplifier's output voltages. Consequently, the goal is for the main amplifier to approximate the desired output voltage as closely as possible such that the remaining deviation, i.e., a voltage ripple, to be compensated by the correction amplifier is as low as possible. The analog correction amplifier then operates with relatively low voltage; even though it processes the full load current, the processed power remains low. This *partial power processing* of the (analog) stage with low efficiency does have only a moderate impact on the system-level efficiency [110].

The concept can be implemented with a two-level digital amplifier with an output filter as shown in **Fig. 8a** and proposed in [111]. Alternatively, the series voltage can be coupled into the main power path via a transformer, which advantageously avoids that the analog correction amplifier

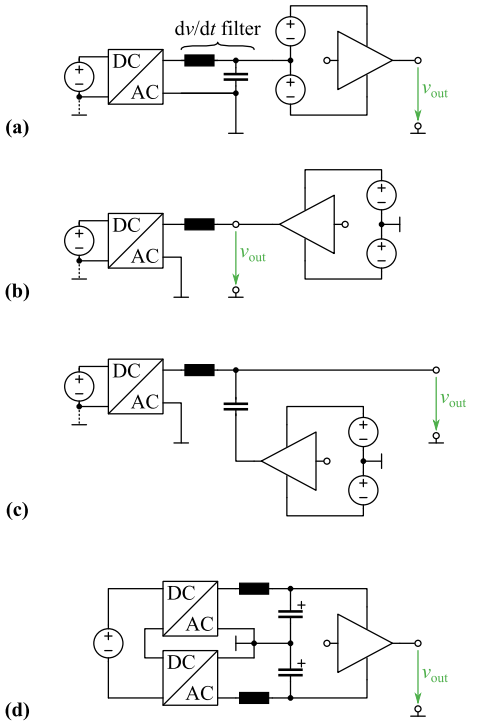

FIGURE 8. D/A-hybrid amplifier concepts. (a) Series configuration (cf. 7a) of a digital main amplifier and a series-connected analog correction amplifier. A dv/dt filter can be employed to reduce the slew rate requirement of the analog correction amplifier. (b) Parallel configuration (cf. 7b), i.e., the analog amplifier directly defines the output voltage while the digital main amplifier provides the bulk of the load current. (c) Capacitive coupling of the analog amplifier reduces its required voltage (and hence power) rating [113]. (d) Envelope-tracking configuration, where the supply voltage of the analog amplifier is adapted according to the output voltage set point in order to reduce losses.

must carry the full load current [106]; this is similar to older concepts for active harmonic filtering [112].

However, to avoid the bandwidth limitation introduced by an output filter suitable for two-level converters, most systems discussed in literature from as early as 1994 [114] (for MRI gradient amplifiers) employ multi-cell digital amplifier stages, which even without PWM can approximate a sinusoidal voltage relatively well as a staircase waveform. The magnitude of the voltage steps, i.e., the DC voltages of the cells, directly defines the required voltage capability of the analog stage. Furthermore, to achieve a clean output waveform, the linear amplifier's slew rate must be higher than the dv/dt of the digital amplifier's switching transitions. Therefore, most systems described in the literature employ a dv/dt filter at the output of the multi-cell digital amplifier. For example, [50], [115], [116] describe a 130 V rms, 1 kW (single-phase) system consisting of nine cascaded converter cells with equal DC voltages, which achieves a large-signal bandwidth of 10 kHz and, thanks to the linear stage, a very high small-signal bandwidth of 600 kHz. The 140 V rms, 500 W hybrid amplifier proposed in [47] achieves a similar small-signal bandwidth of 400 kHz, but uses only four cascaded cells that, however, feature unequal DC voltages and thus can realize 19 voltage levels (instead of nine voltage levels achievable with four cells that have equal DC voltages, see

Section II-C2). In contrast to most systems discussed in the literature, it is also possible to operate the digital multi-cell amplifier of a hybrid D/A amplifier system not with staircase modulation but with (phase-shifted) PWM [117]. However, the LC filter required to attenuate the switching-frequency harmonics generated by the digital multi-cell amplifier then again limits the achievable power bandwidth.

Note that instead of providing an isolated power supply for each of the cascaded cells, it would be possible to move the isolation to the output, i.e., to sum the contributions of all cells and of the linear stage via a transformer [118]. However, in this case, saturation of the transformer core prevents operation with DC or low-frequency signals. Another option has been proposed in [49], where instead of a CHB multi-cell structure, an MMC topology has been employed and hence a single DC supply for the digital amplifier stage is sufficient.

The research in series A/D hybrid amplifiers using multi-cell digital amplifier stages is still ongoing, with [54], [119], [120] describing a 60 kVA, 400 V three-phase system consisting of a 12-cell CHB stage using nearest-level modulation (a sorting algorithm ensuring equal stresses of the cells), a dv/dt filter, and a linear correction amplifier. The CHB cells operate with a DC voltage of 30 V and hence the linear amplifier can provide an output voltage of ± 30 V to compensate the voltage steps. With a bandwidth of the LPA stage of 105 kHz, the system can realize full-scale sinusoidal test signals with up to 60 kHz. A similar system has recently been described in [121].

2) PARALLEL CONFIGURATION

Alternatively, the correction amplifier and the main (digital) amplifier can be connected to a common output in parallel as shown in **Fig. 7b** and **Fig. 8b**. Advantageously, the linear amplifier thus fully defines the output voltage and hence the transient behavior (bandwidth, slew rate). The digital main amplifier is controlled such that it provides most of the load current. The correction amplifier ideally compensates only the ripple current, i.e., acts as an active filter. Thus, the lower the ripple generated by the main amplifier is, the lower the current rating (and hence power rating) of the analog stage becomes. Therefore, multilevel (e.g., parallel-interleaved) digital stages are often considered. However, during transients that are faster than the main amplifier's bandwidth, the linear amplifier must (transiently) deliver the necessary load current, which ultimately could lead to thermal overload. These (and further) aspects of A/D hybrid amplifier systems have been thoroughly discussed in [74]. The direct parallel configuration as shown in **Fig. 8b** is most suitable for low-voltage, low-power applications such as audio amplifiers (see, e.g., [122]–[124]), because the linear amplifier stage must process the full voltage and feature a low high-frequency output impedance.

Fig. 8c shows a slightly different configuration proposed in [113], which couples the analog amplifier capacitively to the common output. This coupling capacitor, which can be seen as part of the digital stage's LC output filter, takes most of the output voltage and the linear amplifier's voltage capability is given by the remaining voltage ripple across the filter capacitor (which would appear if the correction amplifier was not present). According to [113], this implies that the power rating of the linear amplifier can be reduced from typically 10 % . . . 20 % to 1 % . . . 4 % of the output power rating, with corresponding benefits regarding the overall system efficiency and a simplified cooling system. Note that similar concepts are known from active EMI filters [125]–[127]. However, whereas the linear amplifier still ensures very high output voltage quality, it can only improve the small-signal dynamics, and the main amplifier stage with its LC low-pass filter defines the large-signal response. The 400 V, 4 kW prototype described in [113] nevertheless achieves a large-signal bandwidth of 10 kHz with a three-level NPC digital amplifier that switches at 100 kHz and features an LC lowpass filter with a cutoff frequency of 20 kHz. In [128], the same approach is used with a CHB main amplifier. Advantageously, the active filter (analog correction amplifier) can also compensate low-frequency switching distortions, i.e., subharmonics below $2N_{\mathrm{cell}}f_{\mathrm{s}}$, that may appear as a consequence of, e.g., unequal DC voltages of the CHB converter cells. Note that as an alternative to multilevel topologies, two-level digital main amplifiers with *two-stage* (4^{th} order) LCLC output filters could be employed [129], [130] to reduce the ripple current that the analog amplifier stage must process.

3) ENVELOPE-TRACKING POWER SUPPLY

Fig. 8d shows a third hybrid configuration (not shown in the classification from **Fig. 7**), where a digital stage adapts the supply voltage of a linear amplifier according to the desired output voltage, as proposed in 1985 for audio applications [131]. These so-called envelope-tracking approaches improve the efficiency of the analog amplifier, especially for operation with output voltages below the maximum (see **Section II-A**). Thus, a high-power (115 V rms, 1.5 kW) system described in [116], [132] reaches a peak efficiency that is only slightly higher than that of a linear amplifier with constant supply voltages for operation with maximum output voltage, but shows clear benefits at lower output voltages. However, the large-signal bandwidth of 1 kHz is essentially limited by the bandwidth of the tracking power supply. Therefore, the approach is rarely used for power amplifiers as considered here, but mainly for low-power or special applications such as driving piezoelectric transducers [133]. Note that envelope-tracking power supplies in radio-frequency (RF) applications are used to vary the supply voltage of the RF linear amplifier according to the *envelope* of the RF signal to be amplified, i.e., the bandwidth of the tracking power supply must be higher than the envelope of the output signal only [134] (interestingly, the envelope-tracking power supply proposed there is a parallel A/D hybrid configuration, achieving a maximum output frequency of 300 kHz at 50 W and 26 V).

E. DIGITAL/DIGITAL HYBRID AMPLIFIERS

As discussed above, the correction amplifiers shown in **Fig. 7** can also be realized with digital amplifiers, which due to lower power requirements can operate with much higher switching frequencies than the main amplifiers. Hence, these digital correction amplifiers can achieve higher bandwidths and approximate the behavior of a linear amplifier with higher efficiency. The general goal remains to increase the LC output filter's cutoff frequency (for a given output voltage quality), which allows an increase of the overall amplifier systems' bandwidth. Essentially, the resulting systems are structurally very similar to series or shunt active filters, which have been investigated since the 1970s for grid applications [135].

1) SERIES CONFIGURATION

Again, a correction voltage source can be added in series to a main amplifier stage (see **Fig. 7a**). A first option to do so couples the compensation voltage via a transformer into the main power flow path [106], [136], as done for decades in power grid applications [112], [135]. This concept has recently been applied to a grid simulation system in [137], [138], where a standard 400 V, 5 kVA IGBT inverter is combined with a 100 V MOSFET inverter that is responsible for generating higher-order harmonics. Similarly, [139]–[141] use a three-phase transformer to combine the outputs of a 800 V, 12 A three-phase inverter switching at 20 kHz with a 100 V small-signal inverter operating at 200 kHz. In these examples, the low-frequency output transformer limits the achievable bandwidth, e.g., to 2 kHz in [139]–[141]. The roles of the main amplifier and the transformer-coupled small-signal stage are clearly separated (generation of fundamental and higher-order harmonics).

In contrast, a direct series connection of a slow-switching high-power, high-voltage inverter with a fast-switching low-voltage, low-power inverter directly aims at improving the harmonic content of the overall switched output voltage, which in turn allows an increase of the system's output filter cutoff frequency. Advantageously, the main amplifier stage is a multilevel inverter, which, e.g., can operate at the fundamental frequency. The correction amplifier needs a DC voltage that corresponds to the difference of two output voltage levels only, and can then operate with PWM to improve the spectrum of the overall output voltage waveform. Such systems have been proposed in the 1990s for MRI gradient amplifiers [114] or MV drive applications [142], [143], the latter combining a GTO inverter switching at the fundamental frequency with a PWM-operated IGBT inverter.

The power amplifier concept described in [50], [116] uses a similar concept by operating all except one cell of a CHB converter at the fundamental frequency only, generating a staircase waveform. The last cell operates with PWM such that the overall output voltage waveform is a multilevel PWM waveform. Compared to all cells operating with (interleaved) PWM, the effective switching frequency is much lower, however, requiring a lower output filter cutoff frequency.

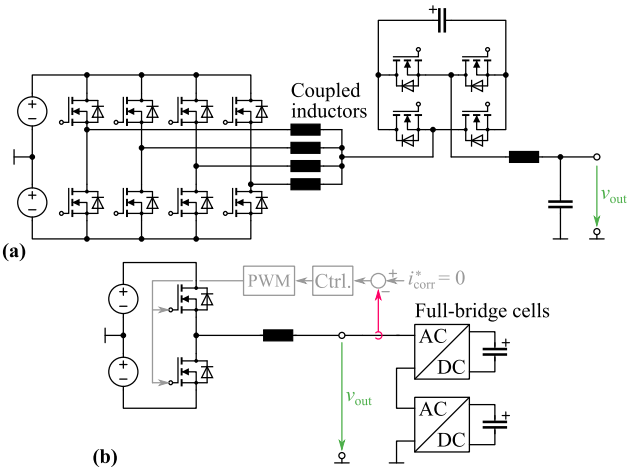

FIGURE 9. D/D-hybrid amplifier concepts. (a) Series configuration (cf. Fig. 7a) of a multilevel (parallel-interleaved; series-interleaved would be possible, too) main amplifier stage and a series-connected digital correction stage (processing only distortion reactive power at a comparably low voltage level) [144]. (b) Parallel configuration (cf. Fig. 7b) of a multicell (series-interleaved) correction stage that directly defines the output voltage and a parallel-connected two-level main stage that delivers the bulk of the load current [55], [145]. Note that the correction stage processes only distortion reactive power and the cells thus do not require power supplies.

Similarly, but targeting HVDC circuit breaker testing, [146] proposes a 10 kV, 30 kA arbitrary voltage source that combines a low-voltage PWM-inverter with a multilevel Marx-type high-voltage staircase voltage generator.

The fast-switching cell can operate as an active filter only, i.e., without processing active power. Therefore, it is not necessary to provide an (isolated) power supply, as proposed in [147]. There, a diode-clamped 5-level inverter is combined with two series-connected H-bridges with flying DC capacitors controlled to two different DC voltages. This active filter improves the output voltage quality without significantly degrading the system's efficiency. Targeting MV applications, [148] similarly describes a CHB system with asymmetric DC voltages of the (supplied) cascaded cells, and two additional cells without a power supply that hence act as active filters only. More recent publications combine an active filter stage without external power supply with a parallel-interleaved multilevel inverter [144], as exemplarily shown in **Fig. 9a**, or instead with an MMC converter as proposed in [149] for driving underwater electroacoustic transducer systems. Both variants share the advantage of needing only a single DC supply (in contrast to CHB-based approaches). Whereas the MMC-based solution can advantageously make use of low-voltage semiconductors, its complexity is clearly much higher than that of a parallel-interleaved main power stage.

Recently, [19] proposed a D/D hybrid emulator for traction batteries, where the battery's resistance must be emulated with a minimum bandwidth of 20 kHz, however, only with relatively low power. Thus, a combination of an 80 kW standard converter delivering the bulk power (at up to 600 V and 500 Hz) and a series-connected low-power full-bridge

active filter (100 V DC, ±300 A) operating with an effective switching frequency of 200 kHz is employed.

2) PARALLEL CONFIGURATION

Parallel configuration (see **Fig. 9b**) of two digital amplifier stages of different characteristics is possible, too. Such concepts have been proposed as active shunt filters for grid applications early on, e.g., in [150] and [151]. In the context of power amplifiers, the goal of parallel-connecting an active filter stage is to shift the cutoff frequency of the required output filter to higher frequencies and hence enable improved dynamic performance of the amplifier system, as discussed earlier. For example, already in 1999, [152] demonstrated a 25 V rms, 40 A rms high-current amplifier system with a main stage switching at 100 kHz and a parallel-connected stage operating at 1 MHz, whereby the auxiliary stage compensates (reduces) the current ripple of the main stage by −29 dB.

For three-phase systems, [153] proposed an active filter approach that connects CHB converter stacks (without cell power supplies) between the main inverter's phases. These active filters remove the ripple current created by the main inverter and hence significantly improve the output voltage quality. Recently, [55], [145], [154] employed a similar topology using three 17-level CHB stacks (effective switching frequency of 1 MHz) in star-configuration to act as an active filter for a three-phase two-level main amplifier (switching frequency max. 14.5 kHz). **Fig. 9b** shows a schematic representation of this concept. A 60 kVA prototype achieves high-bandwidth (100 kHz) output voltages via the CHB system, whereas the current bandwidth of the main amplifier (and hence the power bandwidth of the overall system) is limited to about 2 kHz. This limitation is similar to that of D/A parallel-hybrid systems discussed above.

F. DISCUSSION

Considering the many different amplifier topologies described in literature and described so far, analog amplifiers achieve extreme bandwidth but suffer from high losses. D/A hybrid topologies still employ analog amplifier stages with relatively high losses, and D/D hybrid systems are relatively complex as they combine different types of switch-mode amplifiers. In both cases, the power bandwidth remains limited by the stage processing the bulk power. Whereas this may be sufficient for certain applications, the most suitable approaches for high-power general-purpose UH-PBW amplifiers are parallel- or series-interleaved switch-mode topologies, as they combine high efficiency and, due to interleaving, high power bandwidth. Series-interleaved multicell systems are particularly interesting, as they inherently feature galvanic separation and low realization effort concerning inductive components. This, in addition, enables relatively straightforward scaling to higher power and especially higher voltage levels. Therefore, the following **Section III** explains technical key considerations for the realization of parallel-interleaved and series-interleaved (multicell) UH-PBW amplifiers.

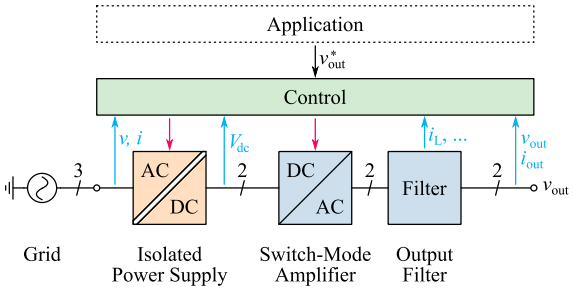

FIGURE 10. Single-line overview diagram of an UH-PBW power amplifier *system*, which, in addition to the actual switch-mode amplifier and output filter (Section III-A) also features a mains interface, i.e., an isolated power supply (Section III-B), and a control system including voltage and current sensors (Section III-C). The application-level software, which is not in the scope of this paper, models, e.g., a specific grid behavior, or emulates a motor behavior, etc. Note that a system with a single-phase output is shown as a basic building block; three output phases could, e.g., be achieved by employing three switch-mode amplifier and three filter stages.

III. CONCEPTS FOR FUTURE UH-PBW AMPLIFIERS

As illustrated in **Fig. 10**, a general-purpose UH-PBW amplifier *system* consists of three subsystems. The following subsections discuss key aspects of these subsystems: the actual switch-mode amplifier stage including a low-pass output filter in **Section III-A**, a typically isolated (to facilitate arbitrary reference potentials of the amplifier's output) mains interface in **Section III-B**, and the control system including voltage and current sensors, high-performance computing hardware and the corresponding firmware in **Section III-C**.

A. SWITCH-MODE AMPLIFIER AND OUTPUT FILTER

The output filter required to remove switching-frequency noise from a switch-mode amplifier's output voltage ultimately limits the feasible maximum full-power output frequency (reactive power consumption of the filter elements) as well as the small-signal bandwidth (quickly increasing filter attenuation above the cutoff frequency, e.g., −40 dB/dec for a single-stage LC filter). Therefore, realizing ultra-high power bandwidth necessitates a high filter cutoff frequency, and thus simple two-level topologies would required extreme switching frequencies. Even the availability of modern WBG power semiconductors facilitates this only up to a point before either the efficiency becomes too low or the design becomes thermally unfeasible.

In contrast, as briefly discussed in the context of **Fig. 4** and **Fig. 5** above, multilevel topologies facilitate an increase of the output filter cutoff frequency for otherwise fixed system parameters (device switching frequency and/or power conversion efficiency, maximum allowable output voltage ripple, etc.). Considering a multicell (CHB) converter with N_{CHB} cells and a single-stage LC filter, it can be shown (see, e.g., [83]) that the maximum cutoff frequency ensuring a certain relative peak-to-peak output capacitor voltage ripple $\hat{v}_{\mathrm{out,pp}}/V$ is given by

$$f_{0,\max} = \sqrt{\frac{32}{\pi^2} N_{\mathrm{CHB}}^3 f_{\mathrm{s}}^2 \frac{\Delta v_{\mathrm{out,pp}}}{V}}, \tag{3}$$

where f_s is the switching frequency of each bridge-leg and V is the sum of all the cells' DC voltages, i.e., $v_{\text{out}} \in [-V, V]$. With the number of half-bridges being $N_{\text{HB}} = 2N_{\text{CHB}}$, we find a generic expression

$$f_{0,\max} = \sqrt{\frac{4}{\pi^2} N_{\text{HB}}^3 f_s^2 \frac{\Delta v_{\text{out,pp}}}{V}} \tag{4}$$

that equally holds also for parallel-interleaved operation of N_{HB} bridge-legs (note that in this case $V = V_{\text{dc}}/2$ such that again $v_{\text{out}} \in [-V, V]$). In the example of **Fig. 4** with $f_s = 200\,\text{kHz}$, $V_{\text{dc}} = 800\,\text{V}$, $\hat{v}_{\text{out}} = 375\,\text{V}$, and $f_{\text{out}} = 20\,\text{kHz}$, the required filter cutoff frequency is calculated to limit the worst-case peak-to-peak output voltage ripple to $0.02 \cdot V_{\text{dc}}/2$. By changing from a single bridge-leg shown in **Fig. 4a** to four parallel-interleaved bridge-legs in **Fig. 4b** or two stacked cascaded cells (four bridge-legs in total, too) in **Fig. 4c**, the cutoff frequency can be increased from about 18 kHz to 144 kHz, i.e., by a factor of 8 as indicated by (2) and in **Fig. 5**.

With the cutoff frequency of a single-stage LC filter being $f_0 = 1/2\pi\sqrt{LC}$, the condition (4) describes a hyperbola in the L-C-plane, i.e., in the so-called *filter design space* [95] shown in **Fig. 11**. Filter designs with $f_0 \leq f_{0,\max}$ satisfy the voltage ripple criterion. For a fixed N_{HB}, $f_{0,\max}$ increases with f_s and hence the area where the combinations of L and C satisfy $f_0 \leq f_{0,\max}$ expands. However, the range of valid filter designs is further constrained by limiting the maximum allowable voltage drop across L at nominal output current, I_{out}, and maximum output frequency, $f_{\text{out,max}}$ to

$$I_{\text{out}} \cdot 2\pi f_{\text{out,max}} L \leq p \cdot V_{\text{out}}, \tag{5}$$

i.e., to a fraction p of the nominal output voltage V_{out}. Similarly, the maximum current through C at nominal output voltage, V_{out}, and maximum output frequency, $f_{\text{out,max}}$ should be limited to

$$V_{\text{out}} \cdot 2\pi f_{\text{out,max}} C \leq q \cdot I_{\text{out}}, \tag{6}$$

i.e., to a fraction q of the nominal output current I_{out}. Both criteria result in straight-line boundaries in the filter design space of **Fig. 11**. Combining both limits results in a lower bound for the filter cutoff frequency as

$$f_{0,\min} = f_{\text{out,max}} \cdot \frac{1}{\sqrt{pq}}. \tag{7}$$

This again represents a hyperbola in the design space, which is pinned to the intersection point of the limits from (5) and (6). Note that further criteria such as relating to the output impedance, etc. could be implemented in the design space, and a similar approach can also be considered for the design of two-stage LCLC filters. These aspects have been discussed in detail in [95].

Finally, by equating $f_{0,\max}(f_s)$ from (4) to $f_{0,\min}$ from (7), a closed-form expression for the required device switching frequency as a function of the number of bridge-legs, N_{HB},

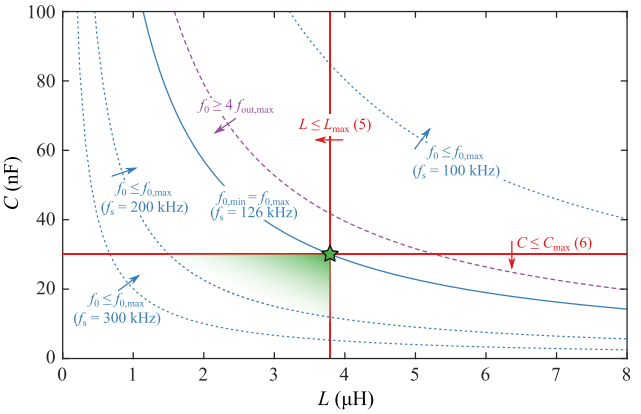

FIGURE 11. **Exemplary design space of a single-stage LC filter for a multilevel topology with $N_{\text{HB}} = 12$ half-bridges, $f_{\text{out,max}} = 100\,\text{kHz}$, $p = 0.15$, $q = 0.3$, and $\Delta v_{\text{out,pp}}/V = 2\%$. Note that the design space (green shading) collapses to a single point if $f_s = 126\,\text{kHz}$ is selected according to (8); see also f_s in Fig. 12 for $N_{\text{HB}} = 12$. The $f_0 \geq 4f_{\text{out,max}}$ criteria could be introduced to spectrally separate the maximum output frequency from the LC filter's resonance. Note that further criteria such as a maximum permissible output impedance, etc. can be mapped to limiting curves in the design space [95].**

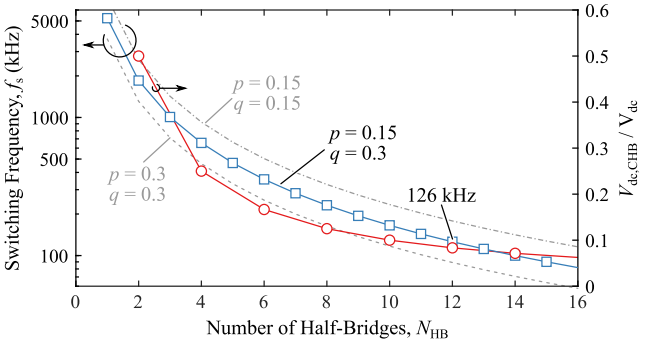

FIGURE 12. **Required device switching frequency in dependence of the topology's number of half-bridges (series- or parallel-interleaving) for $f_{\text{out,max}} = 100\,\text{kHz}$, $p = 0.15$, $q = 0.3$, and $\Delta v_{\text{out,pp}}/V = 2\%$. Note the sensitivity on p and q. For the series-interleaved topology ($N_{\text{CHB}} = N_{\text{HB}}/2$), the red curve shows the required DC voltage per cell normalized to the DC voltage of a corresponding parallel-interleaved structure (right y-axis).**

and for given p, q, $f_{\text{out,max}}$, and $\Delta v_{\text{out,pp}}/V$ can be obtained as

$$f_s = \frac{\pi}{2}\sqrt{\frac{V}{\Delta v_{\text{out,pp}}}} \cdot \frac{1}{\sqrt{pq}} \cdot \frac{1}{N_{\text{HB}}^{3/2}} \cdot f_{\text{out,max}}. \tag{8}$$

Note that if f_s is selected accordingly, the valid design space in **Fig. 11** collapses to a single point, where all criteria are met with the minimum possible switching frequency. The graph of (8) in **Fig. 12** clearly shows the necessity of employing either parallel-interleaving or cascading of converter cells to realize UH-PBW amplifiers that achieve maximum output frequencies in the order of 100 kHz. Whereas a non-interleaved class D amplifier would need a switching frequency in the megahertz range, the same performance can be achieved with a multilevel system with, e.g., $N_{\text{HB}} = 12$ bridge-legs, where a clearly feasible device switching frequency of about 126 kHz suffices (see **Fig. 11**).

So far, both concepts, parallel-interleaving of bridge-legs (see **Fig. 4b**) or cascading of converter cells (see **Fig. 4c**),

show equivalently advantageous characteristics, i.e., the same total number of bridge-legs switching at the same frequency results in equal harmonic performance and hence equal filtering requirements. The complexity of a CHB system tends to be higher, as each cell requires a dedicated isolated power supply. In addition, countermeasures against common-mode ground currents through parasitic capacitances between the cells and ground must be considered [155]. However, as indicated in **Fig. 12**, the switched voltage in case of a CHB system reduces $\propto 1/N_{\mathrm{HB}}$. Thus, as mentioned earlier, MOSFETs with lower blocking voltage ratings and hence lower switching losses and lower specific on-state resistances (scales roughly with $V_{\mathrm{B}}^{-2.5\cdots-2}$ [82]) can be employed. Furthermore, whereas in a parallel-interleaved topology the output voltage ripple occurs at $N_{\mathrm{HB}}\, f_{\mathrm{s}}$, each individual inductor still operates with a current ripple at the single bridge-leg's switching frequency, f_{s}. This is in contrast to the CHB system, where the current ripple in the sole filter inductor already occurs at $N_{\mathrm{HB}}\, f_{\mathrm{s}}$, facilitating more compact inductor designs. Similar benefits can also be achieved with multilevel bridge-legs, e.g., employing a flying-capacitor topology. However, a CHB system is *modular*, which simplifies development and testing, benefits from economies of scale in production, and facilitates scalability to higher output voltages, which is mainly limited by the isolation voltage rating of the cells' power supplies and communication interfaces.

B. MAINS INTERFACE

General-purpose UH-PBW amplifier systems require bidirectional (to enable full four-quadrant operation) power exchange with the feeding grid, e.g., a 400 V three-phase mains. Furthermore, the amplifier output terminals must be galvanically isolated from the mains to ensure full flexibility and (to some extent) arbitrary definition of the output terminals' reference potential. In general, the amplifier's output voltage and current can have arbitrary frequencies between DC and $f_{\mathrm{out,max}}$, i.e., especially also $f_{\mathrm{out}} < f_{\mathrm{grid}}$ can occur. This leads to low-frequency power pulsations that can translate into low-frequency grid current distortions, violating relevant standards such as IEC 61000-3-11 (harmonics) and IEC 61000-3-12 (flicker). Thus, sufficient decoupling, i.e., sufficiently large DC bus capacitors must be provided [156] regardless of the amplifier topology.

1) PARALLEL-INTERLEAVED TOPOLOGIES

Parallel-interleaved UH-PBW amplifiers require a single isolated DC interface. **Fig. 13a** shows the most straightforward realization option, which consists of a low-frequency transformer (LFT) and a standard bidirectional three-phase PFC rectifier. Alternatively, to avoid the volume and weight penalty of an LFT, the three-phase PFC can directly interface the mains and a subsequent bidirectional isolated DC-DC converter provides the galvanic separation with a high-frequency (HF) transformer, see **Fig. 13b**. Thus, the DC voltage level can advantageously be selected independent from the grid voltage. For example, [157] employs a dual-active

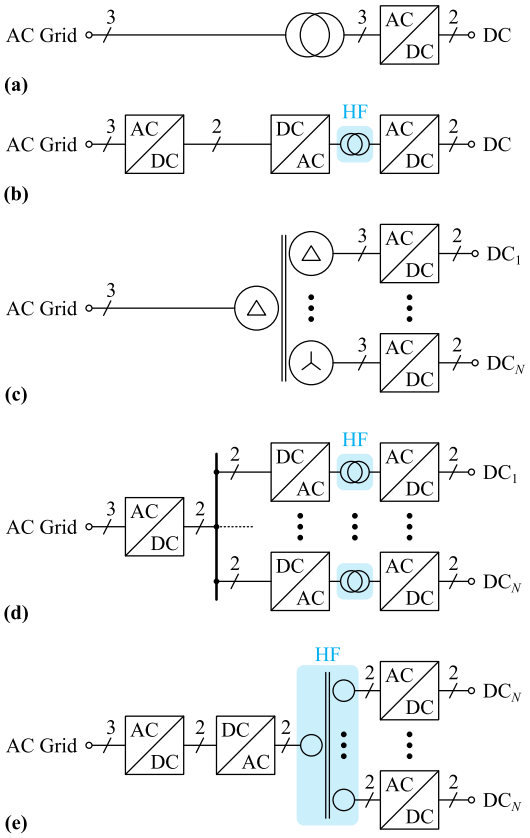

FIGURE 13. Concepts for providing isolated DC supply voltages to the power amplifier stages. Parallel-interleaved amplifiers can be supplied (a) via a grid-frequency transformer and a PFC rectifier or (b) via a gird-side PFC rectifier and a downstream isolated DC-DC converter with a high-frequency (HF) isolation transformer. For series-interleaved power amplifier stages, multiple isolated DC ports are required: (c) shows a low-frequency multi-winding transformer with several secondary-side PFC rectifiers (one per cascaded cell). Alternatively, a shared PFC rectifier stage can be employed in combination with (d) several isolated DC-DC converters operating from a common DC bus, or (e) an integrated isolated DC-DC converter featuring a high-frequency multi-winding transformer [159].

bridge (DAB) DC-DC converter, and [158] describes an isolation stage based on an unregulated series-resonant DC-DC converter (''DC transformer'') and an integrated DC-bus midpoint balancing stage required by the amplifier's three-level bridge-legs.

2) CHB TOPOLOGIES

Whereas parallel-interleaved topologies thus require a power supply with a single isolated DC interface, CHB systems need one isolated DC interface per cell. A first, robust approach shown in **Fig. 13c** employs a low-frequency multi-winding transformer and individually-controlled three-phase PFC rectifiers in each converter cell, see [86] and **Section IV**. By employing a special phase-shifting multiwinding transformer, which achieves harmonic cancellation similar as known from multipulse rectifier systems, the input filters of the cells' three-phase active rectifiers can be omitted [4], resulting in more compact designs.

Alternatively, again high-frequency isolation concepts can be employed. **Fig. 13d** shows a solution with a shared

grid-connected three-phase PFC rectifier and dedicated isolated DC-DC converters for each cell, which can be realized, e.g., as LLC series resonant converters [84], [154]. The primary-side DC-AC stages can be (partially) integrated, resulting in I3DAB [160] or I3SRC [161] structures. Ultimately, an integrated multi-port series-resonant DC-DC converter with a HF multi-winding transformer could be employed [159].

A low-frequency transformer may be relatively bulky, which however can be considered acceptable for stationary applications. Thus, the approach combining a low-frequency transformer and converter cells with individual PFC rectifier stages (i.e., a fully modular system) advantageously features high robustness against grid transients, straightforward scalability to higher voltage levels, and comparably low complexity (fewer switches as compared to a solution with individual isolated DC-DC converters, and independent per-cell local control of the PFC rectifier).

C. AMPLIFIER OUTPUT CONTROL

As indicated in **Fig. 10**, an amplifier's control system receives an output voltage (or output current) reference from a higher-level application (e.g., a power grid or a motor model; a discussion is beyond the scope of this paper) and must ensure that the amplifier's output closely tracks that reference. To do so, the control system processes the reference and measured voltages and currents to ultimately generate the gate signals for the amplifier's power transistors. In a wider sense, the control system also must ensure a constant DC input voltage of the amplifier, i.e., control the mains interface. As standard methods can be employed here, we do not discuss this further but focus on key aspects of the actual amplifier's output voltage control.

1) SENSORS, SAMPLING, SIGNAL PROCESSING, AND MODULATION

Multilevel systems essentially require several modulators that operate with phase-shifted carriers, whereby accurate phase-shifts are needed to ensure the beneficial cancellation of harmonics discussed above. As discussed, e.g., in [163], analog PWM modulation ("naturally sampled PWM") can achieve better performance in terms of bandwidth than regularly sampled PWM (i.e., single- or double-update mode, which introduces relatively long delays in the control loop; note that this can be improved by advanced multirate modulator techniques for parallel- or series-interleaved converters such as described in [164], [165]). However, in case of analog implementations, component tolerances and temperature dependencies of their characteristics lead to difficulties in maintaining accurate carrier phase-shifts.

Therefore, fully-digital implementations are preferable. As shown in [166], oversampling can be used to approximate analog modulation. Oversampling ratios (i.e., number of PWM reference updates per PWM period) of about 8…16 already result in *quasi-analog* behavior. However, considering UH-PBW amplifiers with effective switching

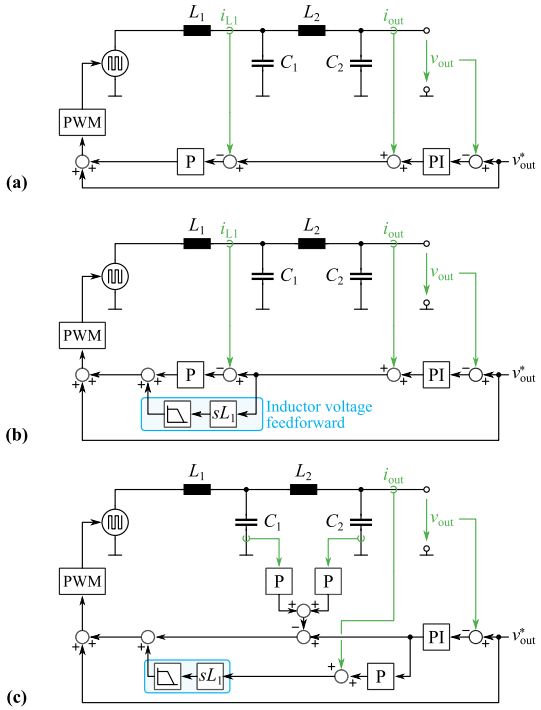

FIGURE 14. Exemplary multi-loop control structures for switch-mode amplifiers with two-stage LCLC output filters. (a) Two-loop cascaded output voltage and inductor current control. (b) Control schematic of (a) extended by a feed-forward of the inductor voltage to increase the current loop bandwidth, see [53]. (c) Alternative approach using capacitor current feedback to actively damp the filter's resonant pole, and direct PI control of the output voltage [96], [162]. The structures are simplified; i.e., delays, measurement and reference filters, etc. are not explicitly shown.

frequencies that can reach, e.g., the 5 MHz range, this first implies the need for current sensors with sufficiently high bandwidth to capture the corresponding current ripple, i.e., advanced hybrid sensors such as [167], featuring bandwidths of 20 MHz to 50 MHz, are needed. Second, the signal processing system must be capable of acquiring measurements at a sampling rate in the order of 80 MS/s (for an oversampling ratio of 16 and $f_{s,\mathrm{eff}} = 5\,\mathrm{MHz}$), and updating at least the current control loop at the same rate. Modern FPGAs can offer the corresponding computing power, but large parts of the controller must be programmed using a hardware description language such as VHDL. Finally, at these very high effective switching frequencies, which are much closer to typical FPGA clock frequencies (e.g., 100 MHz to 200 MHz) than in normal PWM converter topologies, care has to be taken regarding quantization effects, i.e., limited resolution of digitally generated PWM signals. This may become an issue especially for applications that require high resolution of the output voltage, e.g., to generate very low output voltages for controlling a current in a low-impedance load [53]. It may then become necessary to resort to advanced modulator implementations such as described in [168].

2) CONTROL STRUCTURES

Even though so far only single-stage output filters have been discussed for the sake of clarity, practical power amplifier

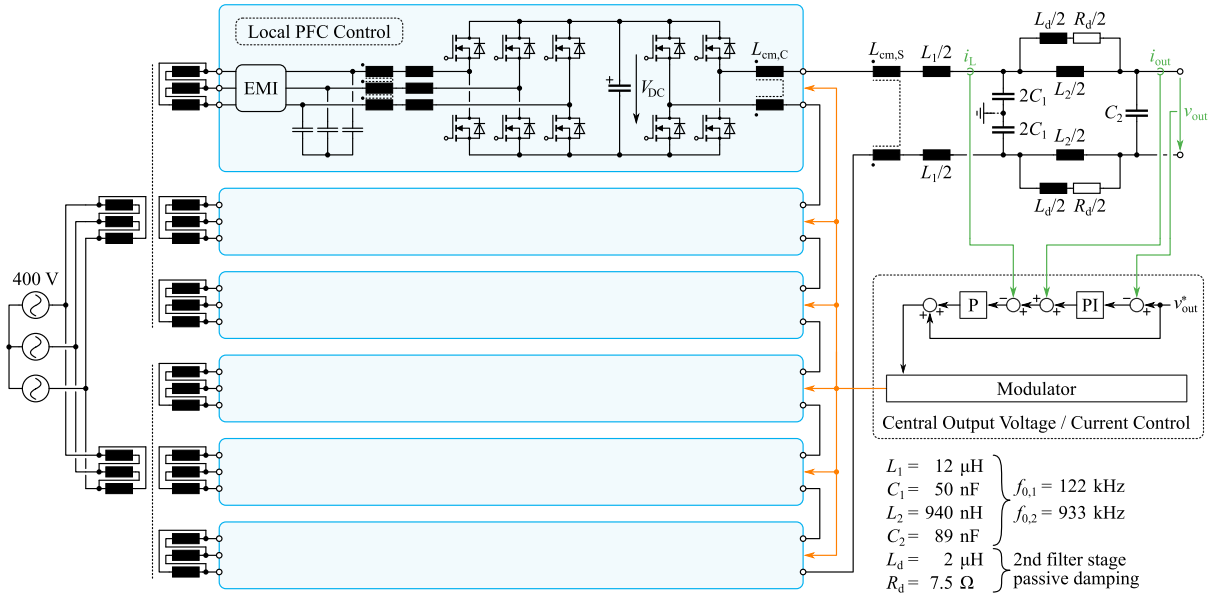

FIGURE 15. Overview diagram of the realized UH-PBW amplifier system with specifications and key characteristics given in Table 1. Fig. 16 shows a photograph of the hardware realization.

systems typically require a two-stage LCLC filter to achieve the desired output voltage quality [95]. Therefore, the following brief discussion of control structures considers such a two-stage filter, see **Fig. 14**.

Literature documents manifold methods for controlling the output voltage (or current) of an inverter with a two-stage LCLC filter. Whereas also advanced approaches such as (model) predictive control [39], [65], [145], [149] have been proposed, the most straightforward option is a cascaded control structure with an inner, fast current control loop and an outer, slower voltage control loop, see **Fig. 14a**. The bandwidth of the current control loop can be improved by adding a feed forward of the inductor voltage [53], see **Fig. 14b**. An alternative multi-loop control scheme directly controls the output voltage with a PI controller, and employs capacitor current feedback to actively damp the filter's resonant pole [96], [162], see **Fig. 14c**. This structure has been found to achieve highest output voltage control bandwidth [53]. A detailed discussion and comparison of these and similar multi-loop control schemes is beyond the scope of this paper; interested readers are referred to [53], [96], [162] instead, and to [169] for a detailed stability analysis and extensions for output impedance emulation (instead of direct output voltage or current control).

IV. UH-PBW AMPLIFIER SYSTEM PROTOTYPE

The last part of this paper discusses an industrial UH-PBW prototype system that employs some of the key concepts discussed in the previous **Section III** to realize the specifications summarized in **Table 1**.

A. SYSTEM DESCRIPTION

Based on the conclusions drawn in **Section III-A**, the amplifier is realized as a series-interleaved CHB topology with

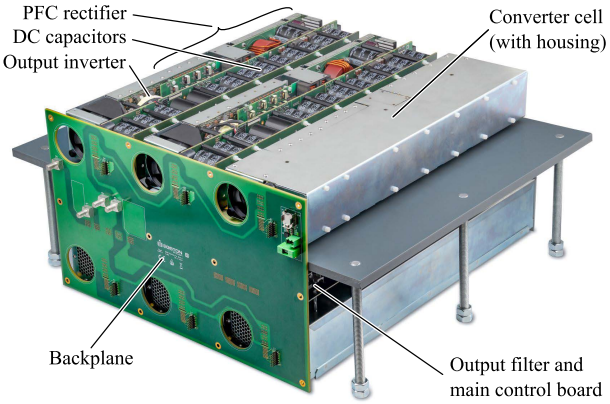

FIGURE 16. Hardware realization of a single phase-stack (consisting of six converter cells, see topology in Fig. 15) of the UH-PBW amplifier system. The width is compatible with 19" racks; the low-frequency transformers and the overall mechanical assembly structure are not shown.

$N_{CHB} = 6$ cells (see **Fig. 15**), each operating with a local DC bus voltage of 100 V. The cells' power supplies are realized with two robust low-frequency multi-winding transformers and individually controlled three-phase PFC rectifiers for each cell (i.e., as discussed in the context of **Fig. 13c**). As the series-interlaved approach reduces the blocking voltage requirements for the transistors (see **Fig. 12**), cost-effective 150 V silicon superjunction MOSFETs facilitate a device switching frequency of 300 kHz for the cells' output full-bridges and hence an effective switching frequency of 3.6 MHz. Common-mode chokes placed at the cells' AC terminals mitigate common-mode ground currents [155]. The photo of the protoype shown in **Fig. 16** highlights the system's modular architecture. For example, three phase stacks could be arranged to form a three-phase grid or motor emulator. Leveraging the modularity of the selected series-interleaved CHB topology, the output voltage capability could easily be

TABLE 1. Specifications and key characteristics of the UH-PBW amplifier prototype shown in Fig. 15 and Fig. 16.

Parameter	Value	
Single-phase AC power	10	kW
DC power	20	kW
Output voltage (AC peak)	325	V (nominal)
	470	V (max)
Output voltage (DC)	±500	V
Output current (DC, AC peak)	62	A
Output current (AC rms)	44	A
Cell DC voltage	100	V
Number of cells	6	
Switching frequency	300	kHz
Eff. sw. frequency	3.6	MHz
Min. output frequency	0	Hz
Max. output frequency	100	kHz (at nom. volt./power)
Small-signal BW	330	kHz (−3 dB, unloaded)

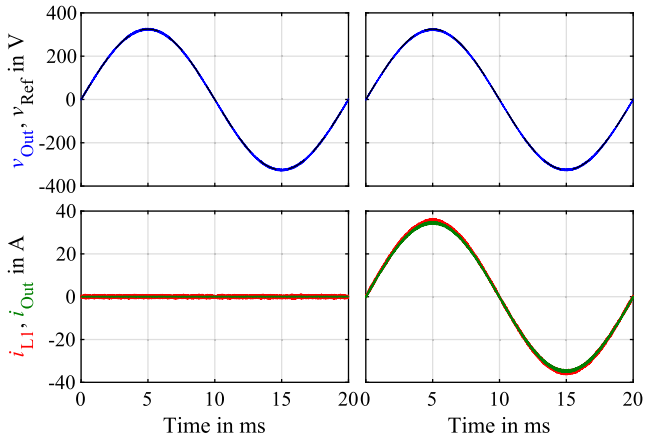

FIGURE 17. Measured output voltage, output current, and filter inductor current for a sinusoidal reference signal of 230 V rms and 50 Hz. Left: unloaded, right: loaded with $Z = 9.4\,\Omega + j\omega \cdot 1\ \mu$H, i.e., mostly resistive load of $P = 5.6$ kW.

increased, e.g., to emulate a 690 V grid, by adding more cascaded converter cells.

Taking into account the two-stage LCLC output filter, the output voltage control uses a straightforward cascaded approach as shown in **Fig. 15** (see also the discussion in the context of **Fig. 14**). The high-bandwidth current sensor described in [167] together with a 125 MS/s ADC converter enables a quasi-analog control and modulation implementation running at 125 MHz on a Xilinx Zynq SoC module. The gate signals for all inverter switches of all cells are thus generated centrally, whereas each cell features a local control module for its PFC rectifier. Ultimately, the UH-PBW amplifier achieves a maximum output frequency of 100 kHz at nominal voltage and current of 230 V rms and 44 A rms, respectively.

B. PERFORMANCE EVALUATION

Fig. 17 and **Fig. 18** show measured output voltage and current waveforms for $f_{out} = 50$ Hz and $f_{out} = 20$ kHz, respectively, for nominal $V_{out} = 230$ V rms and either unloaded or with an (almost purely) resistive load corresponding to $P = 5.6$ kW. A series of such measurements with sinusoidal

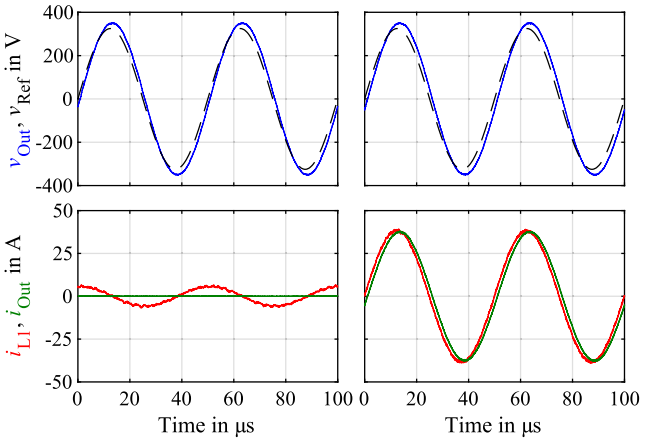

FIGURE 18. Measured output voltage, output current, and filter inductor current for a sinusoidal reference signal of 230 V rms and 20 kHz. Left: unloaded, right: loaded with $Z = 9.4\,\Omega + j\omega \cdot 1\ \mu$H, i.e., mostly resistive load of $P = 5.6$ kW.

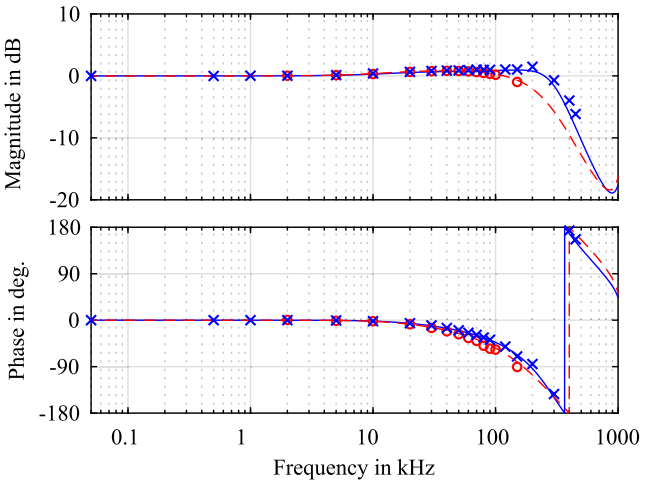

FIGURE 19. Reference-to-output-voltage transfer function of the unloaded (blue) and loaded (red, with $Z = 9.4\,\Omega + j\omega \cdot 1\ \mu$H) amplifier. The curves correspond to the dynamic model calculations and the markers indicate measured values. The measurements have been carried out with nominal $V_{out} = 230$ V rms for $f_{out} < 200$ kHz (and hence with mostly resistive load of $P = 5.6$ kW in the loaded case); for higher frequencies, $V_{out} = 23$ V rms has been used.

reference signals of varying frequencies has been carried out to characterize the reference-to-output-voltage transfer function for unloaded and loaded (about 5.6 kW, mostly resistive) conditions, see **Fig. 19**. The measurements confirm the model calculations and the targeted ultra-high bandwidth. **Fig. 20** demonstrates measurements of a full-power (10 kW) operating point at 305 V rms and 100 kHz.

The ultra-high bandwidth and maximum output frequency facilitate the generation of large-signal arbitrary waveforms such as shown in **Fig. 21** and **Fig. 22**, the latter being a 60 kHz, ±300 V peak triangular signal. The output quality barely changes when the system is loaded with $Z = 9.4\,\Omega + j\omega \cdot 1\ \mu$H, i.e., about $P = 3.2$ kW.

Finally, **Fig. 23** shows measured load step responses of the amplifier, confirming very quick return to the output voltage set point. **Fig. 24** shows measured reference step responses of the unloaded and loaded amplifier, demonstrating a rise time

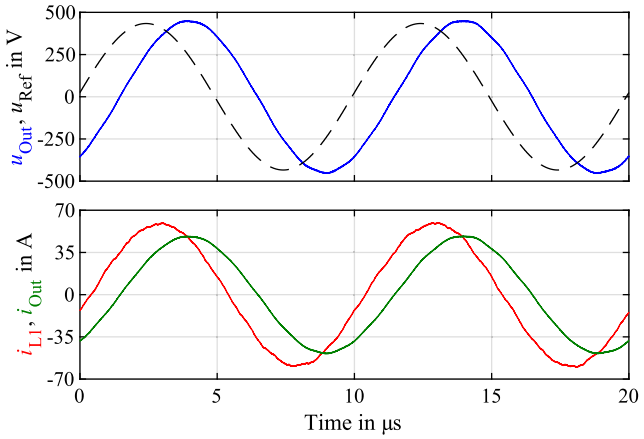

FIGURE 20. Measured output voltage, output current, and filter inductor current for a sinusoidal reference signal of 305 V rms and 100 kHz; the amplifier is loaded with $Z = 9.4\,\Omega + j\omega \cdot 1\,\mu$H, i.e., a mostly resistive load of $P = 10$ kW.

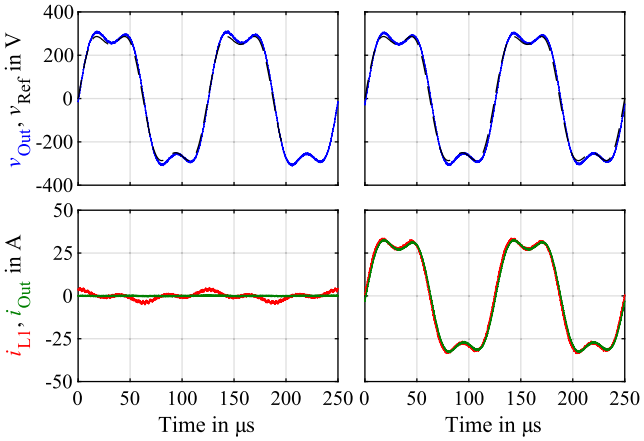

FIGURE 21. Measured output voltage, output current, and filter inductor current for a reference signal that is a superposition of a 230 V rms, 8 kHz sine and a 75 V (amplitude), 24 kHz sinusoidal third harmonic. Left: unloaded, right: loaded with $Z = 9.4\,\Omega + j\omega \cdot 1\,\mu$H.

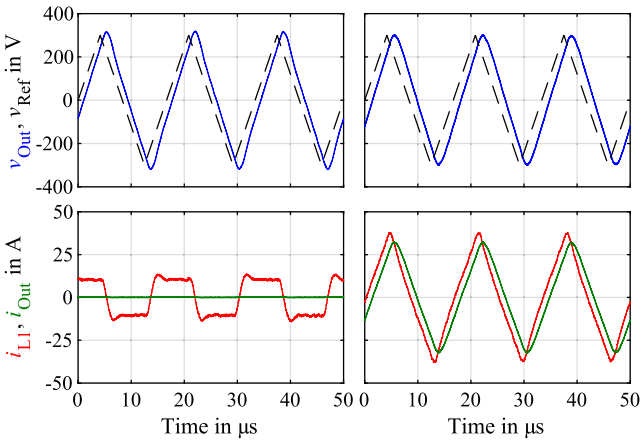

FIGURE 22. Measured output voltage, output current, and filter inductor current for a 60 kHz triangular reference signal with 300 V amplitude. Left: unloaded, right: loaded with $Z = 9.4\,\Omega + j\omega \cdot 1\,\mu$H, i.e., about $P = 3.2$ kW.

from 0 V to 100 V in about 2 µs and a moderate overshoot of less than 20 %. In all cases, the measurements closely match the calculations.

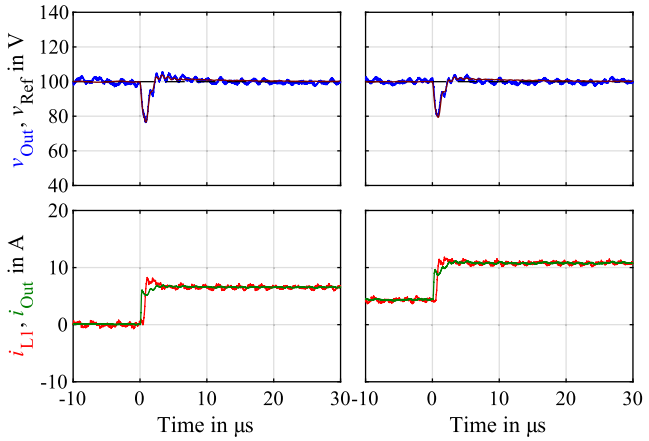

FIGURE 23. Measured (blue) and simulated (brown) output voltage responses to load steps. The measured output current and the filter inductor current are also shown. Left: no-load to 15.7 Ω, right: 23.5 Ω to 9.4 Ω.

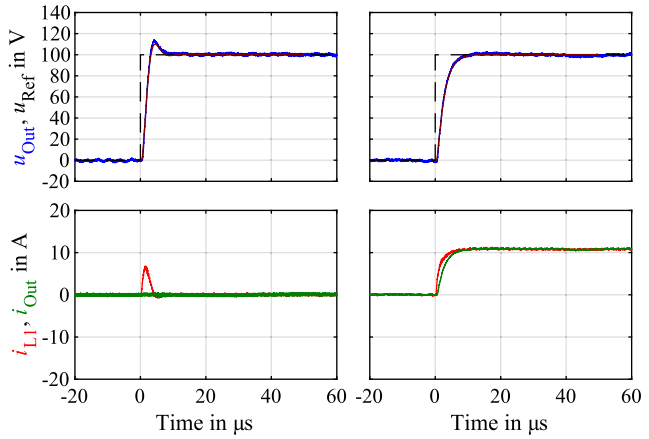

FIGURE 24. Measured (blue) and calculated (brown) output voltage responses to a reference step from 0 V to 100 V. The measured output current and the filter inductor current are also shown. Left: unloaded, right: loaded with $Z = 9.4\,\Omega + j\omega \cdot 1\,\mu$H. Note that a slightly different set of control parameters has been used to achieve faster settling time at the expense of a slightly slower rise time.

We estimate the full-load efficiency of the amplifier stage itself (based on measured semiconductor losses) to be about 95 %. Allowing another 0.5 % of losses for the filter elements and assuming typical efficiencies of 98.5 % for the PFC rectifier stages and the LFTs, the typical overall full-load system efficiency becomes about 92 %. Therefore, forced-air cooling is easily possible. This efficiency estimate is in the same range as values reported for commercially available switch-mode amplifier systems (see, e.g., [27], [34], [35], [42], [45]), and clearly much higher than even the best-case efficiency of linear amplifiers (less than 80 %, see (1), for the amplifier itself, i.e., without considering the mains interface).

The above clearly demonstrates how combining the key concepts cascading of multiple converter cells, multi-loop control structures, and quasi-analog sampling and modulation enable the realization of a 10 kW amplifier (per phase) with an unprecedented UH-PBW of 100 kHz.

V. CONCLUSION

Ever higher switching frequency of today's and future power electronic converter systems, enabled by wide-bandgap power semiconductors, drive a need for power amplifiers with ultra-high power bandwidth (UH-PBW) for P-HIL test environments. This paper focuses on identifying key concepts for the realization of such next-generation UH-PBW amplifiers by first providing a thorough review of the different amplifier concepts described in the literature so far. Analog (linear) amplifiers achieve high bandwidth but suffer from high losses, whereas the bandwidths of more efficient two-level switch-mode amplifiers are ultimately limited by the achievable switching frequency and the need for an output low-pass filter with a cutoff frequency sufficiently lower than that switching frequency.

The two topological key concepts that enable switch-mode UH-PBW amplifiers to overcome this limit are parallel-interleaving of multiple two-level bridge-legs or series-interleaving (i.e., cascading) of converter cells. Both approaches facilitate *effective* switching frequencies that are far higher than the switching frequency of the individual devices. Furthermore, series-interleaving has the advantage of reducing the blocking voltage requirements of the transistors, which enables higher device switching frequencies, and employs a lower number of inductive components. Moreover, series-interleaved multicell topologies are scalable to higher voltage and power levels by adding additional series converter cells, but require a more complicated power supply system (one isolated DC supply per converter cell).

We finally demonstrate a series-interleaved multicell UH-PBW amplifier prototype that employs quasi-analog digital modulation and control enabled by high-performance FPGAs and advanced current sensors. The amplifier provides an output power of 10 kW (per phase), a nominal output voltage of 230 V rms, and a maximum output frequency of 100 kHz at nominal voltage and power and features a small-signal bandwidth of more than 300 kHz.

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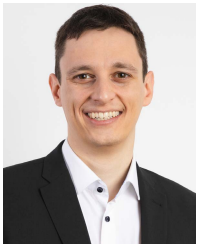

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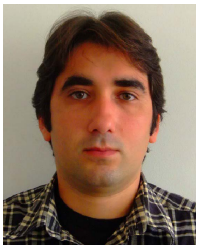

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